VCU128 System Controller GUI Tutorial

May 2019



Revision History

Date	Version	Description	
05/29/19	2.0	Updated for 2019.1. For Production Silicon boards.	
12/10/18	1.0	Initial version.	

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Overview

- > Xilinx VCU128 Board
- > VCU128 SCUI
 - » Clocks
 - Voltages
 - » Power
 - » FMC
 - » GPIO Expander
 - » EEPROM Data
 - About
- > Programming Firmware
- > References



VCU128 Software Install and Board Setup

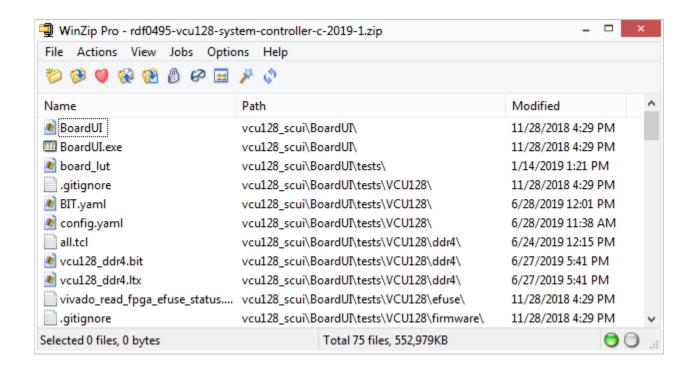
- > Complete setup steps in XTP535 VCU128 Software Install and Board Setup:
 - Software Requirements
 - >> VCU128 Board Setup
 - UART Driver Install
 - >> Ethernet Setup





VCU128 System Controller

- > Open the RDF0495 VCU128 System Controller GUI (2019.1 C) ZIP file
 - >> Extract these files to your C:\ drive





Running the Board Interface Test

> From C:\vcu128_scui/BoardUI, double click on BoardUI.exe





Basic Board Interface Test

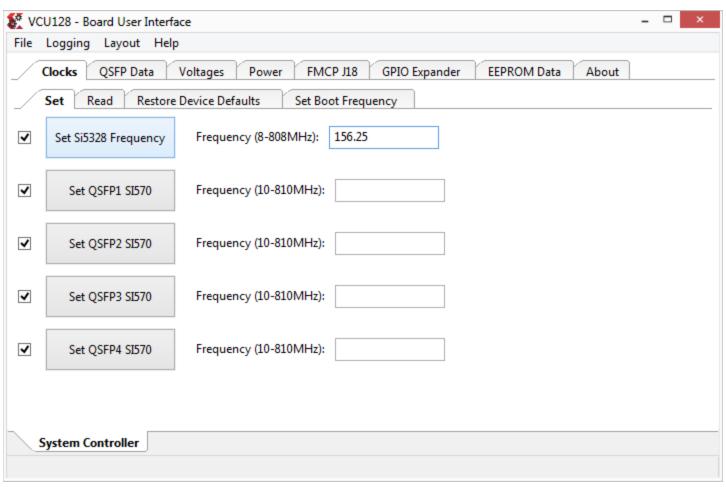
> Select the Board Serial Number from the pulldown and click OK

Enter Board Information				
Board:	VCU128	¥		
Revision:	1.0	¥		
Silicon:	prod	~		
Mode:	default	¥		
Serial Number:		~		
	1281016A0177 OK			



Setting the clocks

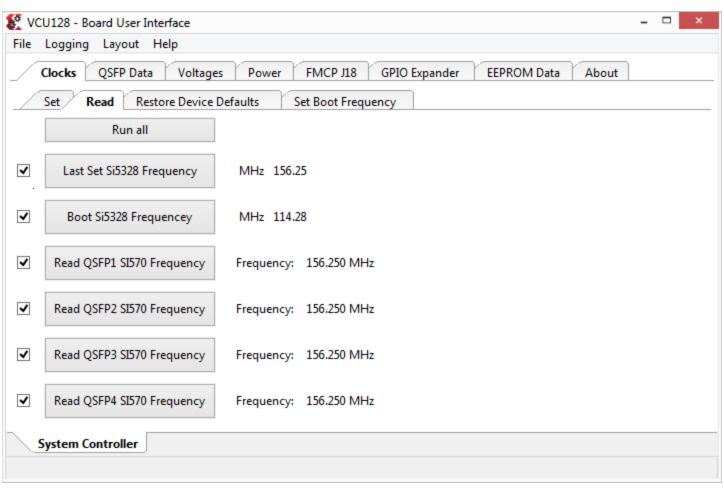
- > Select the Set tab underneath the Clocks tab
- > Enter 156.25 for the Si5328 and click the Set Si5328 Frequency button





Reading the clocks

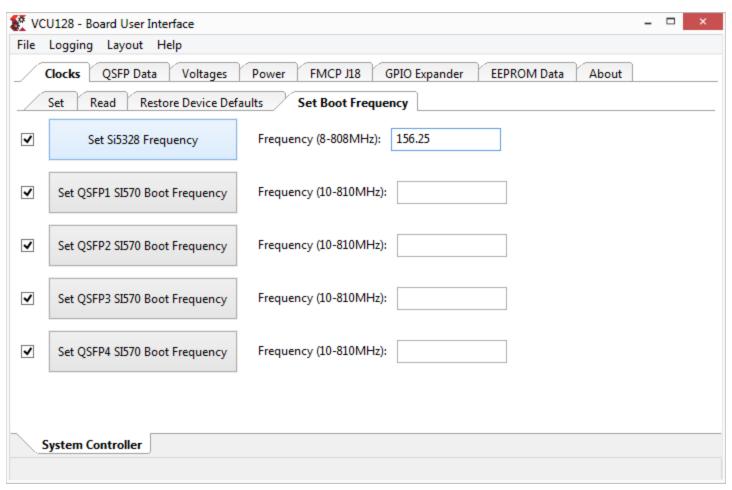
- > Select the Read tab
- > Click each of the Read buttons and verify the frequencies are set as shown





Setting Clock Boot Frequencies

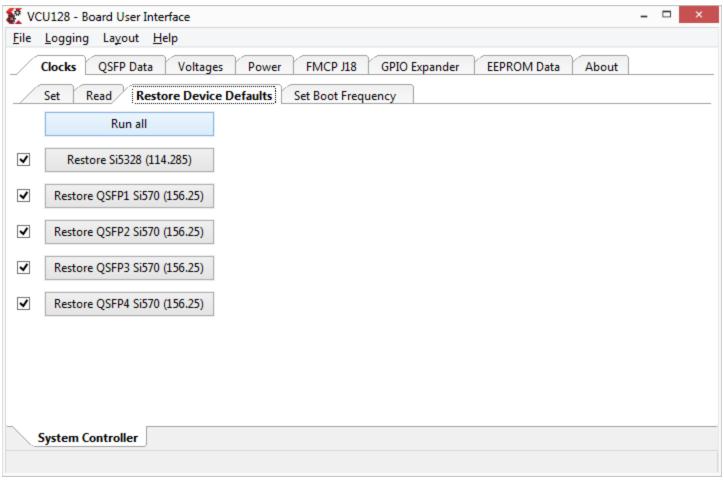
- Select the Set Boot Frequency tab
- Type in your desired boot-up frequency and click the corresponding Set button





Setting the clocks

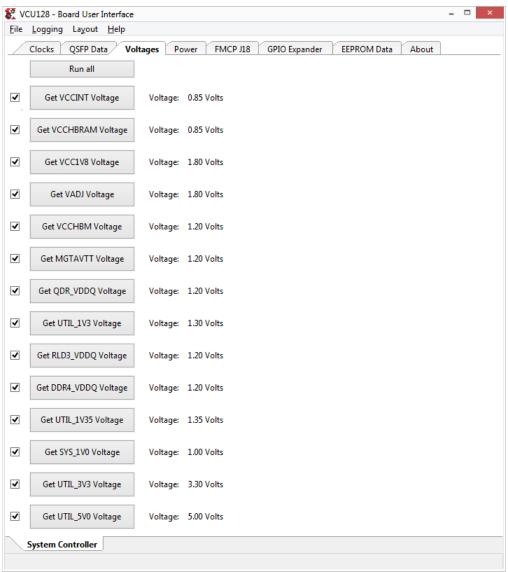
- > Select the Restore Device Defaults tab
- > Click Run All to restore all to the factory settings
- Set the Si5328 back to 156.25 after this step





Reading onboard VCU128 voltages

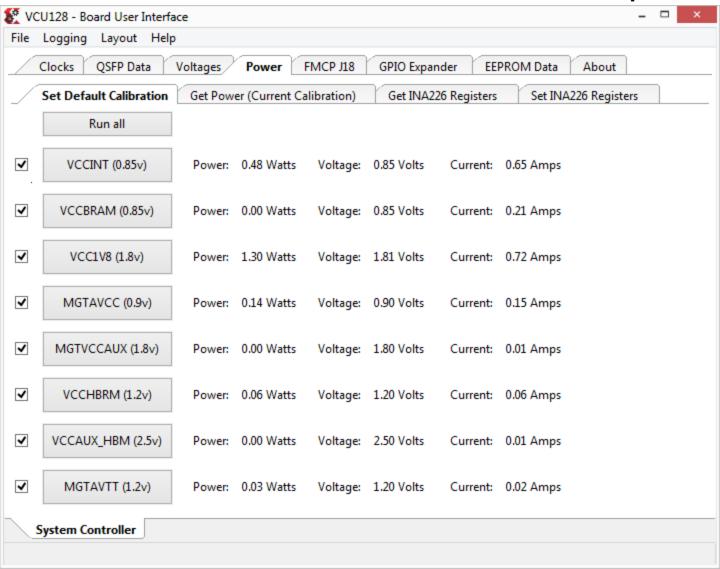
- > Select the Voltages tab
- > Click the Run all





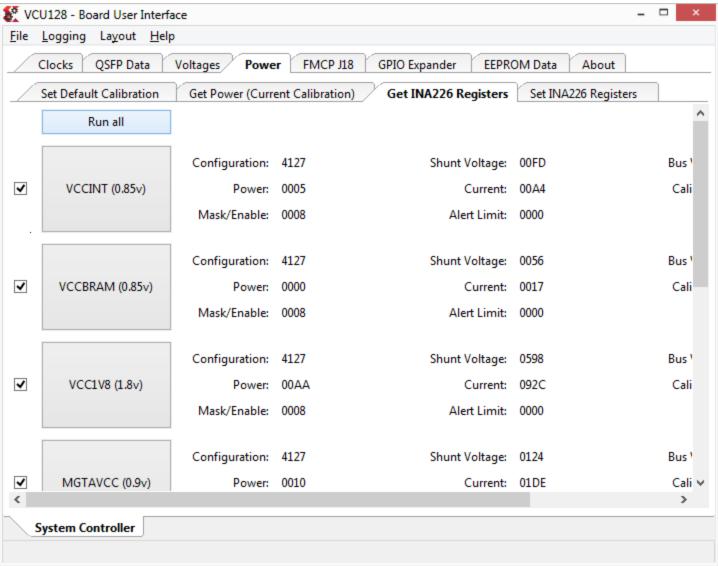
Reading power values using default calibration

- Select the Set Default Calibration tab underneath Power and click Run all
- > This sets the default calibration and returns the calibrated power values



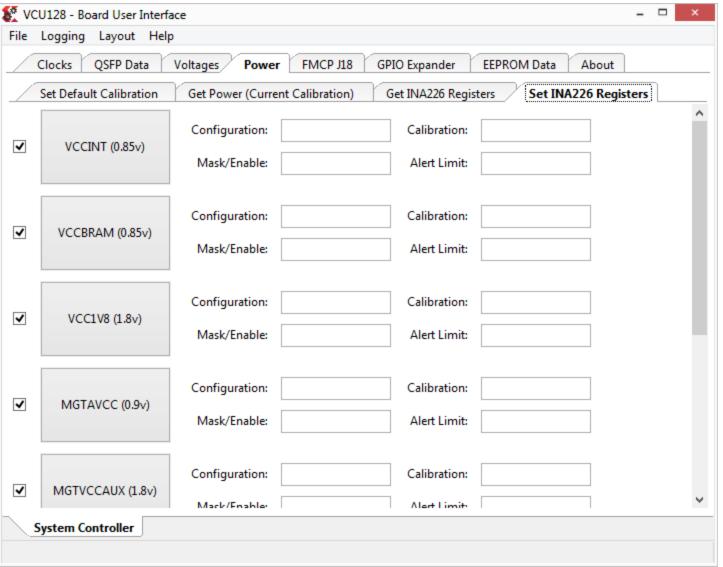
Read INA226 Registers

- > Select the Get INA226 Registers tab and click Run all
- > Observe the INA226 Registers settings



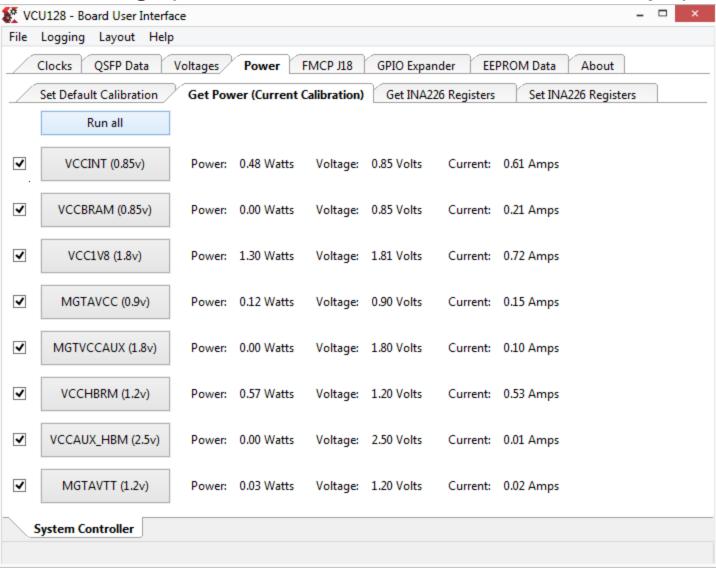
Set INA226 Registers

- Select the Set INA226 Registers tab
- > Review TI INA226 documentation before making changes



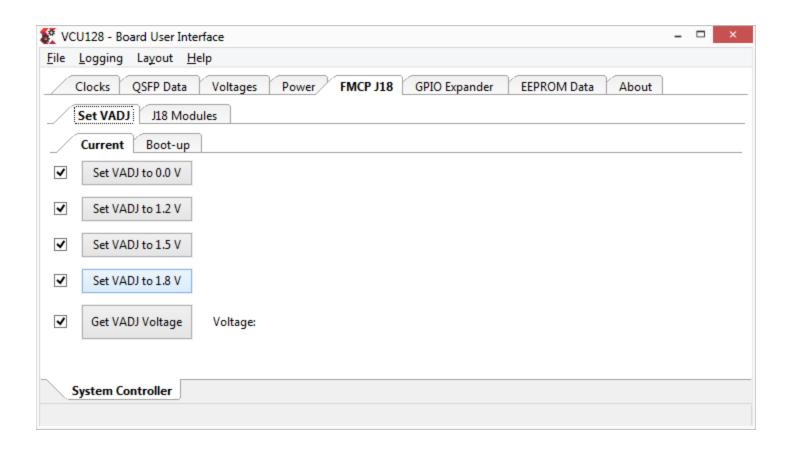
Reading power values using current calibration

- > Select the Get Power (Current Calibration) tab and click Run all
- Observe readings (no calibrations were entered in this example)



Set VADJ

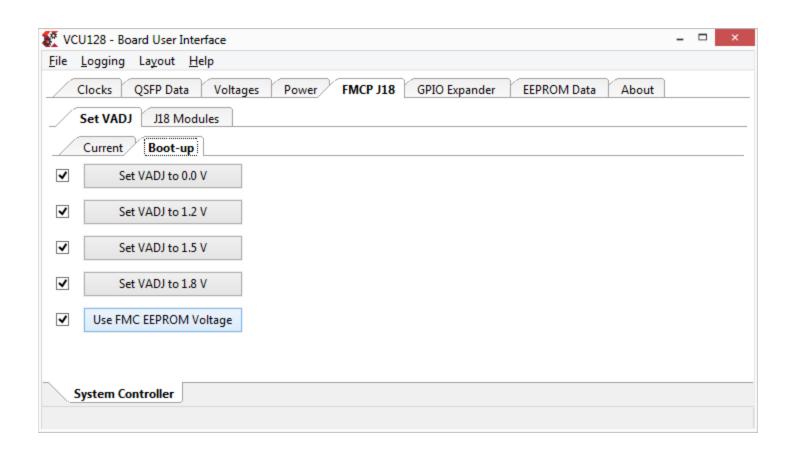
- > Select the Set VADJ tab underneath the FMC J18 tab
- > Under the Current tab, select the desired VADJ voltage
- Some BIT tests expect 1.8 V





Set Boot-Up VADJ

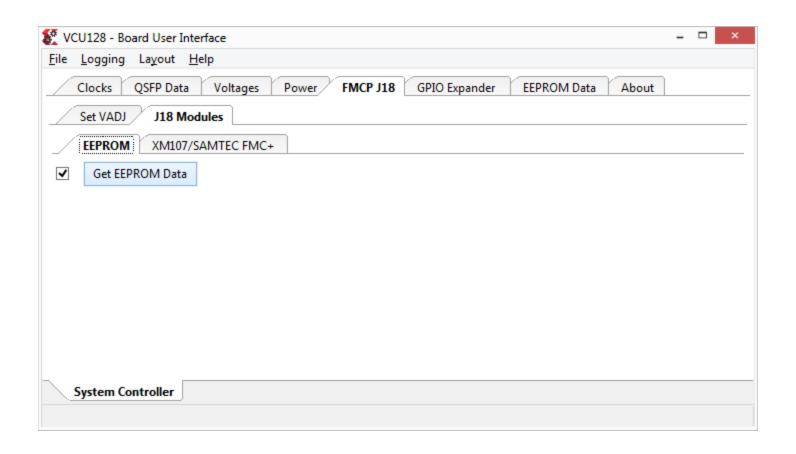
- > Select the Boot-up tab and choose the desired power-on voltage
- The default, Use FMC EEPROM Voltage, will set 1.8 V unless you attach an FMC card with a different setting





Reading FMC EEPROM

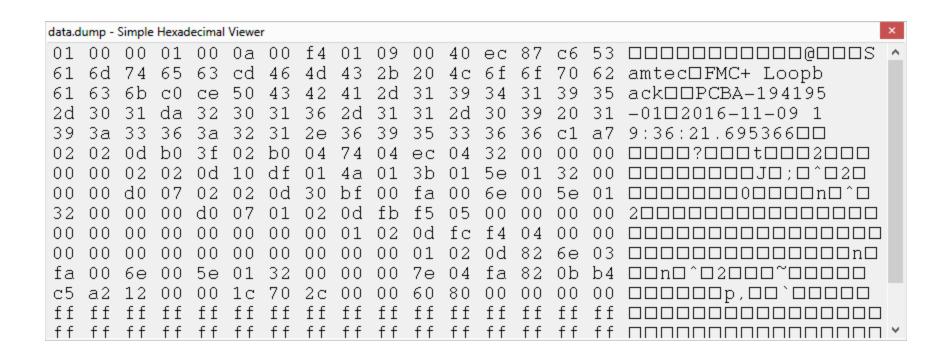
- Select the J18 Modules tab
- > Click the Get EEPROM Data button





Reading FMC EEPROM

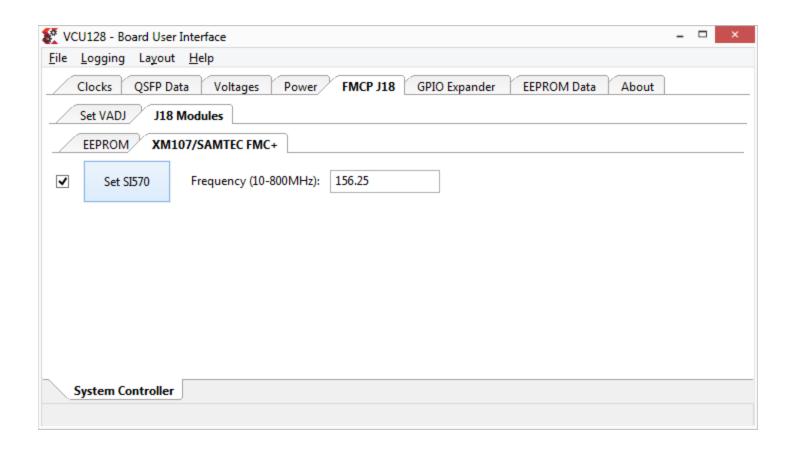
> The EEPROM data will be displayed in a separate window (SAMTEC FMC+ loopback data shown)





Setting FMC HPC clocks

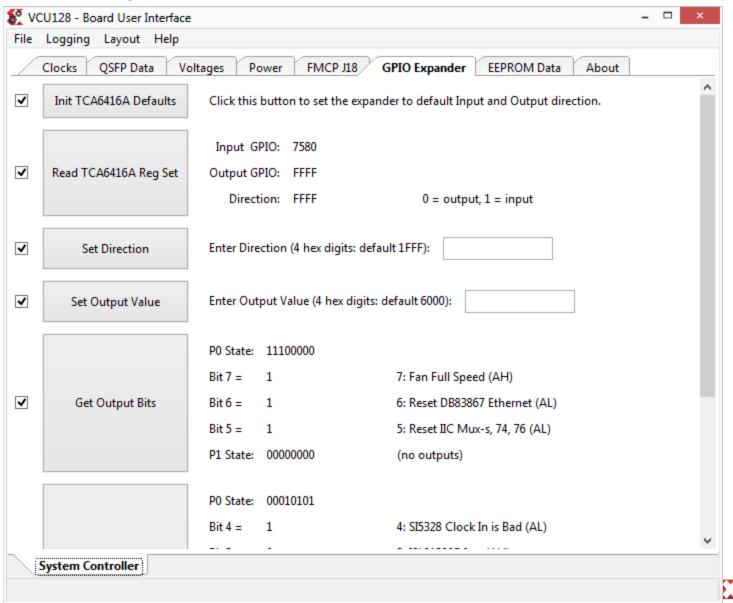
- With an XM107 or SAMTEC FMC+ card attached, select the XM107/SAMTEC tab
- > For the IBERT FMC+ testing, set 156.25, and click the Set SI570 button





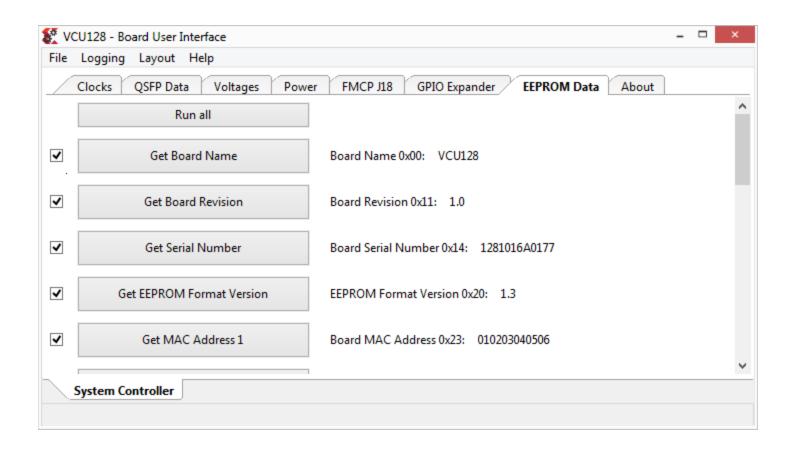
GPIO Expander

> Various setting for the TCA6416 IIC expander



Reading the Board EEPROM Data

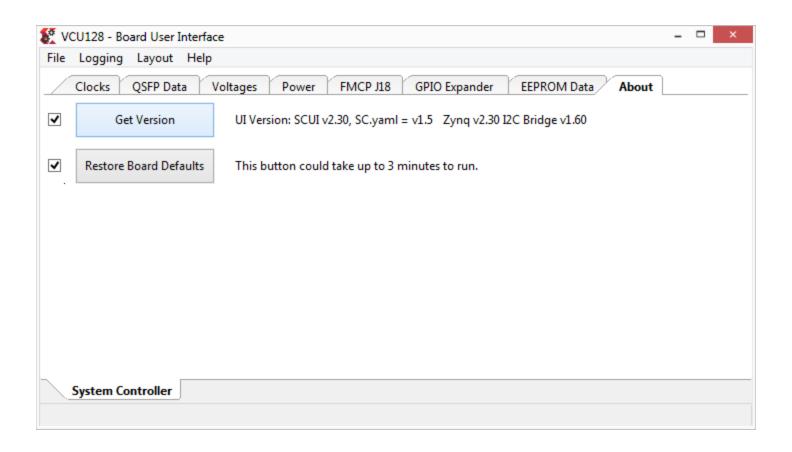
- Select the EEPROM Data tab
- > Click the Run all button





Reading version information

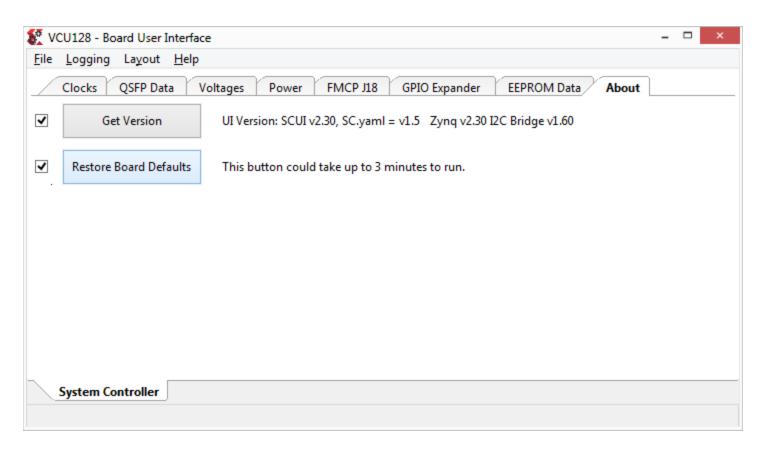
- Select the About tab
- > Click the Get Version button to get MSP430 and SCUI GUI version information





Reading version information

- > Click the Restore Board Defaults button to reset initializations
 - >> This restores the QSFP Si570s clocks to their default of 156.25 MHz
 - Si5328 is reset to Default of 114.285 MHz
 - The FMC VADJ is reset to Use FMC EEPROM Voltage



Note: This step stores values in the Zynq QSPI; it will no longer verify after this has been run





- > Connect a USB Platform Cable to J49 with the Flying Leads
- > Shown here with board flipped over





> Script files are included to program the firmware

Zynq_SC_Firmware	9.64 1/14/2019 1:20:17 pm
iasc	9.64 1/14/2019 1:20:17 pm
■ BOOT.bin	7.08 8/28/2018 5:47:34 pm
■ Jtag_connection_setup.jpg	2.21 8/28/2018 5:47:34 pm
■ programming_README.txt	1,054 8/28/2018 5:47:34 pm
■ program_sysctrl.bat	764 10/30/2018 3:09:33 pm
■ program_sysctrl.tcl	2,316 10/30/2018 2:30:38 pm
■ program_sysctrltcl	2,148 10/30/2018 2:29:33 pm
■ verify_sysctrl.bat	763 10/30/2018 3:09:33 pm
■ verify_sysctrl.tcl	2,321 10/30/2018 3:04:45 pm
■ vivado_lab.jou	725 10/30/2018 3:08:51 pm
■ vivado_lab.log	4,041 10/30/2018 3:08:51 pm
■ vivado_lab_10248.backup.jou	728 10/30/2018 2:47:39 pm
■ vivado_lab_10248.backup.log	4,338 10/30/2018 2:47:39 pm
■ zynq_1b_debug_fsbl.elf	339 KB 8/28/2018 5:47:34 pm



- The Programming BAT files will prompt you to connect the Flying Leads
- > Press any key to continue...

```
Administrator: Command Prompt - program_sysctrl.bat
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.
C:\>cd C:\vcu128_scui\Zyng_SC_Firmware\SC
C:\vcu128_scui\Zynq_SC_Firmware\SC>program_sysctrl.bat
Power off UCU128
Disconnect the USB JTAG UART cable from J2
Attach Xilinx Platform Cable USB to J49 with Flying Lead adapter Flying-Leads to J49 pin mapping [6:1] = [Violet, White, Green, Yellow, Black, Red]
Top to Bottom:
 Pin 6, SYSCTLR_TDO, Violet
 Pin 5, SYSCTLR_TDI, White
 Pin 4, SYSCTLR_TMS, Green
 Pin 3, SYSCTLR_TCK, Yellow
 Pin 2, GND,
 Pin 1, SYS_1V8,
                         Red
Press any key to continue . . .
```





- Important: The current System Controller must be disabled prior to programming
- > Put a jumper on J43, cycle VCU128 power and remove the jumper and press any key to continue...

```
Administrator: Command Prompt - program_sysctrl.bat
Microsoft Windows [Version 6.1.7601]
                                                     All rights reserved.
Copyright (c) 2009 Microsoft Corporation.
C:\>cd C:\vcu128_scui\Zyng_SC_Firmware\SC
C:\vcu128_scui\Zynq_SC_Firmware\SC>program_sysctrl.bat
Disconnect the USB JTAG UART cable from J2
Attach Xilinx Platform Cable USB to J49 with Flying Lead adapter
Flying-Leads to J49 pin mapping [6:1] = [Violet, White, Green, Yellow, Black, Red]
Top to Bottom:
Pin 6, SYSCTLR_TDO, Violet
Pin 5, SYSCTLR_TDI, White
Pin 4, SYSCTLR_TMS, Green
 Pin 3, SYSCTLR_TCK, Yellow
 Pin 2, GND,
                          Black
Pin 1, SYS_108,
                          Red
Press any key to continue . .
Put jumper on J43
Power on VCU128.
Remove jumper on J43.
Press any key to continue . . .
```

- > Programming finished successfully
- > Cycle VCU128 power to enable the System Controller

```
Administrator: Command Prompt - program_sysctrl.bat
SF: 65536 bytes @ 0x6f0000 Read: OK
Zyng> cmp.b FFFC0000 FFFD0000 10000
Total of 65536 byte(s) were the same
Zynq> sf read FFFC0000 700000 10000
device 0 offset 0x700000, size 0x10000
SF: 65536 bytes @ 0x700000 Read: OK
Zynq> cmp.b FFFC0000 FFFD0000 10000
Total of 65536 byte(s) were the same
Zynq> sf read FFFC0000 710000 5764
device 0 offset 0x710000, size 0x5764
SF: 22372 bytes @ 0x710000 Read: OK
Zyng> cmp.b FFFC0000 FFFD0000 5764
Total of 22372 byte(s) were the same
Zyng> INFO: [Kicom 50-44] Elapsed time = 157 sec.

Verify Operation successful.

INFO: [Labtoolstcl 44-377] Flash programming completed successfully

program_hv=cfgmem: Time (s): cpu = 00:00:00; elapsed = 00:04:50. Memory (MB):
peak = 1090.781; gain = 7.383
INFO: [Labtoolstcl 44-464] Closing hw_target localhost:3121/xilinx_tcf/Xilinx/00
000acb466501
# disconnect_hw_server localhost:3121
INFO: [\overline{	ext{Common}} 17-206] Exiting vivado_lab at Tue Jan 15 14:25:59 2019...
Press any key to continue . . .
```



Use the Verify BAT files to check the BOOT.bin programmed into the Zynq QSPI

€	Zynq_SC_Firmware	9.64 1/14/2019 1:20:17 pm
		9.64 1/14/2019 1:20:17 pm
	■ BOOT.bin	7.08 8/28/2018 5:47:34 pm
	■ Jtag_connection_setup.jpg	2.21 8/28/2018 5:47:34 pm
	programming_README.txt	1,054 8/28/2018 5:47:34 pm
	■ program_sysctrl.bat	764 10/30/2018 3:09:33 pm
	■ program_sysctrl.tcl	2,316 10/30/2018 2:30:38 pm
	■ program_sysctrltcl	2,148 10/30/2018 2:29:33 pm
	• verify_sysctrl.bat	763 10/30/2018 3:09:33 pm
	∎ verify_sysctrl.tcl	2,321 10/30/2018 3:04:45 pm
	■ vivado_lab.jou	725 10/30/2018 3:08:51 pm
	■ vivado_lab.log	4,041 10/30/2018 3:08:51 pm
	■ vivado_lab_10248.backup.jou	728 10/30/2018 2:47:39 pm
	■ vivado_lab_10248.backup.log	4,338 10/30/2018 2:47:39 pm
	zynq_1b_debug_fsbl.elf	339 KB 8/28/2018 5:47:34 pm

Note: Verify will not pass after Restore Board Defaults has been run. This is the as-shipped condition. Safe to reprogram, verify, then perform Restore step.



References



References

> Vivado Release Notes

- >> Vivado Design Suite User Guide Release Notes UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ ug973-vivado-release-notes-install-license.pdf
- Vivado Design Suite 2019 Vivado Known Issues
 - https://www.xilinx.com/support/answers/72162.html

> Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide UG908
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ ug908-vivado-programming-debugging.pdf



Documentation



Documentation

- > Virtex UltraScale+ HBM
 - Virtex UltraScale+ FPGA Family
 - https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html

> VCU128 Documentation

- Virtex UltraScale+ FPGA VCU128 Evaluation Kit
 - https://www.xilinx.com/products/boards-and-kits/vcu128.html
- » VCU128 Board User Guide UG1302
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu128/ ug1302-vcu128-eval-bd.pdf
- >> VCU128 Known Issues and Release Notes Master Answer Record
 - https://www.xilinx.com/support/answers/71849.html

