

VCU128 MIG Design Creation

March 2019



Revision History

Date	Version	Description
03/21/19	1.1	Added Board Flow Files ZIP.
12/10/18	1.0	Initial version.

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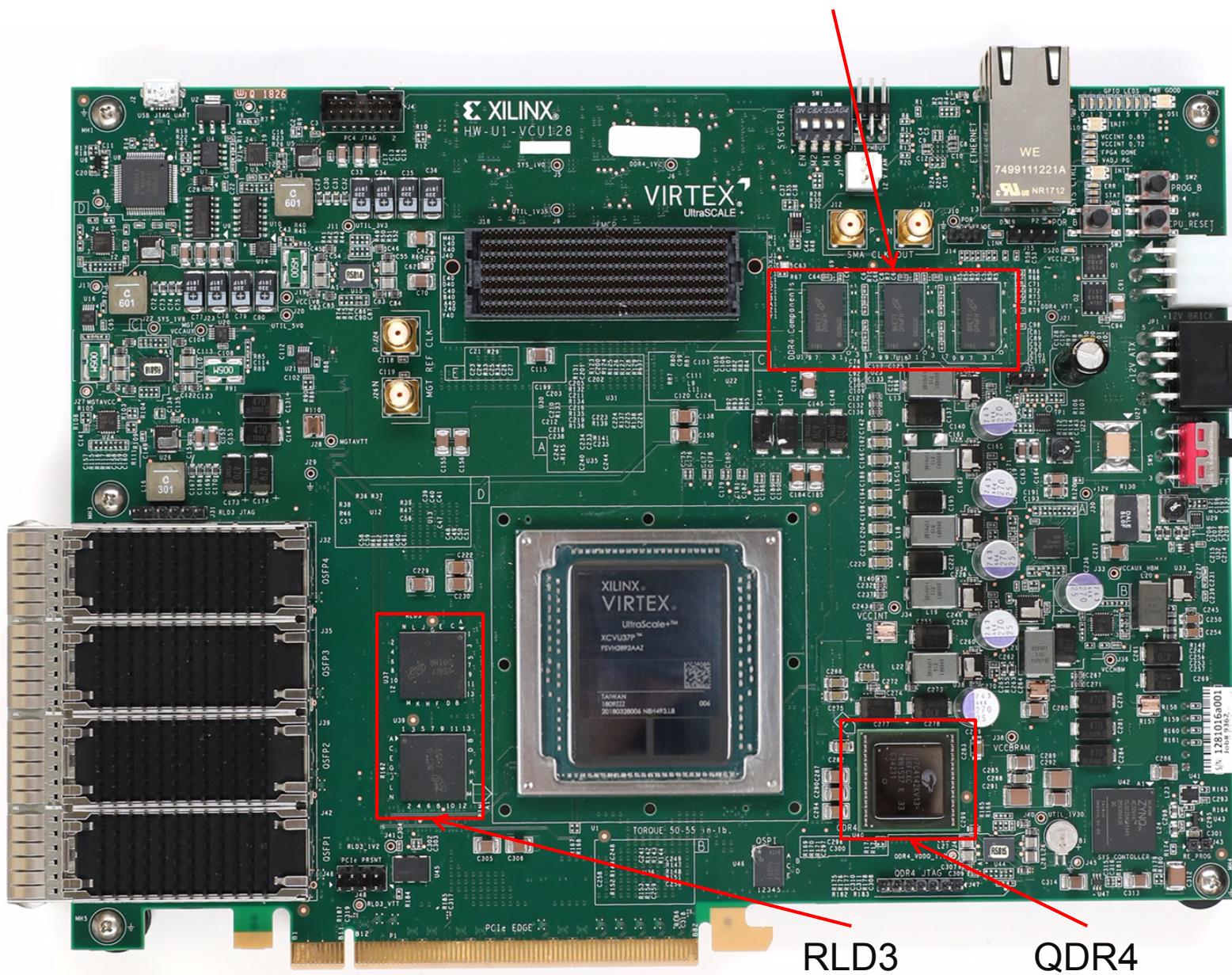
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Overview

- > **Xilinx VCU128 Board**
- > **Software Requirements**
- > **Run MIG Example Designs**
- > **Generate MIG DDR4 Example Design**
 - » Modifications to Example Design
 - » Compile Example Design
 - » VCU128 Setup
 - » Run MIG Example Design
- > **Generate MIG RLD3 Example Design**
- > **Generate MIG QDR Example Design**
- > **References**

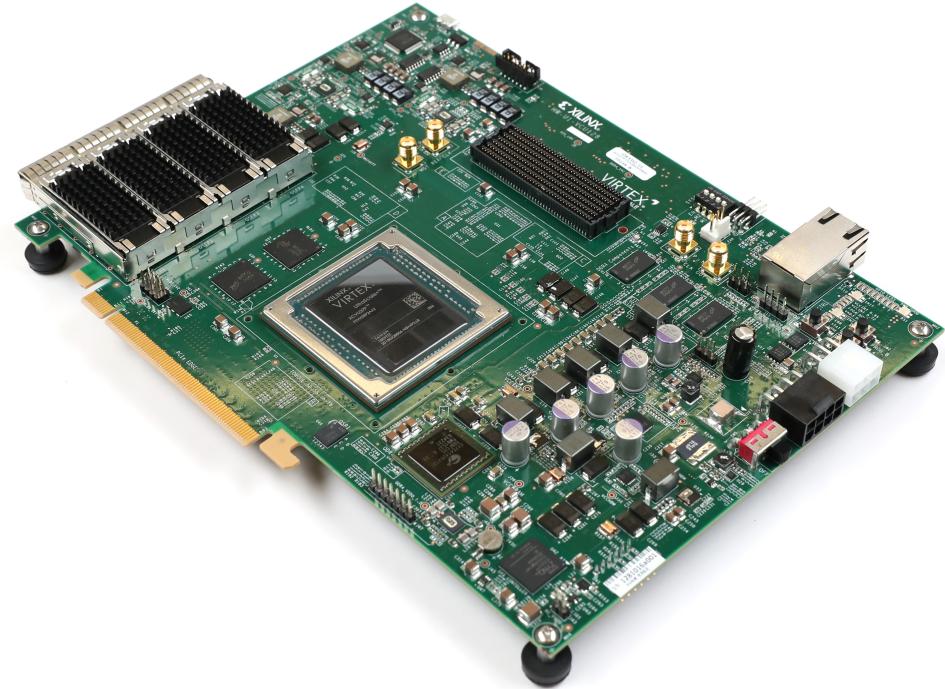
Xilinx VCU128 Board

DDR4 Front & Rear



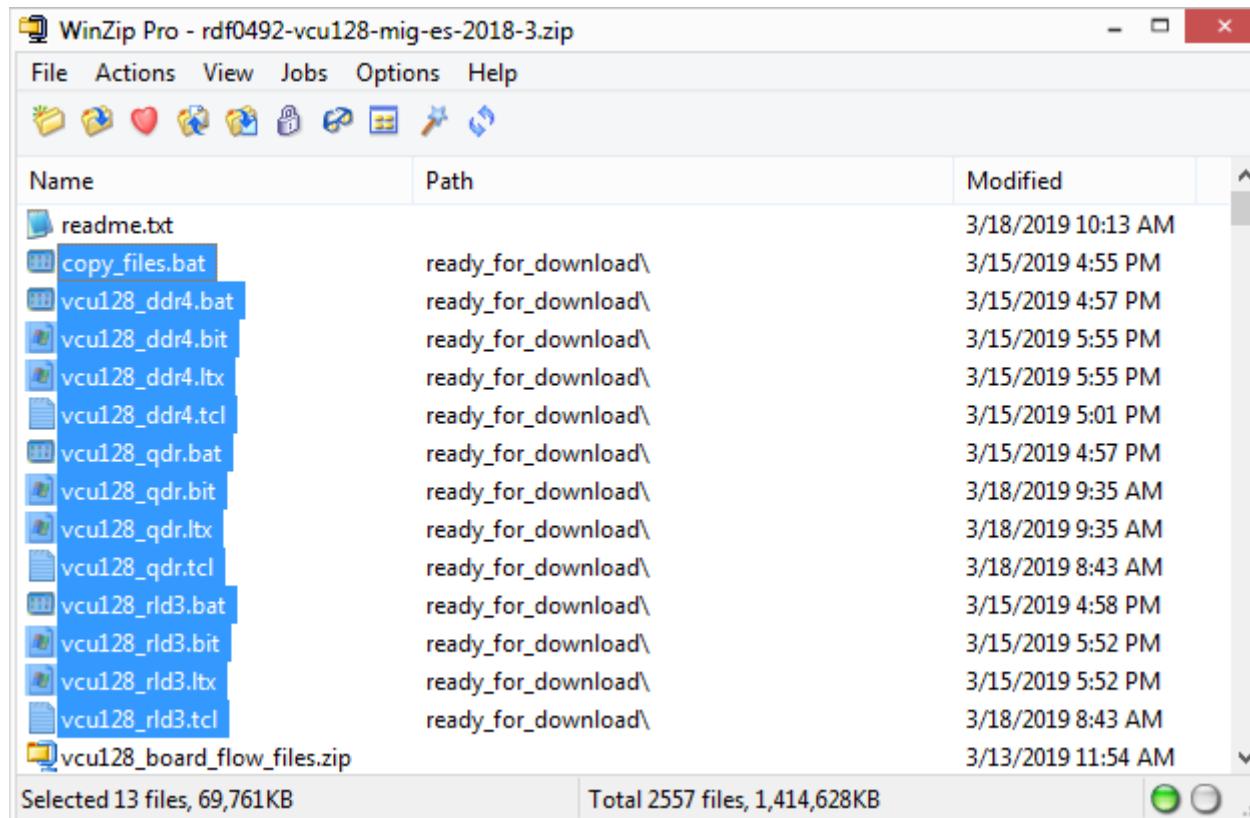
VCU128 Software Install and Board Setup

- > Complete setup steps in XTP449 – VCU128 Software Install and Board Setup:
 - » Software Requirements
 - » VCU128 Board Setup



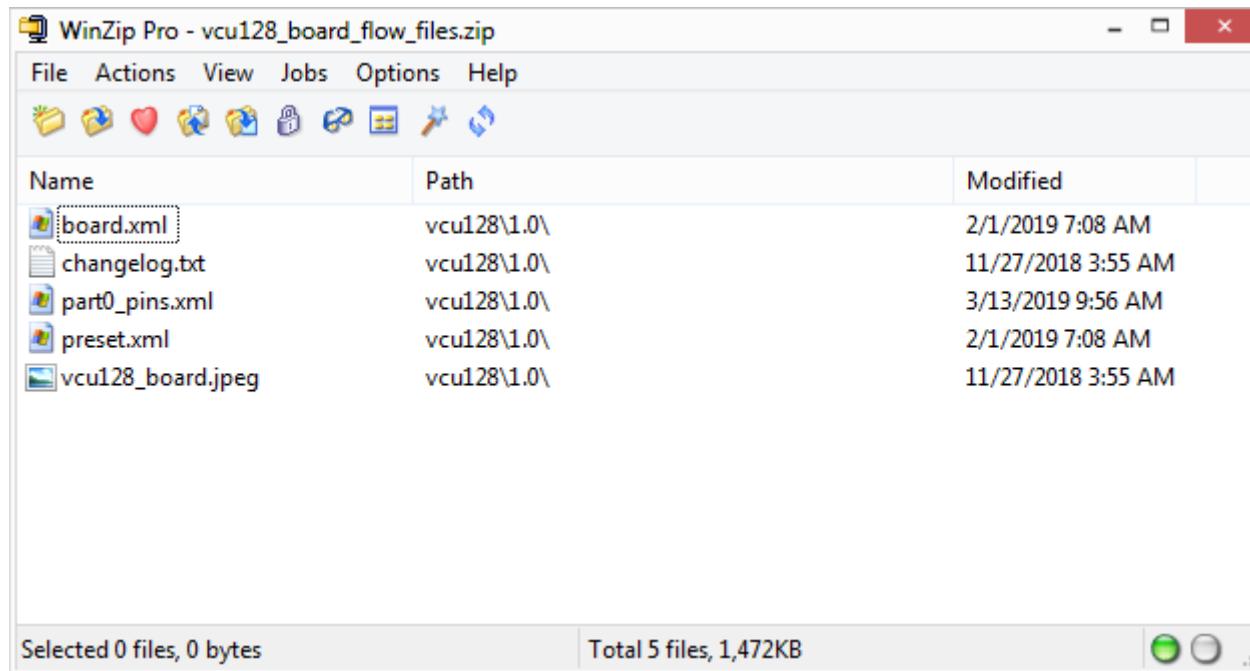
VCU128 Setup

- > Open the RDF0492 - VCU128 MIG Design Files (2018.3 C) ZIP file, and extract the “ready_for_download” files to your C:\ drive:



VCU128 Setup

- > Extract the VCU128 Board Flow Files to
C:\Xilinx\Vivado\2018.3\data\boards\board_files



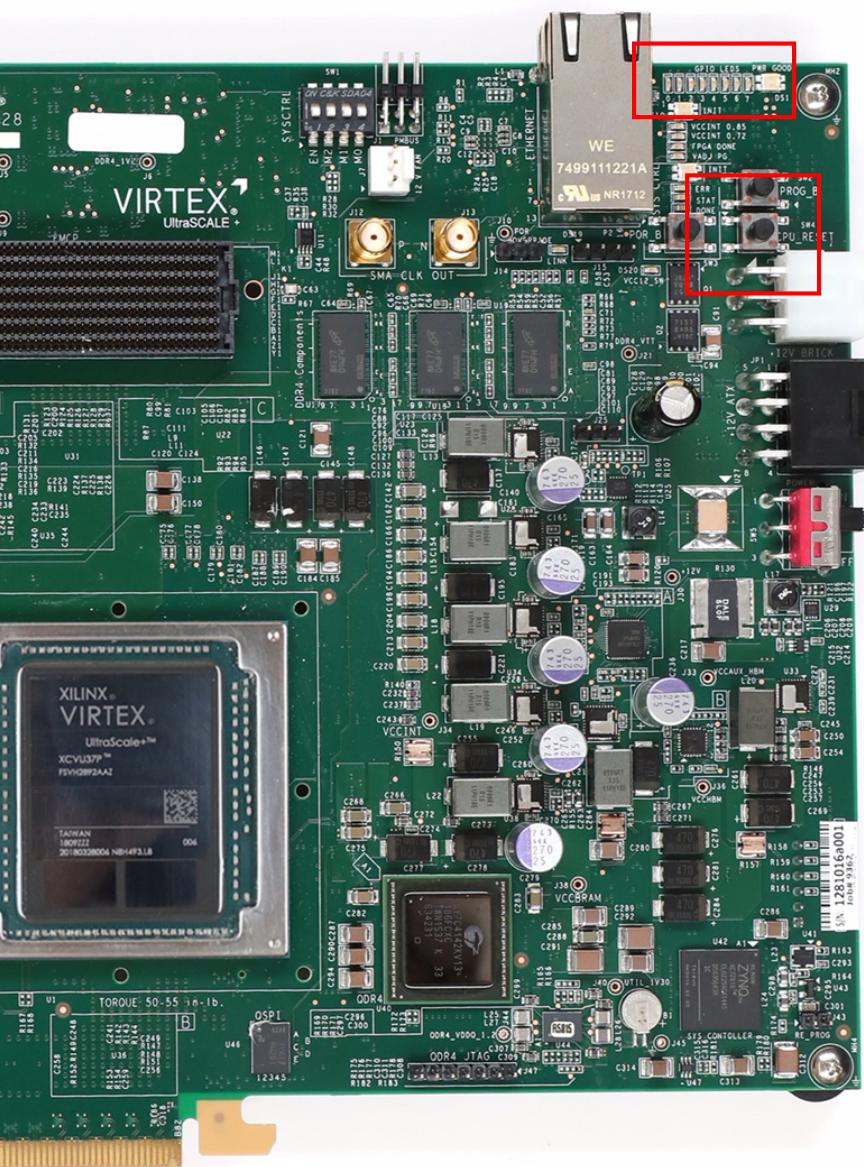
Note: Board Flow Files are also available in the Xilinx Board Store:

<https://github.com/Xilinx/XilinxBoardStore/tree/2018.3/boards/Xilinx>

Run MIG Example Designs



Run MIG Example Design



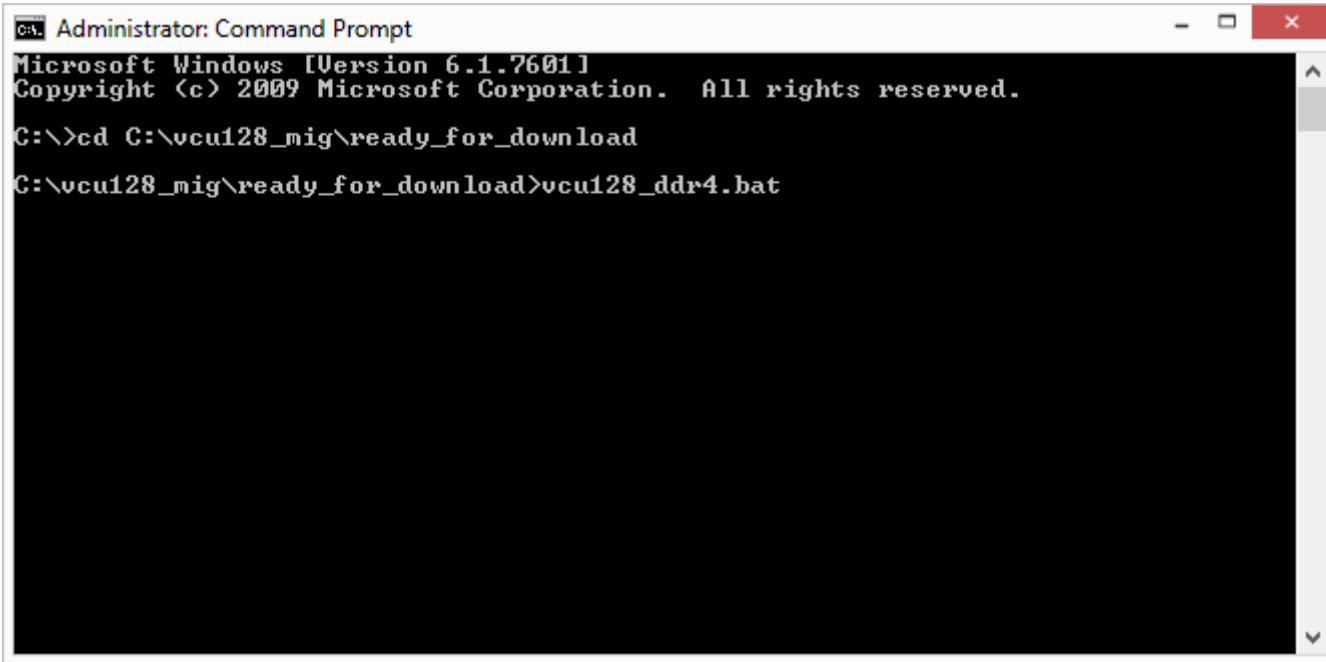
- > For the following tests:
- > After bitstream loads, LED 0 (left most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW4, is the reset

Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\vcu128_mig\ready_for_download  
vcu128_ddr4.bat
```

- > View results on LEDs



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

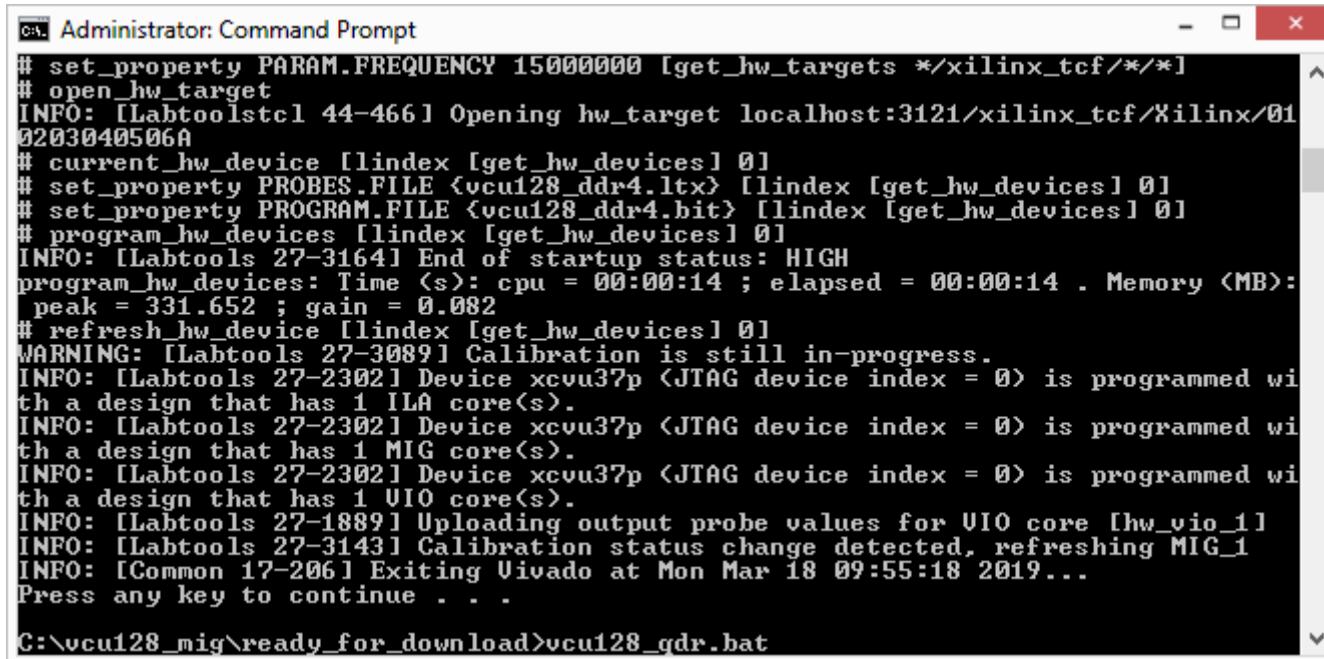
C:>cd C:\vcu128_mig\ready_for_download
C:\vcu128_mig\ready_for_download>vcu128_ddr4.bat
```

Run MIG Example Design

- > Type:

vcu128_qdr.bat

- > View results on LEDs



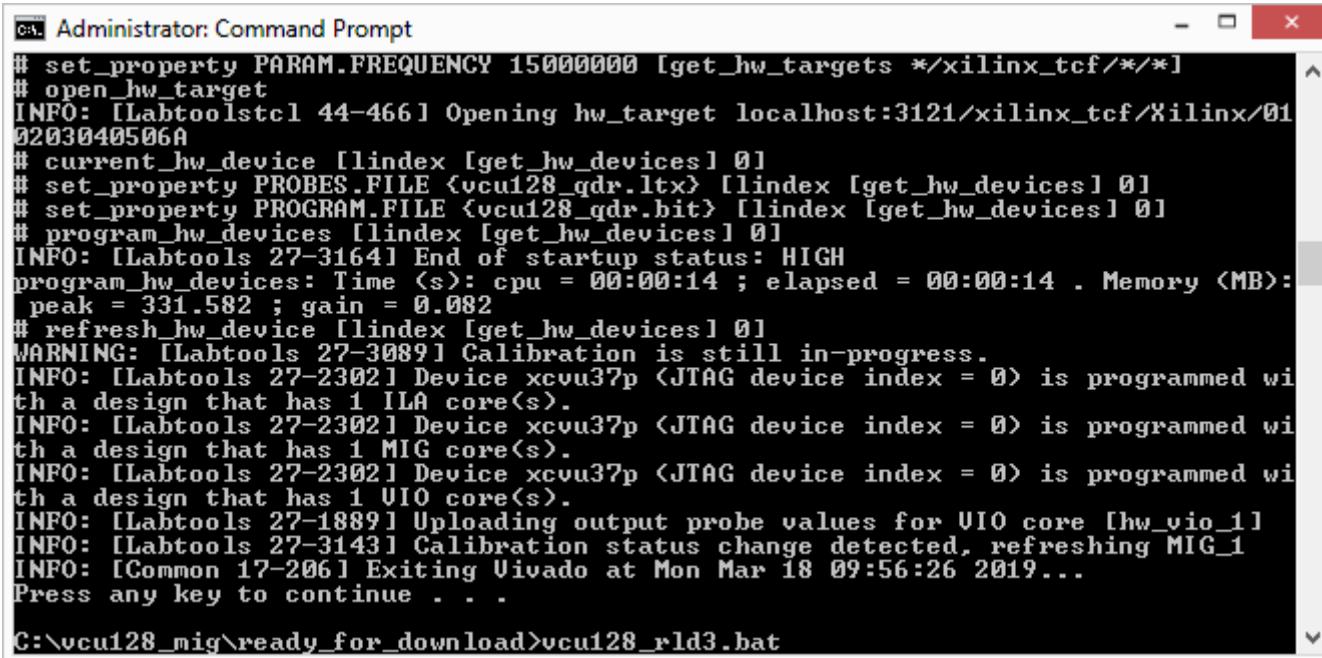
```
C:\ Administrator: Command Prompt
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/*/*]
# open_hw_target
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Xilinx/01
0203040506A
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu128_ddr4.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu128_ddr4.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:14 ; elapsed = 00:00:14 . Memory <MB>:
peak = 331.652 ; gain = 0.082
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu37p (JTAG device index = 0) is programmed wi-
th a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu37p (JTAG device index = 0) is programmed wi-
th a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu37p (JTAG device index = 0) is programmed wi-
th a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
INFO: [Labtools 27-3143] Calibration status change detected, refreshing MIG_1
INFO: [Common 17-206] Exiting Vivado at Mon Mar 18 09:55:18 2019...
Press any key to continue . . .
C:\vcu128_mig\ready_for_download>vcu128_qdr.bat
```

Run MIG Example Design

- > Type:

vcu128_rld3.bat

- > View results on LEDs



```
C:\ Administrator: Command Prompt
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/*/*]
# open_hw_target
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Xilinx/01
0203040506A
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu128_qdr.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu128_qdr.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:14 ; elapsed = 00:00:14 . Memory <MB>:
peak = 331.582 ; gain = 0.082
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu37p (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu37p (JTAG device index = 0) is programmed with a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu37p (JTAG device index = 0) is programmed with a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
INFO: [Labtools 27-3143] Calibration status change detected, refreshing MIG_1
INFO: [Common 17-206] Exiting Vivado at Mon Mar 18 09:56:26 2019...
Press any key to continue . . .
C:\vcu128_mig\ready_for_download>vcu128_rld3.bat
```

Generate MIG DDR4 Example Design

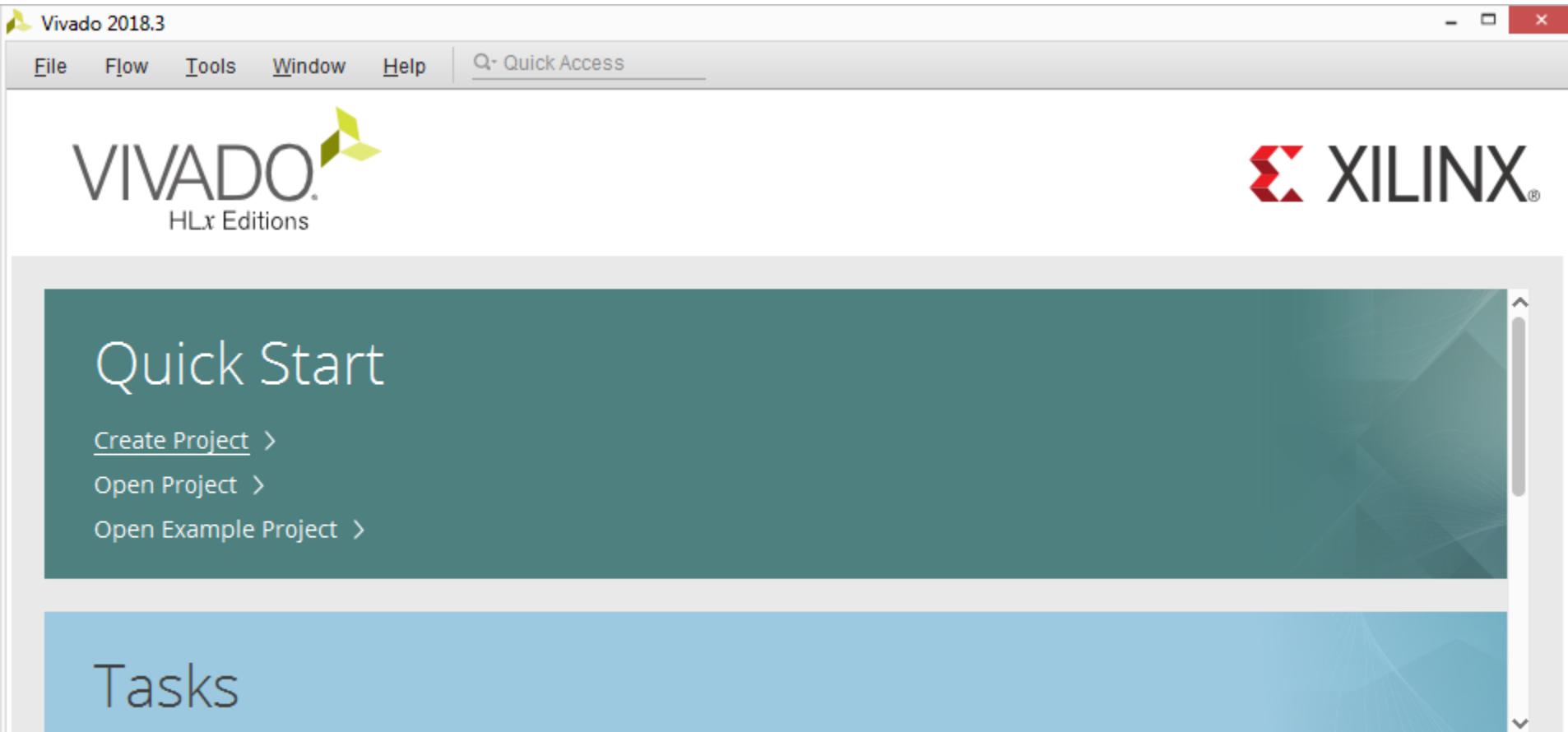


Generate MIG DDR4 Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2018.3 → Vivado

> Select Create Project



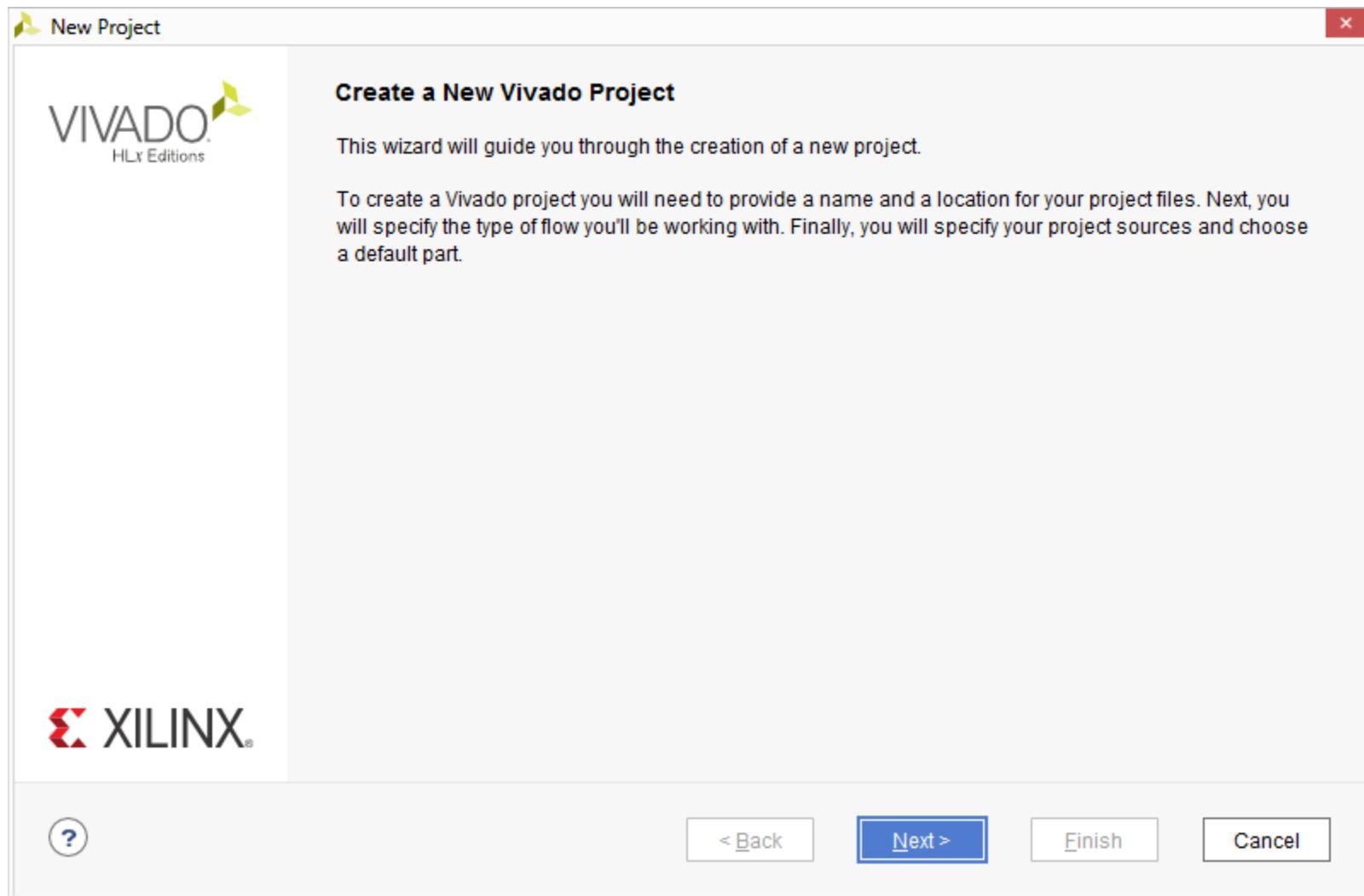
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU128

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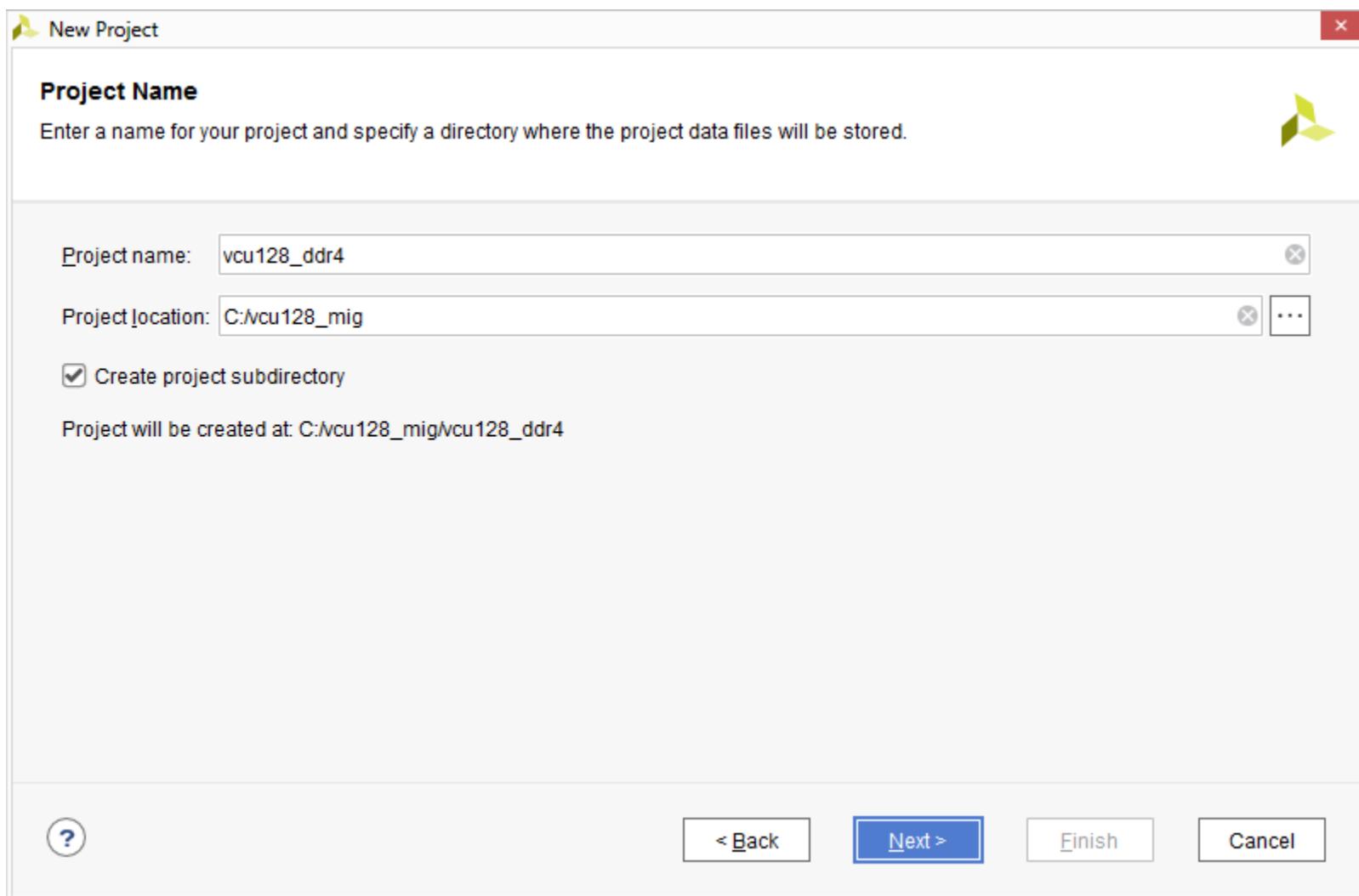
Generate MIG DDR4 Example Design

> Click Next



Generate MIG DDR4 Example Design

- > Set the Project name to vcu128_ddr4 and location to C:/vcu128_mig
 - » Check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Generate MIG DDR4 Example Design

> Select RTL Project

» Select Do not specify sources at this time

The screenshot shows the 'New Project' dialog box with the title 'Project Type'. It asks to 'Specify the type of project to create.' There are five options:

- RTL Project: You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time
- Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time
- I/O Planning Project: Do not specify design sources. You will be able to view part/package resources.
- Imported Project: Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project: Create a new Vivado project from a predefined template.

At the bottom are buttons: '?', '< Back', 'Next >', 'Finish', and 'Cancel'.

Generate MIG DDR4 Example Design

- > Under Boards, select the VCU128

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Vendor: All Name: All

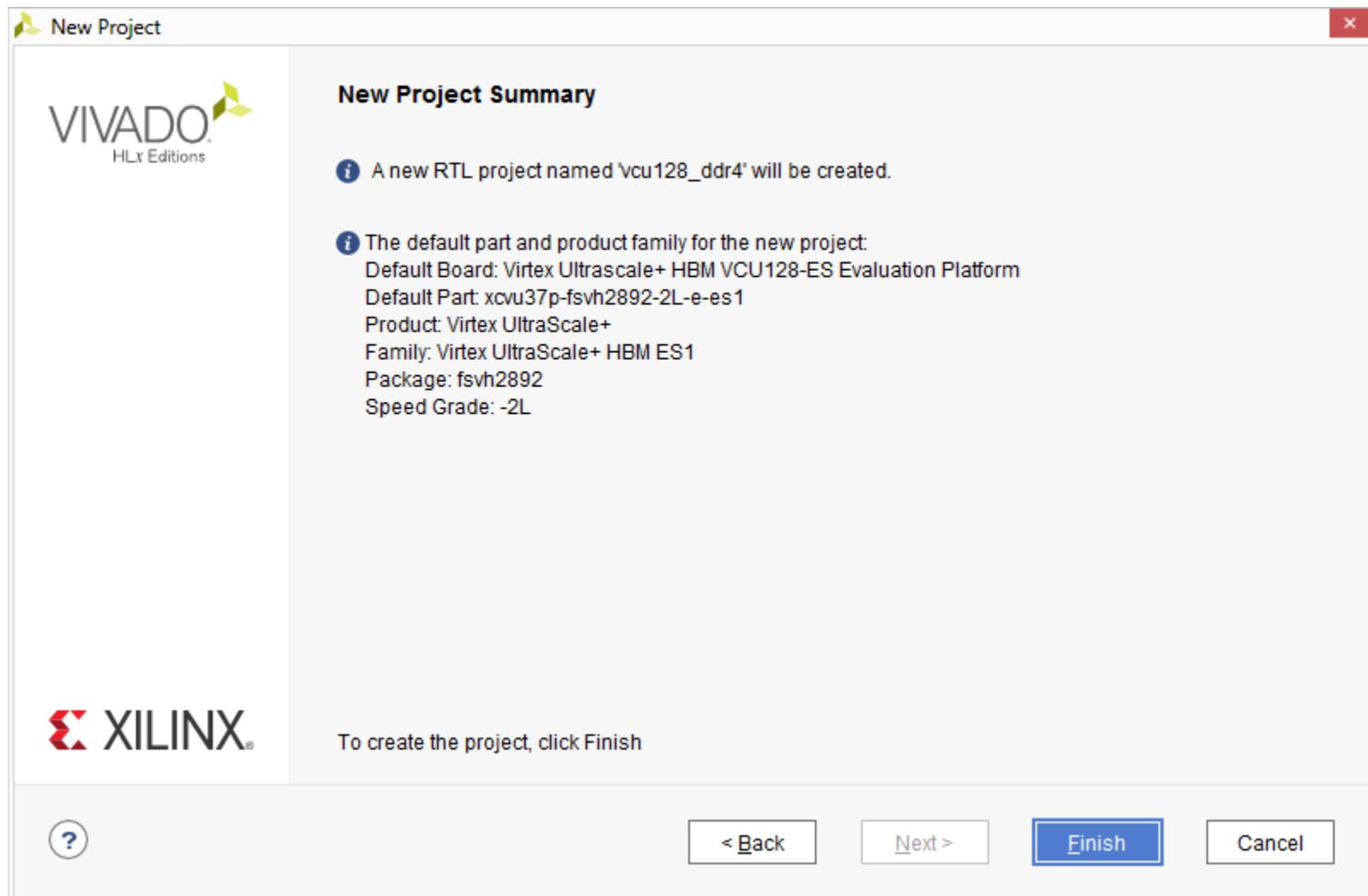
Search: Q-

Display Name	Preview	Vendor	File Version	Part
Virtex-UltraScale VCU110 Evaluation Platform Add Daughter Card Connections		xilinx.com	1.4	xcvu190
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0	xcvu9p-
Virtex Ultrascale+ HBM VCU128-ES Evaluation Platform		xilinx.com	1.0	xcvu37p

< Back Next > Finish Cancel

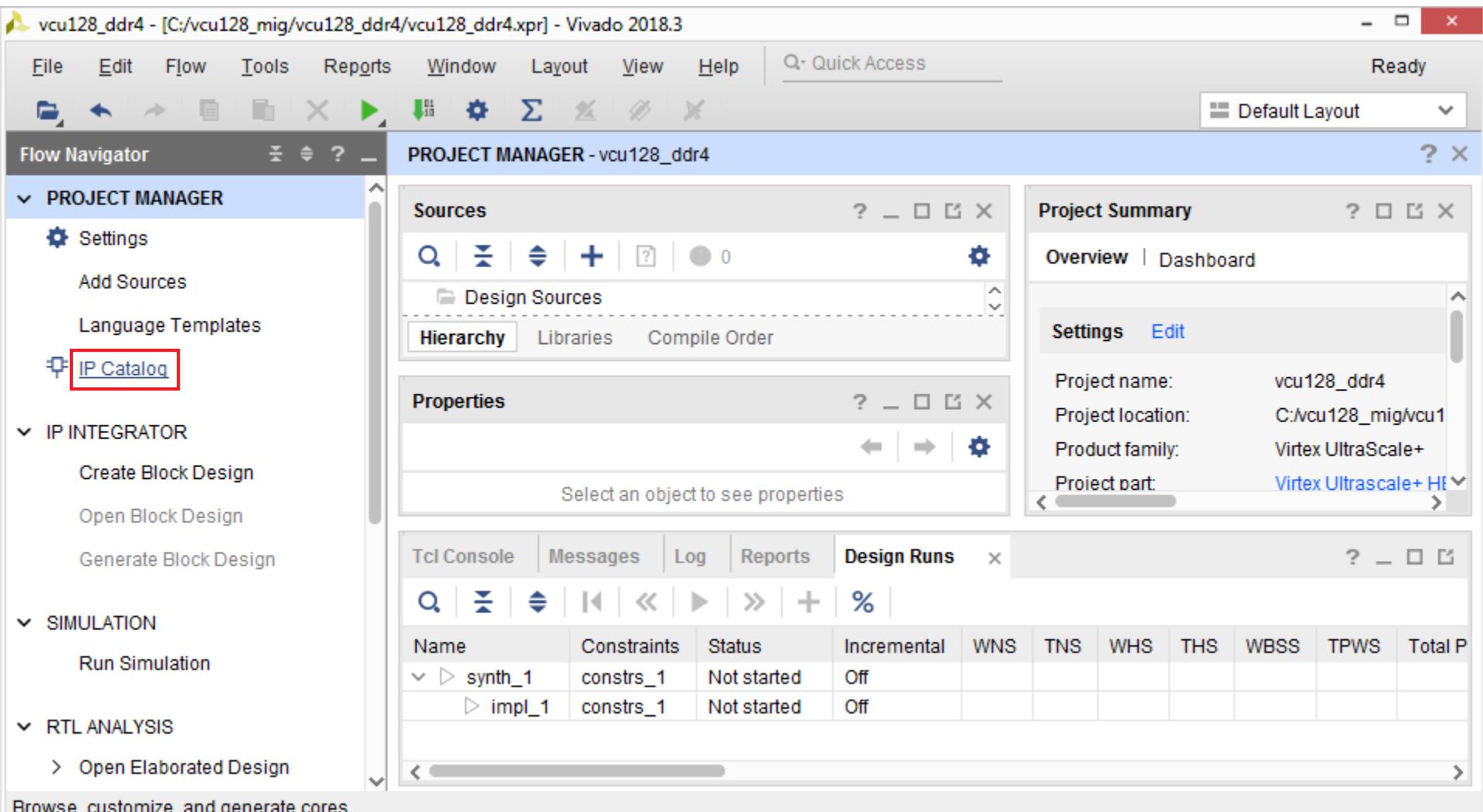
Generate MIG DDR4 Example Design

> Click Finish



Generate MIG DDR4 Example Design

> Click on IP Catalog



Generate MIG DDR4 Example Design

> Select DDR4 SDRAM (MIG), v2.2

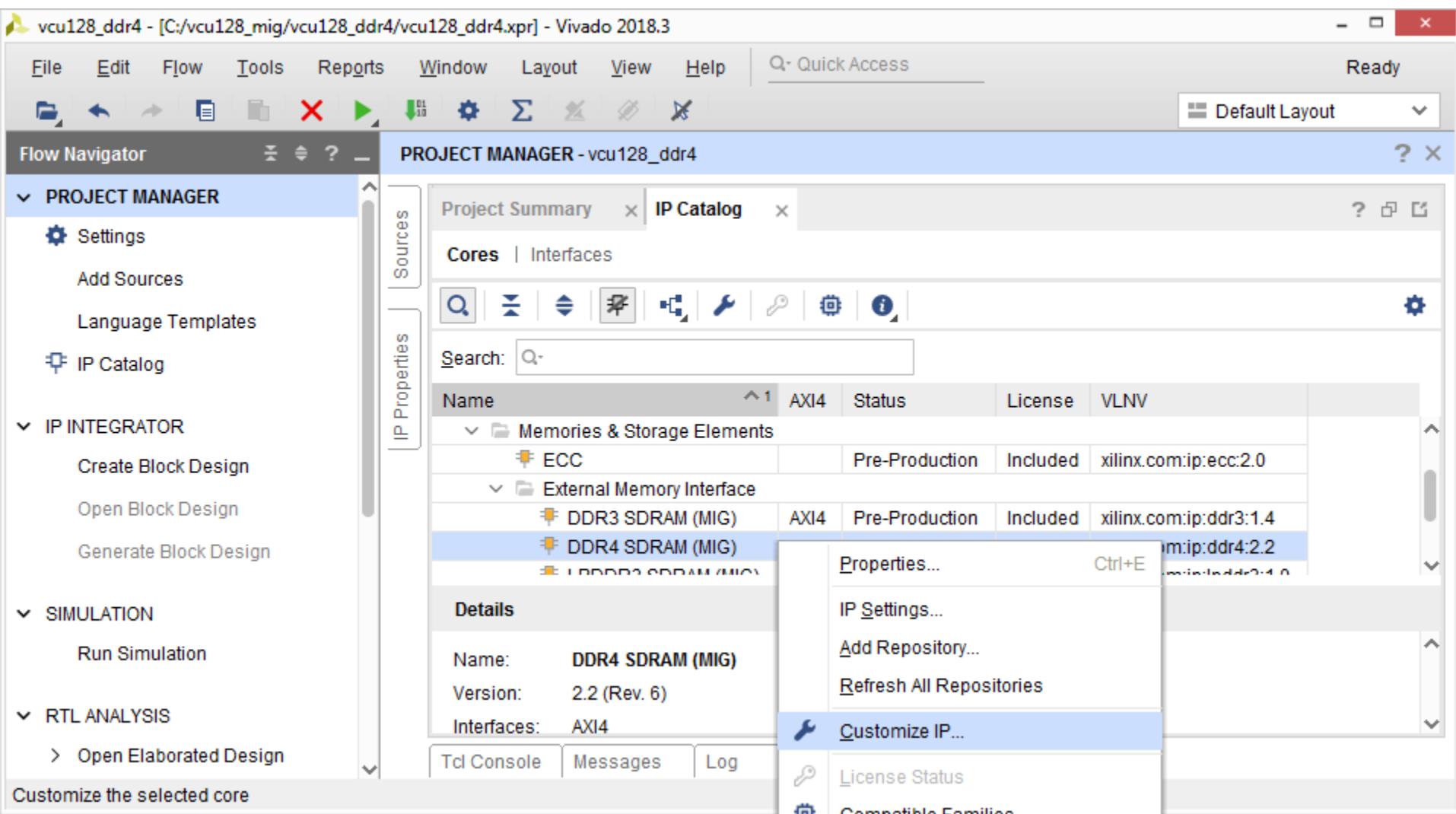
The screenshot shows the Vivado 2018.3 interface with the project "vcu128_ddr4" open. The left sidebar contains the "PROJECT MANAGER" section with options like Settings, Add Sources, Language Templates, and IP Catalog. The "IP Catalog" option is currently selected. The main area displays the "PROJECT MANAGER - vcu128_ddr4" window. In the center, the "IP Catalog" tab is active, showing a search bar and a table of IP components. The table includes columns for Name, AXI4, Status, License, and VLN. The "Memories & Storage Elements" category is expanded, showing "ECC" and "External Memory Interface". Under "External Memory Interface", "DDR3 SDRAM (MIG)" and "DDR4 SDRAM (MIG)" are listed. The "DDR4 SDRAM (MIG)" row is highlighted with a blue selection bar. Below the table, a "Details" panel shows the selected component's name, version (2.2 (Rev. 6)), and interfaces (AXI4). At the bottom of the window, there are tabs for Tcl Console, Messages, Log, Reports, and Design Runs.

Name	AXI4	Status	License	VLAN
ECC		Pre-Production	Included	xilinx.com:ip:ecc:2.0
External Memory Interface				
DDR3 SDRAM (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip:ddr3:1.4
DDR4 SDRAM (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip:ddr4:2.2
DDR4 SDRAM (MIG)		Pre-Production	Included	xilinx.com:ip:ddr4:2.2

Generate MIG DDR4 Example Design

- > Right click on DDR4 SDRAM (MIG)

- » Select Customize IP

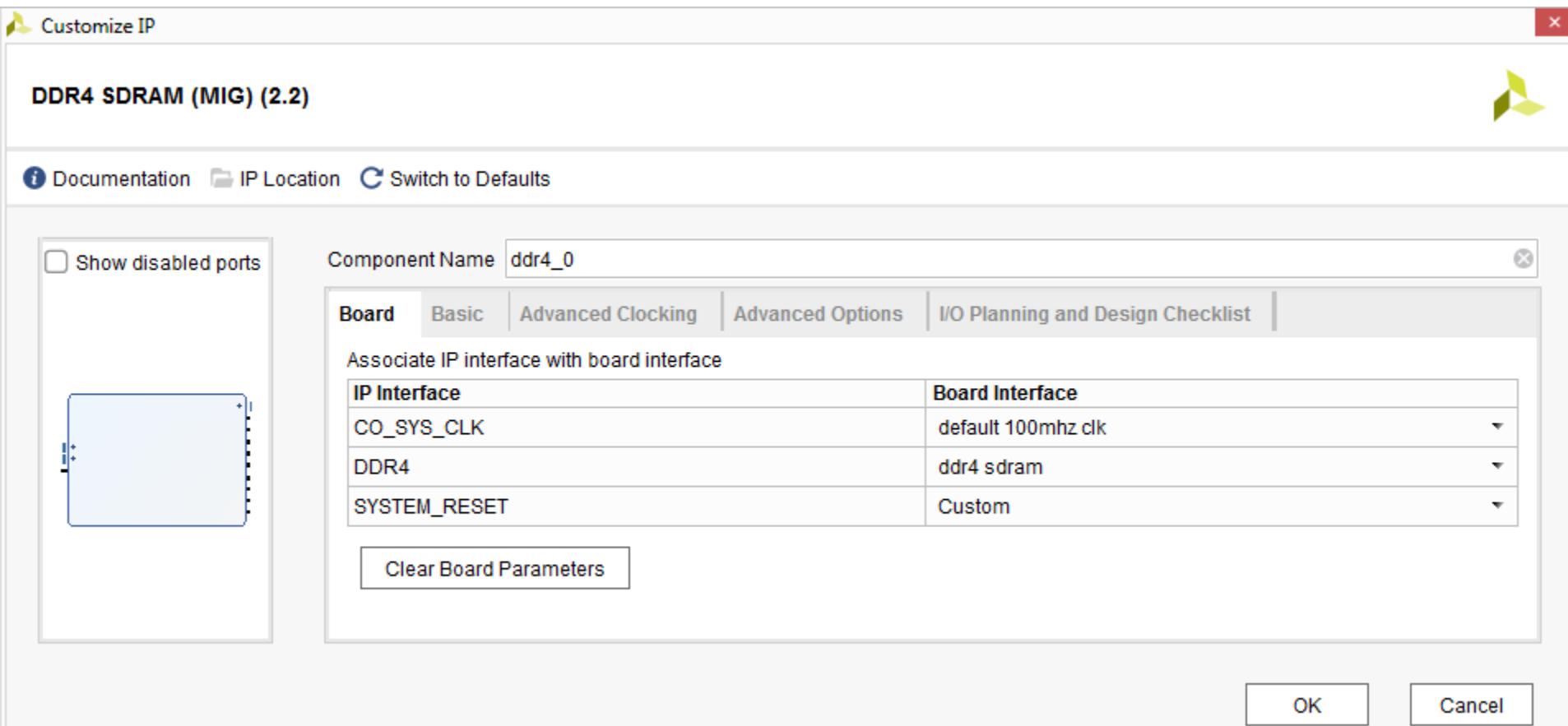


Note: Presentation applies to the VCU128

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Generate MIG DDR4 Example Design

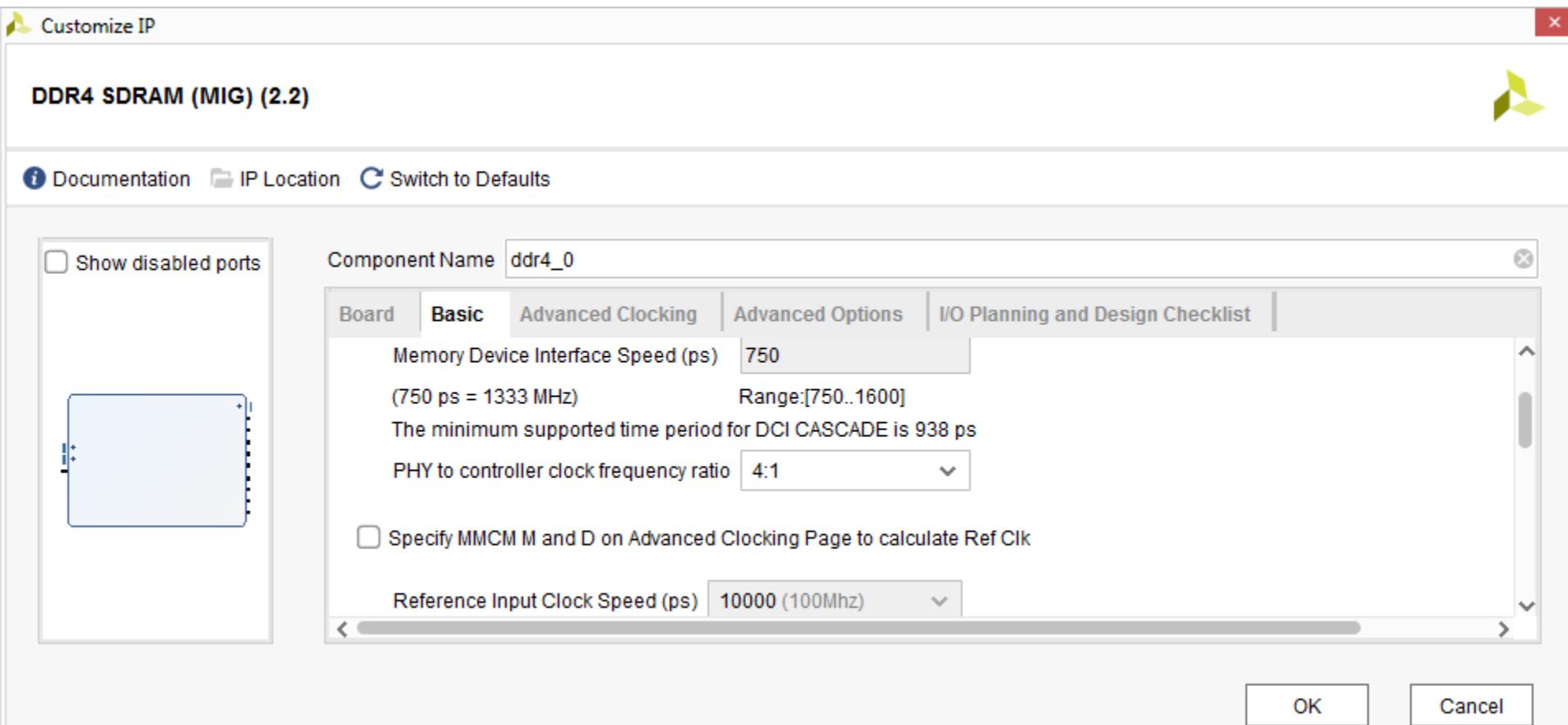
- > Under the Board tab, set the DDR4 interfaces
 - » Set **C0_SYS_CLK** to default 100mhz clk
 - » Set **DDR4** to **ddr4 sdram**
 - » Set **SYSTEM_RESET** to **Custom**



Generate MIG DDR4 Example Design

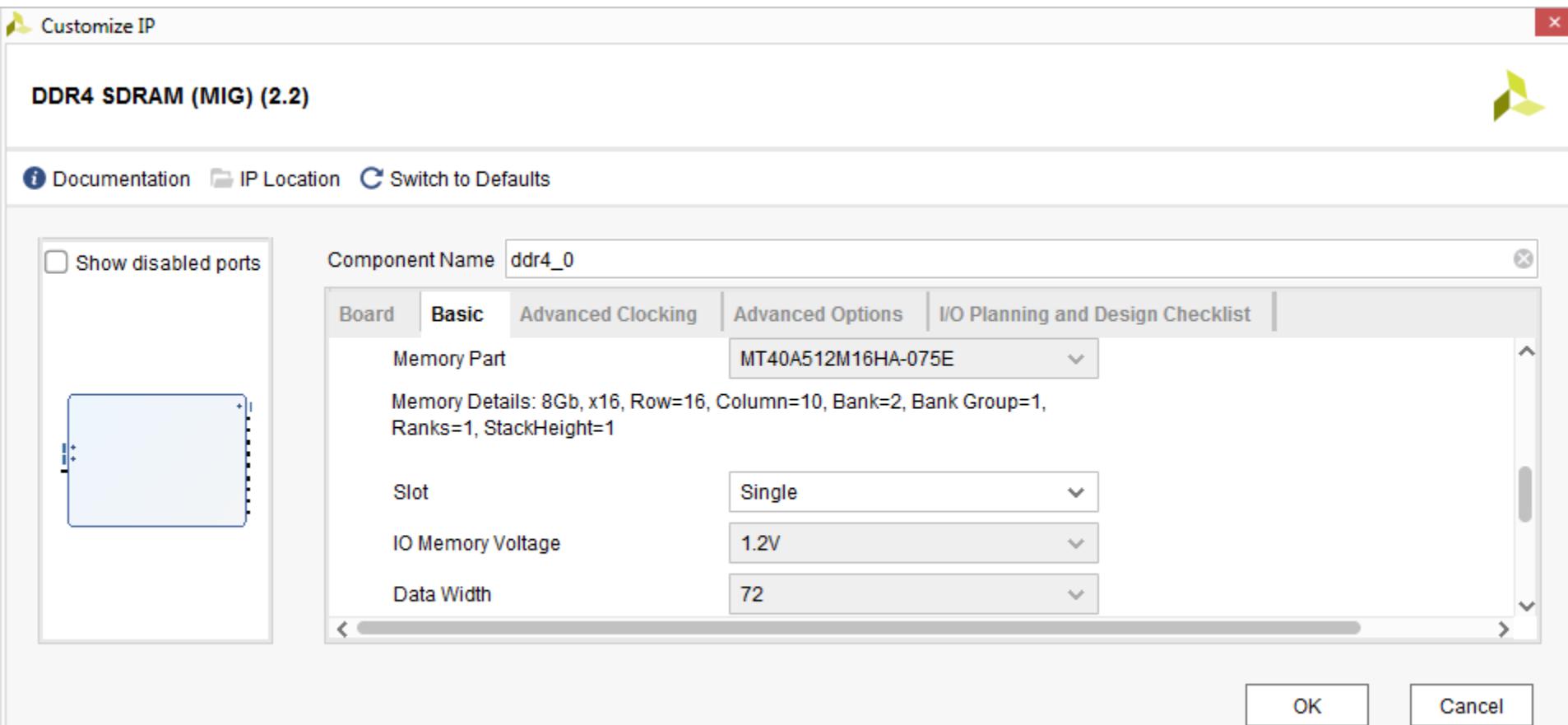
> Under the Basic tab

- » The Clock period is set to **750** for **2667 Mb/s** operation.
- » The Input Clock is set to **10000 ps** for **100 MHz**
- » Scroll down



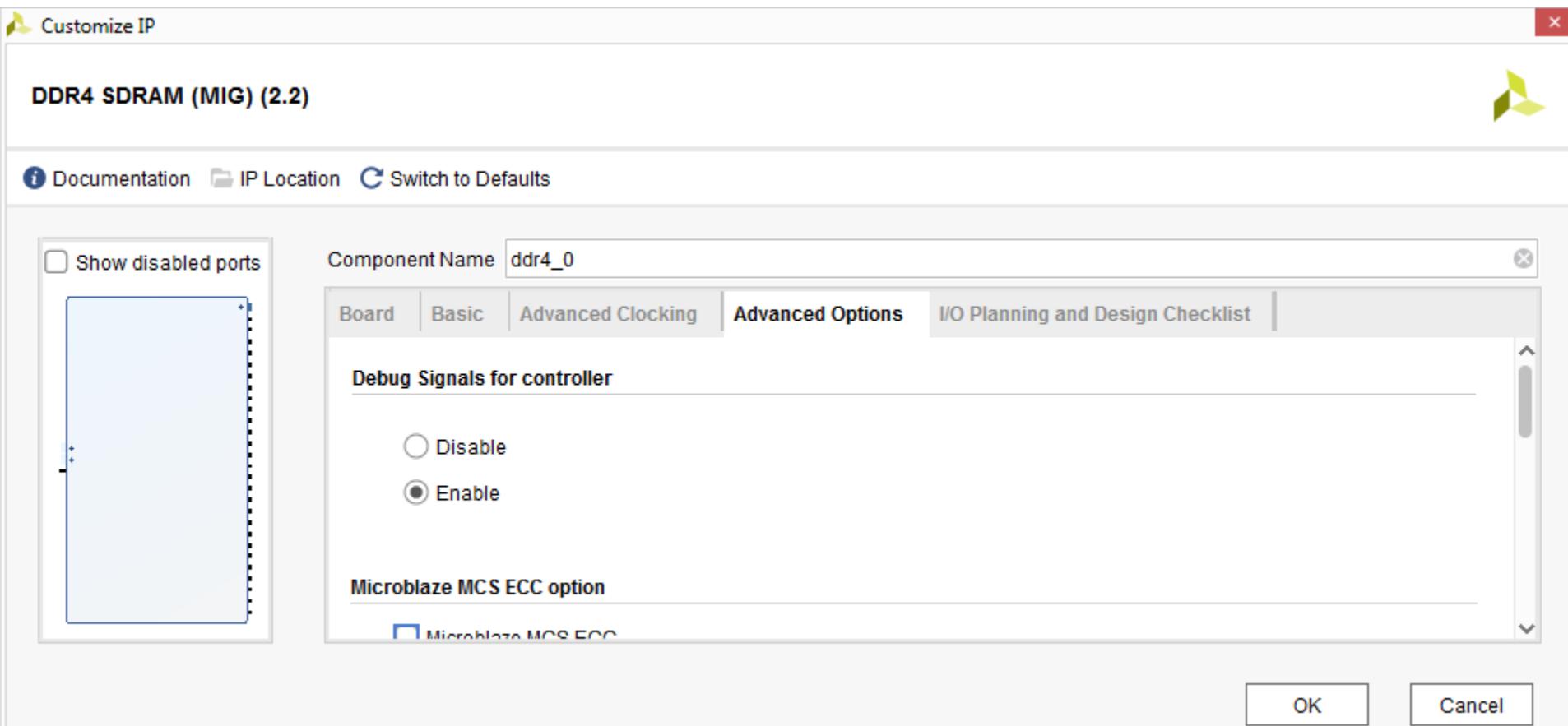
Generate MIG DDR4 Example Design

- > The part is set to MT40A512M16HA-075E
- > The Data Width is set to 72
- > Click the Advanced Options tab



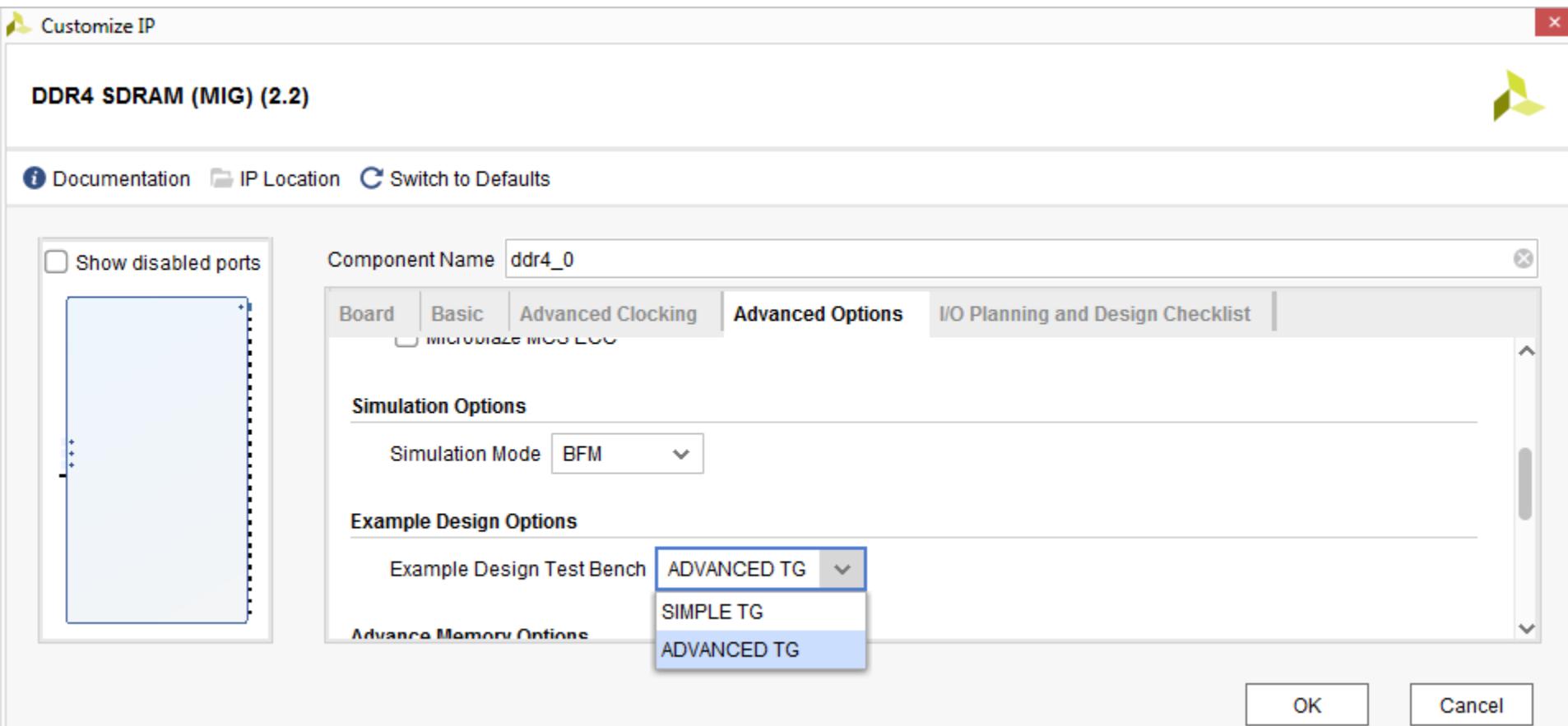
Generate MIG DDR4 Example Design

- > Set the Debug Signals to Enable
- > Scroll down



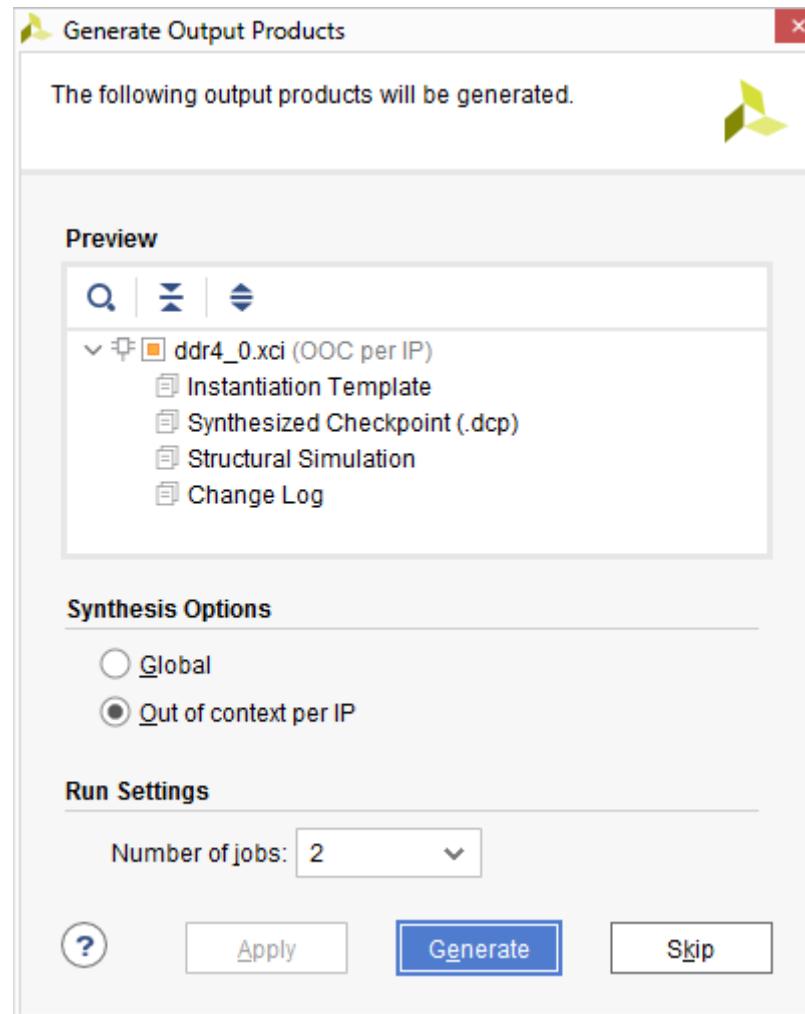
Generate MIG DDR4 Example Design

- > Set the Example Design Test Bench to ADVANCED TG
- > Click OK



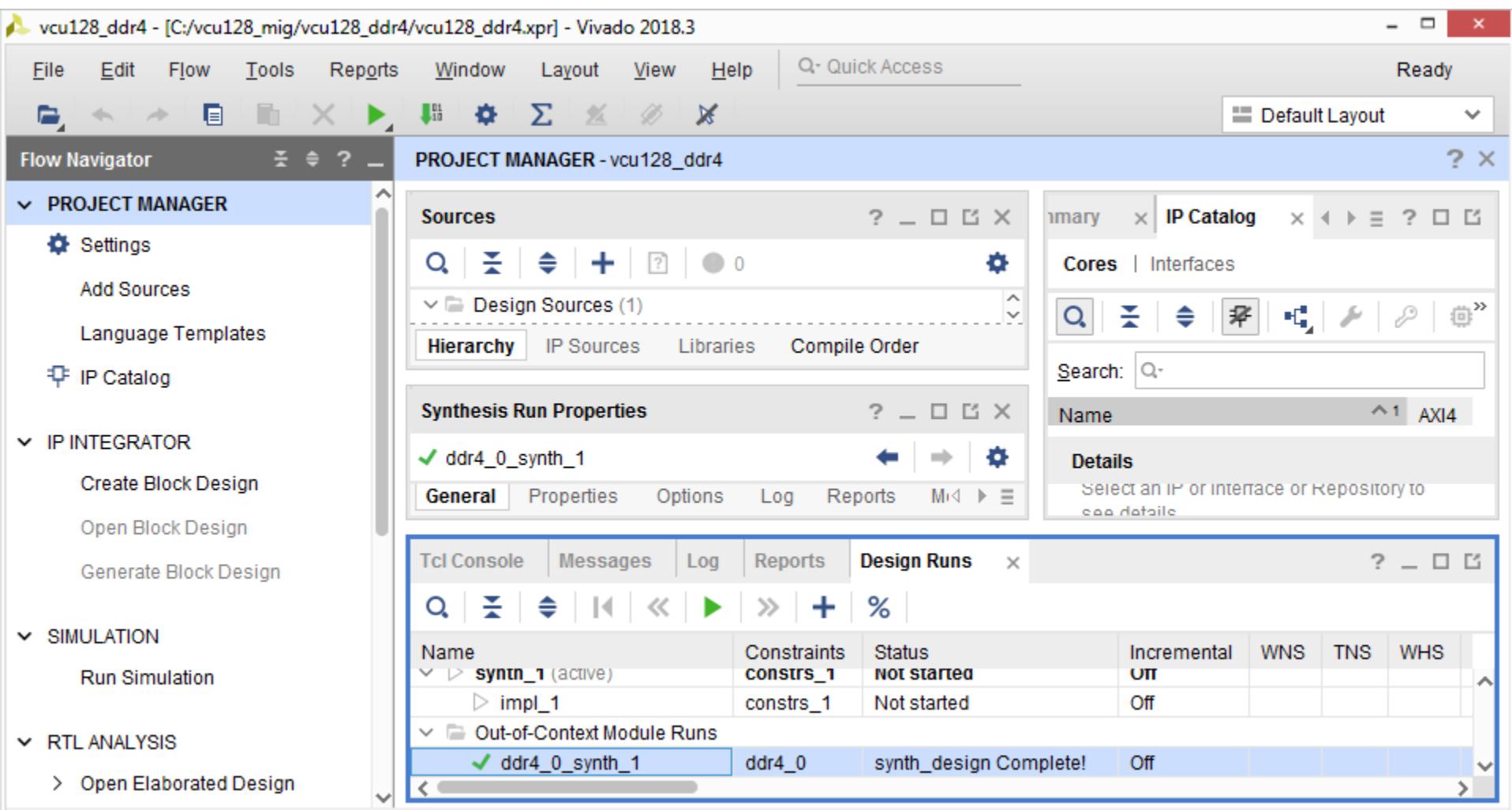
Generate MIG DDR4 Example Design

> Click Generate



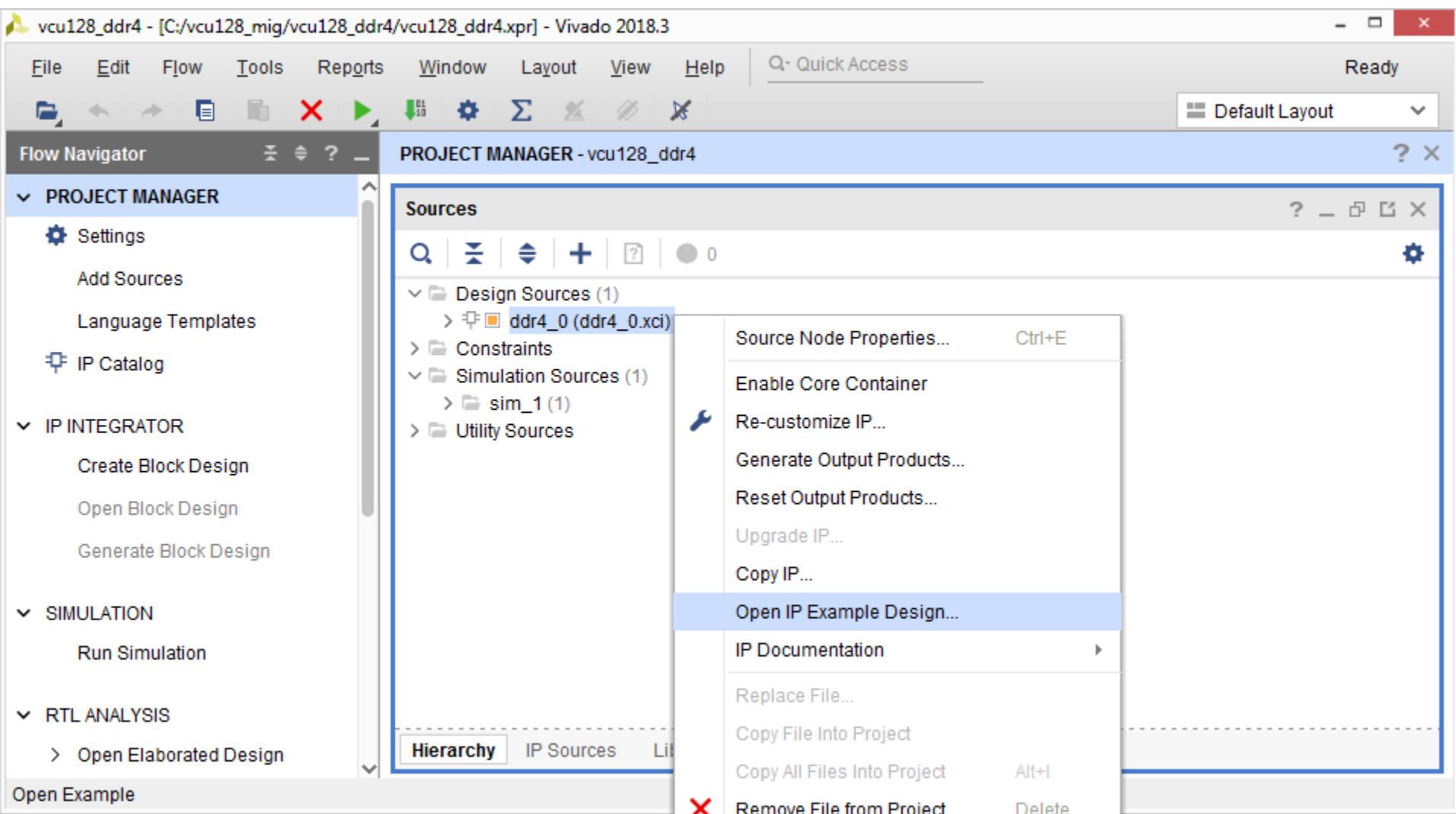
Generate MIG DDR4 Example Design

- > Wait until checkmark appears on ddr4_0_synth_1



Compile Example Design

- > Right click on ddr4_0 and select Open IP Example Design...

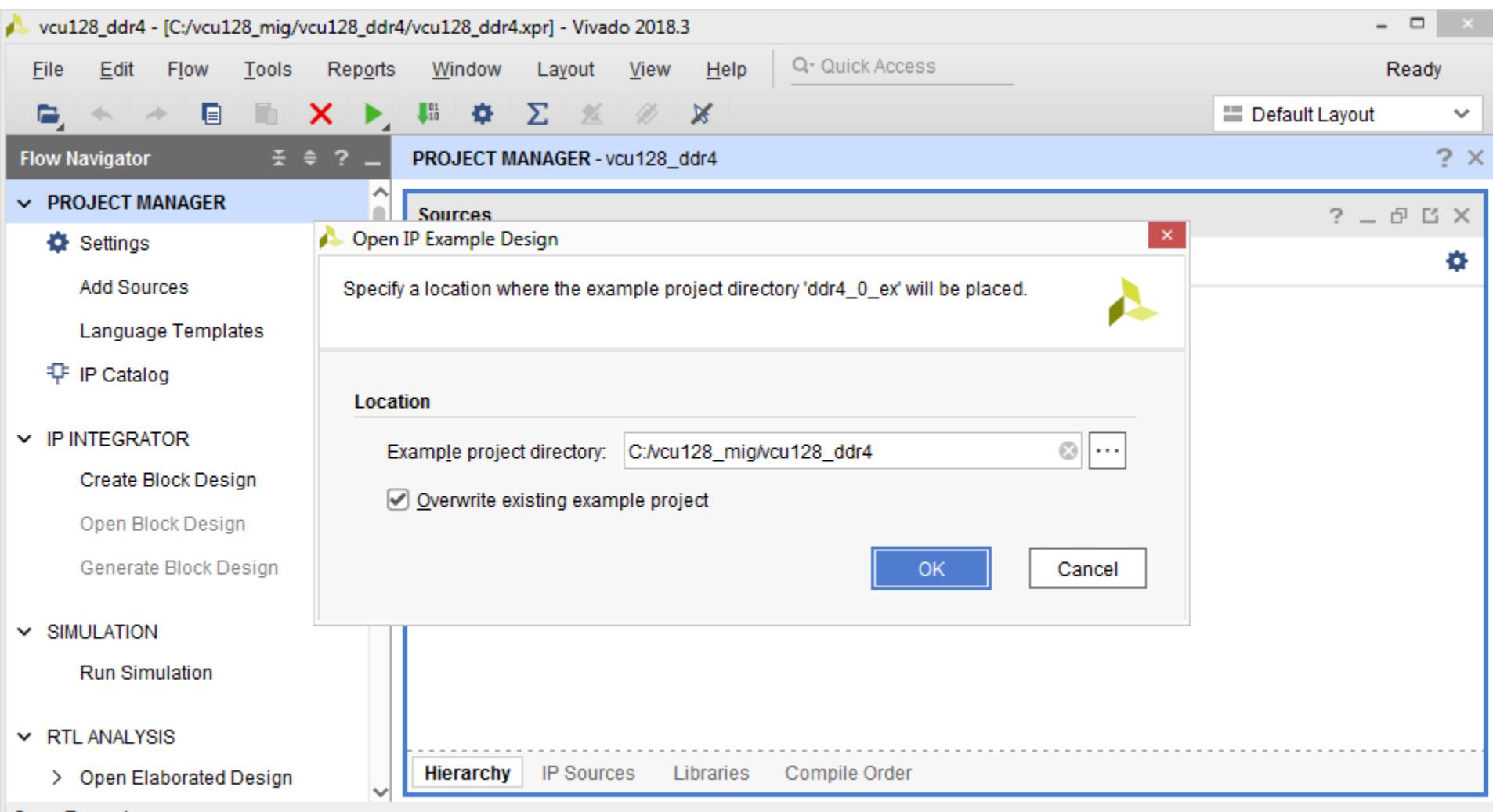


Note: Presentation applies to the VCU128

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Compile Example Design

- > Set the location to C:/vcu128_mig/vcu128_ddr4 and click OK

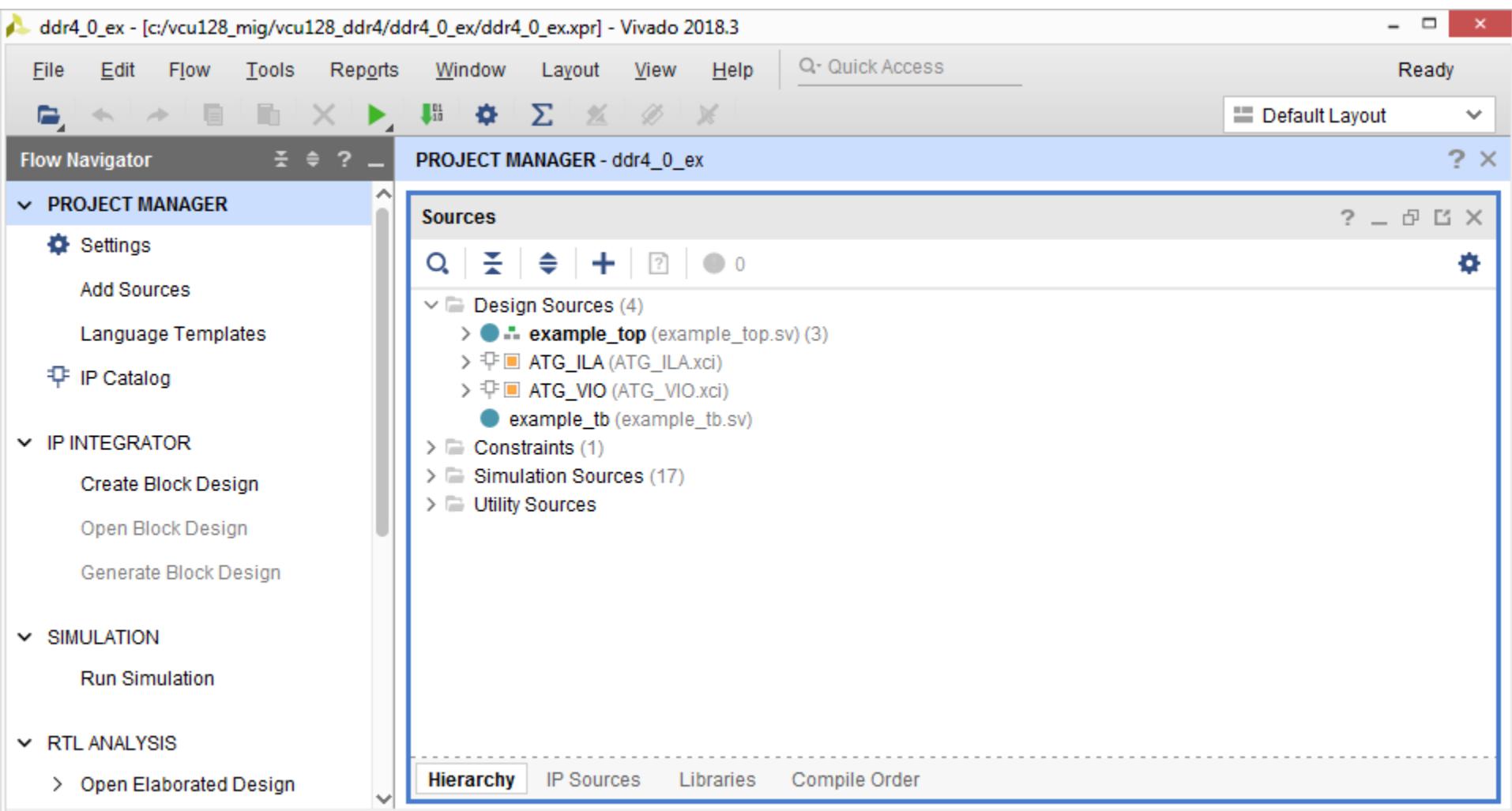


Open Example

Note: Presentation applies to the VCU128

Compile Example Design

- > A new project is created under <design path>/

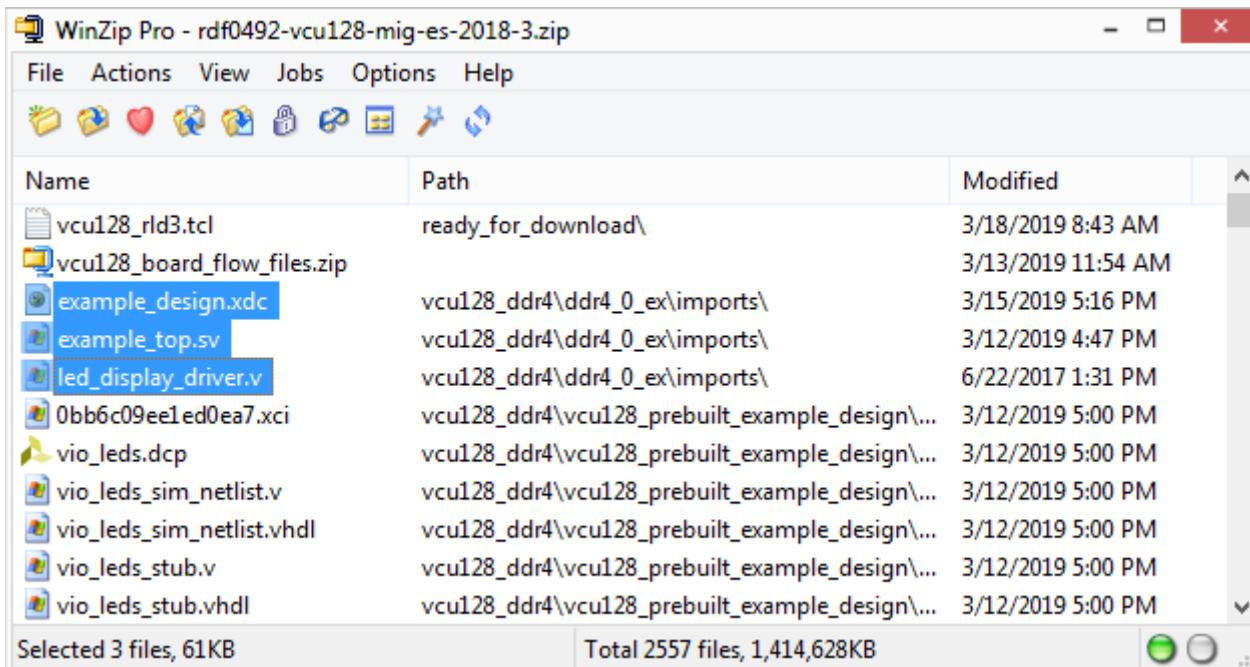


Note: The original project window can be closed

Modifications to Example Design

> From the RDF0492 - VCU128 MIG Design Files (2018.3 C) ZIP file

- » Extract the **vcu128_ddr4** files, **example_design.xdc**, **example_top.sv**, and **led_display_driver.v**
- » Overwrite these three existing files in your **vcu128_ddr4** MIG design
- » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs
- » The following commands will add the **led_display_driver.v** and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse
```

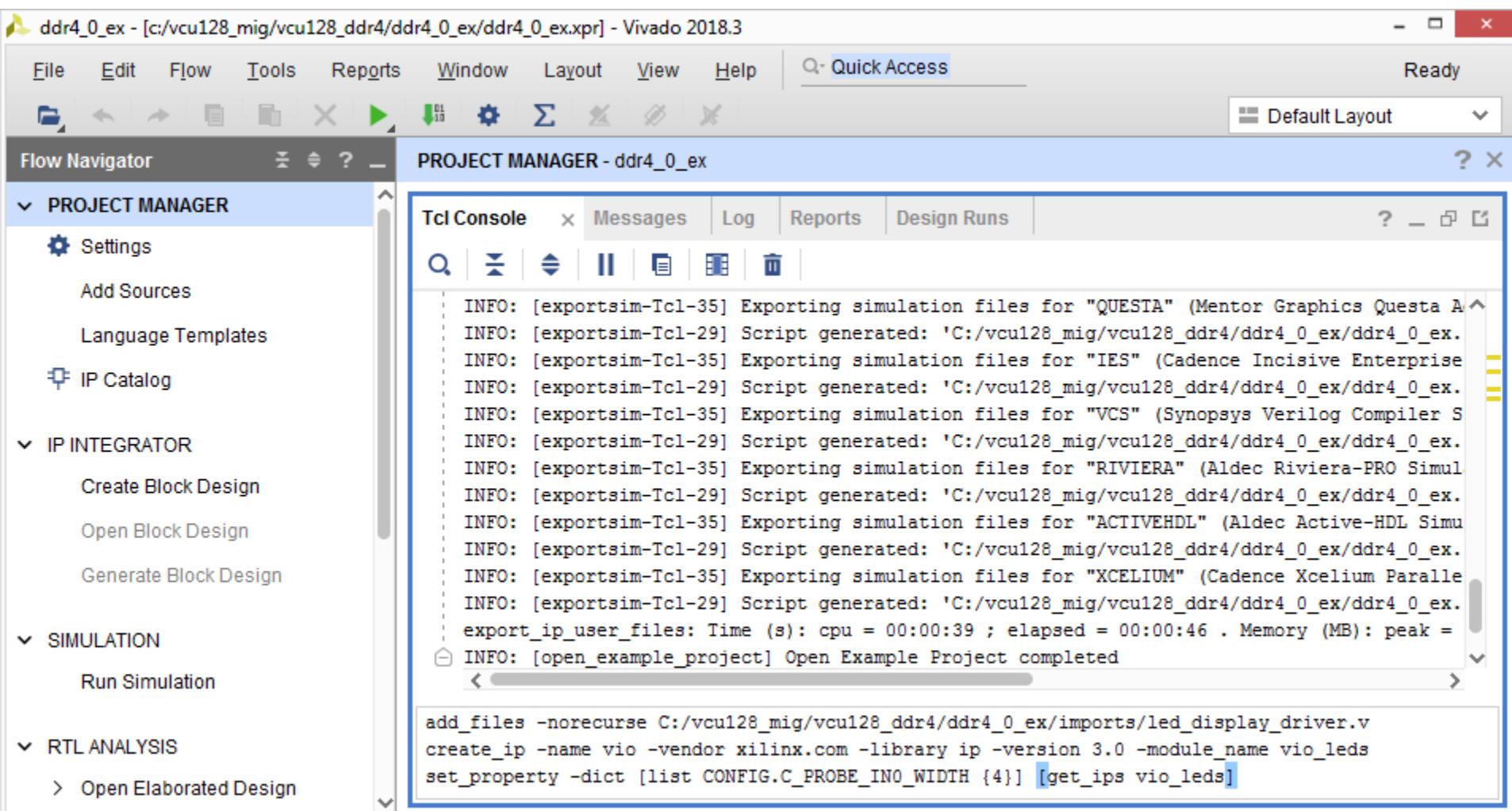
```
C:/vcu128_mig/vcu128_ddr4/ddr4_0_ex/imports/led_display_driver.v
```

```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

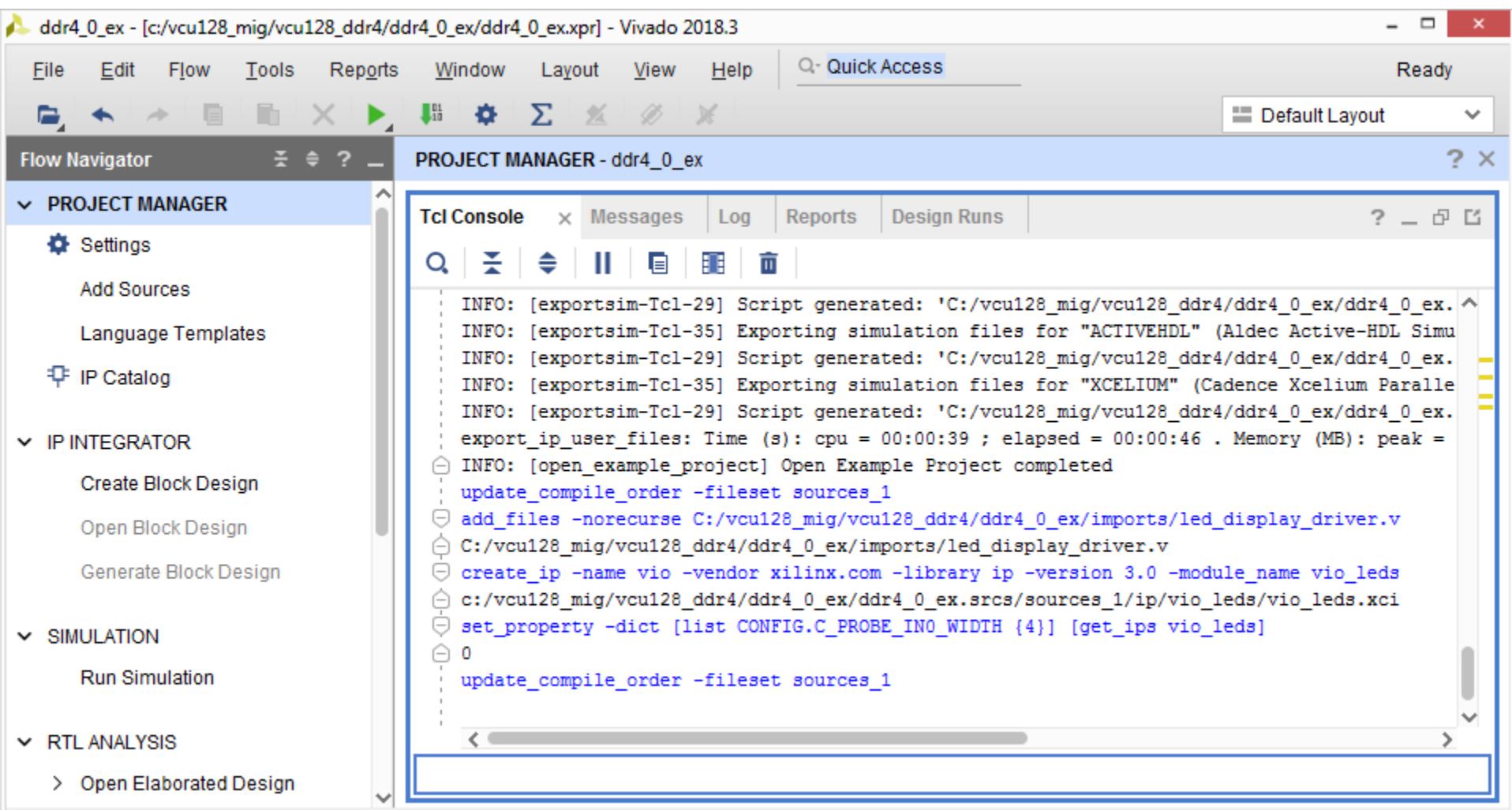
Modifications to Example Design

- > Press enter after entering Tcl commands



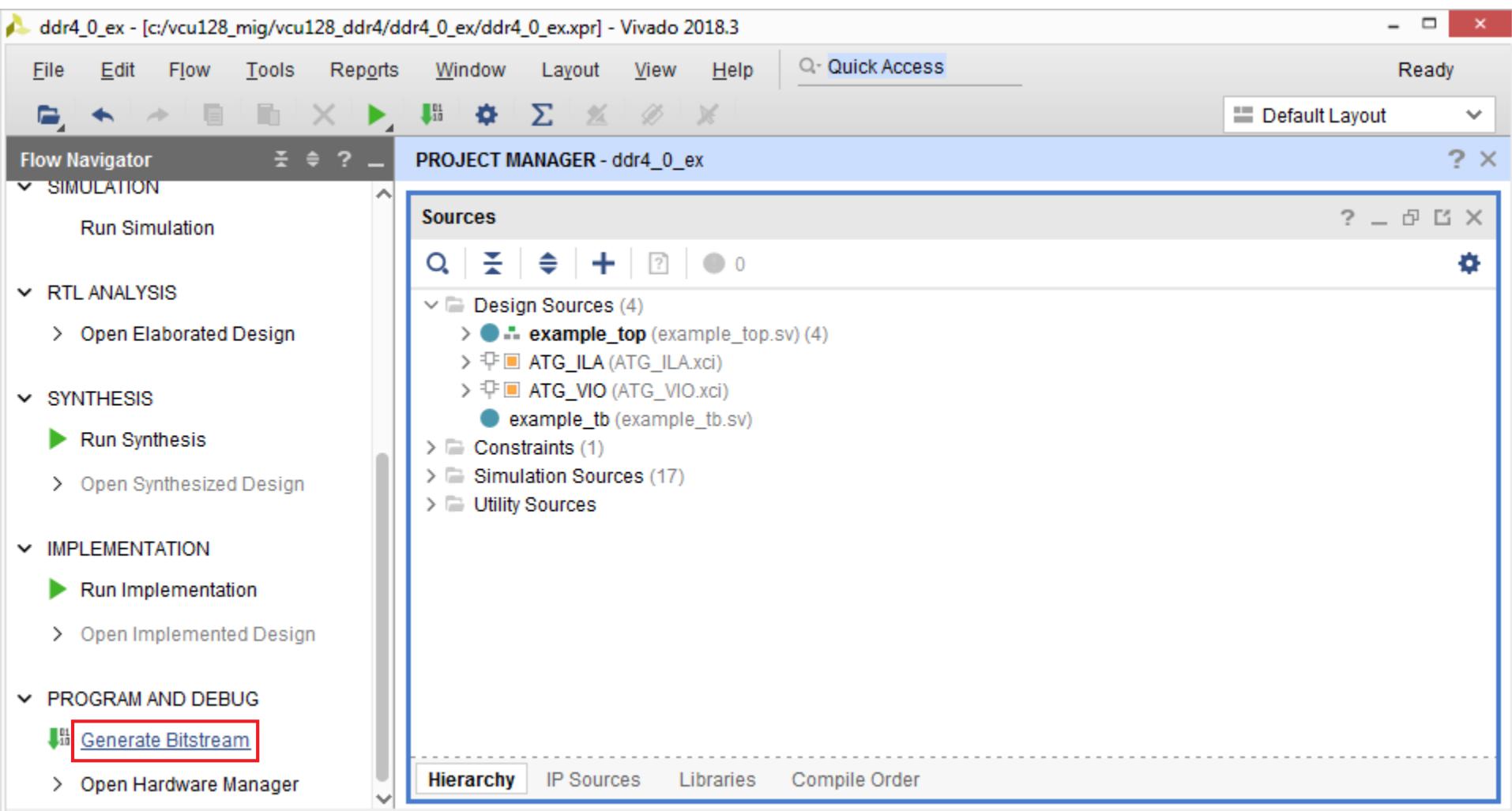
Modifications to Example Design

- > Tcl commands completed successfully



Compile Example Design

- > Click on Generate Bitstream

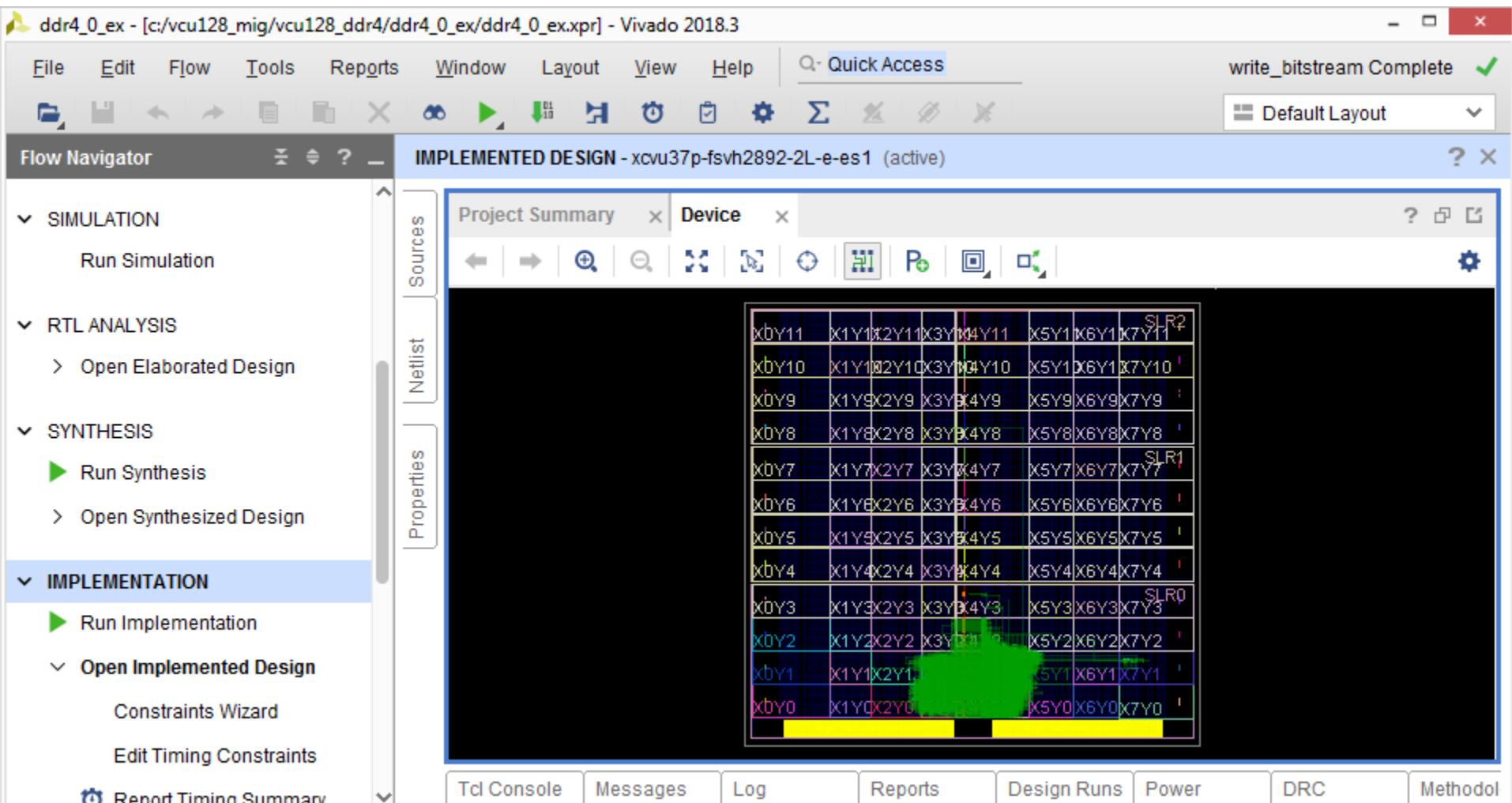


Note: Presentation applies to the VCU128

 XILINX

Compile Example Design

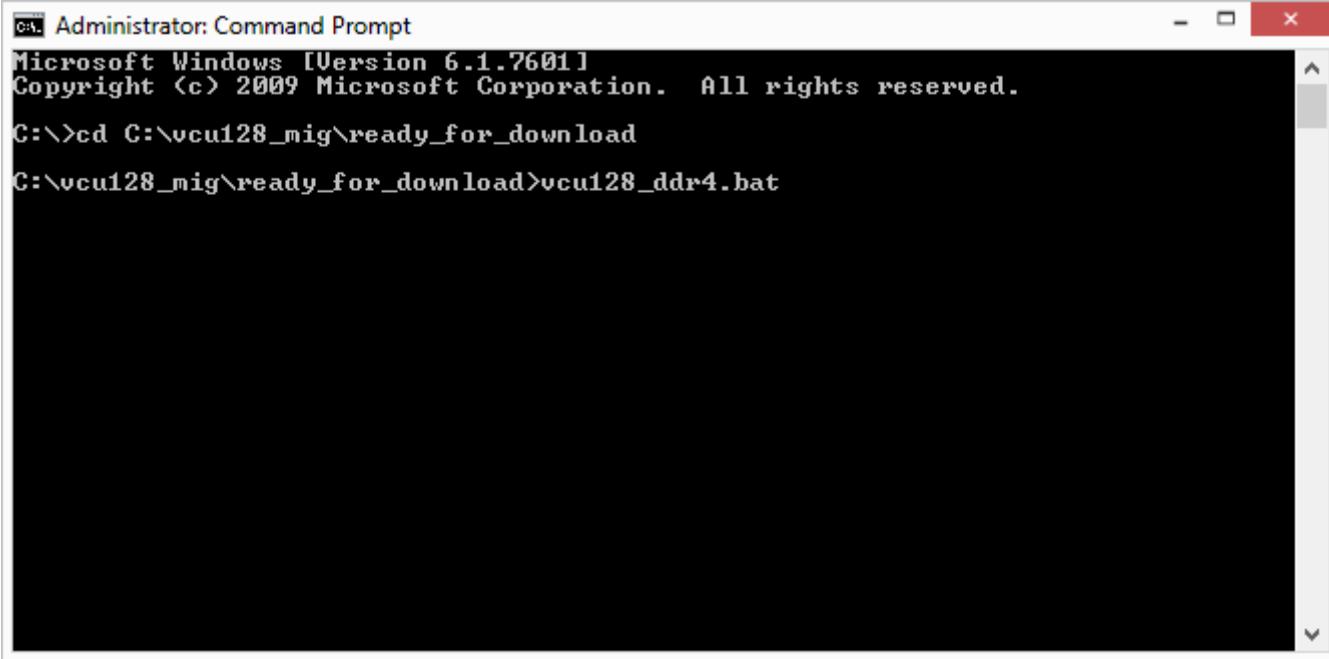
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\vcu128_mig\ready_for_download  
vcu128_ddr4.bat
```



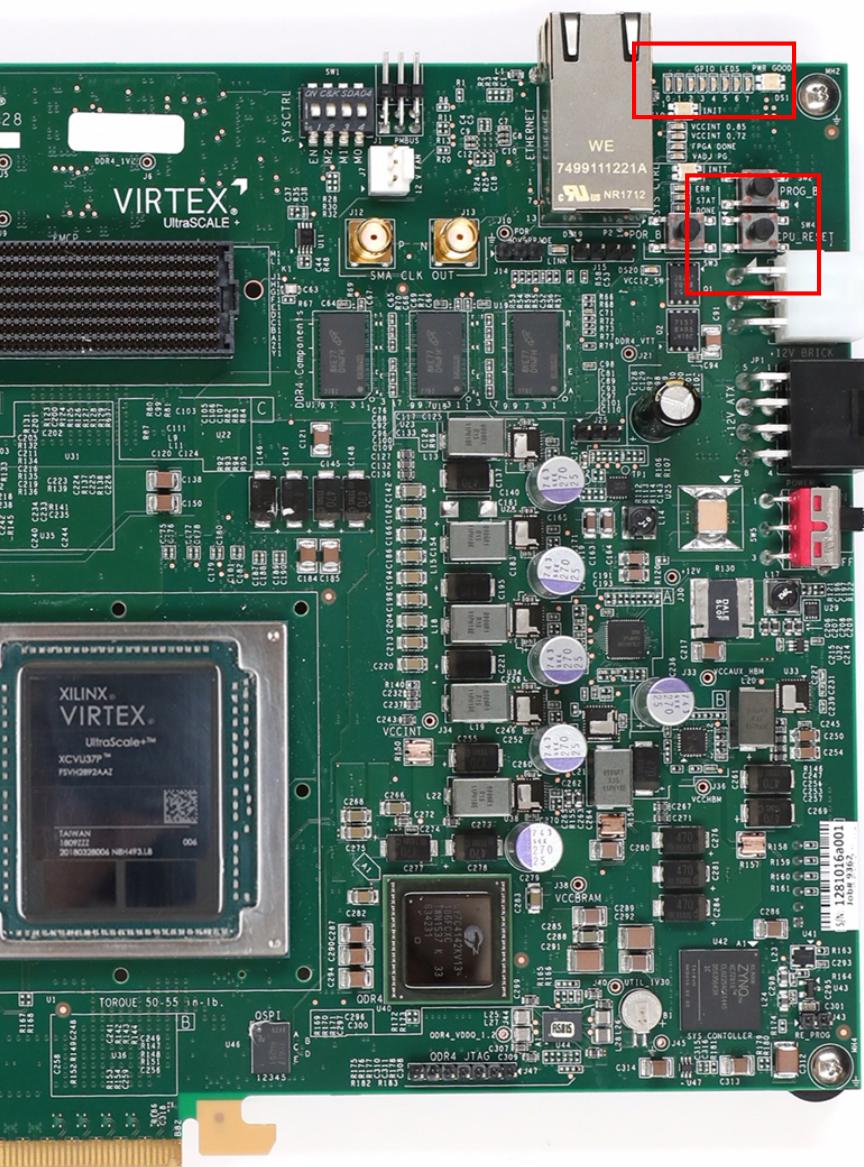
The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu128_mig\ready_for_download
C:\vcu128_mig\ready_for_download>vcu128_ddr4.bat
```

The command "cd" changes the current directory to "C:\vcu128_mig\ready_for_download". The command "vcu128_ddr4.bat" is then executed from this directory. The window has a standard Windows title bar and a scroll bar on the right side.

Run MIG Example Design



- > After bitstream loads, LED 0 (left most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW4, is the reset

Generate MIG RLD3 Example Design

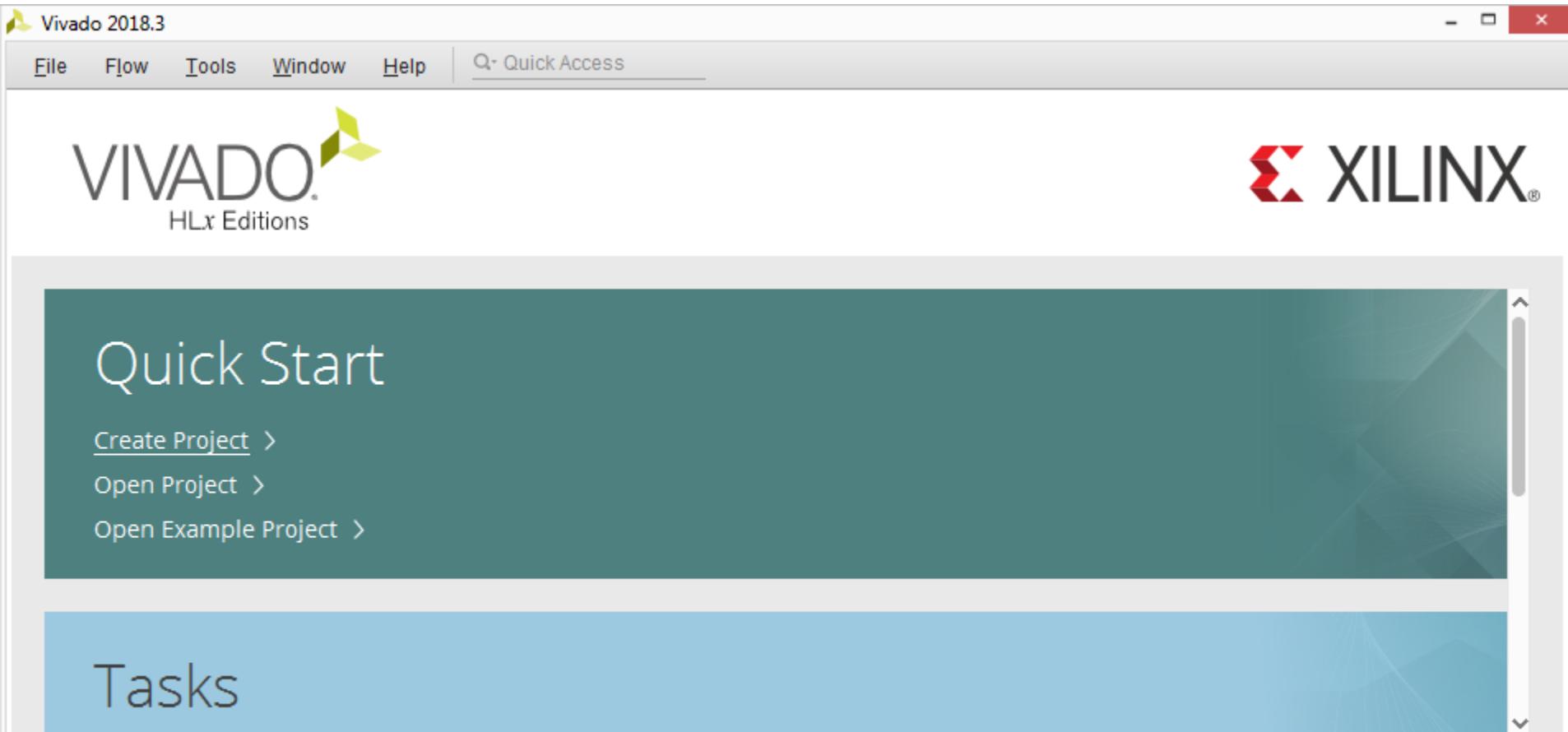


Generate MIG RLD3 Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2018.3 → Vivado

> Select Create Project



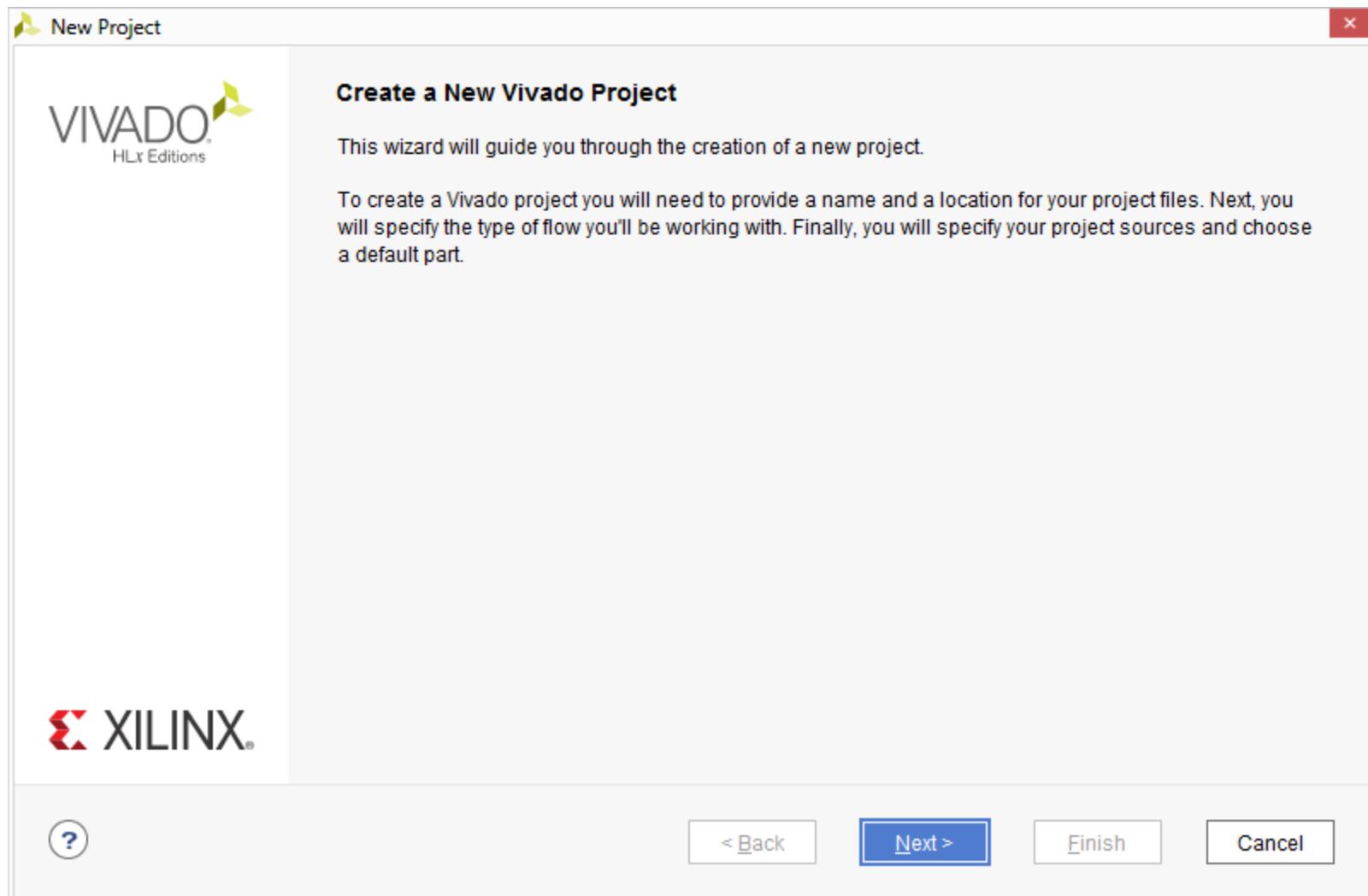
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU128

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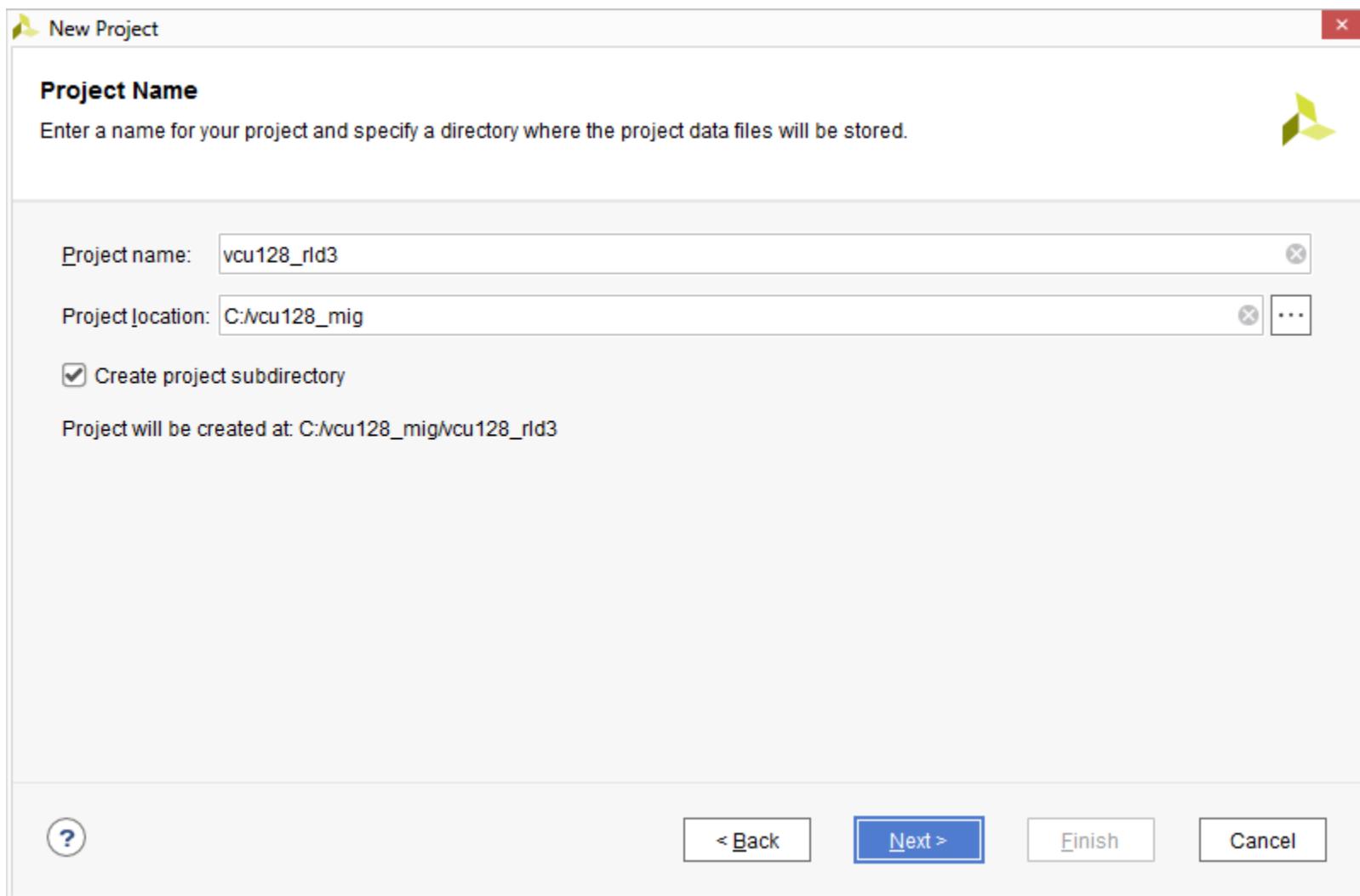
Generate MIG RLD3 Example Design

> Click Next



Generate MIG RLD3 Example Design

- > Set the Project name to vcu128_rld3 and location to C:/vcu128_mig
 - » Check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Generate MIG RLD3 Example Design

> Select RTL Project

» Select Do not specify sources at this time

New Project X

Project Type
Specify the type of project to create.



RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Generate MIG RLD3 Example Design

- > Under Boards, select the VCU128

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Vendor: All Name: All

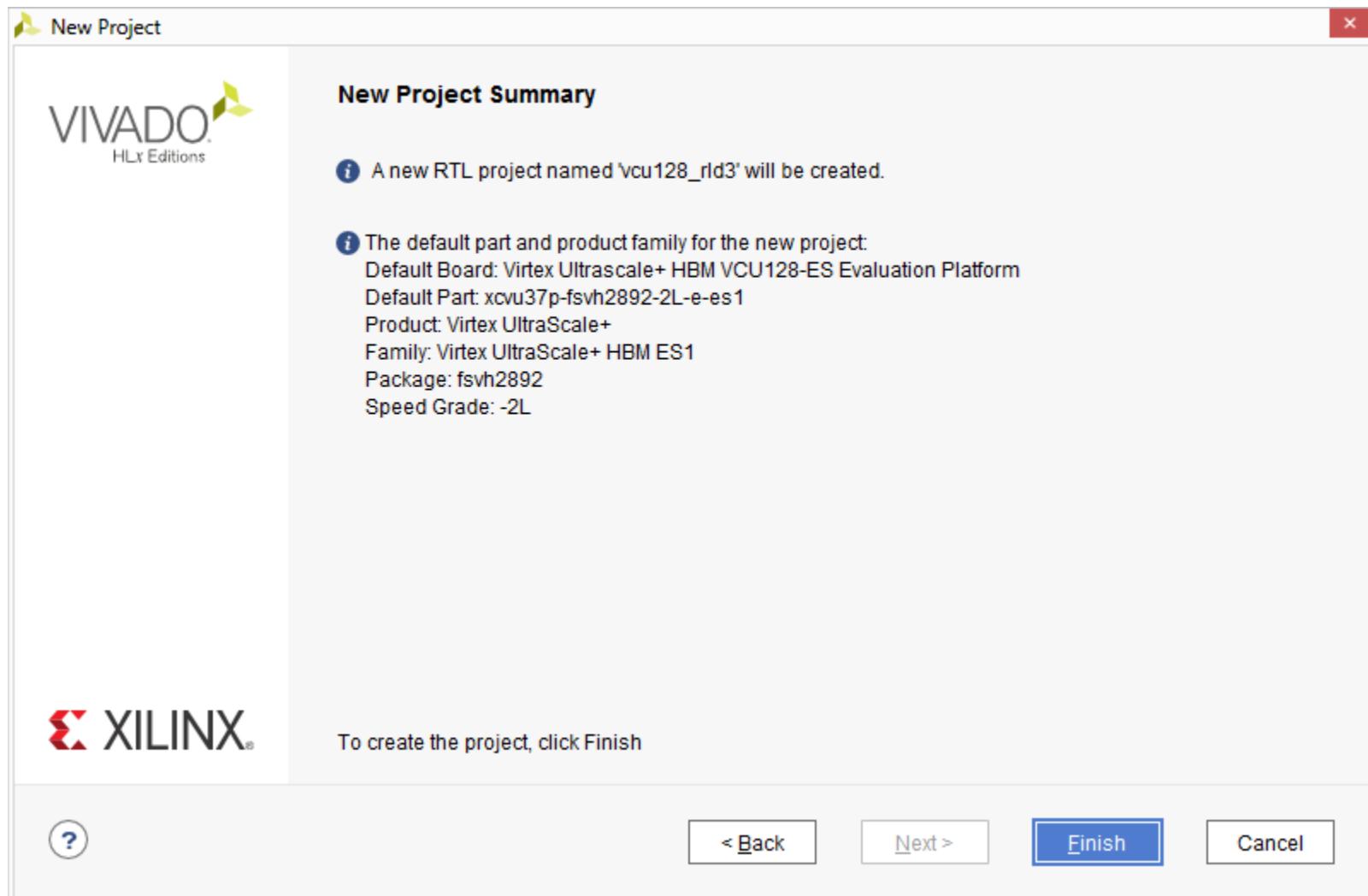
Search: Q-

Display Name	Preview	Vendor	File Version	Part
Virtex-UltraScale VCU110 Evaluation Platform Add Daughter Card Connections		xilinx.com	1.4	xcvu190
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0	xcvu9p-
Virtex Ultrascale+ HBM VCU128-ES Evaluation Platform		xilinx.com	1.0	xcvu37p

< Back Next > Finish Cancel

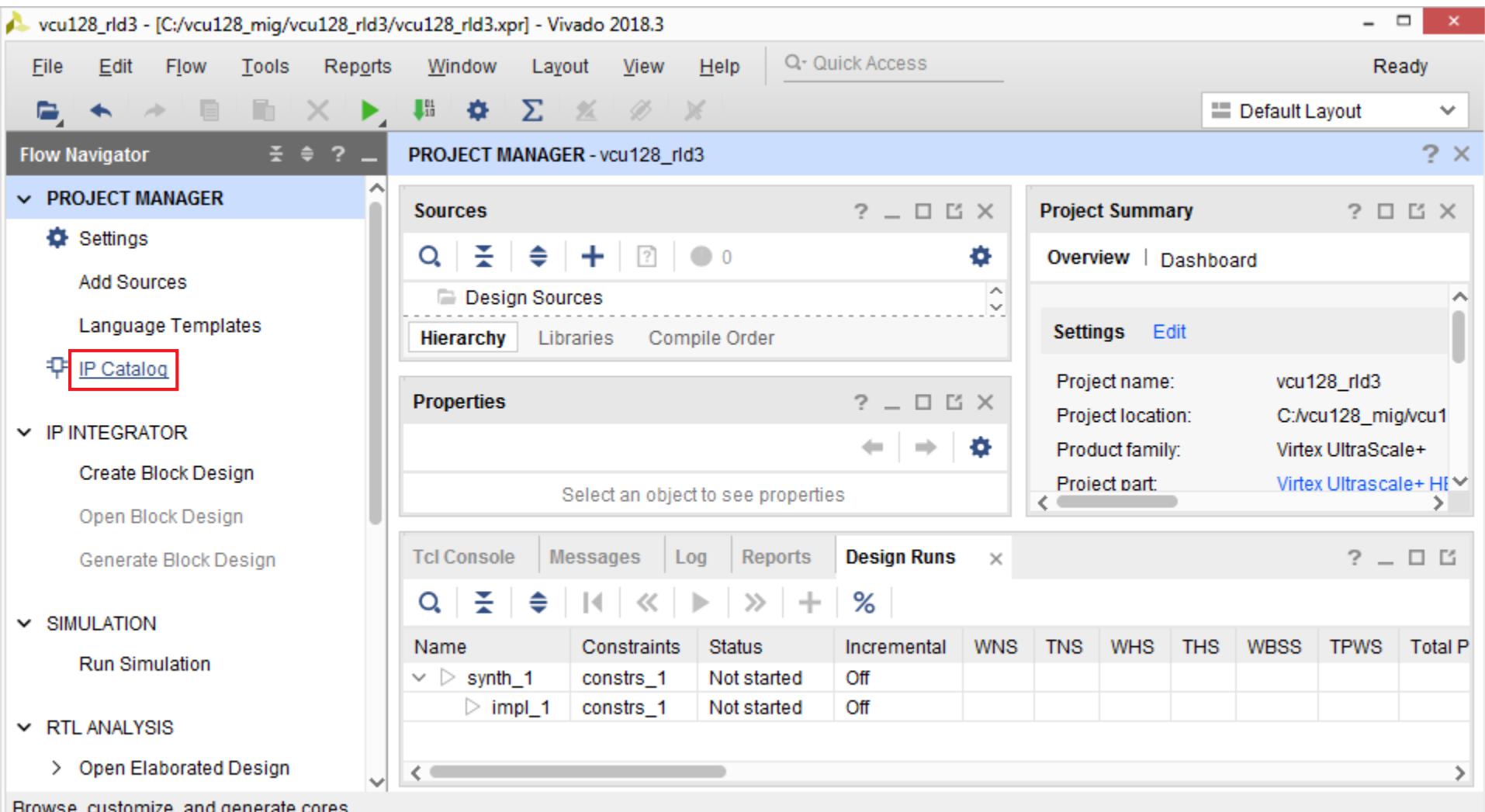
Generate MIG RLD3 Example Design

> Click Finish



Generate MIG RLD3 Example Design

> Click on IP Catalog



Generate MIG RLD3 Example Design

> Select RLDRAM3 (MIG), v1.4

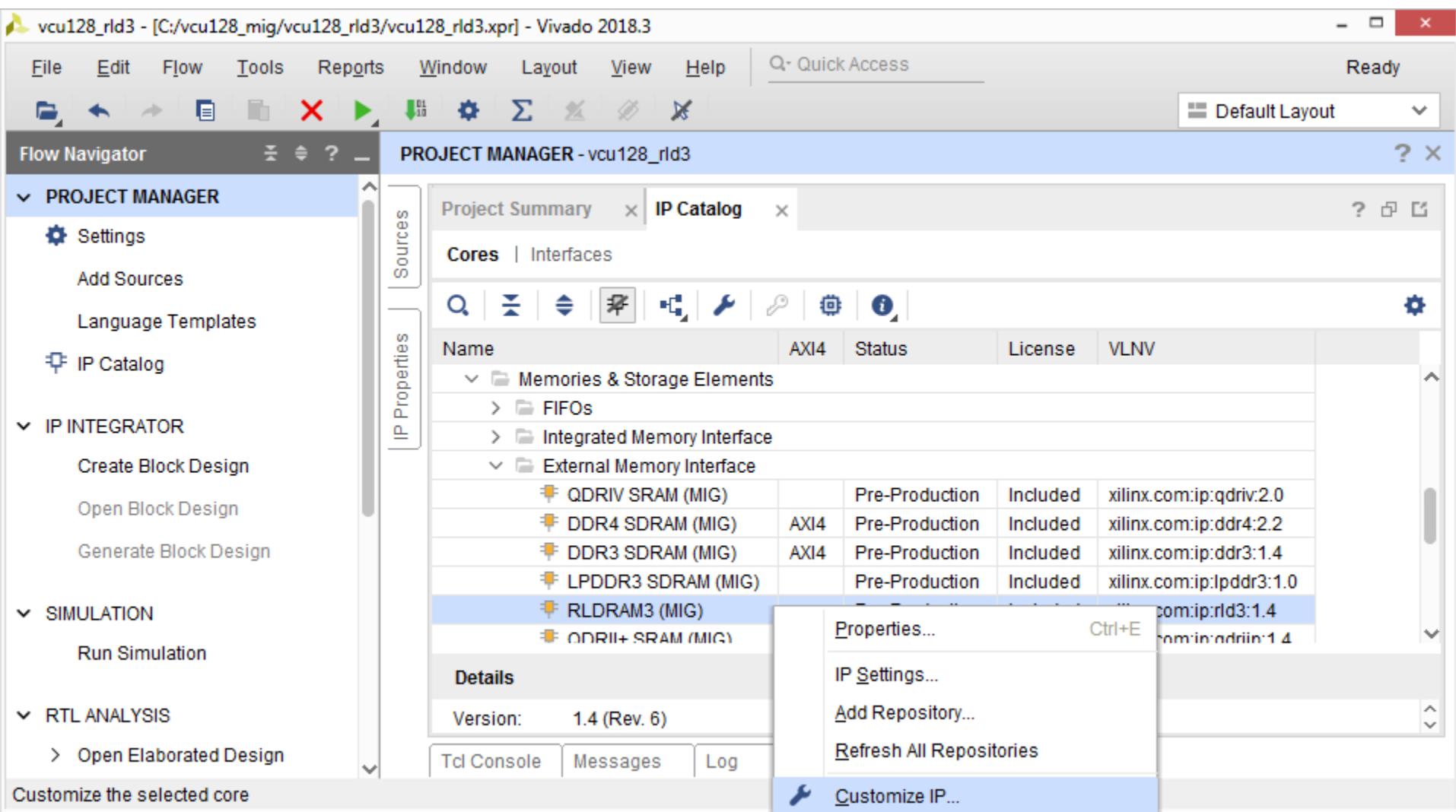
The screenshot shows the Vivado 2018.3 interface with the project "vcu128_rld3" open. The left sidebar contains the "PROJECT MANAGER" section with options like Settings, Add Sources, Language Templates, and IP Catalog. The main area is the "PROJECT MANAGER - vcu128_rld3" window, which has tabs for Project Summary and IP Catalog. The IP Catalog tab is active, displaying a list of cores and interfaces. Under "Memories & Storage Elements", the "External Memory Interface" folder is expanded, showing several MIG IP cores: QDRIV SRAM (MIG), DDR4 SDRAM (MIG), DDR3 SDRAM (MIG), LPDDR3 SDRAM (MIG), RLDRAM3 (MIG), and QDRII+ SRAM (MIG). The "RLDRAM3 (MIG)" entry is highlighted with a blue selection bar. Below the table, a "Details" section shows the Version: 1.4 (Rev. 6).

Name	AXI4	Status	License	VLAN
QDRIV SRAM (MIG)		Pre-Production	Included	xilinx.com:ip:qdriv:2.0
DDR4 SDRAM (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip:ddr4:2.2
DDR3 SDRAM (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip:ddr3:1.4
LPDDR3 SDRAM (MIG)		Pre-Production	Included	xilinx.com:ip:lpddr3:1.0
RLDRAM3 (MIG)		Pre-Production	Included	xilinx.com:ip:rld3:1.4
QDRII+ SRAM (MIG)		Pre-Production	Included	xilinx.com:ip:qdrii:1.4

Generate MIG RLD3 Example Design

- > Right click on RLDRAM3 (MIG)

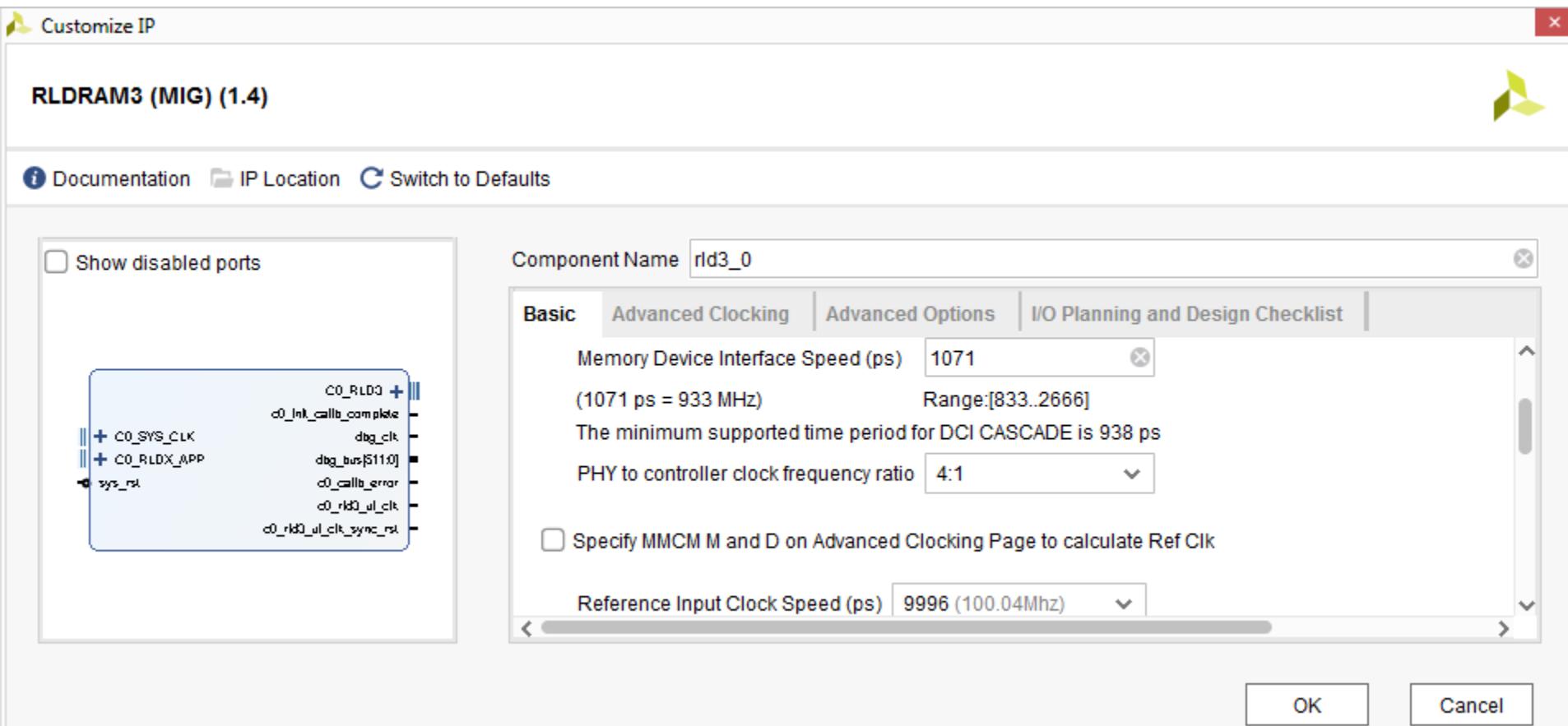
- » Select Customize IP



Note: Presentation applies to the VCU128

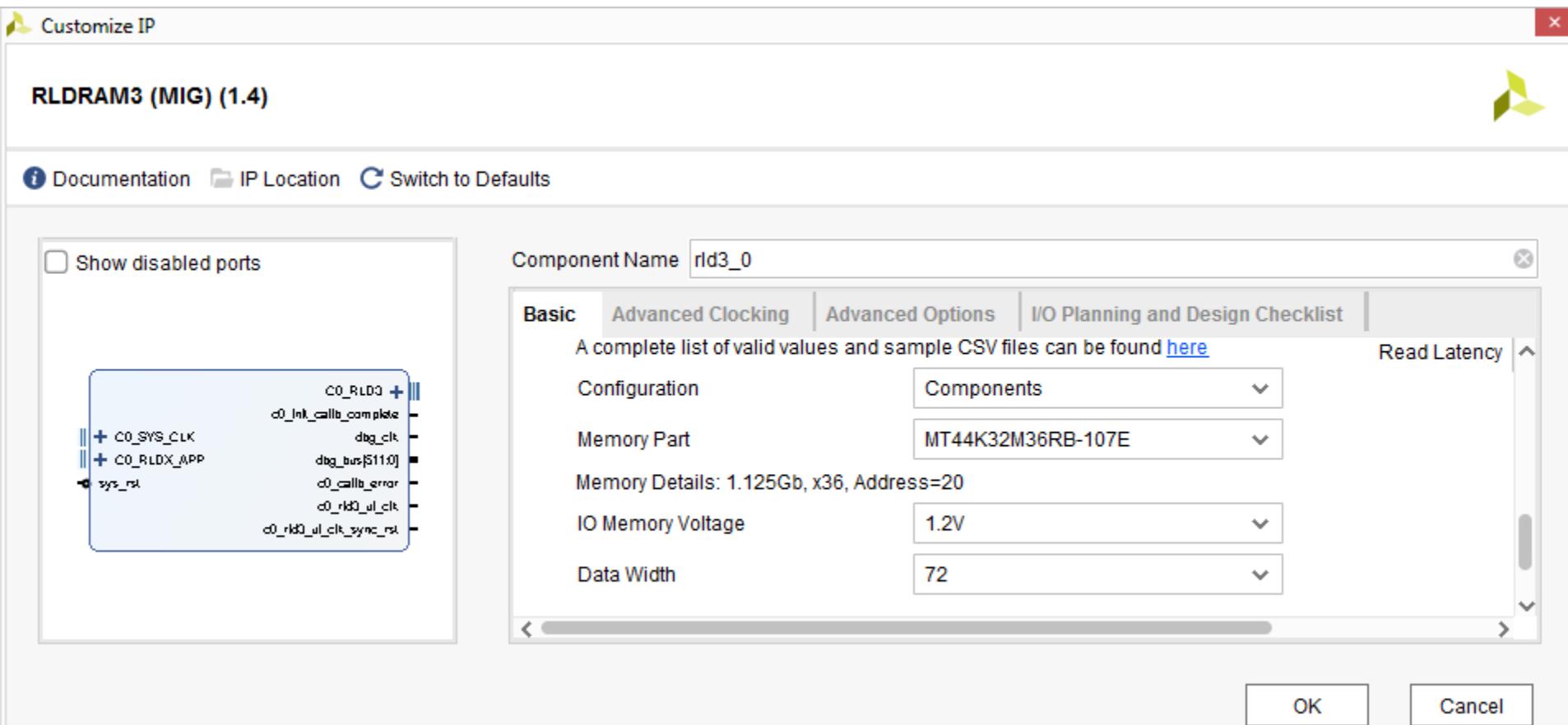
Generate MIG RLD3 Example Design

- > Set Clock period to 1071 for 1866 Mb/s operation.
- > Set the Input Clock to 9996 ps for 100 MHz
- > Scroll down



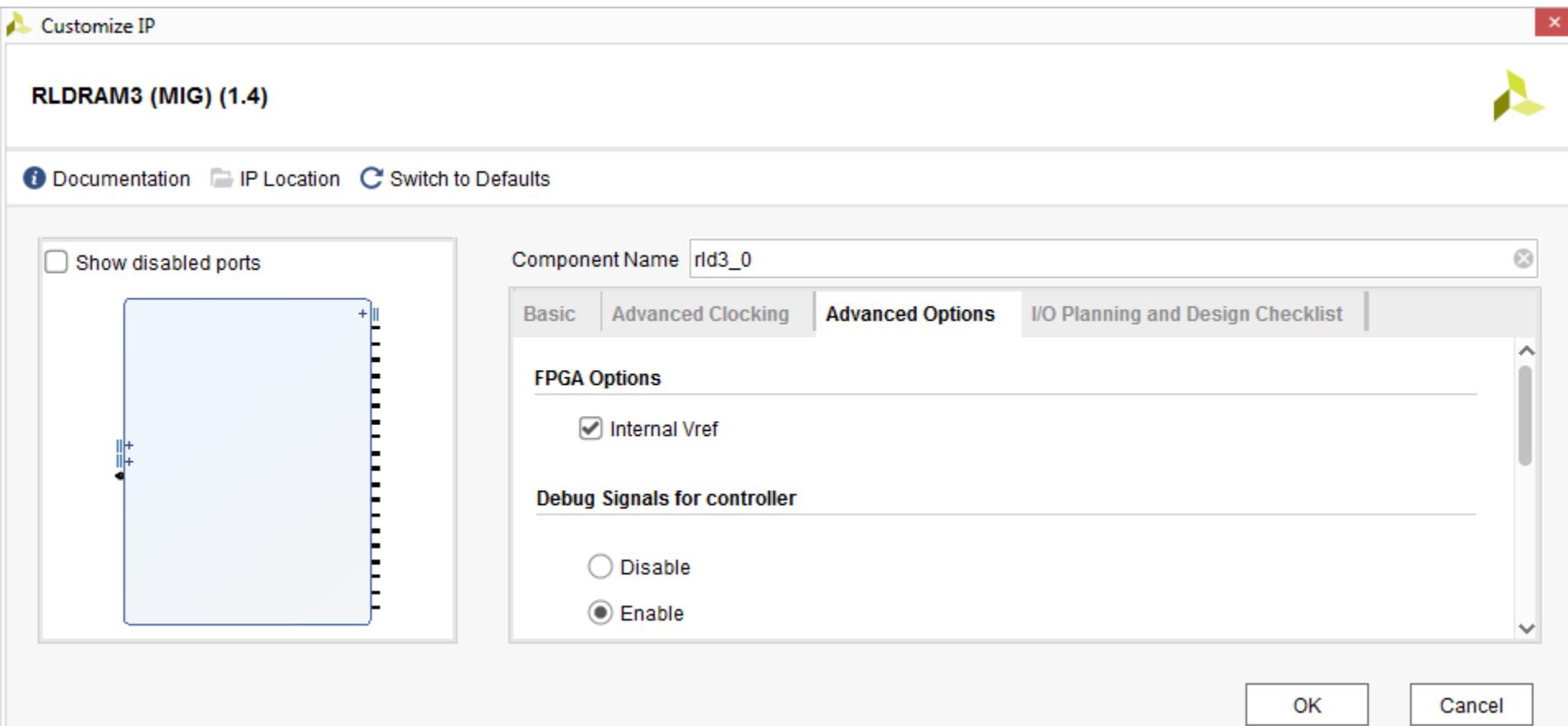
Generate MIG RLD3 Example Design

- > Select the part MT44K32M36RB-107E
- > Set the Data Width to 72 and click the Advanced Options Tab



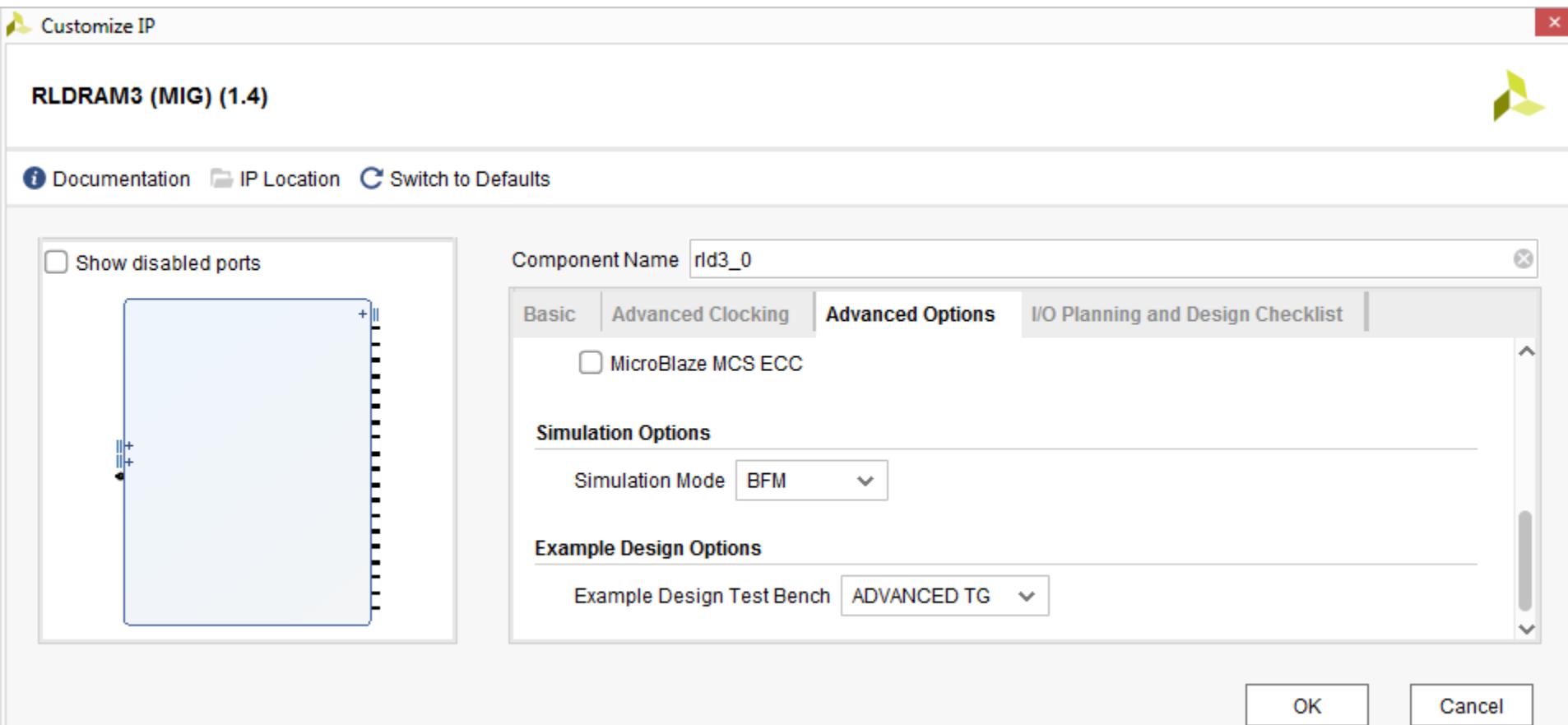
Generate MIG RLD3 Example Design

- > Set the Debug Signals to Enable
- > Scroll down



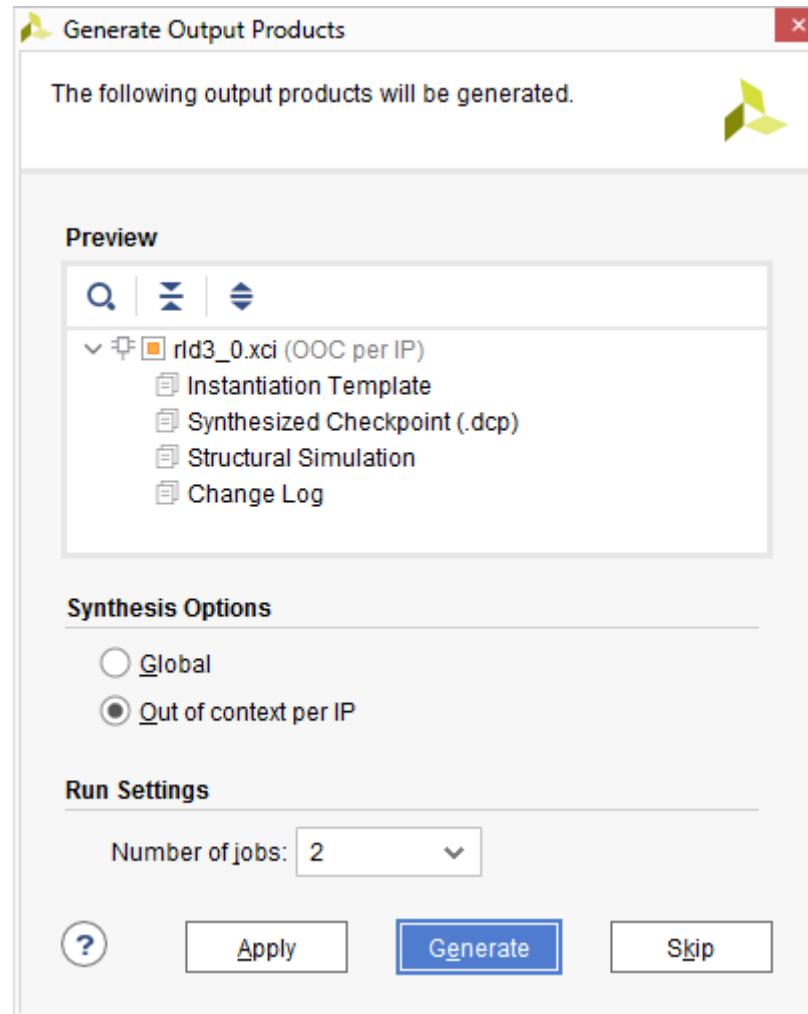
Generate MIG RLD3 Example Design

- > Set the Example Design Test Bench to ADVANCED TG
- > Click OK



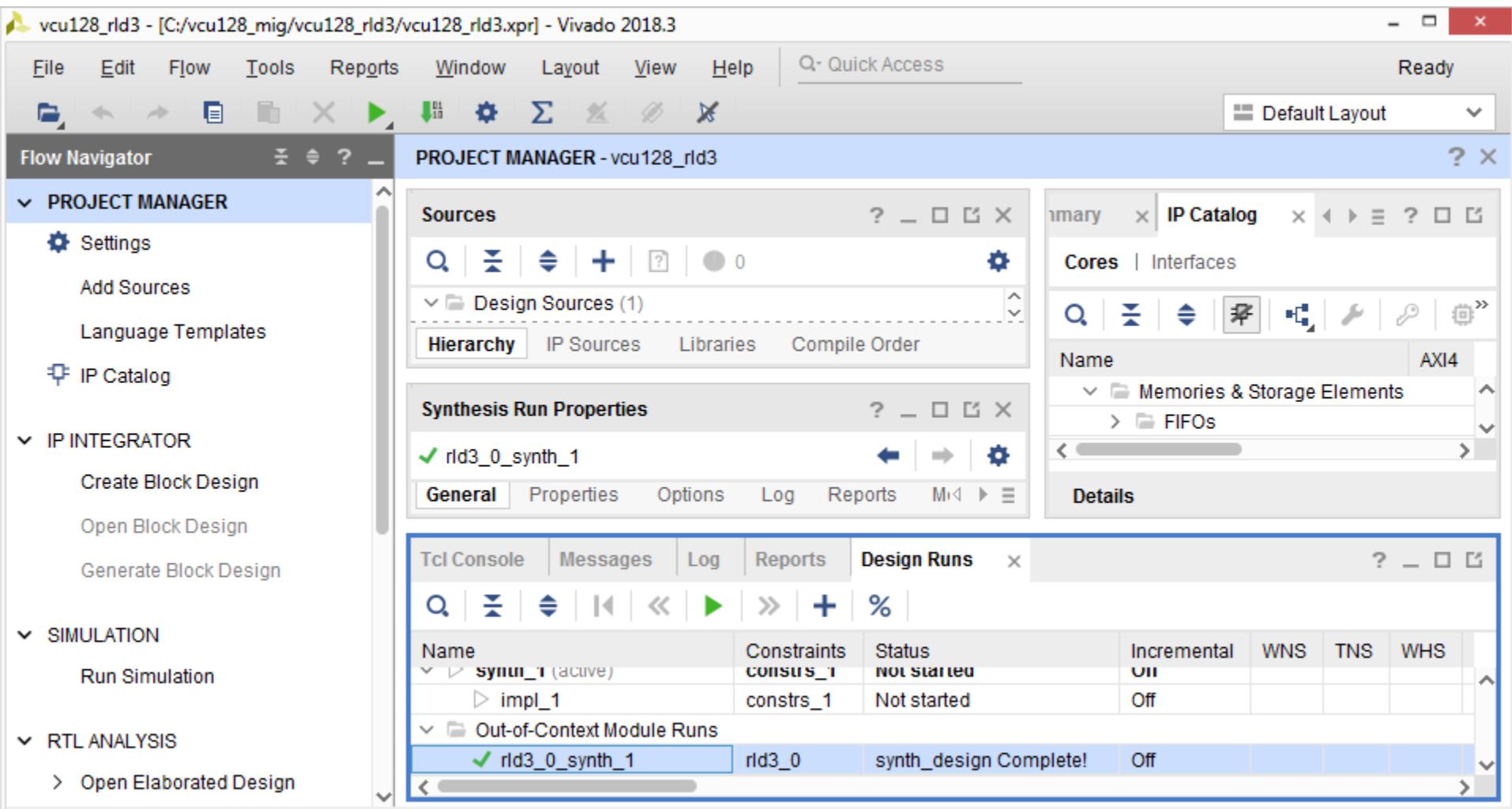
Generate MIG RLD3 Example Design

> Click Generate



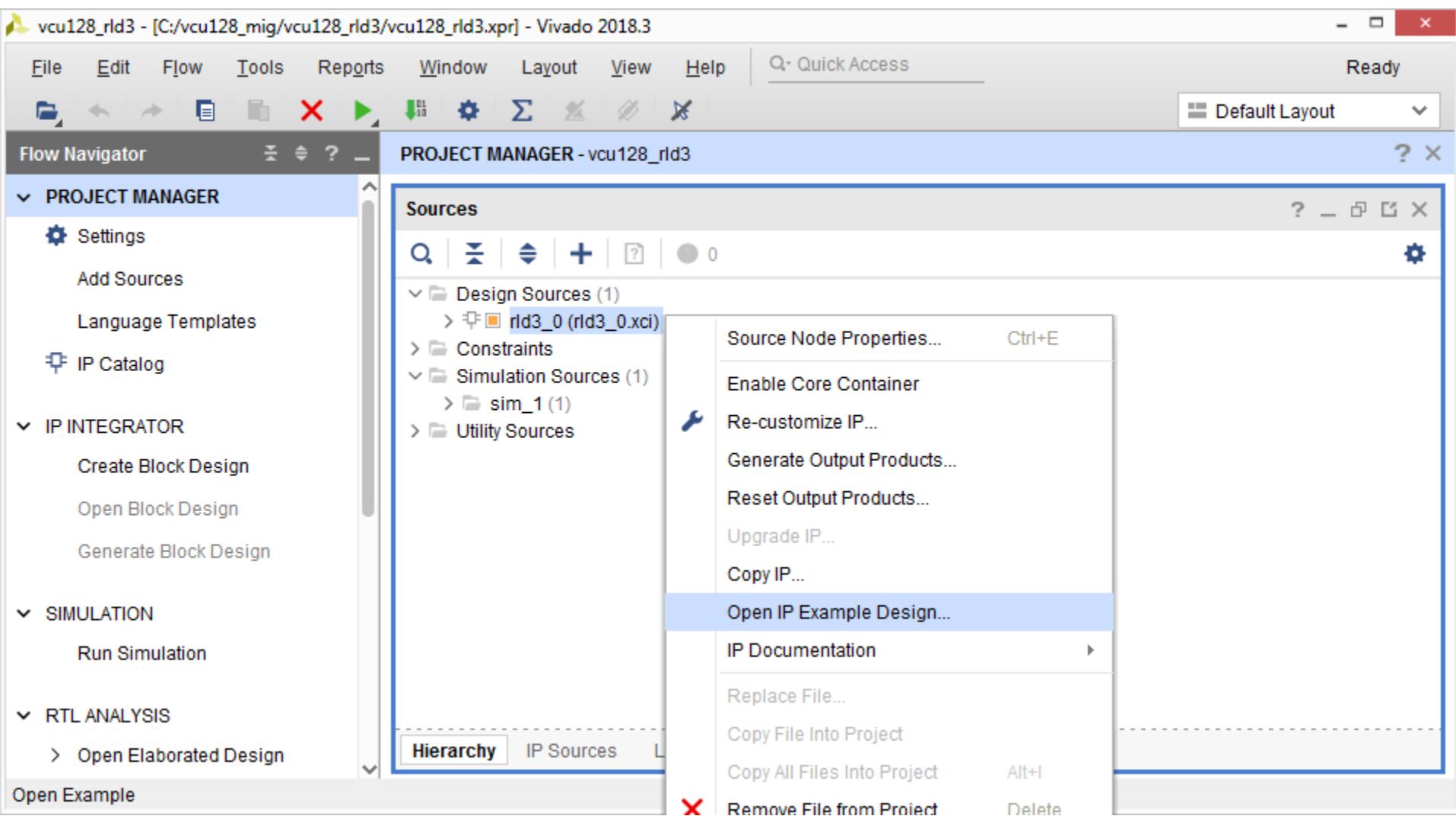
Generate MIG RLD3 Example Design

- > Wait until checkmark appears on rld3_0_synth_1



Compile Example Design

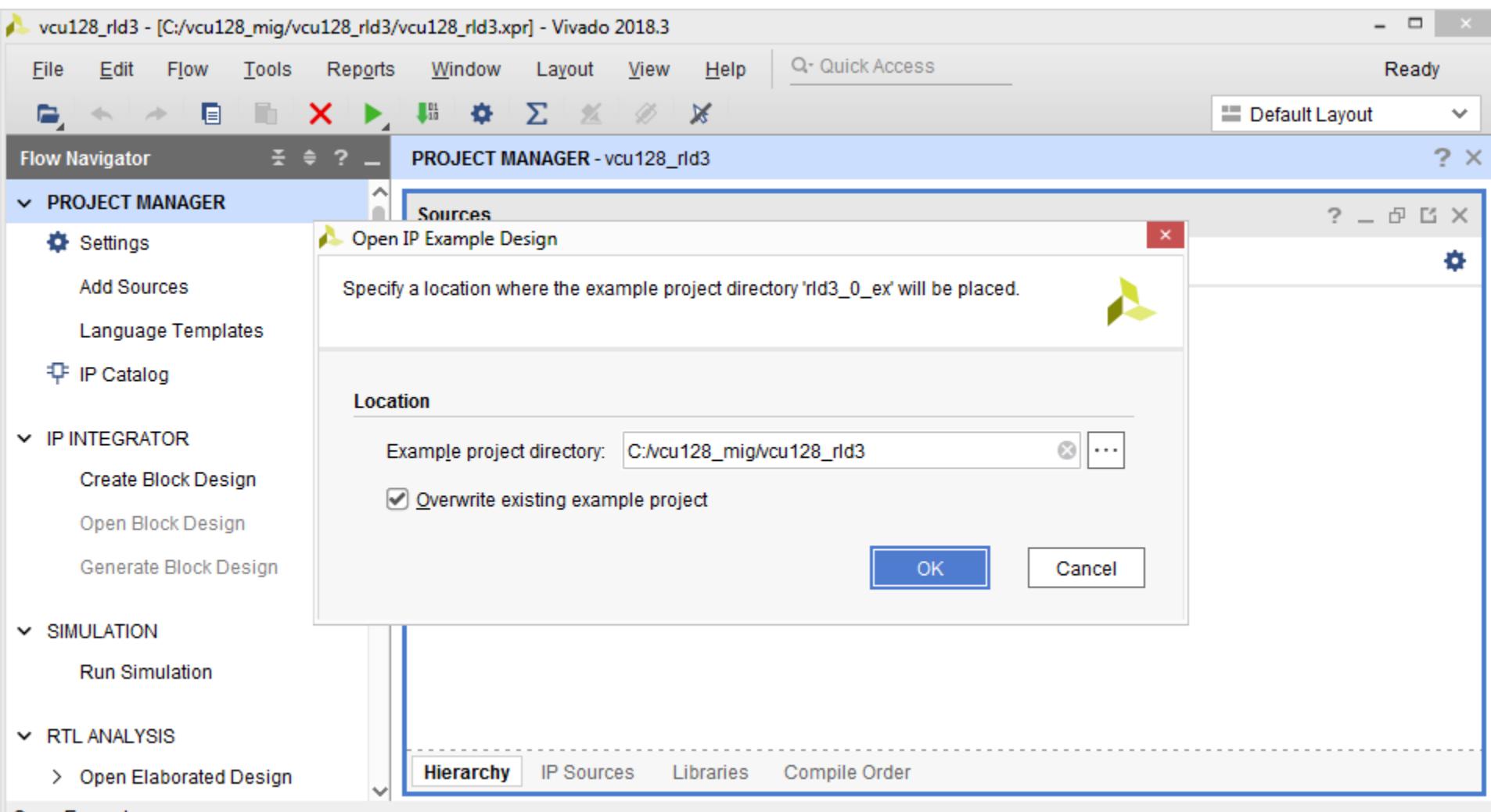
- > Right click on rld3_0 and select Open IP Example Design...



Note: Presentation applies to the VCU128

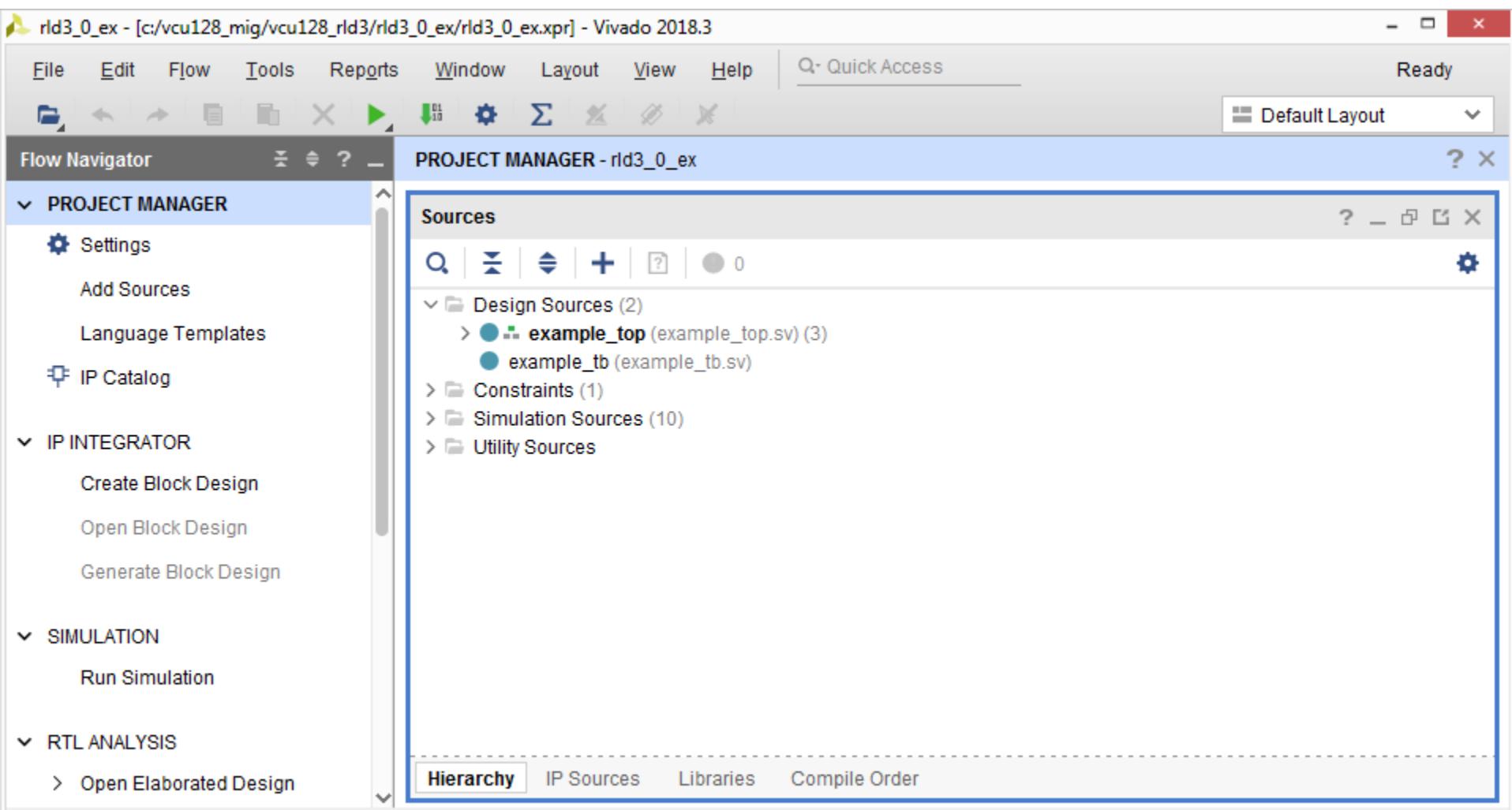
Compile Example Design

- > Set the location to C:/vcu128_mig/vcu128_rld3 and click OK



Compile Example Design

- > A new project is created under <design path>/

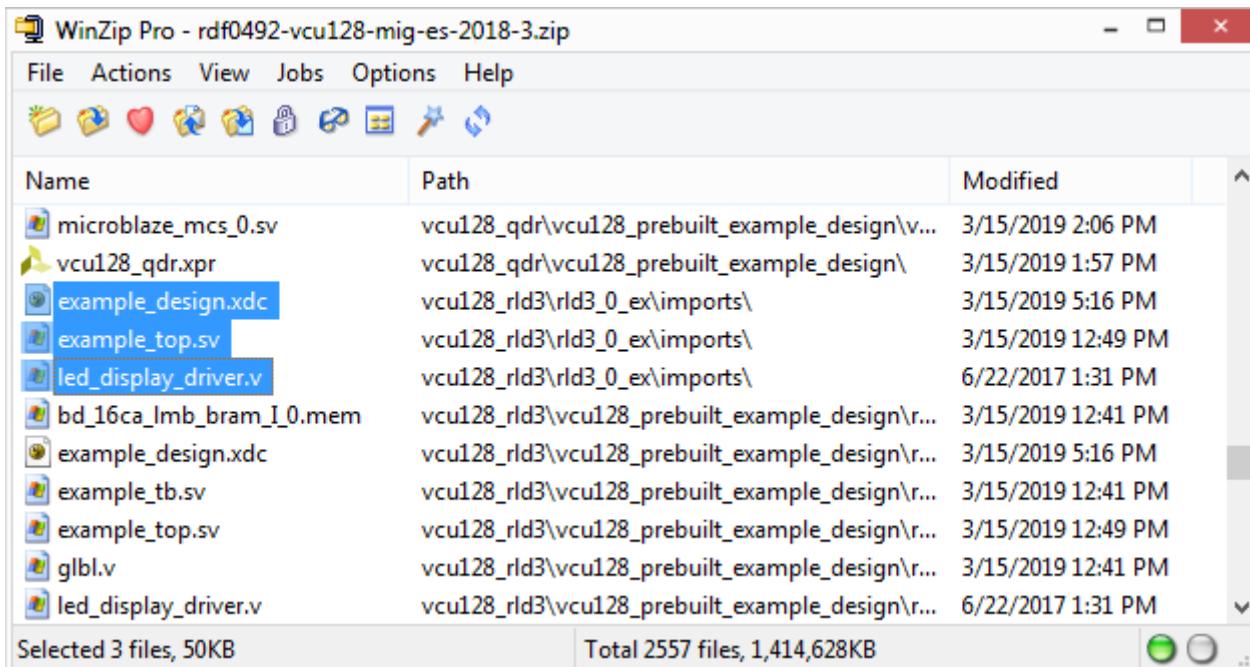


Note: The original project window can be closed

Modifications to Example Design

> From the RDF0492 - VCU128 MIG Design Files (2018.3 C) ZIP file

- » Extract the **vcu128_rld3** files, **example_design.xdc**, **example_top.sv**, and **led_display_driver.v**
- » Overwrite these three existing files in your **vcu128_rld3** MIG design
- » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs
- » The following commands will add the **led_display_driver.v** and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse
```

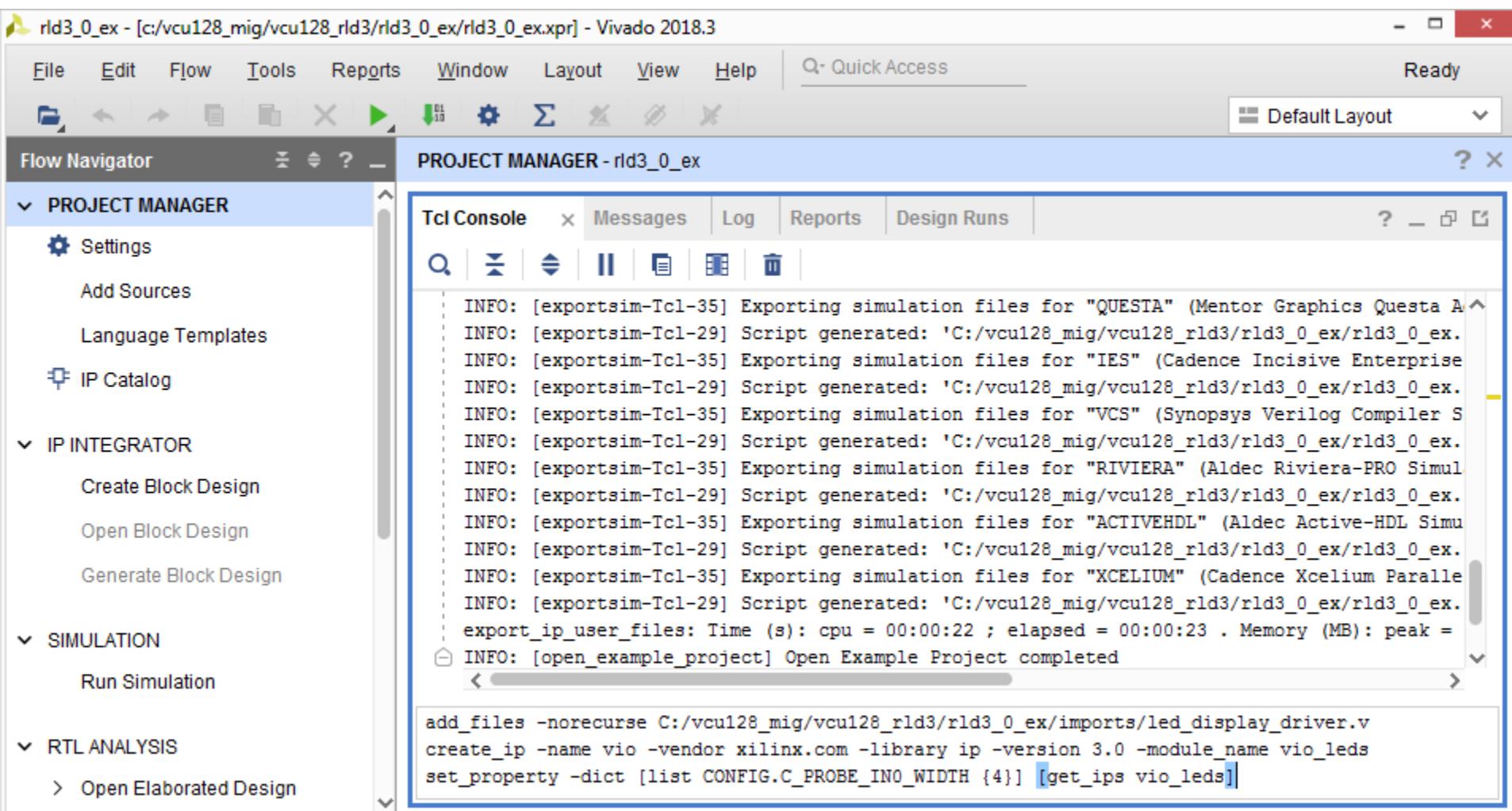
```
C:/vcu128_mig/vcu128_rld3/rld3_0_ex/imports/led_display_driver.v
```

```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

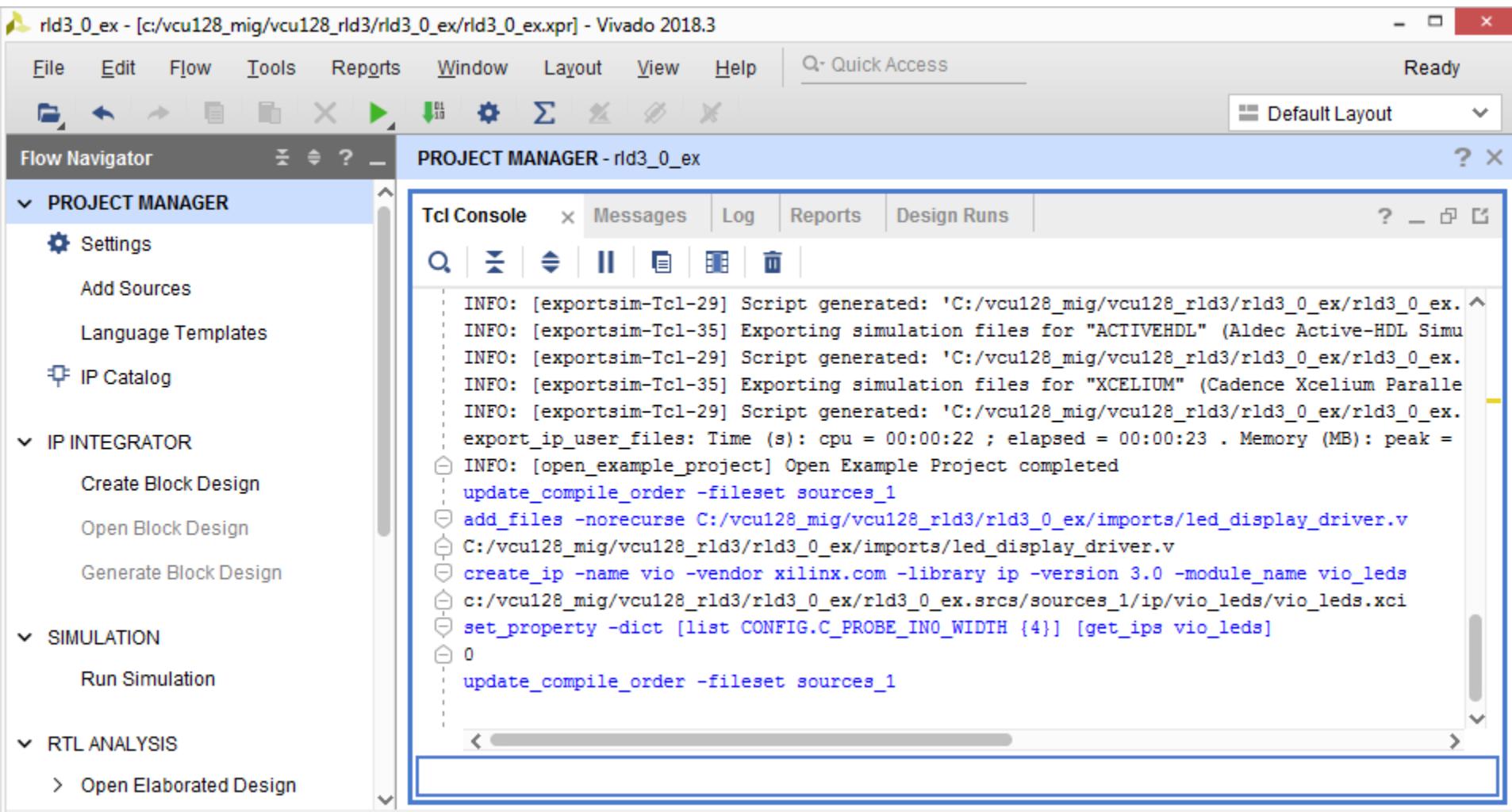
Modifications to Example Design

- > Press enter after entering Tcl commands



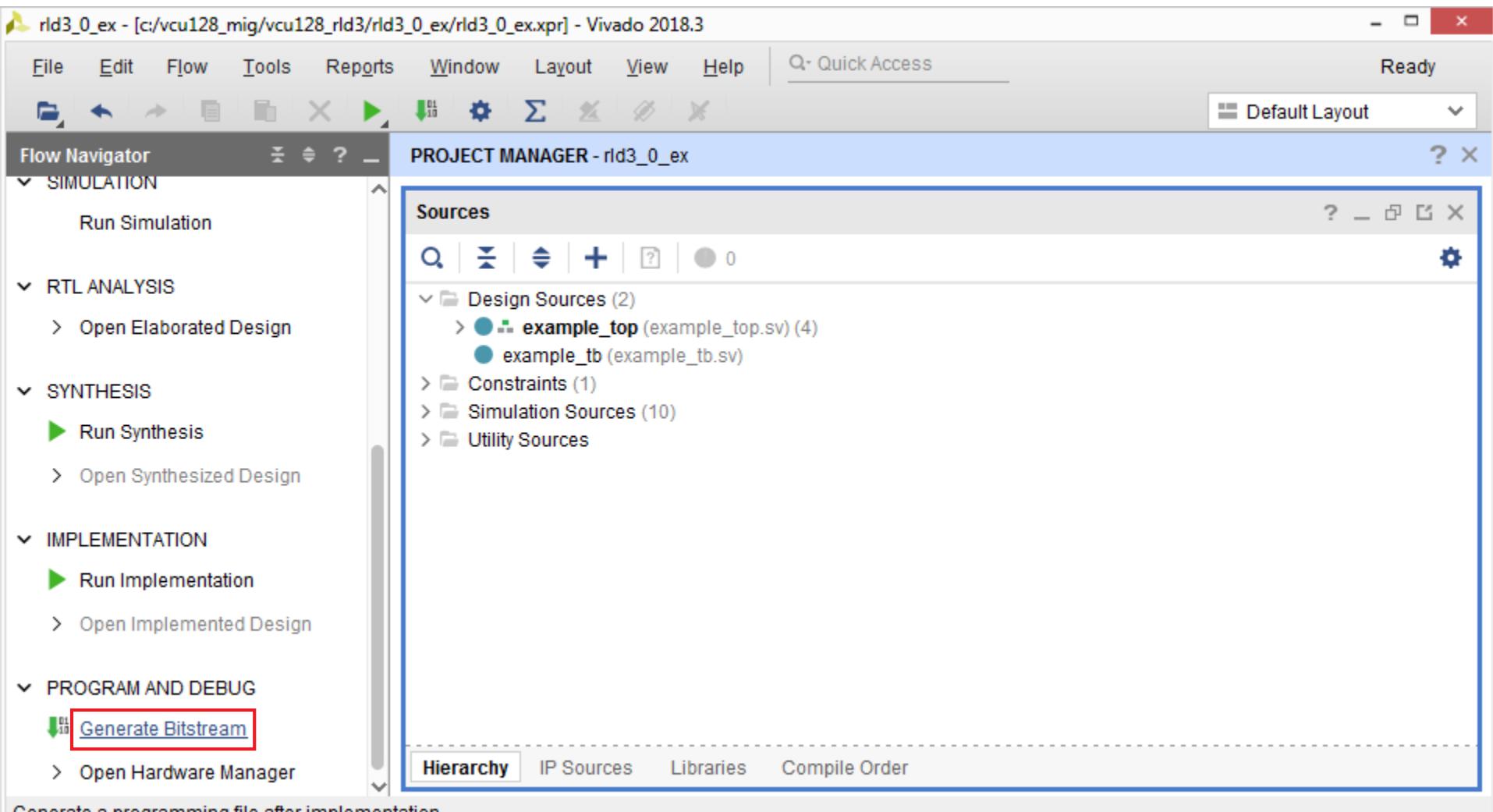
Modifications to Example Design

- > Tcl commands completed successfully



Compile Example Design

- > Click on Generate Bitstream



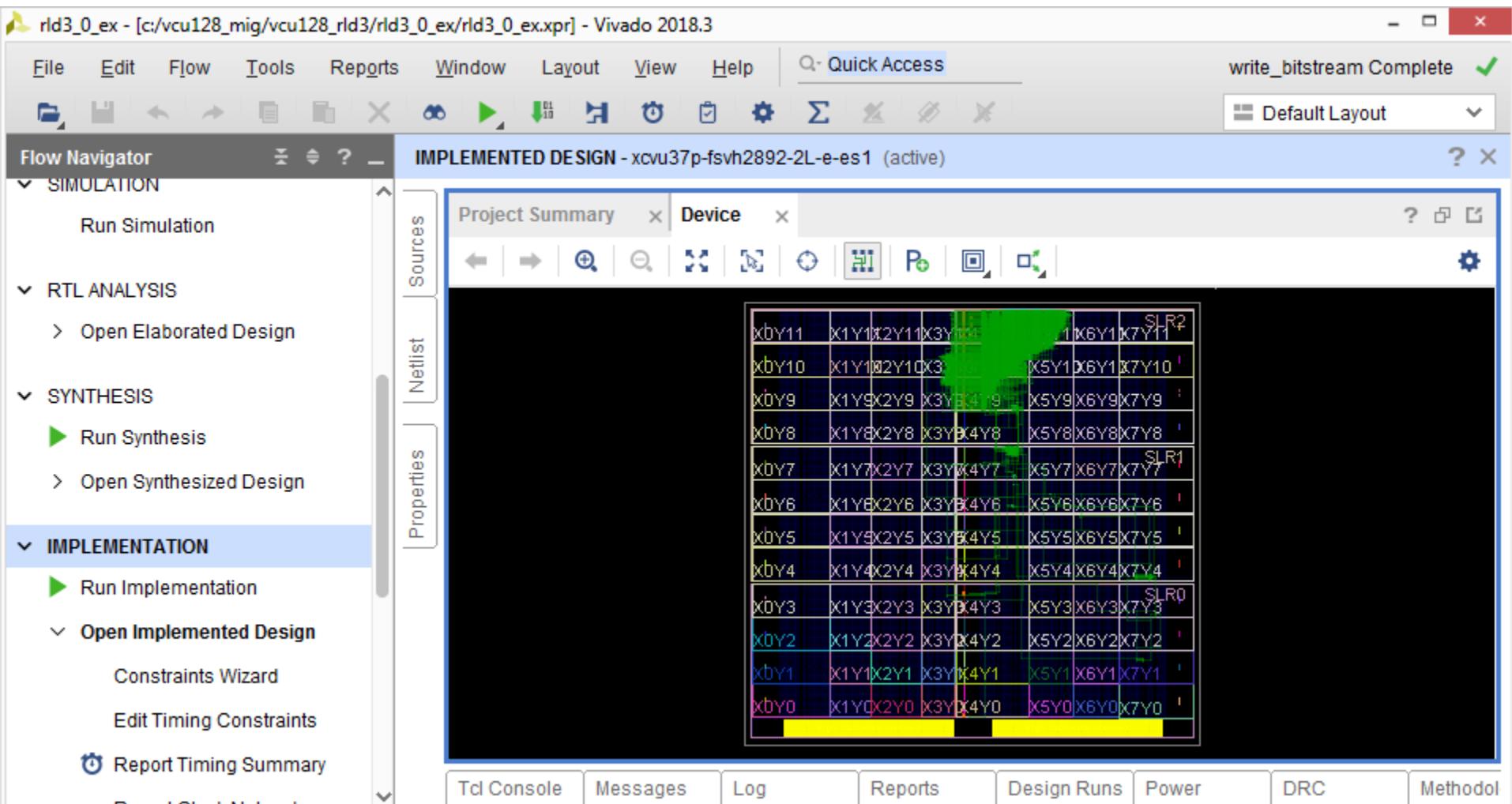
Generate a programming file after implementation

Note: Presentation applies to the VCU128

 XILINX

Compile Example Design

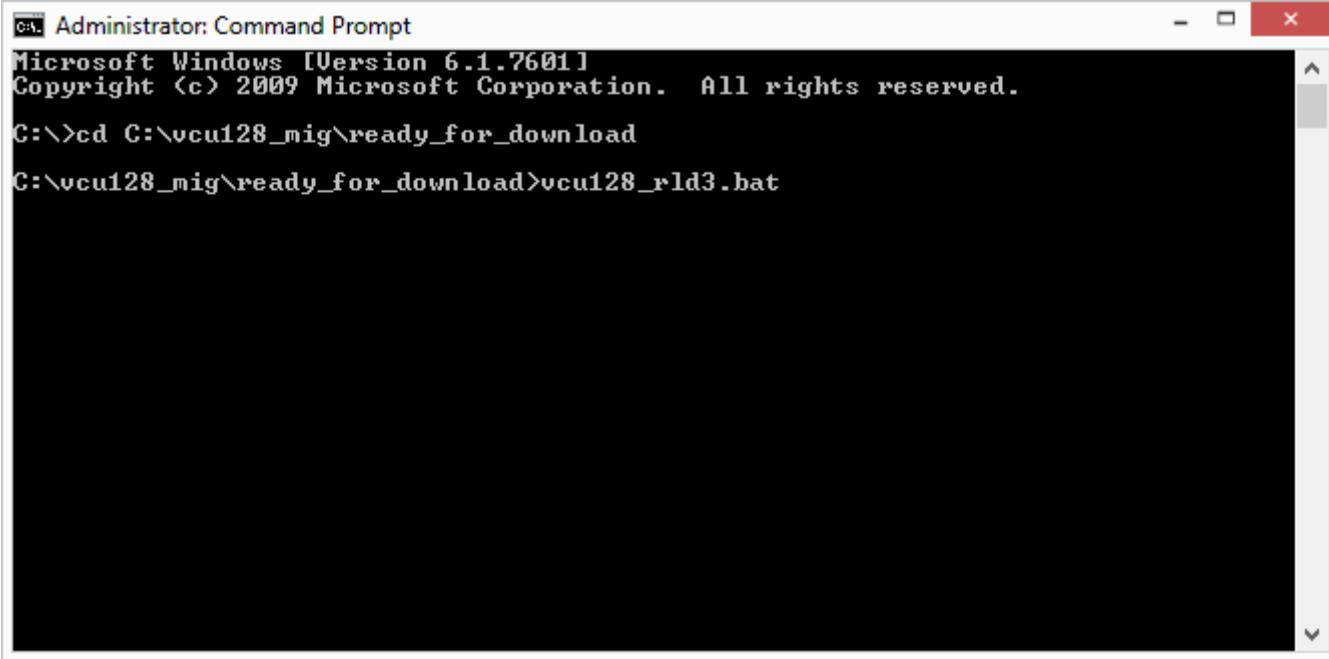
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\vcu128_mig\ready_for_download  
vcu128_rld3.bat
```

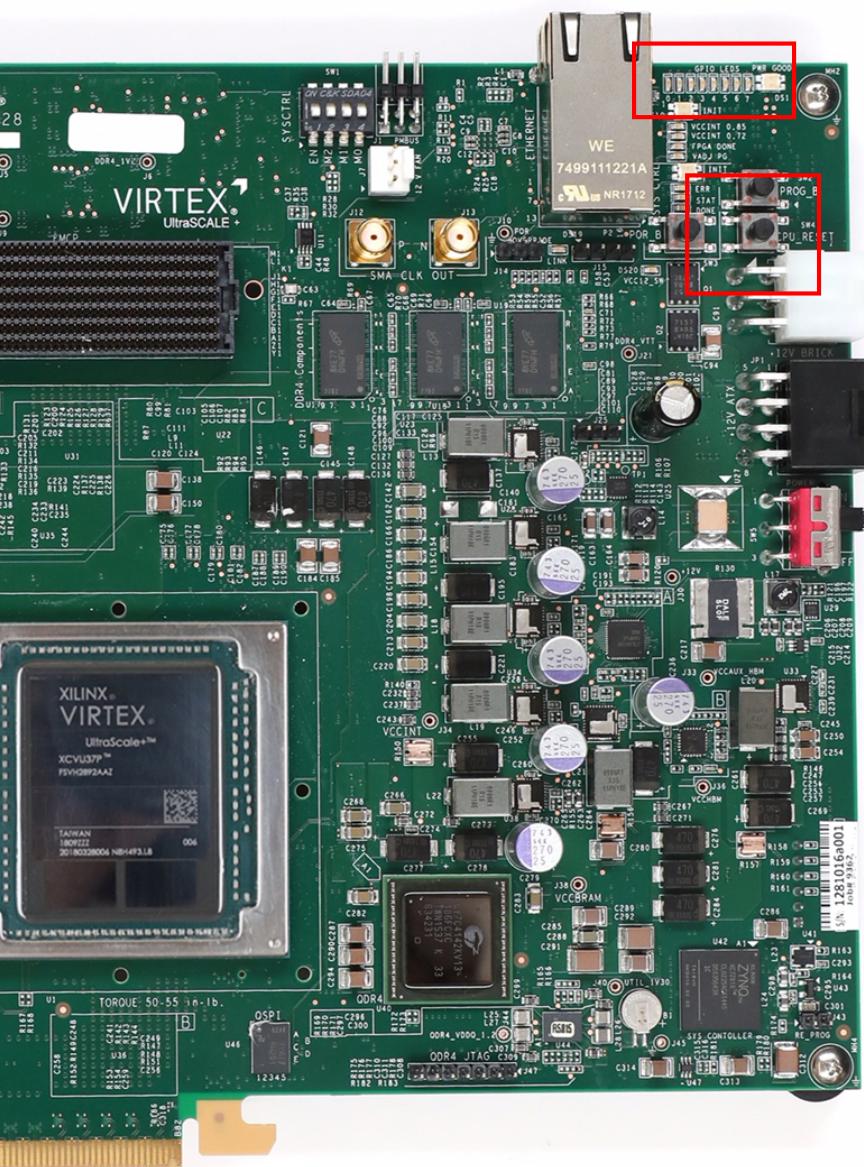


The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu128_mig\ready_for_download
C:\vcu128_mig\ready_for_download>vcu128_rld3.bat
```

Run MIG Example Design



- > After bitstream loads, LED 0 (left most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW4, is the reset

Generate MIG QDR Example Design

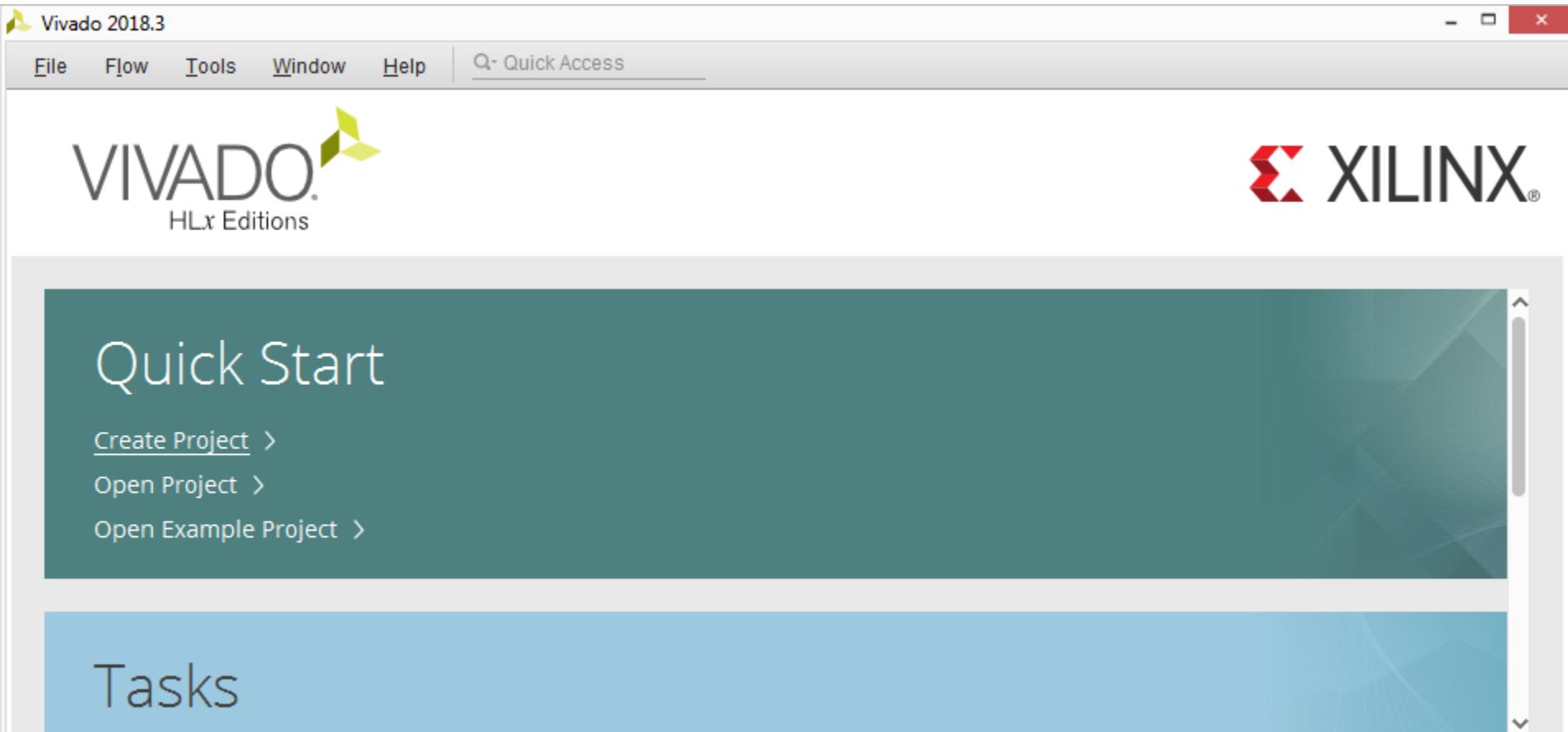


Generate MIG QDR Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2018.3 → Vivado

> Select Create Project



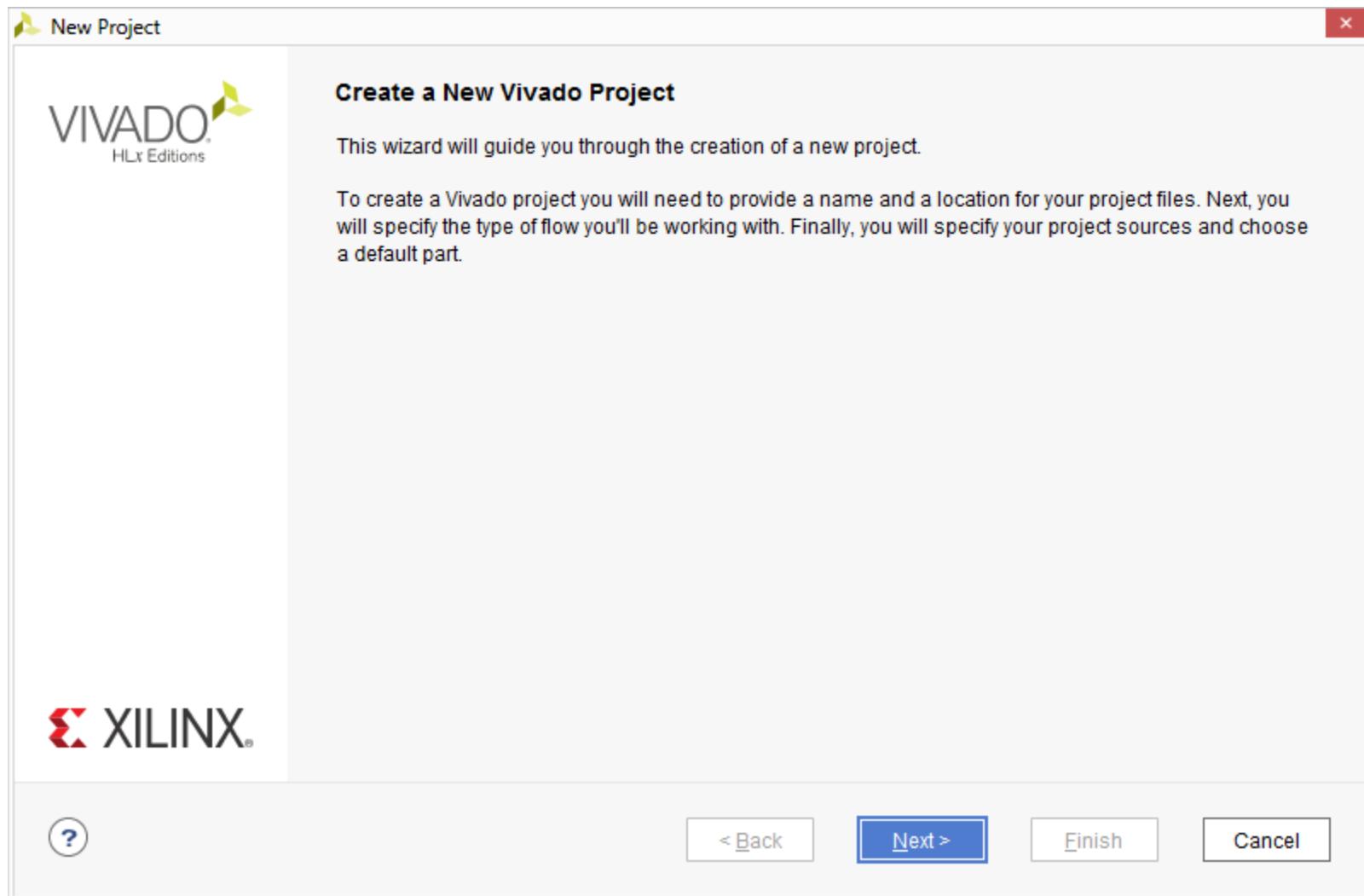
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU128

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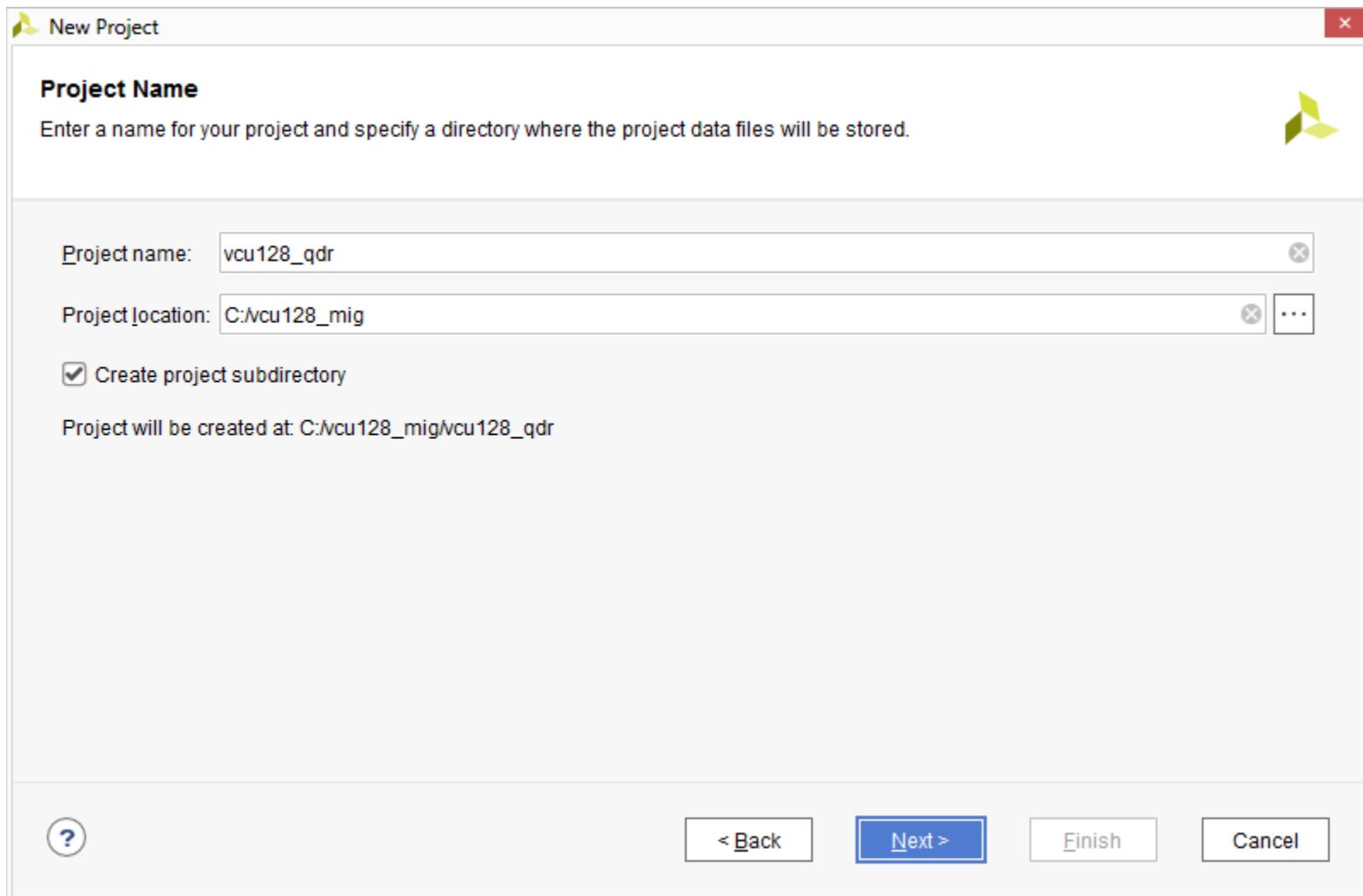
Generate MIG QDR Example Design

> Click Next



Generate MIG QDR Example Design

- > Set the Project name to vcu128_qdr and location to C:/vcu128_mig
 - » Check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Generate MIG QDR Example Design

> Select RTL Project

» Select Do not specify sources at this time

New Project X

Project Type
Specify the type of project to create.



RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Generate MIG QDR Example Design

- > Under Boards, select the VCU128

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search: Q-

Display Name	Preview	Vendor	File Version	Part
Virtex-UltraScale VCU110 Evaluation Platform Add Daughter Card Connections		xilinx.com	1.4	xcvu190
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0	xcvu9p-
Virtex Ultrascale+ HBM VCU128-ES Evaluation Platform		xilinx.com	1.0	xcvu37p

?

< Back

Next >

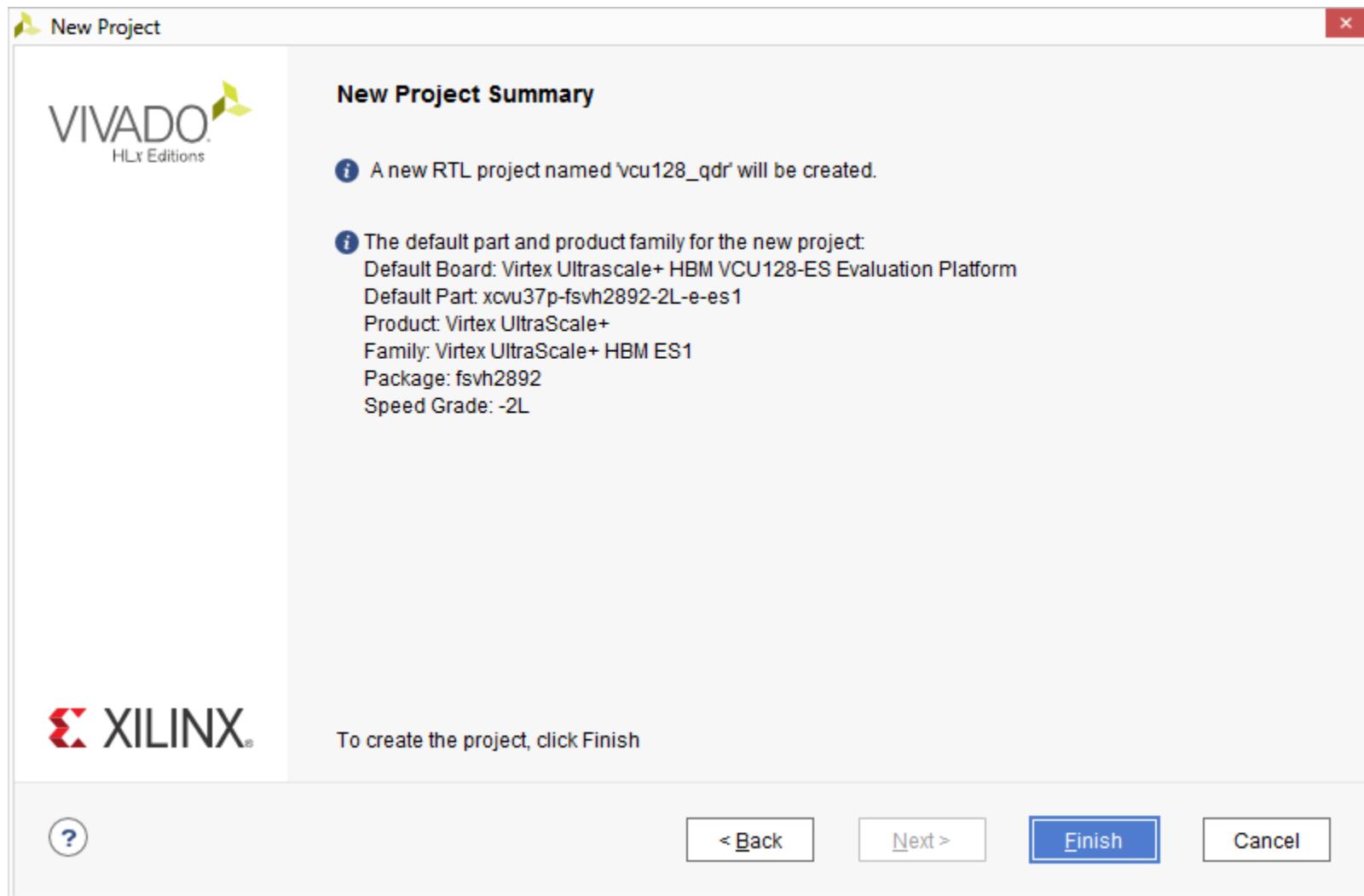
Finish

Cancel

LINX

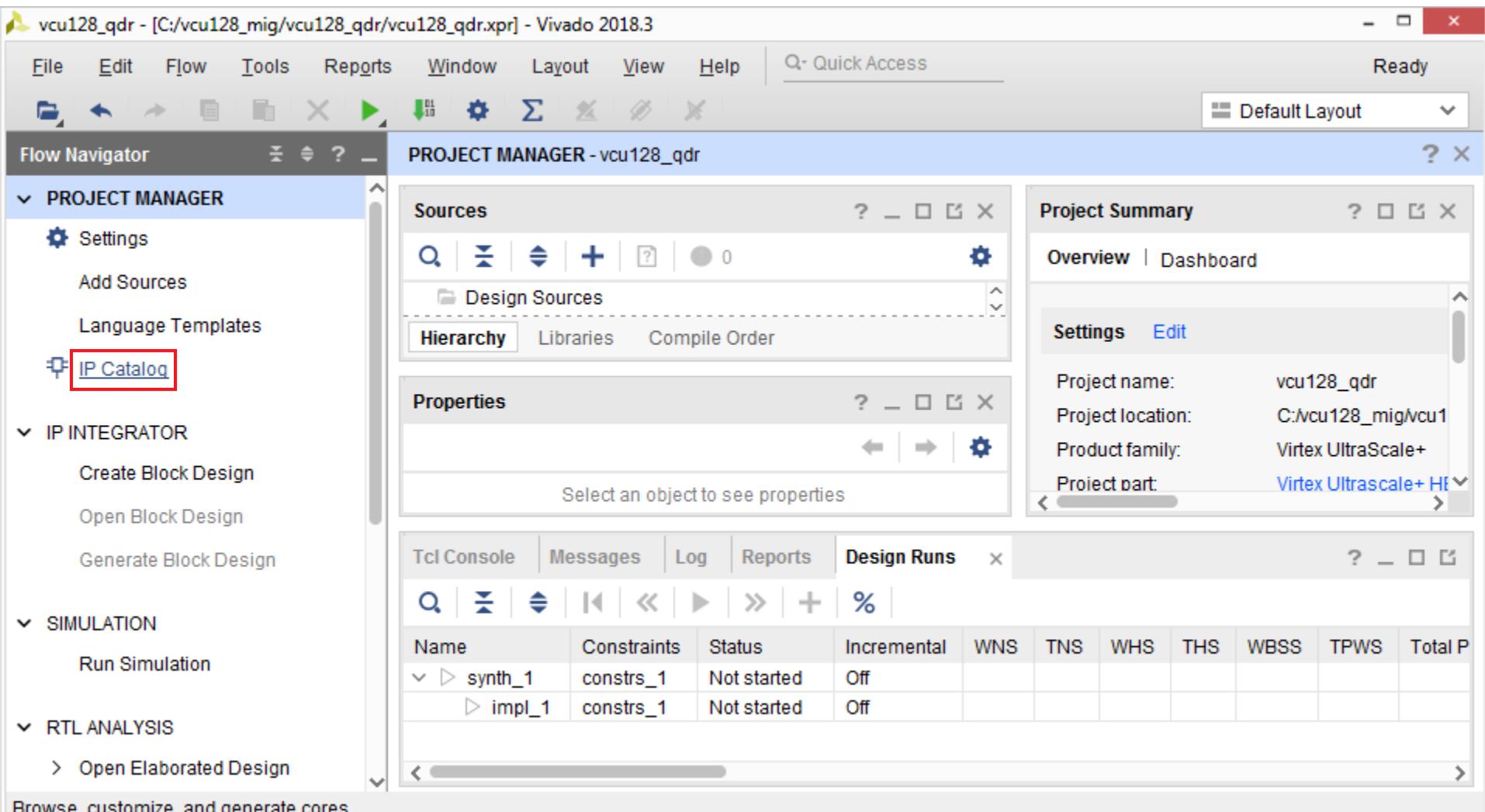
Generate MIG QDR Example Design

> Click Finish



Generate MIG QDR Example Design

> Click on IP Catalog



Generate MIG QDR Example Design

> Select QDRIV SRAM (MIG), 2.0

The screenshot shows the Vivado 2018.3 interface with the project "vcu128_qdr" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, and RTL Analysis sections. The IP Catalog section is currently active, displaying the IP Catalog tab. The catalog lists various IP cores, including Memories & Storage Elements like ECC, External Memory Interface (DDR3 SDRAM, DDR4 SDRAM, LPDDR3 SDRAM, QDRII+ SRAM, and QDRIV SRAM), and other components. The "QDRIV SRAM (MIG)" entry is highlighted with a blue selection bar. Below the table, a "Details" section shows the version as "2.0 (Rev. 6)". The bottom navigation bar includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs.

Name	AXI4	Status	License	VNV
ECC		Pre-Production	Included	xilinx.com:ip:ecc:2.0
External Memory Interface				
DDR3 SDRAM (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip:ddr3:1.4
DDR4 SDRAM (MIG)	AXI4	Pre-Production	Included	xilinx.com:ip:ddr4:2.2
LPDDR3 SDRAM (MIG)		Pre-Production	Included	xilinx.com:ip:lpddr3:1.0
QDRII+ SRAM (MIG)		Pre-Production	Included	xilinx.com:ip:qdrii:1.4
QDRIV SRAM (MIG)		Pre-Production	Included	xilinx.com:ip:qdriv:2.0

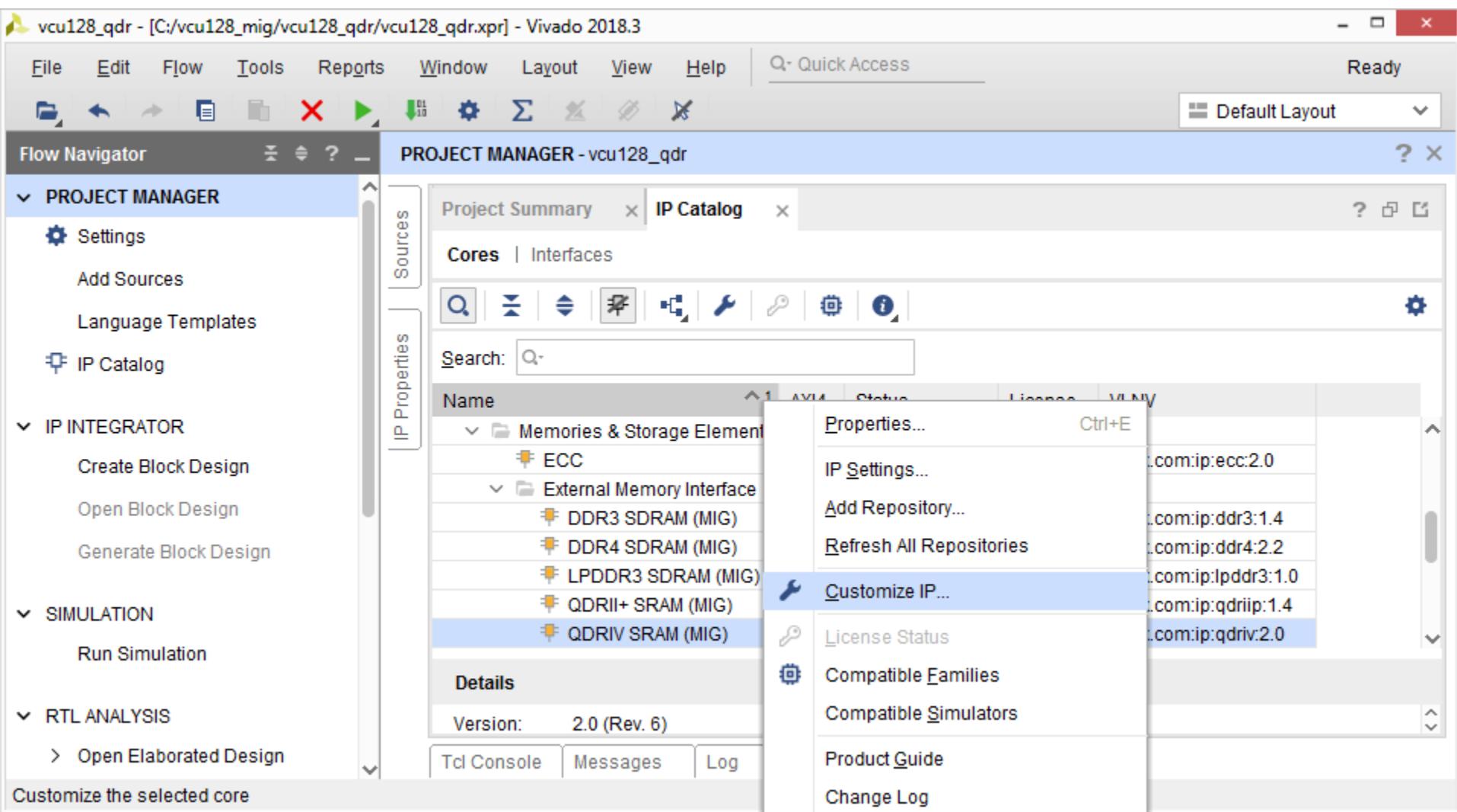
Note: Presentation applies to the VCU128

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Generate MIG QDR Example Design

- > Right click on QDRIV SRAM (MIG)

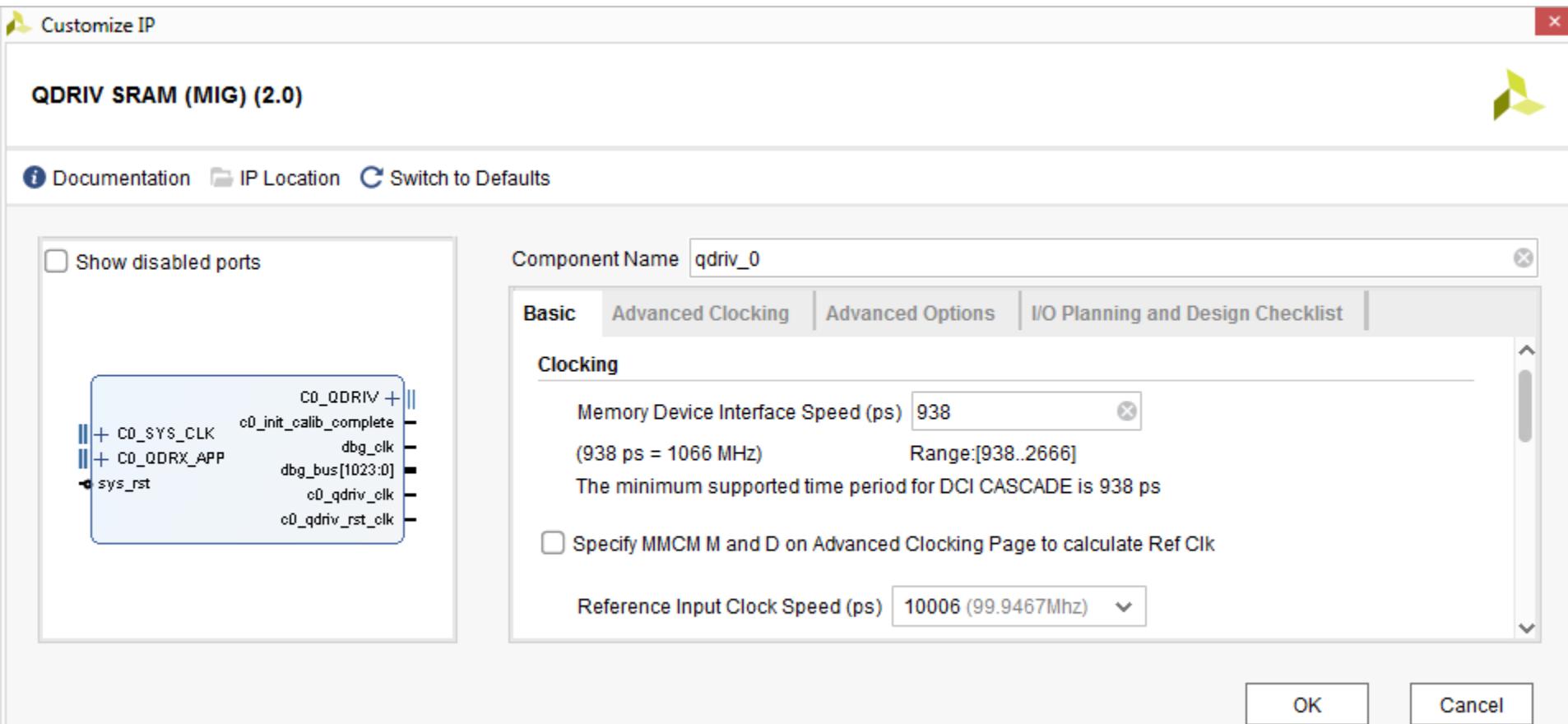
- » Select Customize IP



Note: Presentation applies to the VCU128

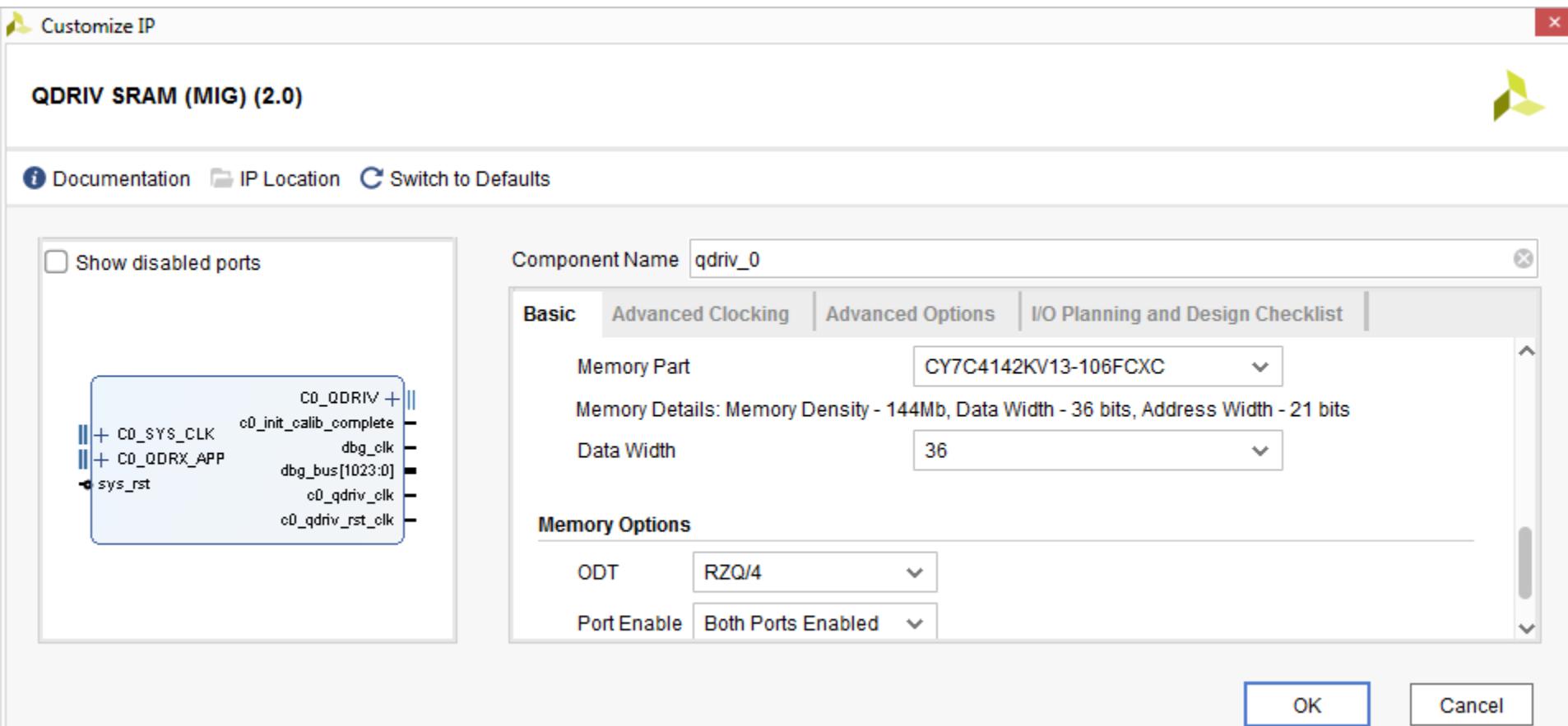
Generate MIG QDR Example Design

- > Set Clock period to 938 for 1066 Mb/s operation.
- > Set the Input Clock to 10006 ps for 100 MHz
- > Scroll down



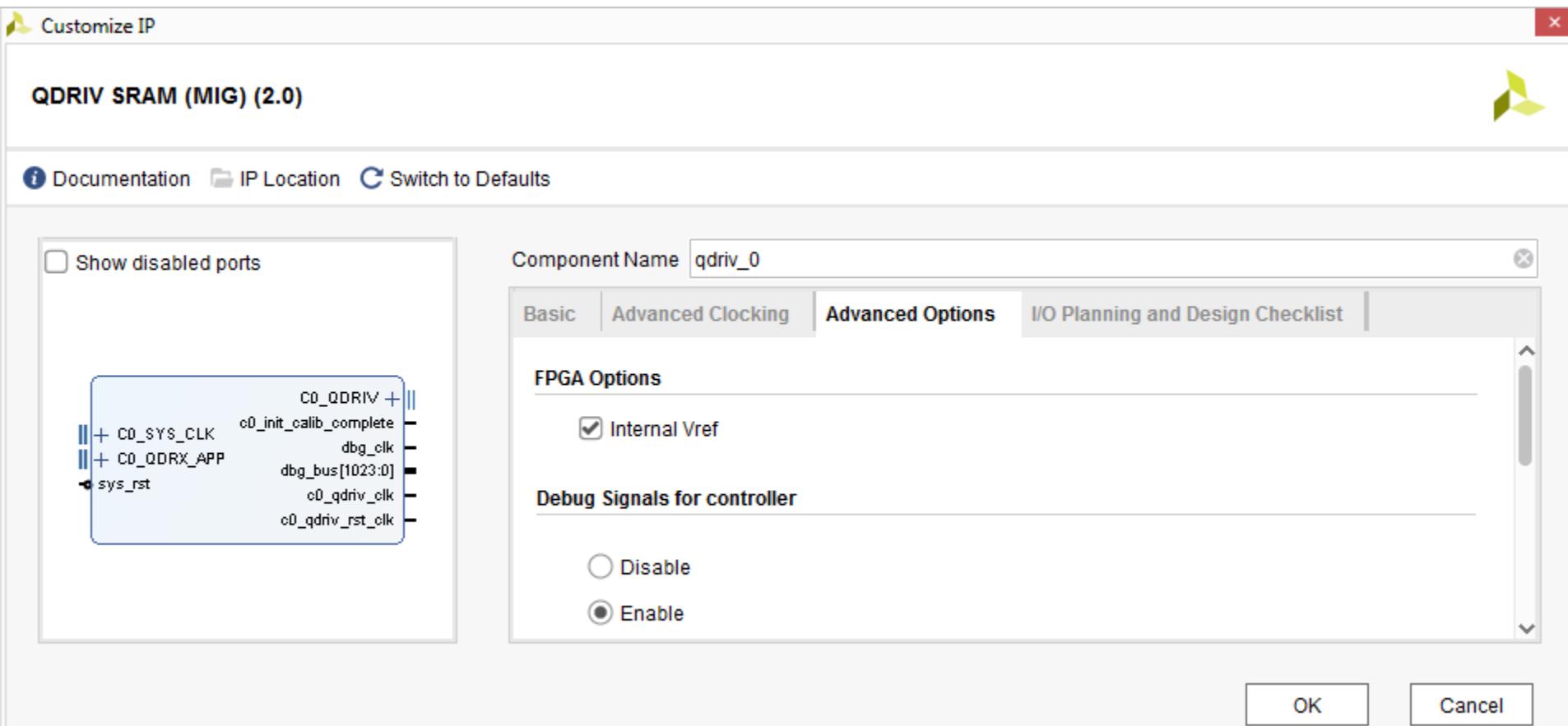
Generate MIG QDR Example Design

- > Select the part CY7C4142KV13_106FCXC
- > Set the Data Width to 36 and click the Advanced Options tab



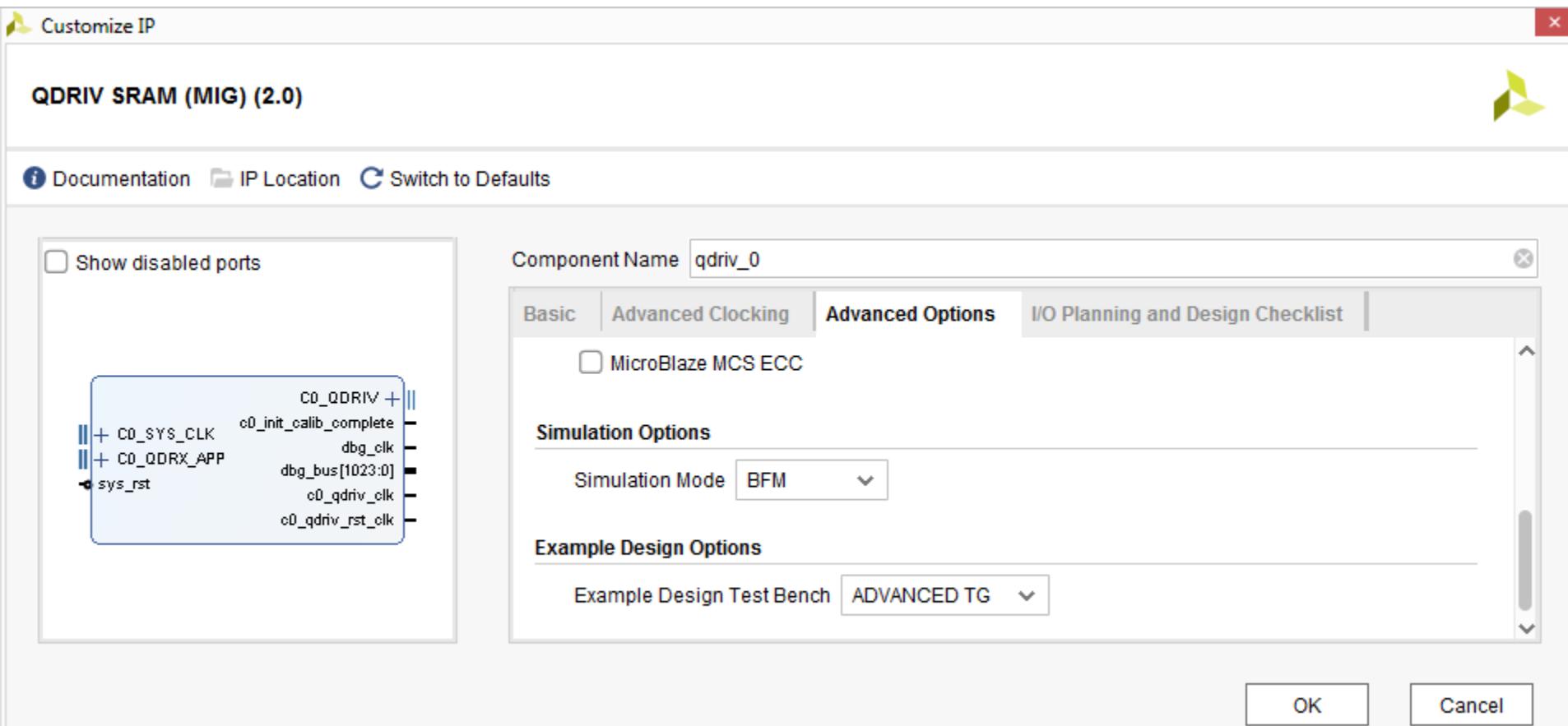
Generate MIG QDR Example Design

- > Set the Debug Signals to Enable
- > Scroll down



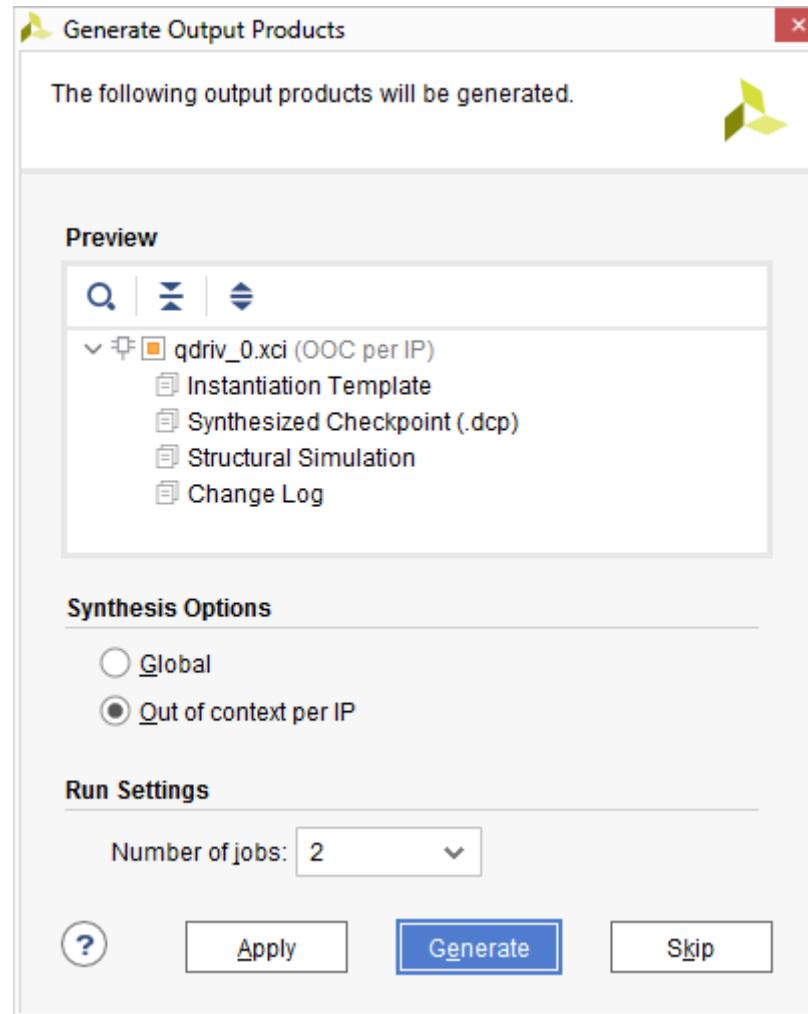
Generate MIG QDR Example Design

- > Set the Example Design Test Bench to ADVANCED TG
- > Click OK



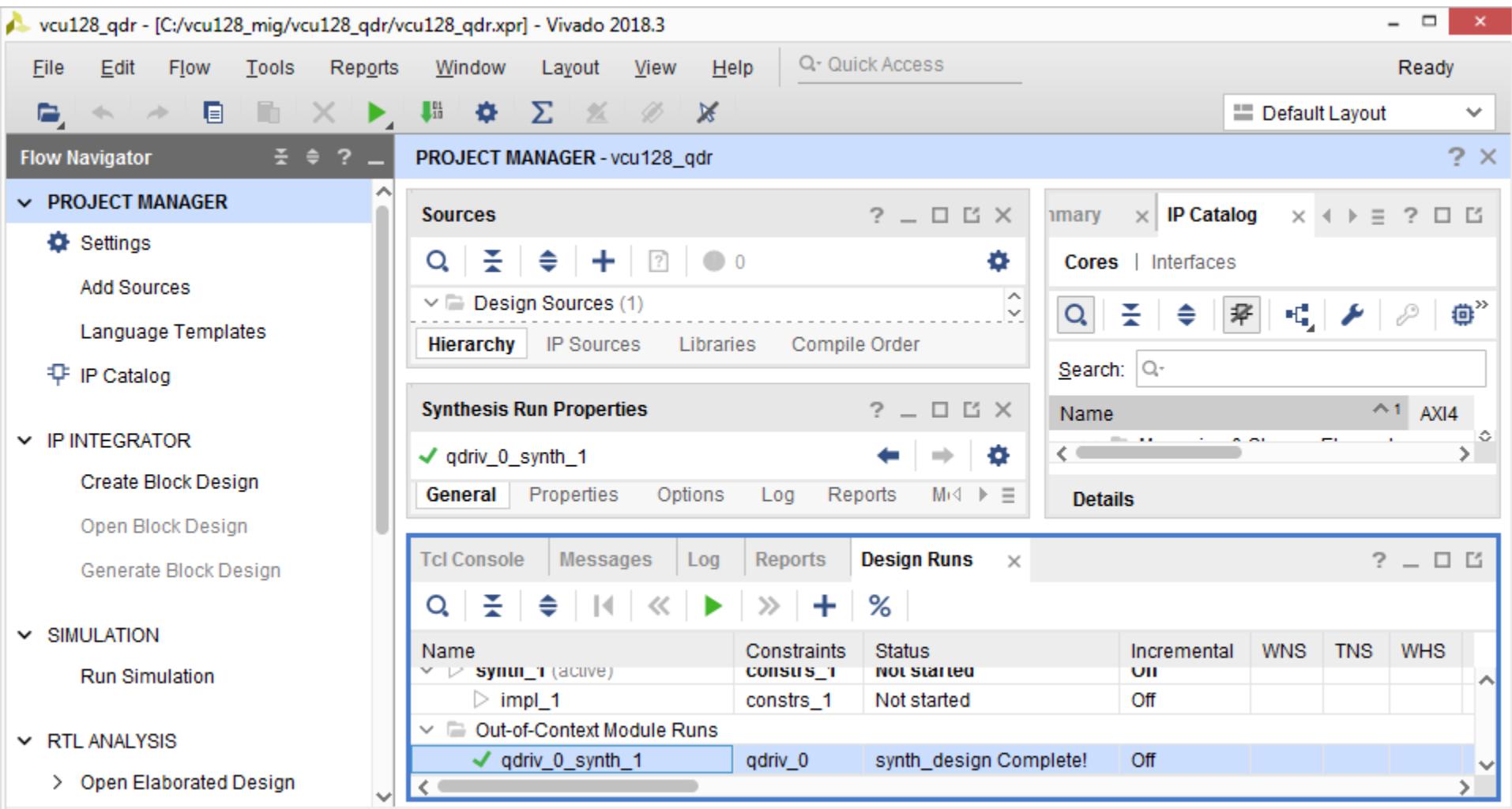
Generate MIG QDR Example Design

- > Click Generate



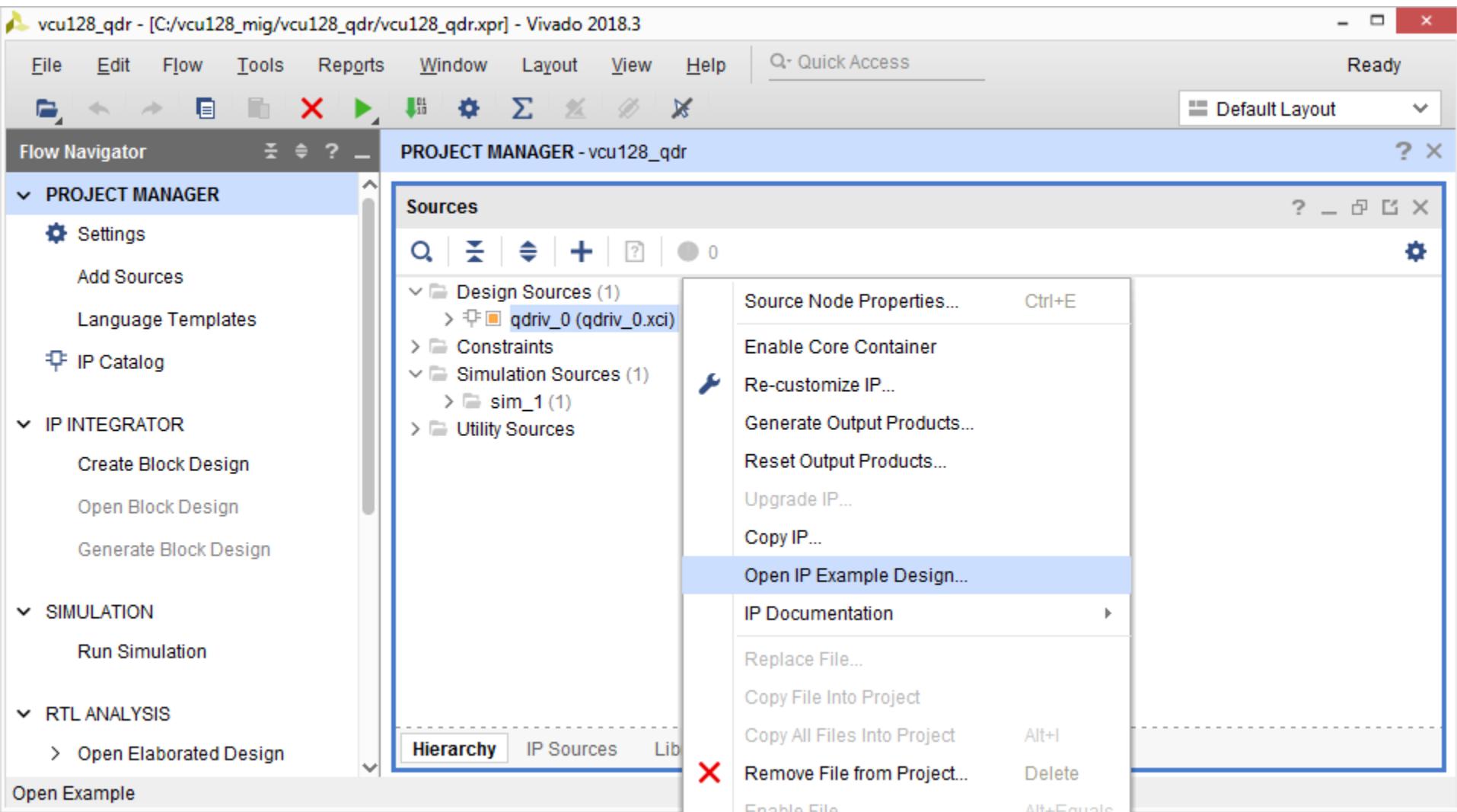
Generate MIG QDR Example Design

- > Wait until checkmark appears on qdriv_0_synth_1



Compile Example Design

- > Right click on qdriv_0 and select Open IP Example Design...

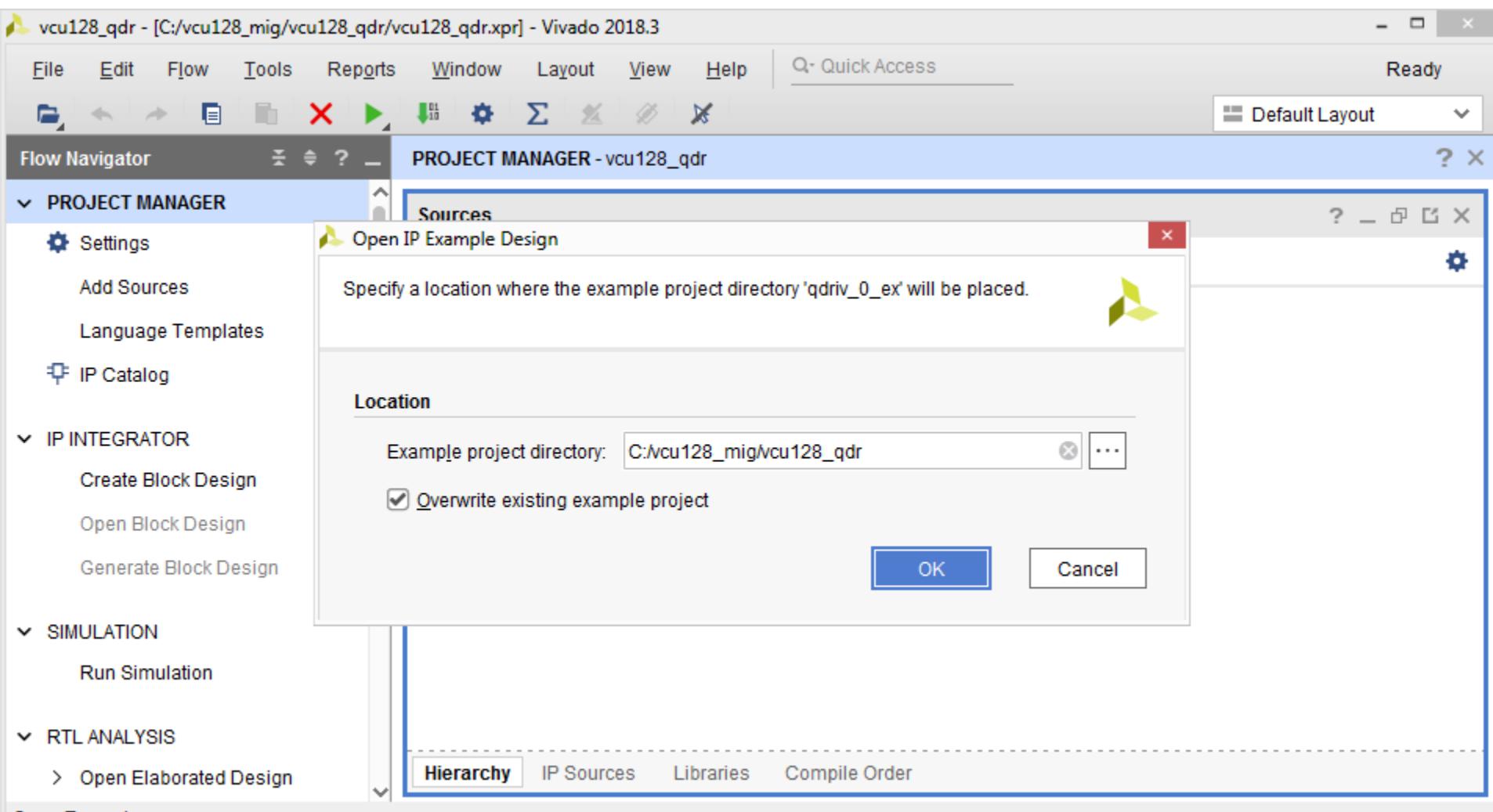


Note: Presentation applies to the VCU128

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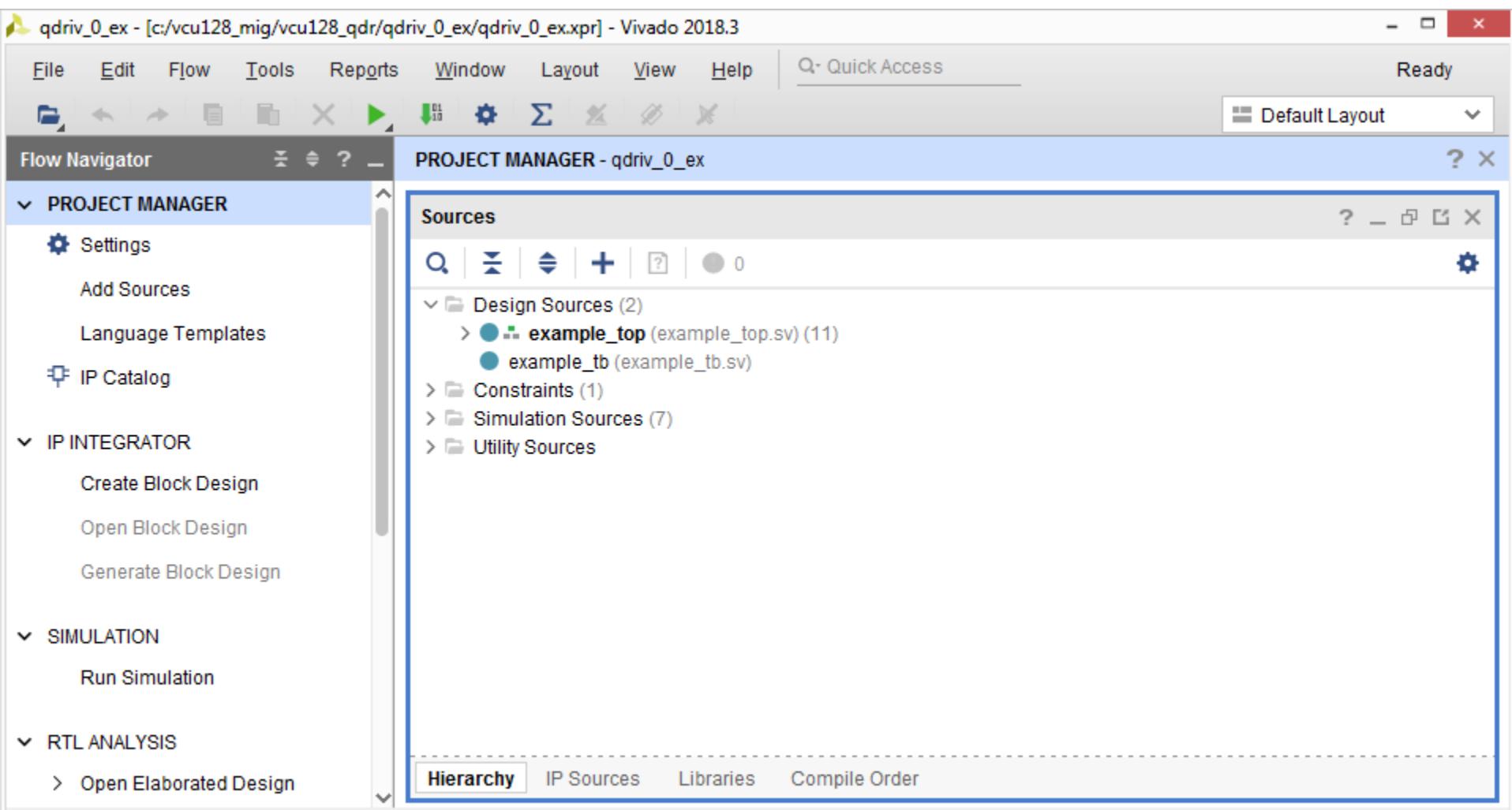
Compile Example Design

- > Set the location to C:/vcu128_mig/vcu128_qdr and click OK



Compile Example Design

- > A new project is created under <design path>/

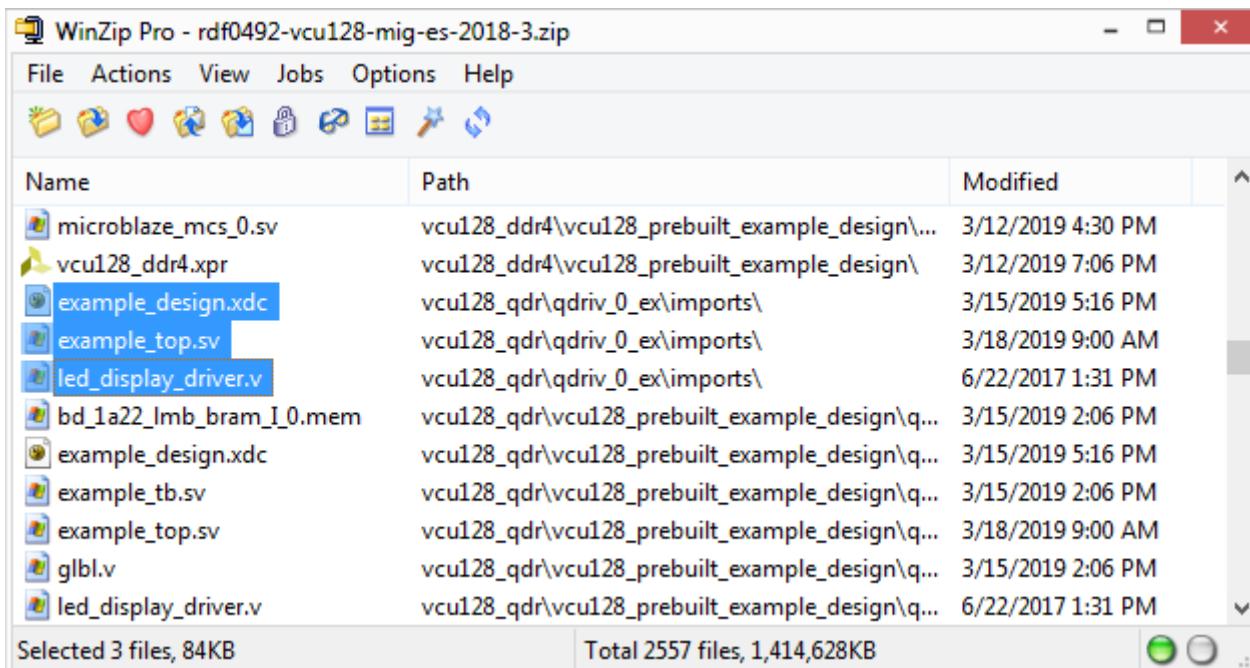


Note: The original project window can be closed

Modifications to Example Design

> From the RDF0492 - VCU128 MIG Design Files (2018.3 C) ZIP file

- » Extract the **vcu128_qdr** files, **example_design.xdc**, **example_top.sv**, and **led_display_driver.v**
- » Overwrite these three existing files in your **vcu128_qdr** MIG design
- » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs
- » The following commands will add the **led_display_driver.v** and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse
```

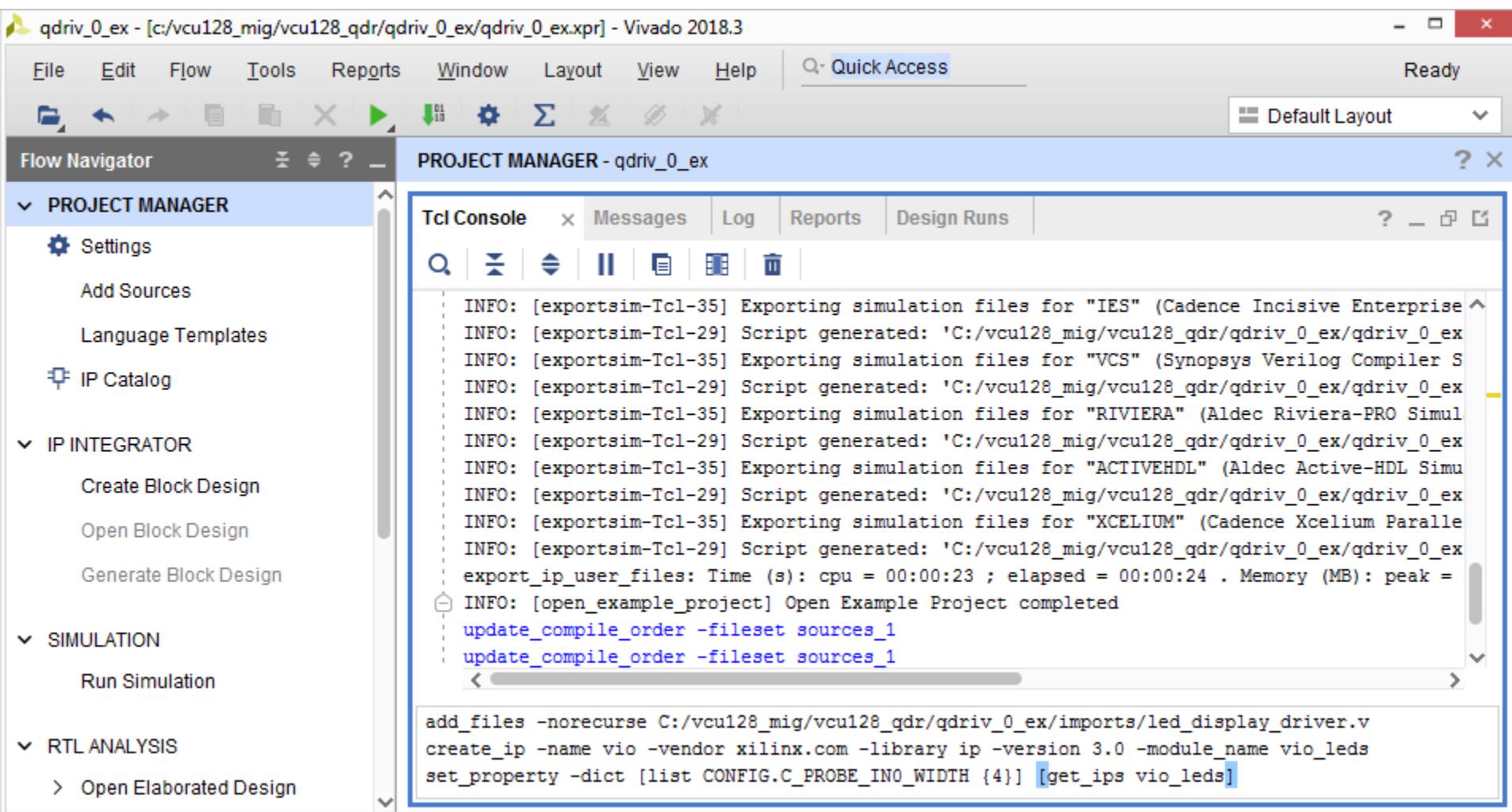
```
C:/vcu128_mig/vcu128_qdr/qdriv_0_ex/imports/led_display_driver.v
```

```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

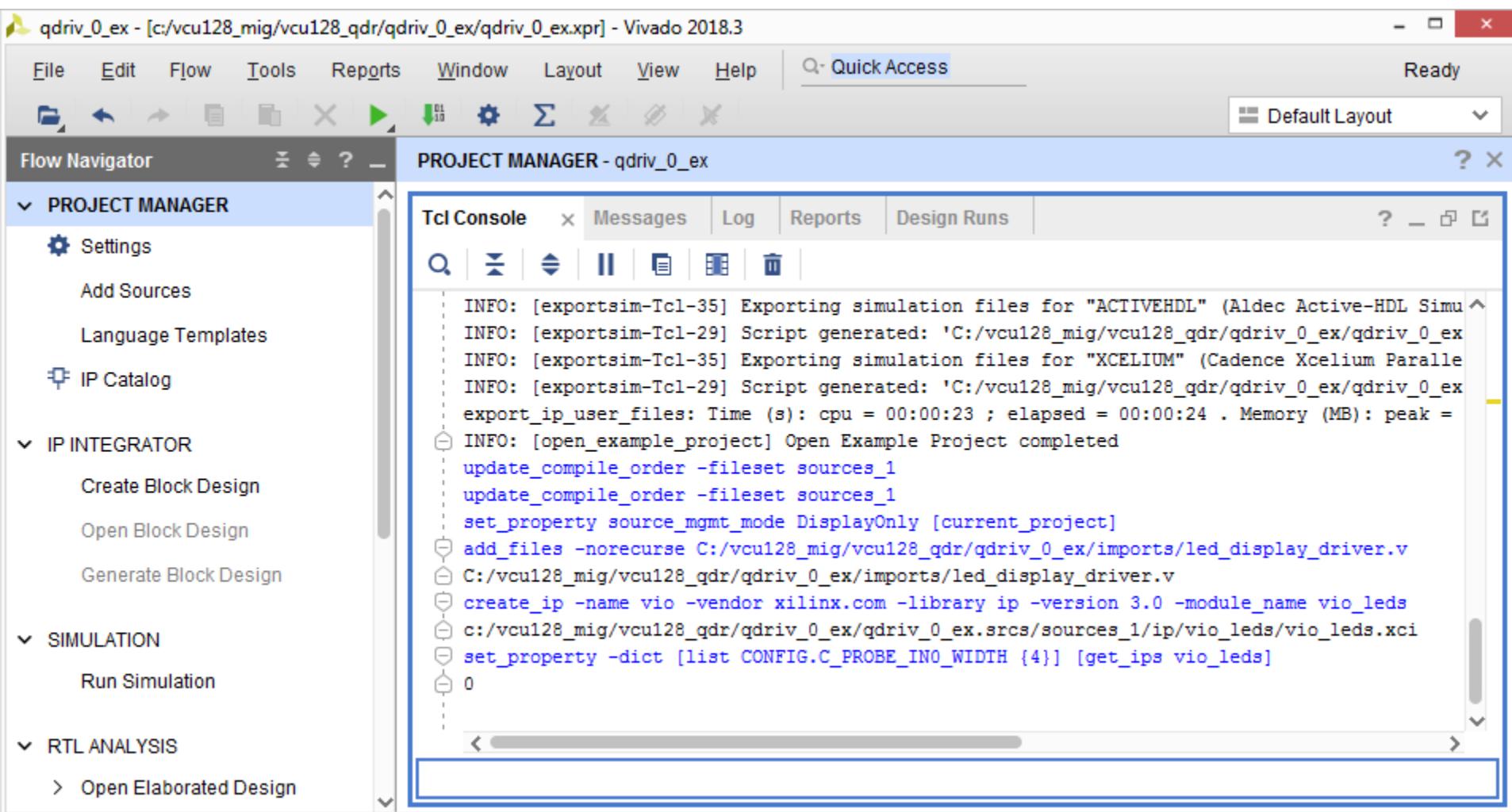
Modifications to Example Design

- > Press enter after entering Tcl commands



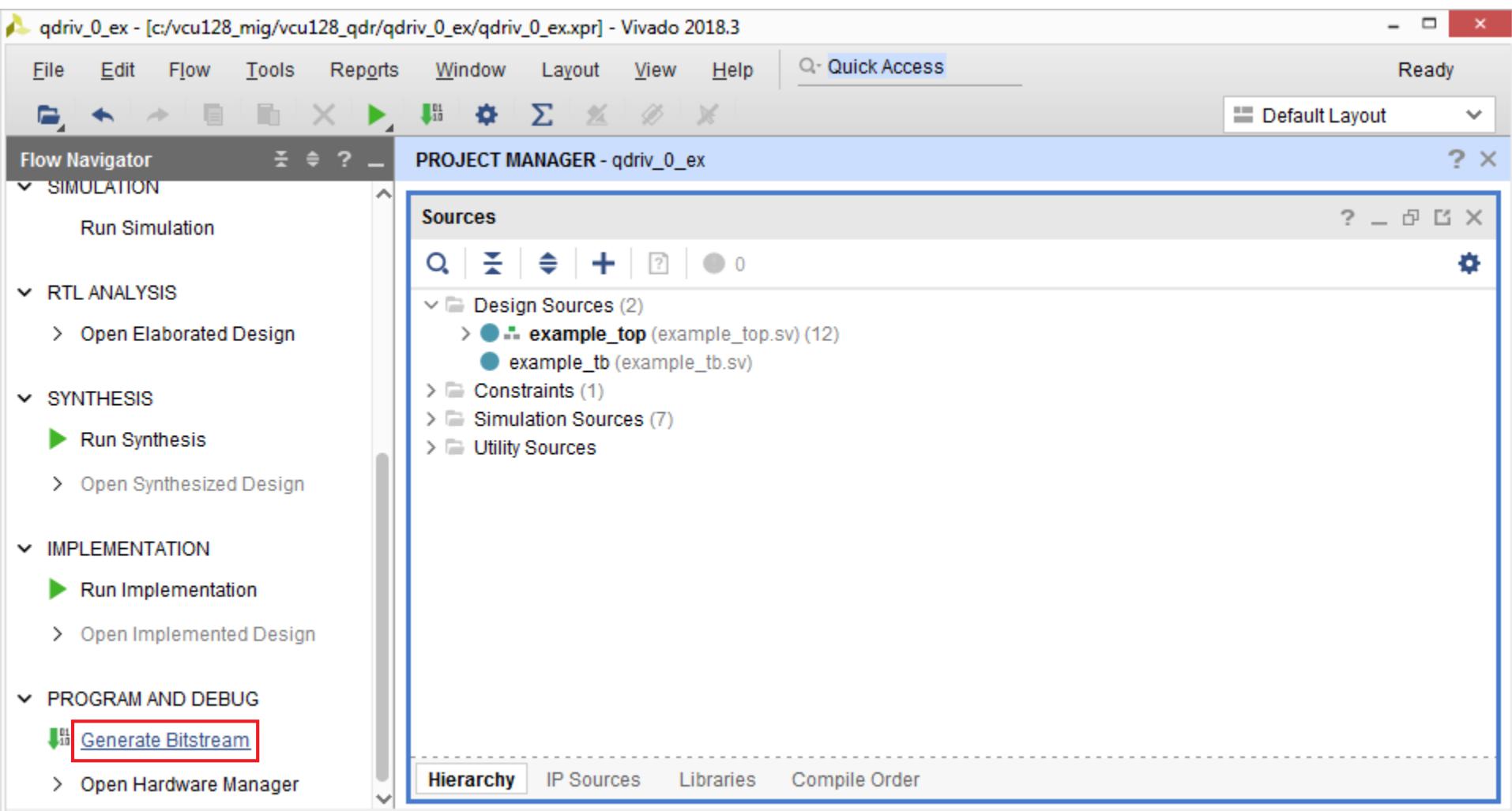
Modifications to Example Design

- > Tcl commands completed successfully



Compile Example Design

- > Click on Generate Bitstream



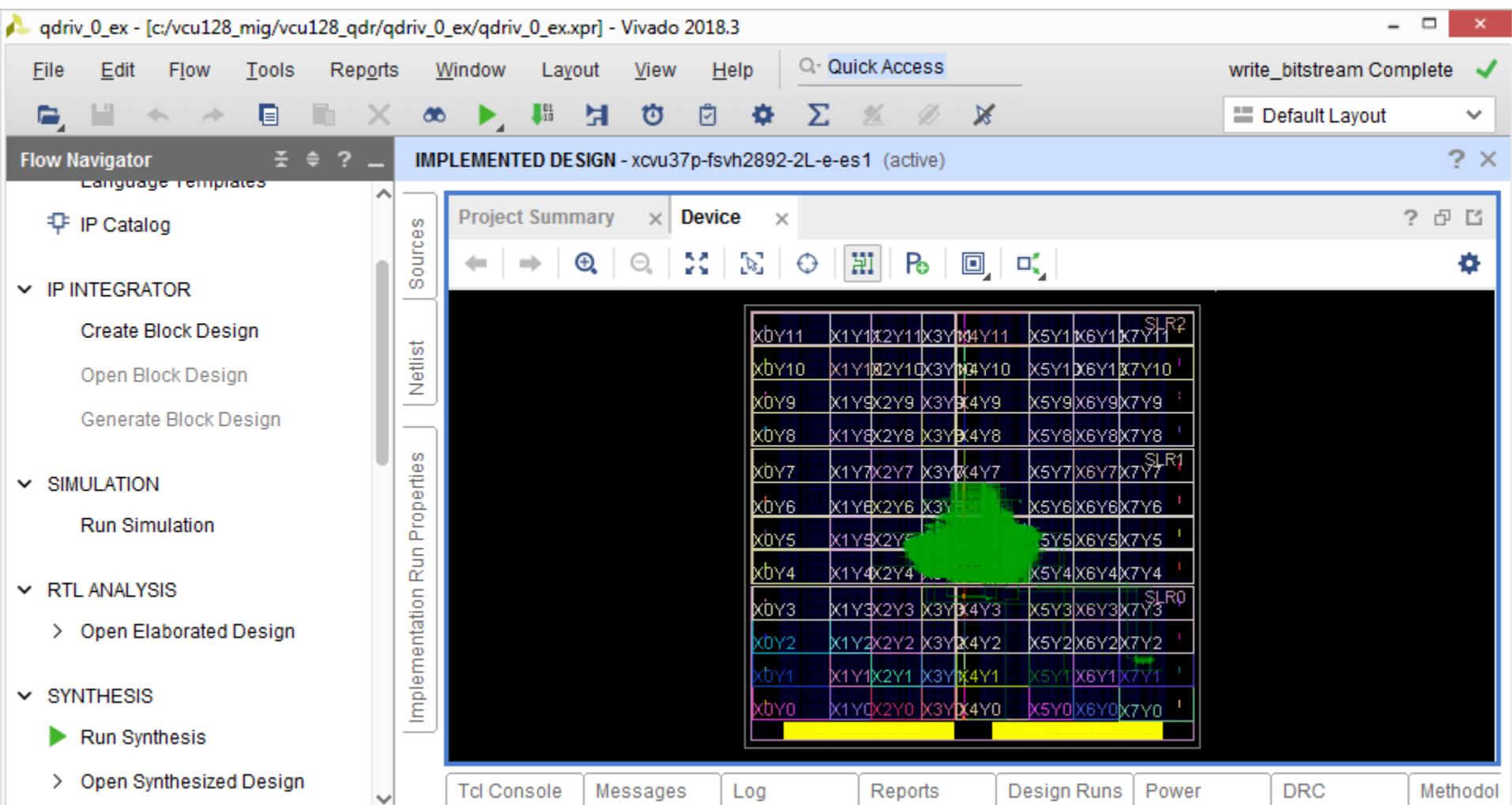
Generate a programming file after implementation

Note: Presentation applies to the VCU128

 XILINX

Compile Example Design

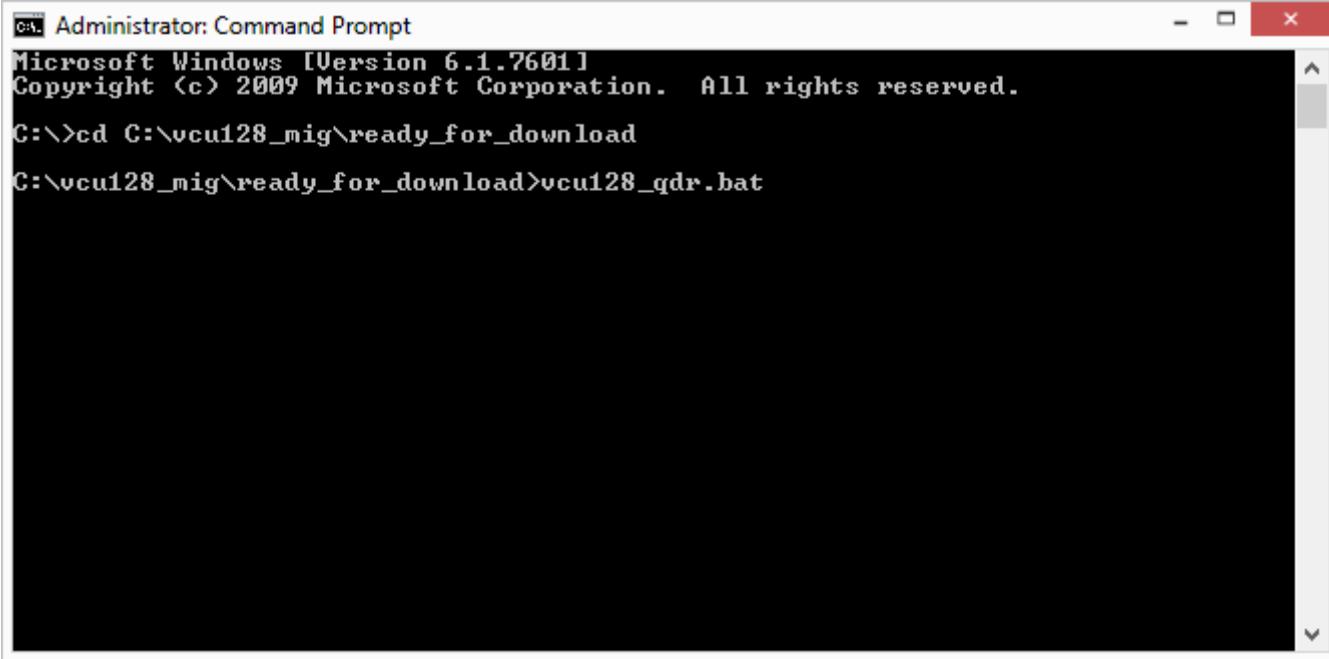
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\vcu128_mig\ready_for_download  
vcu128_qdr.bat
```

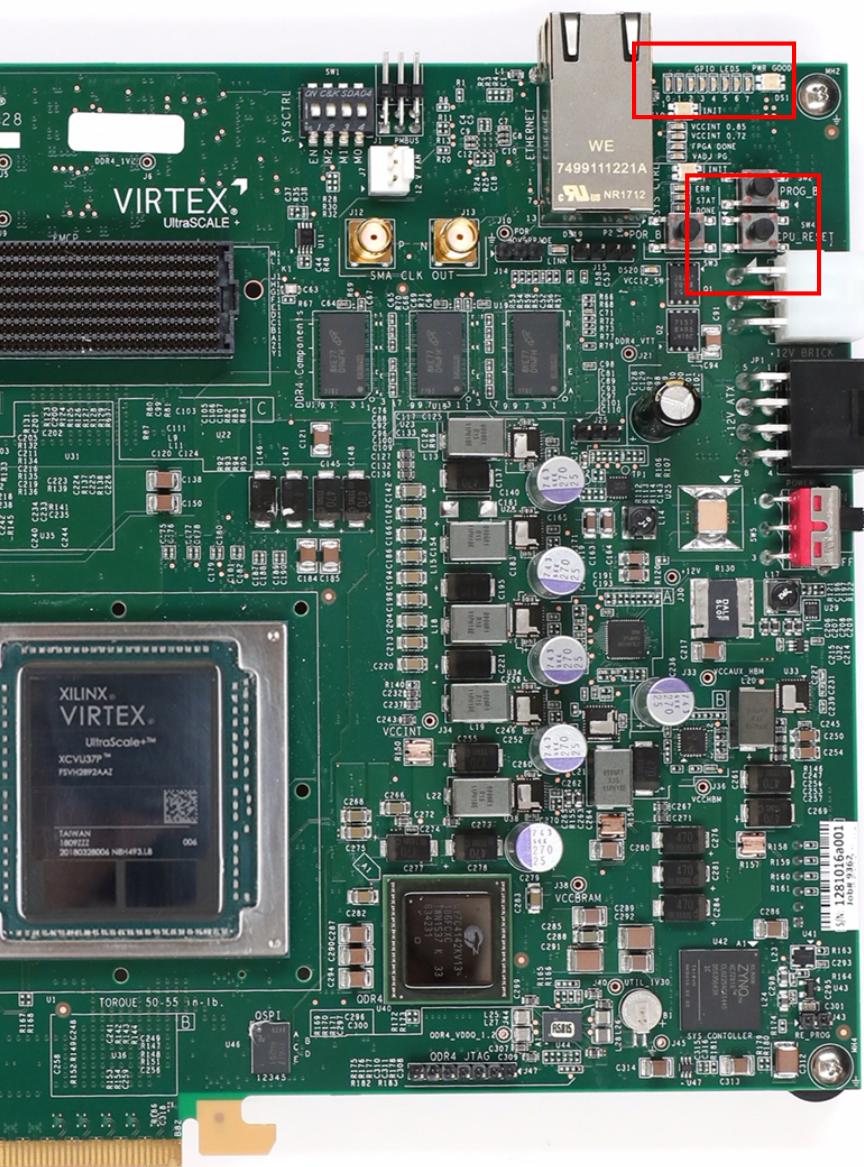


The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu128_mig\ready_for_download
C:\vcu128_mig\ready_for_download>vcu128_qdr.bat
```

Run MIG Example Design



- > After bitstream loads, LED 0 (left most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW4, is the reset

References



References

> Virtex UltraScale Memory

- » UltraScale FPGA Memory Interface Solutions Product Guide – PG150
 - https://www.xilinx.com/support/documentation/ip_documentation/ultrascale_memory_ip/v1_4/pg150-ultrascale-memory-ip.pdf

> Vivado Release Notes

- » Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_3/ug973-vivado-release-notes-install-license.pdf
- » Vivado Design Suite 2018 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/70860.html>

> Vivado Programming and Debugging

- » Vivado Design Suite Programming and Debugging User Guide – UG908
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_3/ug908-vivado-programming-debugging.pdf

Documentation



Documentation

> Virtex UltraScale+ HBM

- » Virtex UltraScale+ FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html>

> VCU128 Documentation

- » Virtex UltraScale+ FPGA VCU128 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/vcu128-es1.html>
- » VCU128 Board User Guide – UG1302
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu128/ug1302-vcu128-eval-bd.pdf
- » VCU128 - Known Issues and Release Notes Master Answer Record
 - <https://www.xilinx.com/support/answers/71849.html>