UltraScale FPGAs Transceivers Wizard Demo Script

Introduction

In this demonstration, you will customize a transceiver and generate and implement its example design.

Preparation:

- Required files: `$us_transceiver/demo`
- Required hardware: None
- Supporting materials: "UltraScale Architecture Transceivers" module

UltraScale FPGAs Transceivers Wizard

Action with Description	Point of Emphasis and Key Takeaway
• Launch the Vivado Design Suite 2019.1.	
• Click the **Create Project** link in the Quick Start section of the Getting Started page.	• The New Project link in the Getting Started page allows you to create a new Vivado Design Suite project.

• Create a new project using the New Project Wizard with the following details:
  • Project name: *transceiver_demo.xpr*
  • Project location: `$us_transceiver/demo`
  • Enable **Do not specify the sources at this time**.
  • Select the **KCU105** Board.
  • Click **Finish** to create the project.
	• By default, the Vivado IDE creates the project name as *project_1*.

• Select **IP Catalog** under Project Manager in the Flow Navigator.	Open the IP catalog.

Action with Description	Point of Emphasis and Key Takeaway
• In the IP catalog, expand **FPGA Features and Design** > **IO Interfaces** and double-click **UltraScale FPGAs Transceivers Wizard**.	Open the Transceiver Wizard.
• Examine the links under the headline.	The GUI offers general information: • Link to documentation • List of presets • IP location on host • Switching to default settings
• Select the **IP Symbol** tab in the left frame and explain the graphical view window. • Enable and disable the **Show disabled ports** option under the IP Symbol tab.	The GUI offers an IP Symbol graphic that will be updated during configuration. • Where would you find what the functionality of the ports shown in the diagram are?
• Select the **Physical Resources** tab in the left frame and review the graphical view window. • Use the scroll bar to view all content.	The GUI offers a graphical representation of the physical resources that will be updated during configuration. This includes clocking connectivity. • What resources are described in this tab?

Action with Description	Point of Emphasis and Key Takeaway
• Select the **Basic** tab and observe the configuration options.	The Basic tab provides customization options for fundamental transceiver features, including transceiver type, transmitter, and receiver settings. It also provides the ability to select a transceiver configuration preset. • What type of presets are available? • What does the Transceiver type select?
• In the System section (Transceiver Configuration Preset), select **GTH**:**CPRI 10 Gb/s**.	Transmitter and receiver parameters will be set according to the selected protocol.
• Select any parameter in the Transmitter section and observe the customization options.	Try a few customization options (alter the user data width). • Does this change alter the symbol generated? Go to the IP Symbol graphic, which may be updated.
• Select the **Physical Resources** tab and observe the configuration options.	The Physical Resources tab provides table and graphical interfaces to select specific transceiver channel sites to enable as well as reference clock routing options. • Record the pins used for channel X0Y0. Verify their location in the Pin Planning view later.

Action with Description	Point of Emphasis and Key Takeaway
• Select a different channel and reference clock source. Use the scroll bar in the Physical Resources graphical window to show the new settings. • Finally, select **GTHE3_CHANNEL_X0Y0** and **MGTREFCLK0**.	Demonstrate channel and clocking assignment. • Why does the QPLL0 assignment not change by selecting a different channel? • From the physical resources pane record that QPLL0 and QuadX0Y0_clk0 was used by default. Verify their location in the Pin Planning view later.
• Select the **Optional Features** tab and explain some of the options.	The Optional Features tab provides extensive configuration options for optional or advanced features, if appropriate for the application.
• Expand the **Receiver comma detection and alignment** section. Notice that all parameters are set.	8B/10B encoding requires K characters for operation.
• Select the **Structural Options** tab and observe the configuration options.	The Structural Options tab provides location choices for each available helper block and the optional port enablement interface. • Review the helper blocks.
• Expand the **Quad PLL Ports** section. Select the **qpll0lock_out** port. • Click **OK** to create the directory.	Demonstrate enabling additional ports. • Can you verify that this new port was made? **Hint:** View the IP Symbol pane.
• Name the transceiver IP component as **my_trx**.	Replace the generic component name with a user-specific name.
• Click **OK**.	Generate the core configuration file.

Action with Description	Point of Emphasis and Key Takeaway
• In the Generate Output Products dialog box, click **Generate**.	Generate the core files. Synthesis of the core will be performed. • What is the purpose of each of these output files?
• Observe the design hierarchy in the Sources tab. • Review the other tabs as well.	The IP core source file is just the XCI file. • Are there any pin assignments associated with the creation of this core? How can you verify this? • Refer to the IP Sources tab, expand the Synthesis folder, and review the contents of the XDC files.
• Review the **IP Sources** tab. • Observe the different IP products generated under my_trx.	By default the following IP products are generated: • Instantiation template • Synthesis • Simulation • Change log • DCP • Stub
• Expand each IP output products folder and observe the different files under them.	• Explore the generated files.
• In the Sources window, under Design Sources, right-click **my_trx (my_trx.xci)** and select **Open IP Example Design**.	• This creates the IP example design that will be stored in a different directory. The original design will be untouched.

Action with Description	Point of Emphasis and Key Takeaway
• In the Open Example Design dialog box, browse to the `$us_transceiver/demo` directory to store the example design. • Click **OK**.	• A new Vivado Design Suite session opens with the IP example design.
• Observe the design hierarchy. • Review the other tabs as well.	• The generated example design includes all files for synthesis, simulation, and implementation. • The design hierarchy includes the pattern generation and checking blocks. • Note that *my_trx_example_top* is the top-level name for the new project. How did the pin assignments get made? *example_wrapper_inst* includes the helper block files for (as specified in the Transceiver Wizard): • TX user clock • RX user clock

Summary

In this demo, you walked through the customization of an UltraScale FPGA transceiver using the Transceiver Wizard. This new version of the wizard supports detailed IP core customization and the use of flexible helper blocks. You also generated an example design.