Vivado Boot Camp Day 1 Notes

Resources:  
 User Guides

Product Guides

**Vivado Synthesis Guide 901 –** coding attributes!!!

https://slideplayer.com/slide/5967461/

**Training Overview**:

**CLB**s:

Slices

LUTs

**CIB**s (Configurable Interconnect Blocks; Interconnect Fabric).

Memory Resources (UltraRAM vs HBM?):

**LUT**s

**Distributed** **RAM**

**B**lock **RAM**,

**UltraRAM** (288Kb SRAM) ???

High Bandwidth memory (HBM) ???

FIFO

DSP Resources

Interfacing:

I/O

SERDES design,

DDR4 Physical Layer Interfaces.

Clocking Resources:

MMCM (clock manager)

PLL

**Day 1 Overview**:

Architecture.

CLB Resources.  
HDL Coding Techniques.

Memory Resources.

DSP Resources.

**Day 2 Overview**:

IO Resources

Component Mode

Native Mode

Clocking Resources

**Day 3 Overview**:

Clocking Resources.

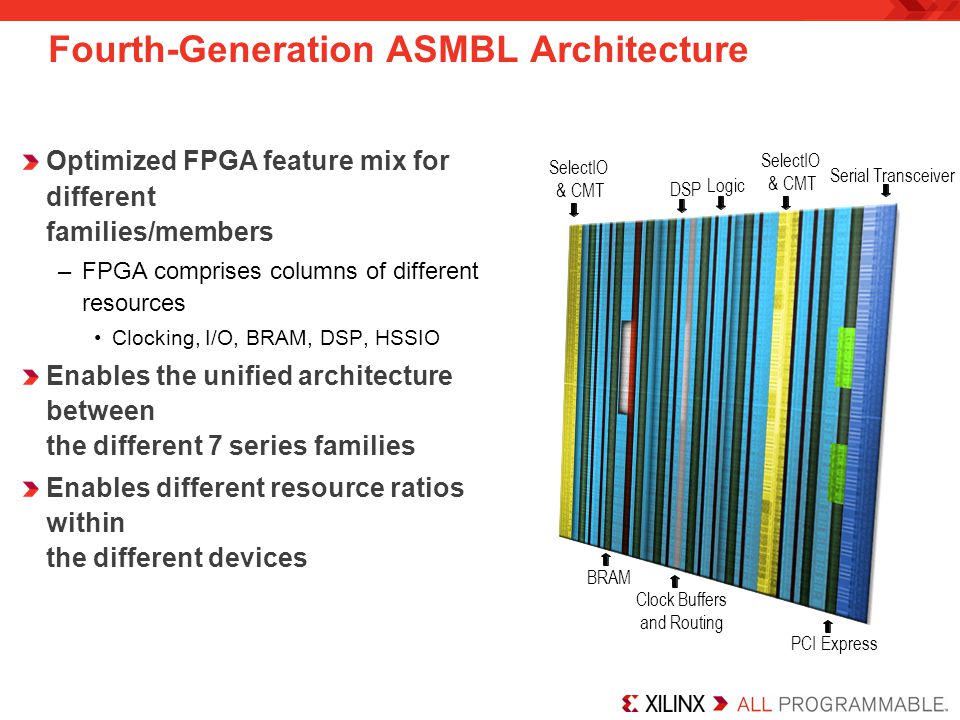
Dedicated Hardware (ADCs and such)

Transceivers.

Migration methodology.

Zynq SoC Architecture Overview.

Starting with the 7-series and up the Fourth Generation ASMBL Architecture (everything is organized in columns) is used:



Logic (CLB) Columns.

DSP Columns.

BRAM Columns and UltraRAM Columns.

Clock Buffers and Routing Columns.

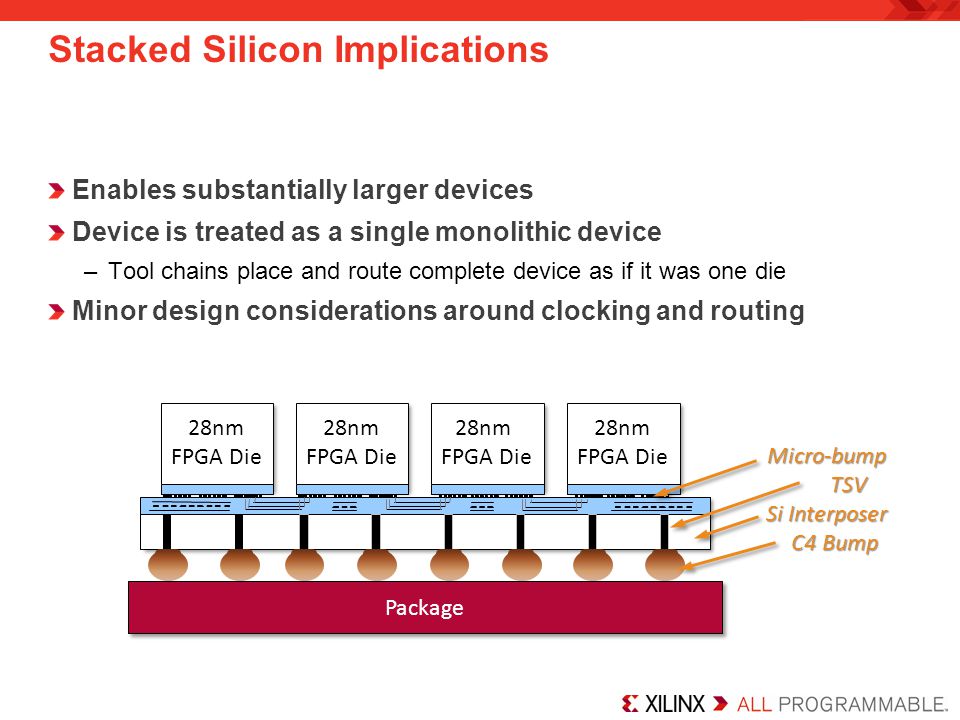
IO and CMT (Clock Management Tiles) Columns.

Serial Transceiver Columns.

PCI Express.

HSSIO

**Stacked** **Silicon** **Interconnect** **Technology** – Stacks multiple **FPGA**s onto a single chip

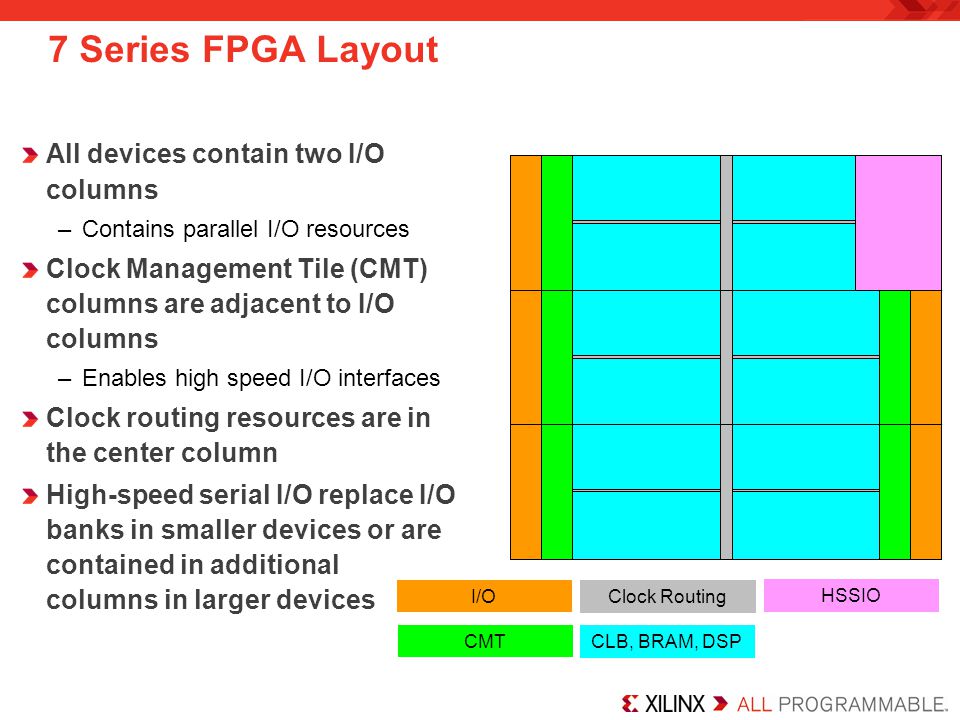


Each FPGA Die subunit is referred to as **Super Logic Region** (**SLR**)

The chip comprised of **SLRs** is referred to as **Silicon Interposer** (**Si Interposer**).

Adjacent **SRL**s are interconnected via **interposers** using Through-Silicn Vias (TSVs).

7-Series SLR layout:



IO columns.

Clock Management Tile (**CMT**) columns:

**MMCM** (clock manager).

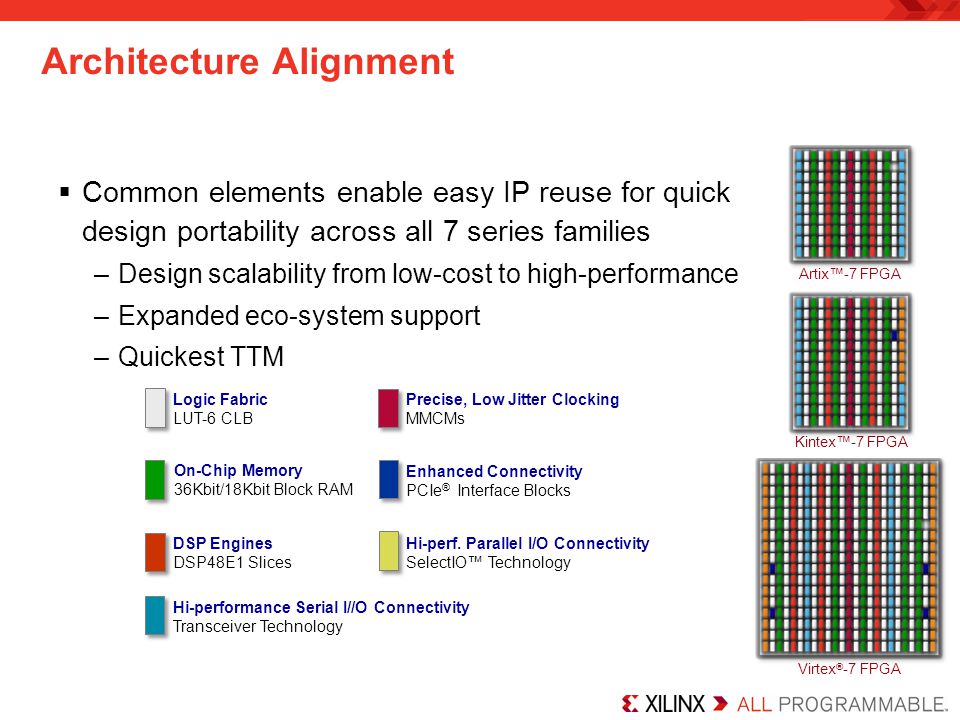
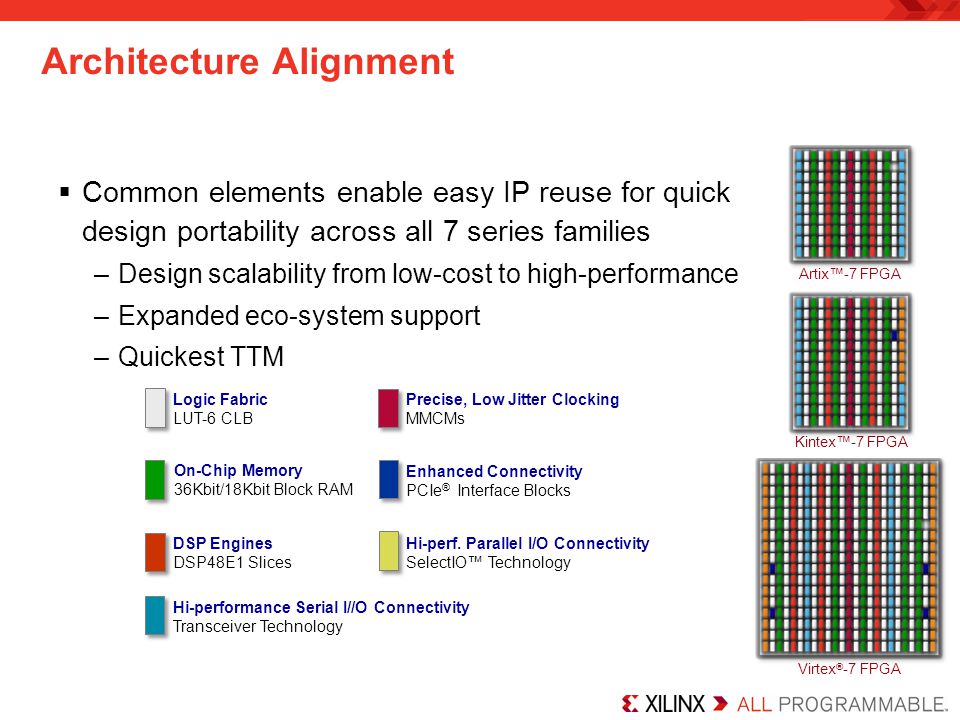
**PLL**.

Clock Routing resources.

**HSSIO** columns (High Speed Source Synchronous Interfaces).

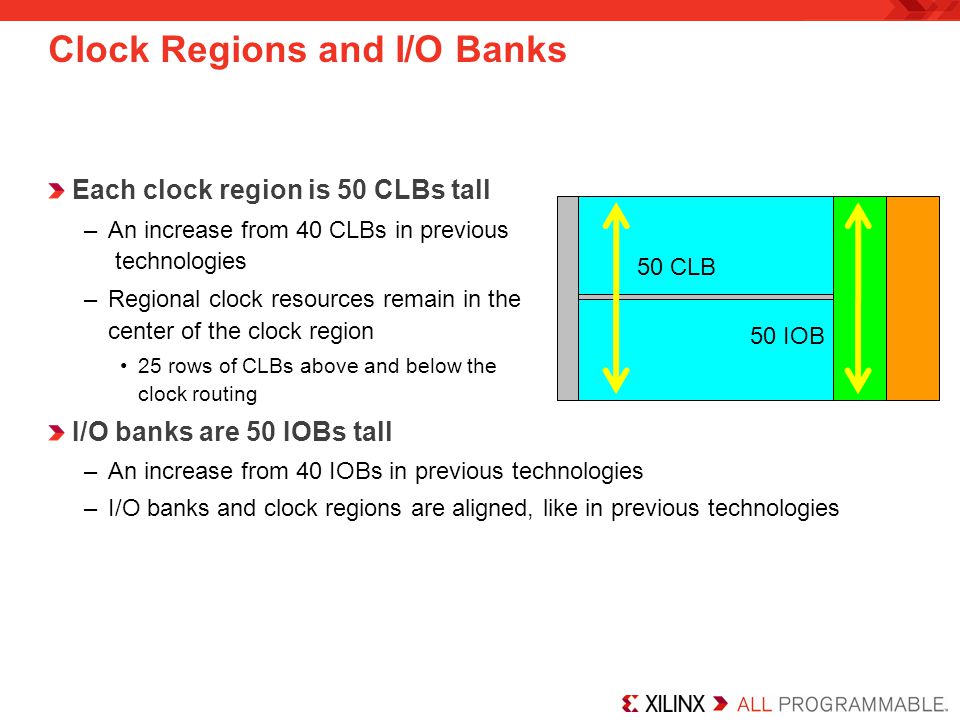
**CLB**, **BRAM**, **DSP** columns.

Architectural Alignment:



Enabled flexible device migration across all 7 series device families by reusing the same components among devices with different layouts.

Clock Regions and IO Banks:



Two types of clocking:

Regional clocking.

Global Clocking.

The boundaries between the Regional and Global clocking is grey area which often overlap.

Clock region aligns with an IO Bank

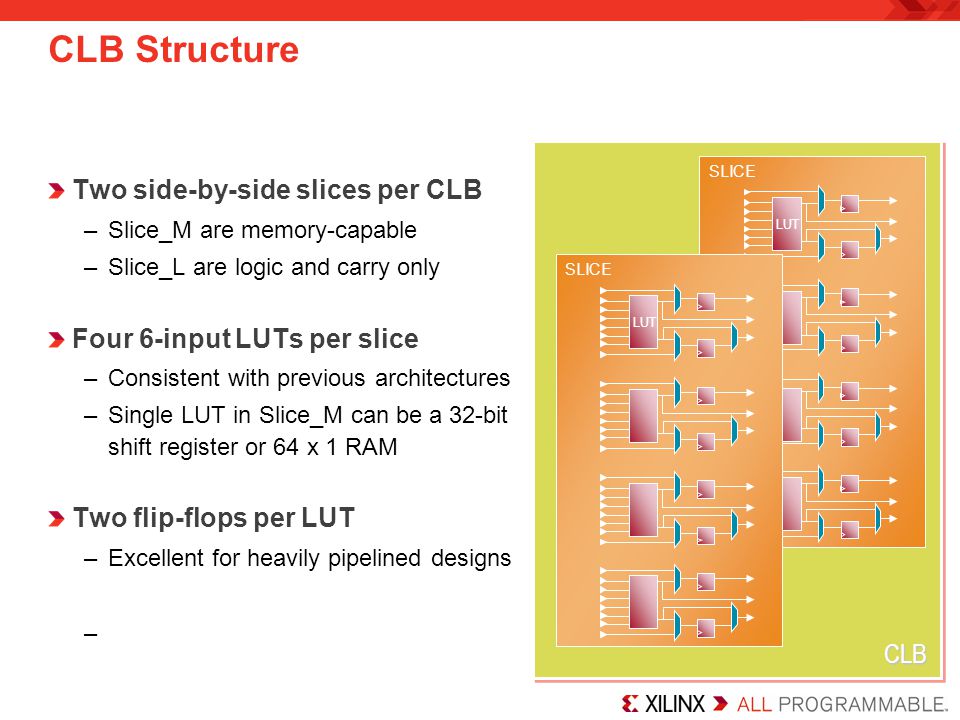
A clock region is about half the chip.

Within a given clock region, you have 50 CLBs and 50 IOBs.

Typical external clock sourcing involves:  
 **Synchronous**: oscillator -> **mmcm** -> multiple clocks with a common clock root.

**Asynchronous**: don’t share the same clock source (handled via fifo, or synchronization circuit).

CLB (Configurable Logic Block) Structure:



CLB contains:

Carry logic.

6-input LUTs.

Registers on the output.

Each CLB contains 2 side by side slices:

A slice contains 4 6-input LUTs.

A slice contains 2 flip-flops per each LUT (8 flip-flops per Slice).

**Slice\_M** (25% of Total Slices; every 4th Slice) – memory capable Slice.

LUTs are user definable as 64x1 RAM/ROM (**Distributed RAM**), or 32-bit shift register.

**Slice\_L** (75% of Total Slices) – Logic and Carry Slice.

Logic functionality only and not to be used as RAM/ROM.

Has carry logic built-in.

Clocking:

Utilizes

CMT (Clock Management Tile; upto 24 CMTs per device) which contains:

MMCM (1 per CMT)

PLL (1 per CMT)

Clock Buffers to support high clock fan out.

Set up for low-skew clock distribution.

Dedicated Hardware:

Transceivers – support various protocols.

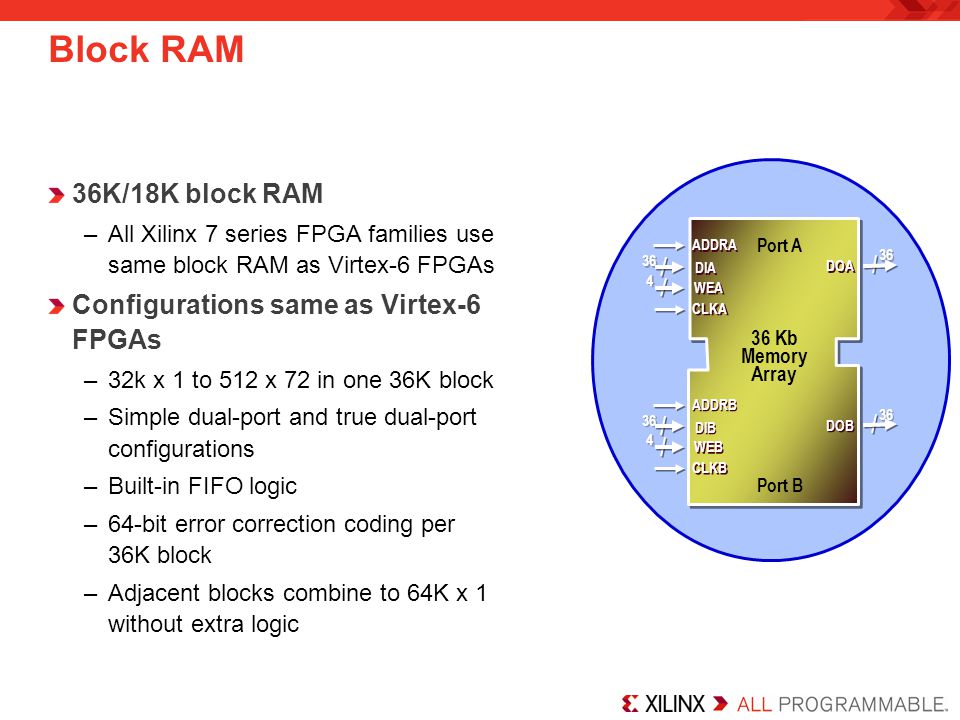
PCIe – various generations and lane widths depending on the FPGA family.

XADC - can be used for internal and external purposes.

**Memory**:

**Distributed RAM** - derived from LUTs of Slices.

**Block RAM:**

****

Large fully functional RAM Cells

Organized into Columns.

Can be size configured as **simple dual-port** RAM or **true** **dual-port** RAM.

Includes hardened built-in FIFO logic implementation.

Includes hardened Built-in **ECC** for 64-bit error correction coding per each 36Kb block.

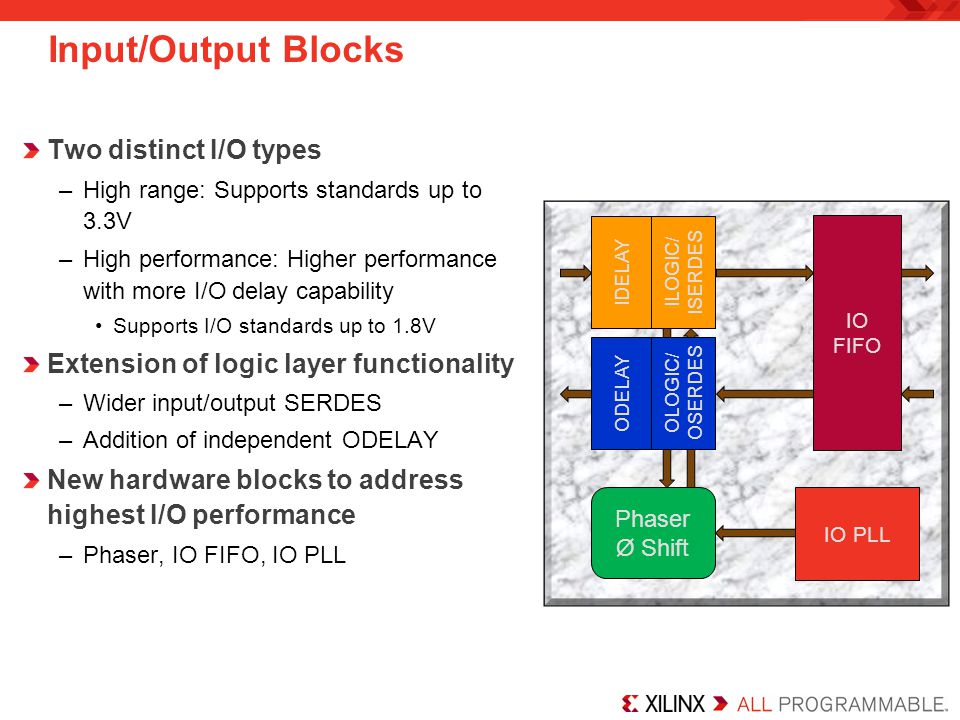
**Single** **bit** **detection + correction**

**Multi bit** **detection**.

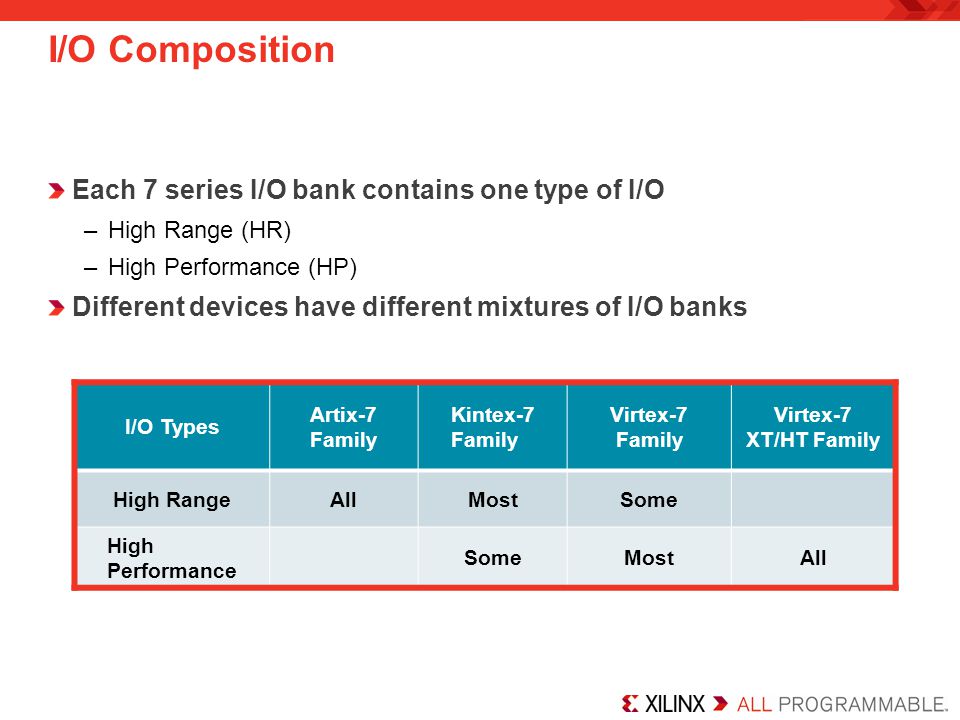
Can be size configured as a **Single 36Kb** **RAM,** or **Two 18Kb** where one is **RAM** and the other one is either **RAM** or **FIFO**.

Each adjacent 36Kb block contains a dedicated cascade logic to

**IO Blocks**:



Two types:



**HR (High** **Range)** **IO**: supports voltages up to **3.3V**

**HP (High** **Performance) IO**: higher performance with more IO delay capability; supports up to **1.8V**

Contain:

Simple Input/Output Buffers.

Registers.

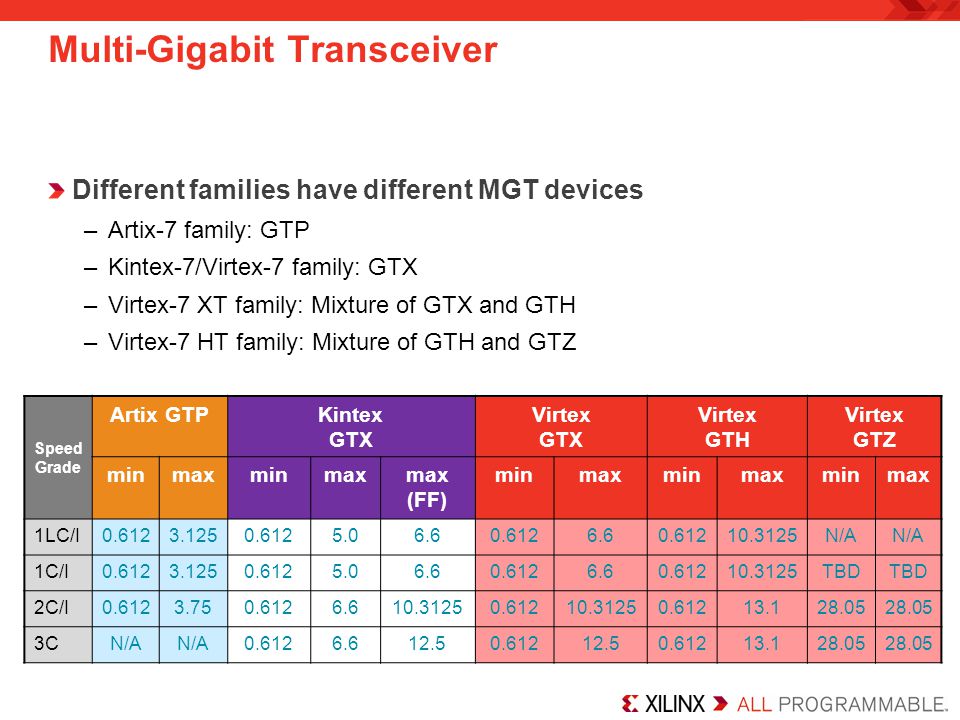
Delay Elements.

PLL.

Phase Shifter.

Variety of Voltage Standard support but with this limitations - bank dependent thus one **REF** and **VCCO** pin per a bank.

**Transceivers**:



**GTP**:

Up to **6.6 Gbps**

Ultra high volume transceivers.

Wire bond package capable.

**GTX**:

Up to **12.5 Gbps**

Support for most common **10 Gbps** Protocols

**GTH**:

Up to **13.1 Gbps**

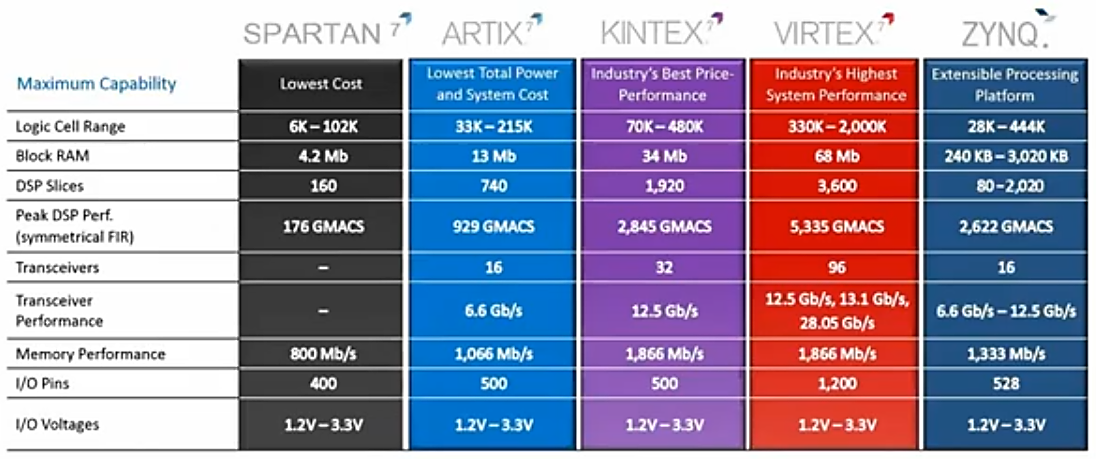
Support **10 Gbps** protocols with high FEC overhead.

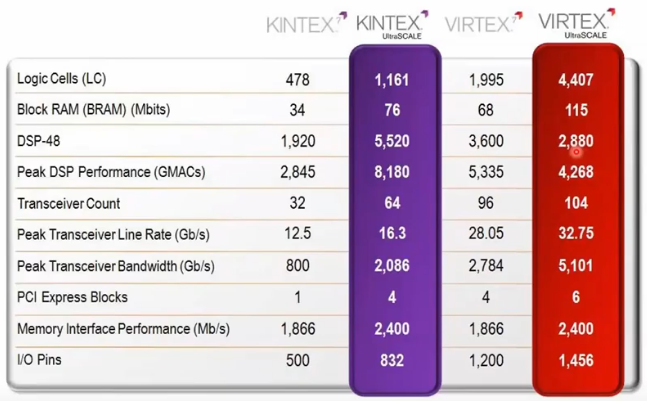
**GTZ**:

Up to **28.05 Gbps**

Enables **100-400 Gbps** communication.

**FPGA Family Comparison**:





**Spartan**:

Lowest price and highest performance-per-watt (power efficiency)

Industrial, automotive, infotainment, motor and motion control

**Artix**:

Lower prices and high performance

Battery powered devices, automotive, commercial digital cameras.

**Kintex**:

Best price/performance ratio.

Wireless and wired communications, medica, broadcast.

**Virtex**:

Highest performance and largest capacity.

High-end wired communication, Test and measurement, Advanced RADAR, High-performance computing.

UltraScale Architecture addresses Interconnect Bottleneck:

**Routing** **delay**: dominates overall delay.

**Clock** **Skew**: consumes more timing margin

**Sub**-**optimal** **CLB** **packing**: reduces performance and utilization.

UltraScale Clock Routing architecture: