Alex Baret
CS5780 Prelab6

1. What is hysteresis and how does it help prevent bad behavior on digital inputs?

    - Hysteresis changes the voltage threshold depending on the currently detected digital state. By changing the voltage threshold for transitions to digital low, unwanted transitions will be avoided.

2. What is quantization?

    - Quantization is the process of mapping a high-resolution signal to a manageable lower-resolution one.

3. What does Nyquist theory explain? What is the problem with sampling a signal too slowly?

    - Nyquist theory explains the relationship between how often you sample an input signal and whether or not you'll be able to tell what it is afterwards.

4. The maximum resolution of the ADC is 12-bits. How many quantization steps/values does this give us?

    - 2^12 = **4096** quantization steps/values

5. What are the steps to perform an ADC calibration?

    - From the Peripheral Manual, the steps to perform an ADC calibration are:

      Calibration software procedure

      1. Ensure that ADEN = 0 and DMAEN = 0.
      2. Set ADCAL = 1.
      3. Wait until ADCAL = 0.
      4. The calibration factor can be read from bits 6:0 of ADC_DR.

6. What's the difference between right and left-aligned data in the DAC registers?

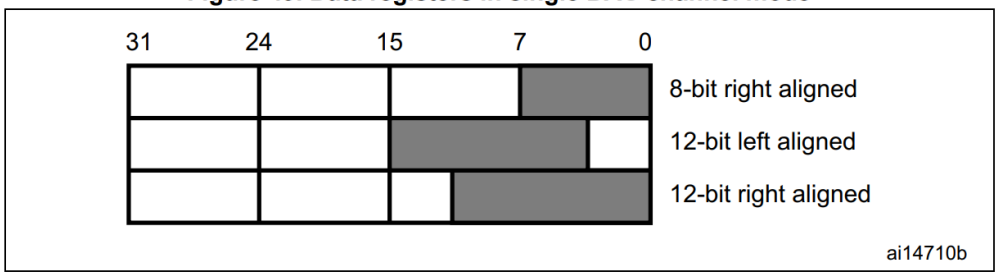
- The difference between right and left-aligned data is the bit positioning within the DAC registers.

  There are three possibilities:

  - 8-bit right alignment: the software has to load data into the DAC_DHR8Rx [7:0] bits (stored into the DHRx[11:4] bits)
  - 12-bit left alignment: the software has to load data into the DAC_DHR12Lx [15:4] bits (stored into the DHRx[11:0] bits)
  - 12-bit right alignment: the software has to load data into the DAC_DHR12Rx [11:0] bits (stored into the DHRx[11:0] bits)

  Depending on the loaded DAC_DHRyyyx register, the data written by the user is shifted and stored into the corresponding DHRx (data holding registerx, which are internal non-memory-mapped registers). The DHRx register is then loaded into the DORx register either automatically, by software trigger or by an external event trigger.

  Figure 49. Data registers in single DAC channel mode

- Depending on which mode (left/right) is selected, determines where the bits are in the registers. Left-aligned mode is typically used for selecting the upper bits of a 16-bit number, allowing the DAC to act on 16-bit data without any conversion or shifting (with some minor loss in precision provided by low-order bits).

7. What DAC register would you use to write 8-bit right-aligned data? (use the peripheral reference manual)

   - You would use the **DAC_DHR8Rx** register

8. Name something you found confusing or unclear in the lab manual. If everything was clear, simply answer that you didn't have any issues

   - The ADC calibration is in section 13.3.2 of the Peripheral Manual, not section 13.4.1