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Thread-Like CMOS Logic Circuits Enabled by Reel-Processed Single-Walled Carbon Nanotube Transistors via Selective Doping

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The realization of large-area electronics with full integration of 1D thread-like devices may open up a new era for ultraflexible and human adaptable electronic systems because of their potential advantages in demonstrating scalable complex circuitry by a simply integrated weaving technology. More importantly, the thread-like fiber electronic devices can be achieved using a simple reel-to-reel process, which is strongly required for low-cost and scalable manufacturing technology. Here, high-performance reel-processed complementary metal-oxide-semiconductor (CMOS) integrated circuits are reported on 1D fiber substrates by using selectively chemical-doped single-walled carbon nanotube (SWCNT) transistors. With the introduction of selective n-type doping and a nonrelief photochemical patterning process, p- and n-type SWCNT transistors are successfully implemented on cylindrical fiber substrates under air ambient, enabling high-performance and reliable thread-like CMOS inverter circuits. In addition, it is noteworthy that the optimized reel-coating process can facilitate improvement in the arrangement of SWCNTs, building uniformly well-aligned SWCNT channels, and enhancement of the electrical performance of the devices. The p- and n-type SWCNT transistors exhibit field-effect mobility of 4.03 and 2.15 $cm^2 V^{-1} s^{-1}$, respectively, with relatively narrow distribution. Moreover, the SWCNT CMOS inverter circuits demonstrate a gain of 6.76 and relatively good dynamic operation at a supply voltage of 5.0 V.

Recently, wearable electronics have gained a considerable interest in both textiles and electronics industry due to their wide application area. Among various wearable electronic devices, textile-based electronic systems or the electronic-textiles (e-textiles) have the advantages of light-weight, good adaptability to human motion, comfortability, etc.[1–6] In order to realize the textile-based electronic systems, various electronic devices such as transistors, capacitors, and resistors should be developed as well as their integration on/with textile substances. Up to now, mainly two different approaches have been demonstrated; (i) integration of current electronic devices on 2D fabric substrates[7,8] and (ii) integrated (weaved) e-textiles with 1D electronic functional fibers.[9–12] Although the integration of present electronic devices on 2D fabrics seems to be timely and easier to realize, the irritation caused by foreign matters, less conformability with the body, and the difficulty of integrating various electronic systems remain still problematic. For such reasons, realizing

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e-textiles with 1D electronic functional fibers is of importance based on the facts that the 1D structure can be more suitable for realizing complex and large-area e-textiles by a simple reel-to-reel process and weaving technology (integration) of functional fiber units into a 2D textile form.[13–16]

In previous studies, organic materials have been widely used as an active material for the 1D fiber transistors due to their great structural flexibility and low-temperature processability.[14,15] However, the low electrical performance and rather poor stability have been limiting their general utilization in various e-textile devices. Therefore, in 1D fiber devices, alternative active materials including high electrical performance, good stability, and ease of process are highly desired.[16] In these regards, single-walled carbon nanotubes (SWCNTs) can be considered as a good candidate for 1D fiber transistors owing to their high carrier mobility, good structural flexibility, and simple fabrication using a solution process.[17–19] Moreover, the semiconductor type of SWCNTs can be intentionally controlled from p-type to n-type by a simple doping process such as surface chemical doping, alkali metal doping, or metal contact engineering[20–23] and consequently, complementary metal-oxide-semiconductor (CMOS) integrated circuits can be realized solely by using the SWCNT transistors.

Herein, we demonstrate a CMOS integrated circuitry on a 1D fiber substrate based on reel-processed SWCNT active channels. Particularly, by using one-step dip coating method, well-aligned SWCNT films were successfully formed on fiber substrates exhibiting high carrier mobility. Also, by a selective doping using (4-(1,3-dimethyl-2,3-dihydro-1H-benzoimidazol-2-yl)phenyl)-dimethylamine (N-DMBI), n-type and p-type SWCNT transistors were realized on a single fiber substrate as well as their integrated circuits. As a result, a fully functional fiber-based CMOS inverter circuits were successfully demonstrated exhibiting high noise margin of 4.97 V and a gain of 6.76 at a supply voltage of 5.0 V.

Figure 1a demonstrates the fabrication process of a 1D fiber-type CMOS circuitry using reel-processed SWCNTs transistors. Also, the full fabrication steps were schematically depicted in Figure 1b. As a fiber substrate, an optical fiber having a diameter of 125 μm was used. The optical fiber has relatively smooth surface compared to metallic or polymer fibers, which is favorable for achieving uniform and defect-free films. On the fiber substrate, Cr gate electrode and Al_2O_3 gate dielectric layers were sequentially deposited by using sputtering and atomic layer deposition (ALD) process, respectively with unpatterned structures. Afterward, Au source/drain electrodes were formed on the gate dielectric layer. As a channel layer and a passivation layer, semiconducting SWCNTs wrapped with regioregular poly (3-dodecylthiophene) (rr-P3DDT)[24] and poly(4-vinlyphenol) (PVP) were coated by using a home-made reel-coating equipment, which is similar to the well-known dip coater. To achieve a full flexibility in the reel-process, precut fiber segments (around 3–5 cm in length) were loaded on a carrier fiber. While pulling-up the fibers with an optimized speed (SWCNT: 0.78 mm s^{-1}, PVP: 3.57 mm s^{-1}), the coated fibers could be prebaked by passing through a heating zone (SWCNT: no heating, PVP: 150 °C). During this process, the solvent molecules in the as-coated films are evaporated and the films become dense solid networks on the fiber substrates, maintaining the coating uniformity. After the SWCNT channel formation, a selective deep ultraviolet (DUV) exposure was followed to isolate the SWCNT channels using a low-pressure mercury lamp (LPML) [emitting photon energies of 4.88 eV ($\lambda \approx 254$ nm, 90%) and 6.70 eV ($\lambda \approx 185$ nm, 10%)]. The DUV irradiation was carried out in N_2-rich environment with a shadow mask where the exposed regions were electrically

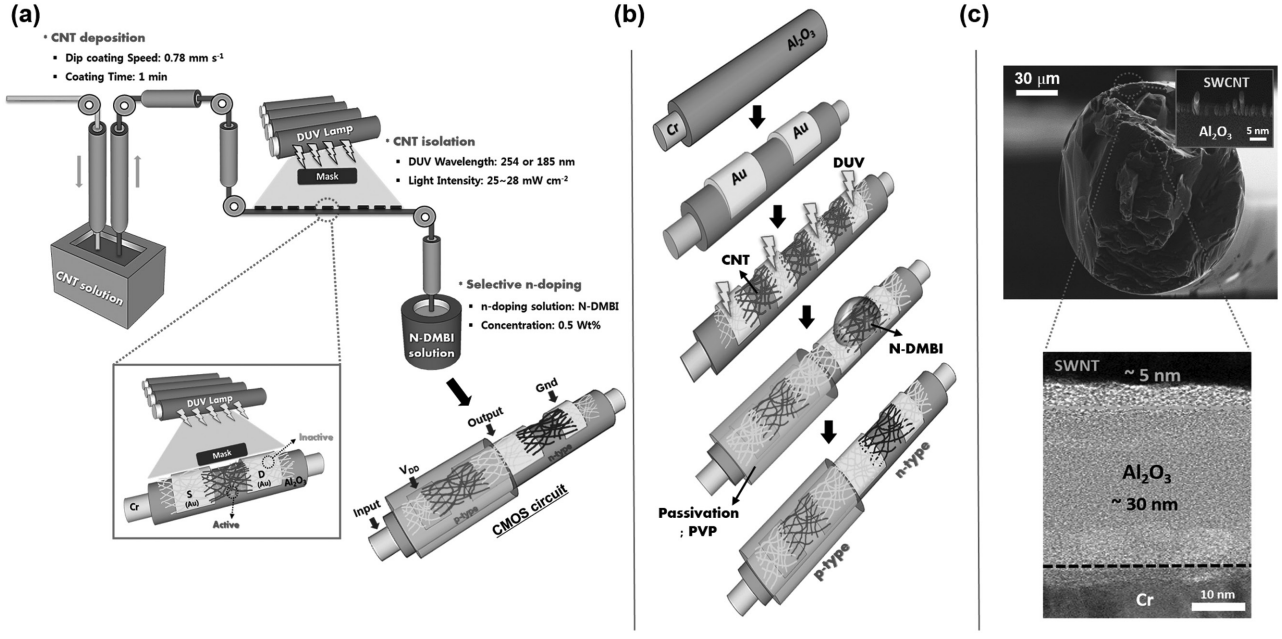

Figure 1. a) Schematic illustration for fabrication process of 1D fiber-type CMOS circuitry and b) the full fabrication steps. c) The cross-sectional field-emission scanning electron microscopy (FE-SEM) and transmission electron microscopy (TEM) images of an SWCNT transistor on the fiber substrate.

deactivated, isolating the unexposed channels. The isolation of SWCNT channels is particularly important as to effectively reduce the off-state and gate-leakage currents and consequently to minimize the static power consumption of the circuitry. Finally, after the channel isolation, a selective n-doping using N-DMBI was carried out for n-channel regions while passivating the p-type regions with a PVP layer.

Figure 1c shows the cross-sectional field-emission scanning electron microscopy (FE-SEM) and transmission electron microscopy (TEM) images of an SWCNT transistor at the channel region. As clearly observed, uniform films of Cr gate electrode, Al_2O_3 gate dielectric layer, and SWCNT channel were successfully formed on the fiber substrate. The thickness of the ALD-deposited Al_2O_3 gate dielectric layer was set as ≈30 nm to ensure the structural flexibility and reasonable insulating properties. To investigate the insulating properties of the Al_2O_3 gate dielectric, the current density versus electric field (*J*–*E*) and the areal capacitance versus frequency (*C*–*F*) characteristics were analyzed. As shown in Figure S1a and Sb (Supporting Information), the Al_2O_3 gate dielectric deposited on a fiber substrate exhibited low leakage current density of 4.17×10^{-8} A cm^{-2} at 2 MV cm^{-1} and a high breakdown field of 6.4 MV cm^{-1}. Also, the areal capacitance and the dielectric constant were measured to be 115 nF cm^{-2} at 1 kHz and 5.82, respectively. These results clearly demonstrate that the Al_2O_3 film deposited on fiber substrates exhibits excellent electrical properties which suffice for both a gate dielectric and insulating layer of transistors.

In SWCNT-based transistors, achieving a well-aligned SWCNT network is important since the randomly oriented SWCNT network typically exhibits low carrier mobility owing to low SWCNT density and highly resistive nanotube-to-nanotube junctions.[25,26] Previously, various coating methods for SWCNTs have been reported including chemical vapor deposition, spin-coating, dry filtration, slot-die coating, immersion coating, and dip-coating process.[27] In the case of fiber substrates, a simple reel-to-reel-based dip-coating method is very attractive since it is a continuous process and self-assembled and highly oriented SWCNTs can be achieved during the vertical withdrawing process. Also, in SWCNT-based transistors, aligning the SWCNTs parallel to the charge transport direction is beneficial in achieving high conductance,[28] similar to organic transistors with anisotropic charge transport characteristics.[29] Here, to investigate the influence of coating methods on self-alignment of SWCNTs, we compared dip-coating and immersion-coating methods as illustrated in **Figure 2**a. Figure 2c,d shows the FE-SEM images of SWCNT films coated by using immersion-coating and dip-coating method, respectively. It can be observed that the SWCNT films coated by dip-coating exhibited a well-aligned network oriented along with the drawing direction, while the SWCNT film coated by immersing method showed a randomly oriented network. In previous reports, the dip-coating method generally resulted in a random SWCNT network in planar substrates,[30–32] whereas in our case, the combination of reel-based coating and vertical withdrawing process with cylindrically shaped substrate are more likely to induce evaporative self-assembly of SWCNTs on the fiber surface resulting in a highly aligned network (Figure 2d). As reported, the solvent evaporation and fluid flow at the meniscus induced shearing force over anisotropic nanomaterials, such as metal nanowires and nanotubes.[33,34] Even further, the micrometer range cylindrical substrates (diameter of 125 mm) strengthen the capillary fluid effect which help the alignment of carbon nanotubes.[24,35]

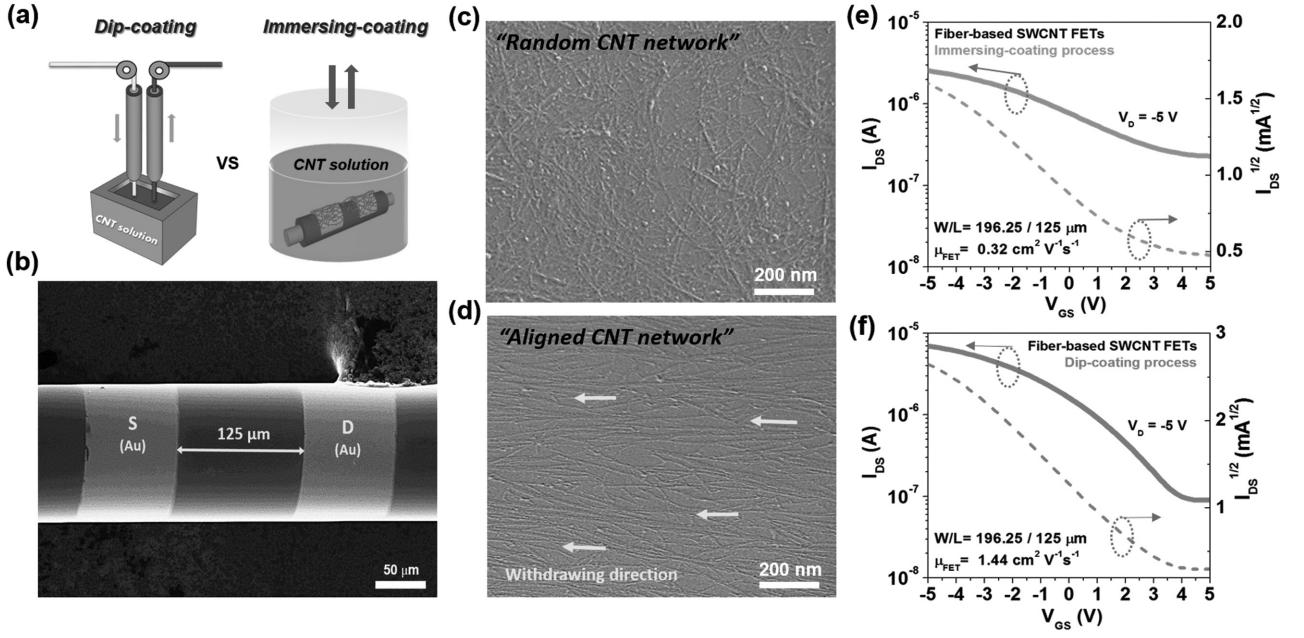

Figure 2. a) Schematic process of immersing coating and dip-coating methods for alignment of SWCNTs. b) Top-view FE-SEM image of an SWCNT transistor on a 1D fiber substrate (W/L = 196.25/125 μm). The FE-SEM images of SWCNT films coated by using c) immersion-coating and d) dip-coating method. The transfer characteristics of SWCNT transistors on a fiber substrate with e) an immersion-coated and f) a dip-coated SWCNT channel layers.

Figure 2e,f shows the transfer characteristics of SWCNT transistors using an immersion-coated SWCNT channel and a reel-coated (dip-coated) SWCNT channel, respectively. As expected, the dip-coated SWCNT transistors exhibited enhanced field-effect mobility, $I_{on/off}$ ratio, and subthreshold slope characteristics. Particularly, the dip-coated SWCNT transistors had an average field-effect mobility of 1.45 $cm^2\ V^{-1}\ s^{-1}$ (standard deviation of 0.14 $cm^2\ V^{-1}\ s^{-1}$) while that of immersion-coated SWCNT transistors was 0.13 $cm^2\ V^{-1}\ s^{-1}$ (standard deviation of 0.1 $cm^2\ V^{-1}\ s^{-1}$) as noted in Figure S2 (Supporting Information). The dip-coated SWCNT transistors, however, still have relatively low $I_{on/off}$ ratio of $\approx 10^2$ which may hinder their utilization in digital logic circuits due to high static current and corresponding large power consumption in system level. Therefore, it is essential to electrically isolate the SWCNT channels to achieve the high $I_{on/off}$ ratio. In order to isolate the SWCNT channels, we employed a nonrelief photochemical patterning process to prevent any chemical or plasma damages of SWCNTs during the etching process. Aforementioned, the low-temperature photochemical routes via DUV irradiation have been known to be effective in cleaving specific chemical bonds,[36] which inspired us to utilize the release of highly energetic photon on SWCNT area to obtain spacially isolated functional regions. Therefore, upon the DUV irradiation, chemical bond dissociation and a subsequent loss of carrier transport properties are expected, enabling electron delocalization within the extended SWCNT network.[37] In fact, the development of photonic-based nonrelief etching process in reel-processed soft matter electronics would greatly facilitate the full development of a scalable fabrication, overcoming process discontinuity while providing uniformly isolated structures.

Figure 3a,b shows the transfer and output characteristics of SWCNT transistors fabricated with nonisolated and isolated SWCNT channels, respectively. As can be seen, the off-state current is significantly reduced after the channel isolation resulting in high $I_{on/off}$ ratio of 10^4–10^5. The significant reduction in off-state current is attributed to the isolation of SWCNTs which effectively limits the percolate charge transport or bridging pathway between the unpatterned SWCNTs. Figure 3c shows the saturation mobilities acquired at different positions in a single fiber. An average field-effect mobility of 3.61 $cm^2\ V^{-1}\ s^{-1}$ with standard deviation of 0.3 $cm^2\ V^{-1}\ s^{-1}$ was obtained, indicating highly uniform SWCNT channel layer formation by a simple reel-processed dip-coating method. Interestingly, as shown in Figure 3, the photochemically isolated SWCNT transistors exhibited higher mobility (3.61 $cm^2\ V^{-1}\ s^{-1}$) than that of pristine devices (average of 1.45 $cm^2\ V^{-1}\ s^{-1}$ with standard deviation of 0.14 $cm^2\ V^{-1}\ s^{-1}$). It has been reported that the polymer molecules wrapping around the SWCNTs may work as a potential barrier for charge transfer between SWCNTs, deteriorating the carrier mobility.[38] Although the active channel region is protected by a shadow mask during the channel isolation process, some of the DUV light may penetrate into the air gap between the fiber and the shadow mask by scattering, and partly dissociate the rr-P3DDT molecules.

To gain a more insight into the molecular structure change of SWCNTs by the DUV exposure, a series of Raman spectroscopy analyses were performed for SWCNT films with different degrees of DUV irradiation: (i) no DUV irradiation (pristine), (ii) DUV irradiation with a shadow mask (partially DUV-exposed), and (iii) DUV irradiation without using a shadow mask (fully DUV-exposed). Figure S3 (Supporting Information)

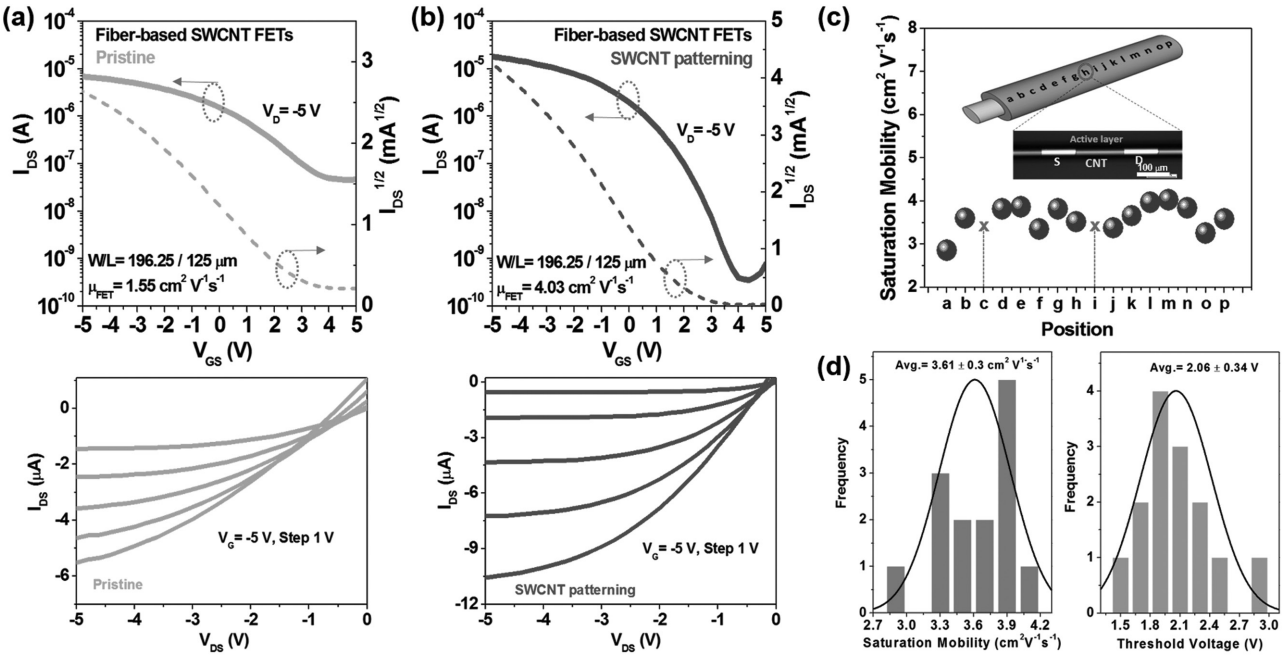

Figure 3. Comparison of the electrical characteristics of SWCNT transistors using a) nonisolated and b) isolated SWCNT channel layer. c) The saturation mobility of device using isolated SWCNT channel layer as a function of different positions. d) Statistical distribution of saturation mobility and threshold voltage of isolated SWCNT transistor on a fiber substrate. The inset of (d) illustrates a schematic representation of measurement positions of 16 devices fabricated on a single fiber substrate.

shows the Raman spectra of SWCNT films with the different post-treatments; pristine, partially DUV-exposed, and fully DUV-exposed SWCNT films. The G- and 2D-peaks of rr-P3DDT-wrapped SWCNTs are located at wavenumbers of 1590 and 2614 cm^{-1}, respectively. Also, the peaks at 1381 and 1445 cm^{-1} correspond to rr-P3DDT. From the Raman spectra, it can be seen that the characteristic peaks related to SWCNT and rr-P3DDT were largely modulated by the DUV exposure. In partially DUV-exposed SWCNT films, a noticeable decrease of peaks at 1381 and 1445 cm^{-1} were observed, corresponding to rr-P3DDT, while the peaks for SWCNTs remain relatively unchanged (1590 and 2614 cm^{-1}). In a fully DUV-exposed sample, the characteristic peaks related to SWCNT and rr-P3DDT were nearly disappeared supporting that the controlled DUV irradiation can effectively manipulate the molecular structures of SWCNT and rr-P3DDT, enabling both chemical patterning of SWCNT and enhancement of π–π transition of charged carriers in the SWCNT networks, respectively. Similar results can be also observed in graphene wrapped with poly(methyl methacrylate) (PMMA) as shown in Figure S4 (Supporting Information). In the experiments, by adjusting the dose of DUV light, the peaks at G and 2D for graphene could be manipulated, indicating different electrical functionality of each irradiated region. Consequently, it is believed that the inherent electrical properties of SWCNT films could be recovered by lowering the potential barrier created by the rr-P3DDT, resulting in improved carrier transport in the SWCNT channel region. In fact, it was found that the contact resistance between the SWCNT channel and source/drain electrodes was decreased from 1–1.25 MΩ to 300–400 kΩ after the DUV irradiation (partially DUV-exposed SWCNT transistors) (Figure S5, Supporting Information). Although it is still a topic of debate for the underlying mechanism, we believe that the above mentioned parameters can be some of the reasons for enhancing the electrical characteristics of the partially DUV-exposed SWCNT transistors. However, a more systematic study is still needed to identify the detailed mechanism and optimized processes about the molecular structure manipulation of SWCNT and rr-P3DDT molecules by the DUV irradiation. Additionally, to examine the bending stability of our thread-like SWCNT transistors, we intentionally bent the fiber transistors and analyzed the variation in the electrical properties. The bending radius (R) was varied from 14 to 7.5 mm as shown in the inset of Figure S6 (Supporting Information). As shown in the figure, a slight positive shift of transfer curve was observed by bending the device with R = 14 mm. However, as the bending radius was decreased further, the transfer curve began to return to its original position. Although it shows a slight variation of on-current and field-effect mobility as a function of bending radius, it can be seen the fiber-type SWCNT transistors exhibited relatively stable operation under bent condition.

In order to realize a complementary circuitry using SWCNT transistors, specific channel regions need to be converted into n-type channels. Here, we used N-DMBI for n-type doping of SWCNTs. The N-DMBI has been frequently utilized as a highly efficient class of molecular dopants for various organic semiconductors, graphene, and SWCNTs.[39–41] Furthermore, since the N-DMBI can be deposited as a solution form, it can be easily translated into our reel-processed dip coating. As shown in **Figure 4**a, the prepatterned SWCNTs were converted into

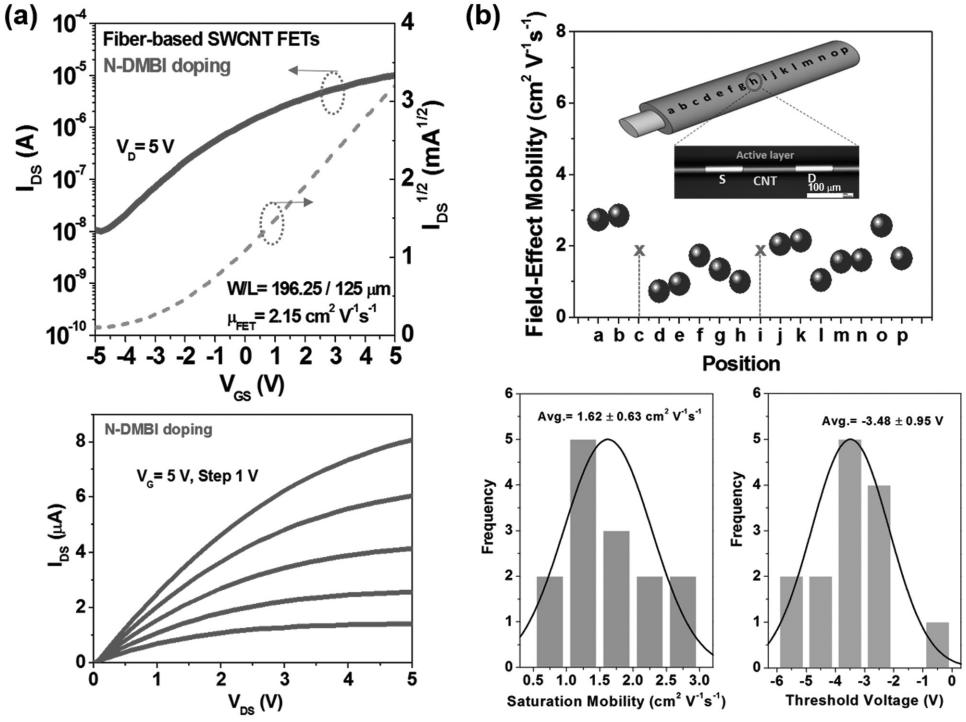

Figure 4. a) The electrical characteristics of n-type SWCNT transistors using N-DMBI doping on a fiber substrate. b) The saturation mobility of device using isolated SWCNT channel layer as a function of different positions and statistical distribution of saturation mobility and threshold voltage of N-DMBI-doped SWCNT transistor on a fiber substrate.

an n-type semiconductor by a simple soaking or dropping of N-DMBI solution. A slight upshift of G-peak in N-DMBI-doped SWCNTs indicates the successful conversion from p-type to n-type.[41] To further investigate the n-type doping characteristics, X-ray photoelectron spectroscopy (XPS) analysis was also performed. Figure S3b,c (Supporting Information) shows the N 1s and C 1s XPS spectra of pristine and N-DMBI-doped SWCNT films, respectively. The results show that the intensity of the N 1s peak was substantially increased after the N-DMBI doping and also the C 1s peak was shifted to higher binding energy from 284.64 to 284.99 cm^{-1}. These results of Raman spectroscopy and XPS analyses clearly indicate the successful electron transfer from N-DMBI dopant to SWCNTs and corresponding n-type doping.

Figure 4a,b shows the electrical characteristics of n-type SWCNT transistors and statistical distribution of 16 devices fabricated on a single fiber substrate, respectively. The devices clearly show n-type behaviors with an average field-effect mobility and threshold voltage (V_{TH}), of 2.15 cm^2 V^{-1} s^{-1} (standard deviation of 0.63 cm^2 V^{-1} s^{-1}) and −3.2 V (standard deviation of 0.95 V), respectively. In the case of n-type SWCNT transistors, the environmental stability in air is particularly important since the SWCNTs can be readily converted back to p-type by the adsorbates such as oxygen and water molecules present in the ambient air. Figure S7 (Supporting Information) shows the time-dependent electrical variation of n-type SWCNT transistors. As shown, the n-type SWCNT transistors exhibited relatively good environmental stability up to 240 h with a minimal degradation. Only a slight decrease of mobility around 10–20% was observed after a 10 d storage in ambient air without any passivation layer over the sample. Using the n-doped SWCNT transistors and pristine p-type SWCNT transistors, a complementary SWCNT inverter was fabricated on a single fiber substrate as shown in Figure S8 (Supporting Information). For the efficient measurement of the electrical characteristics of the devices, unpatterned gate electrode structure is utilized since gate contact pads for the measurement are not available for this fiber-type structure (therefore, a large overlap capacitance between gate and source/drain electrodes is formed). To prevent the perturbation of p-type semiconducting properties during the n-doping process, a PVP passivation layer was coated over the selective p-type region, preventing the penetration of N-DMBI solution while retaining the original SWCNT semiconducting properties (Figure S9, Supporting Information). The thread-like 1D complementary inverters exhibited a maximum voltage gain of ≈6.76 at a supply voltage (V_{DD}) of 5.0 V and a noise margin of 4.97 V, as shown in **Figure 5**b,c. Although we demonstrated relatively good operation of the thread-like CMOS logic circuits with high voltage gain and large noise margin, the circuits were frequently suffered from incomplete rail-to-rail operation. Relatively high off-current possibly due to large overlap between gate and source/drain electrodes, less optimized n-doping process, and high source/drain contact resistance from the bottom contact device configuration can be mainly attributed to the unconventional operation. From our simulation results in Figure S10 (Supporting Information), it is believed that suppression of off-current, contact resistance, and careful tuning of threshold voltage are more favorable option to achieve full operation of the CMOS logic circuits. Additionally, to ensure the dynamic operation of the CMOS circuits, we also investigated the frequency response of the inverter. Figure S11 (Supporting Information) indicates that the inverter was indeed able to follow the 50 Hz input signal, although the output signal was notably distorted and lost the logic properties at higher input frequency (2 kHz) possibly due to the large RC-induced propagation delay as a result of the extremely high output capacitance. From this result, it can be seen that small gate-to-source/drain overlap capacitance (output capacitance) and minimal contact resistance will be of great importance for future high performance logic and analog fiber-based circuits. Nevertheless, we believe that this is the first demonstration of a fiber-based complementary SWCNT circuit, and from these results, we envision that the strategy presented in current study to efficiently control the electrical characteristics of SWCNT transistors and to form these devices with a reel-process may enable the realization of a complementary e-textile circuitry for the next generation wearable systems.

In conclusion, we successfully demonstrated high-performance thread-like CMOS logic circuits using reel-processed SWCNT transistors. Through selective chemical doping, reliable n- and p-type SWCNT transistors were achieved, enabling successful CMOS inverters fabrication on a cylindrical shaped fiber substrate. Additionally, we also demonstrated a simple

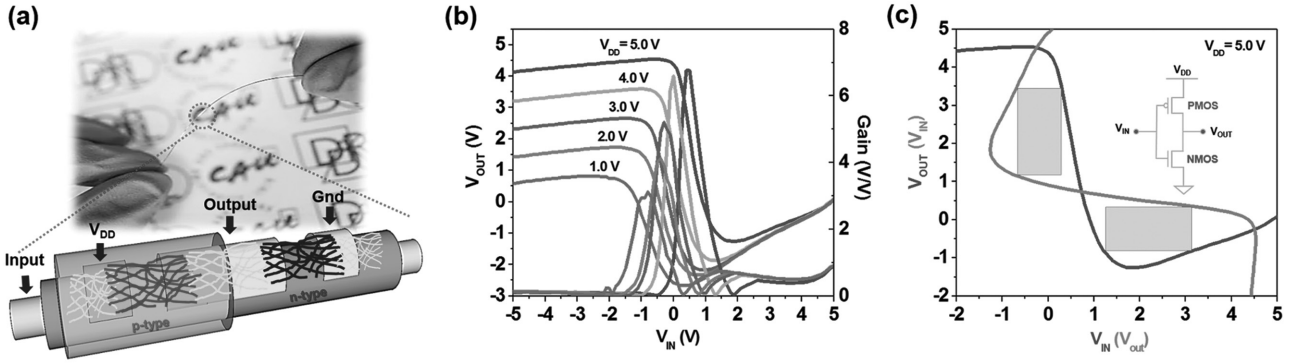

Figure 5. a) Schematic illustration of a complementary SWCNT inverter with selectively N-DMBI doping and PVP passivation layer by reel-processed dip-coating. b) Voltage transfer and gain characteristics of the thread-like 1D complementary inverters at various supplied voltages (V_{DD}), ranging from 1.0 to 5.0 V. c) A noise margin characteristic (at V_{DD} = 5.0 V) and (inset) circuit configuration of the complementary SWCNT inverter.

reel process to form well-aligned SWCNT channels and their nonrelief patterning for electrical isolation using DUV-induced photochemical reactions. The fabricated SWCNT CMOS transistors and circuits exhibited high electrical performance with ease process, which could be translated into a variety of implementations for e-textile applications. These results indicate that the thread-like SWCNT CMOS circuitry can be a promising candidate for a building block of next generation e-textile systems.

Experimental Section

Solution Preparation (SWCNT, PVP, and N-DMBI): The SWCNTs solution was prepared by suspending high-pressure CO (HiPCO) SWCNTs (5 mg) and P3DDT (6.25 mg) in toluene (25 mL). This suspended solution was sonicated (Ultrasonic processors, 400 W, BRANSON SONIFIER 450) for 30 min in a temperature-controlled cooling bath. Sequentially, the SWCNTs solution was centrifuged for 1 h at 10 000 rpm to remove SWCNT bundles and insoluble metallic SWCNT. Then, the supernatant in the centrifuge tube was placed into a glass vial to obtain a sorted semiconducting SWCNT solution. For a passivation layer, a polymer solution was prepared by dissolving PVP and poly(melamine-coformaldehyde) methylated (crosslinking agent), in propylene glycol monomethyl ether acetate with a weight ratio of 2:1. The dissolved solution was stirred for 1 h at 75 °C. In addition, for n-type doping of SWCNTs, N-DMBI (0.5 wt%) was dissolved in methanol and stirred at room temperature for 30 min.

Film Deposition and Device Fabrication: For the bottom gate electrode, Cr (88 nm) was deposited on an optical fiber substrate by using a radio frequency (RF)-magnetron sputtering system. Then, Al_2O_3 gate dielectric layer was deposited by using an atomic-layer-deposition (ALD) system at 150 °C. The thickness of the Al_2O_3 gate dielectric layer was ≈30 nm. The top-contact electrode (Au) was deposited on the Al_2O_3 gate dielectric layer through by thermal evaporation and patterned by using a shadow mask. Next, the SWCNTs solution was dip coated by using reel process with a withdrawal velocity of 0.78 mm s^{-1} for aligned SWCNT formation. For the isolation/patterning of SWCNT channels, a selective DUV exposure was carried using an LPML (wavelengths of 254 and 185 nm) for 1 h in N_2-rich environment. For selective n-type doping of SWCNTs, the half part of a single fiber substrate was immersed in a PVP solution for 1 min and subsequently pulled out by using a reel-processed dip coater with a withdrawal speed of 3.57 mm s^{-1}. Then, the fiber substrate was thermally annealed at 150 °C for 30 min by passing through a heating zone. The PVP coating process was repeated for several times to achieve a uniform and dense film. Afterward, n-type doping was carried out by drop casting (or dipping) an N-DMBI solution on the unpassivated channel region followed by a thermal annealing at 80 °C for 1 h in N_2 ambient.

Device and Film Characterizations: The dielectric properties of ALD-deposited Al_2O_3 films were analyzed using an LCR meter (inductance (*I*), capacitance (*C*), and resistance (*R*); Agilent 4284A, Agilent Technologies) and a semiconductor parameter analyzer (Agilent 4156C, Agilent Technologies). The capacitance and leakage current characteristics were obtained from a metal/insulator/metal structures (Cr-fiber/Al_2O_3/Au) on the fiber substrates. The electrical characterizations of the fiber-type SWCNT TFTs were carried out by using a semiconductor parameter analyzer (Agilent 4156C, Agilent Technologies) with standard field-effect geometry under ambient condition. The atomic bonding states and structural properties of SWCNTs and n-doped SWCNTs were analyzed by X-ray photoelectron spectroscopy (XPS; K-Alpha$^+$, ThermoFisher Scientific). Raman spectra were measured using a WiTech confocal Raman microscope which is equipped with a piezo-scanner and an intensity-tunable 532 nm Nd:YAG laser (neodymium-doped yttrium aluminium garnet). Also, the structures of fiber-based SWCNT TFTs were characterized by field-emission SEM and high-resolution transmission electron microscopy (JEM-3010 microscope, JEOL).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

complelentary metal-oxide-semiconductor (CMOS) integrated circuits, deep UV irradiation, single-walled carbon nanotubes (SWCNTs), thread-like fiber electronic devices, transistors

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[1] N. Matsuhisa, M. Kaltenbrunner, T. Yokota, H. Jinno, K. Kuribara, T. Sekitani, T. Someya, *Nat. Commun.* **2015**, *6*, 7461.
[2] W. Zeng, L. Shu, Q. Li, S. Chen, F. Wang, X.-M. Tao, *Adv. Mater.* **2014**, *26*, 5310.
[3] K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, G. Tröster, *Adv. Mater.* **2010**, *22*, 5178.
[4] T.-K. Kang, *Sci. Rep.* **2016**, *6*, 24406.
[5] W. Seung, M. K. Gupta, K. Y. Lee, K. Shin, J. Lee, T. Y. Kim, S. Kim, J. Lin, J. H. Kim, S. Kim, *ACS Nano* **2015**, *9*, 3501.
[6] S. Takamatsu, T. Lonjaret, E. Ismailova, A. Masuda, T. Itoh, G. G. Malliaras, *Adv. Mater.* **2016**, *28*, 4485.
[7] I. Locher, M. Klemm, T. Kirstein, G. Tröster, *IEEE Trans. Adv. Packag.* **2006**, *29*, 777.
[8] D. H. Kim, Y. S. Kim, J. Wu, Z. Liu, J. Song, H. S. Kim, Y. Y. Huang, K. C. Hwang, J. A. Rogers, *Adv. Mater.* **2009**, *21*, 3703.
[9] J. Yoon, Y. Jeong, H. Kim, S. Yoo, H. S. Jung, Y. Kim, Y. Hwang, Y. Hyun, W. K. Hong, B. H. Lee, S. H. Choa, H. C. Ko, *Nat. Commun.* **2016**, *7*, 11477.
[10] M. Hamedi, R. Forchheimer, O. Inganäs, *Nat. Mater.* **2007**, *6*, 357.
[11] X. Tao, V. Koncar, C. Dufour, *J. Electrochem. Soc.* **2011**, *158*, H572.
[12] C. Muller, M. Hamedi, R. Karlsson, R. Jansson, R. Marcilla, M. Hedhammar, O. Inganas, *Adv. Mater.* **2011**, *23*, 898.
[13] T.-H. Yoo, B.-I. Sang, D. K. Hwang, *J. Korean Phys. Soc.* **2016**, *68*, 599.
[14] J. Jang, S. Nam, J. Hwang, J.-J. Park, J. Im, C. E. Park, J. M. Kim, *J. Mater. Chem.* **2012**, *22*, 1054.
[15] H. M. Kim, H. W. Kang, D. K. Hwang, H. S. Lim, B. Ju, J. A. Lim, *Adv. Funct. Mater.* **2016**, *26*, 2706.
[16] C. J. Park, J. S. Heo, K.-T. Kim, G. Yi, J. Kang, J. S. Park, Y.-H. Kim, S. K. Park, *RSC Adv.* **2016**, *6*, 18596.

[17] D. Sun, M. Y. Timmermans, Y. Tian, A. G. Nasibulin, E. I. Kauppinen, S. Kishimoto, T. Mizutani, Y. Ohno, *Nat. Nanotechnol.* **2011**, *6*, 156.
[18] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, J. A. Rogers, *Nat. Nanotechnol.* **2007**, *2*, 230.
[19] A. Chortos, G. I. Koleilat, R. Pfattner, D. Kong, P. Lin, R. Nur, T. Lei, H. Wang, N. Liu, Y. C. Lai, M. G. Kim, J. W. Chung, S. Lee, Z. Bao, *Adv. Mater.* **2016**, *28*, 4441.
[20] V. Derycke, R. Martel, J. Appenzeller, P. Avouris, *Nano Lett.* **2001**, *1*, 453.
[21] G. Li, Q. Li, Y. Jin, Y. Zhao, X. Xiao, K. Jiang, J. Wang, S. Fan, *Nanoscale* **2015**, *7*, 17693.
[22] V. Derycke, R. Martel, J. Appenzeller, P. Avouris, *Appl. Phys. Lett.* **2002**, *80*, 2773.
[23] H. Wang, P. Wei, Y. Li, J. Han, H. R. Lee, B. D. Naab, N. Liu, C. Wang, E. Adijanto, B. C.-K. Tee, S. Morishita, Q. Li, Y. Gao, Y. Cui, Z. Bao, *Proc. Natl. Acad. Sci. USA* **2014**, *111*, 4776.
[24] H. W. Lee, Y. Yoon, S. Park, J. H. Oh, S. Hong, L. S. Liyanage, H. Wang, S. Morishita, N. Patil, Y. J. Park, J. J. Park, A. Spakowitz, G. Galli, F. Gygi, P. H.-S. Wong, J. B.-H. Tok, J. M. Kim, Z. Bao, *Nat. Commun.* **2011**, *2*, 541.
[25] S. Park, G. Pitner, G. Giri, J. H. Koo, J. Park, K. Kim, H. Wang, R. Sinclair, H. S. P. Wong, Z. Bao, *Adv. Mater.* **2015**, *27*, 2656.
[26] T. A. Shastry, J. W. T. Seo, J. J. Lopez, H. N. Arnold, J. Z. Kelter, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, *Small* **2013**, *9*, 45.
[27] C. Wang, K. Takei, T. Takahashi, A. Javey, *Chem. Soc. Rev.* **2013**, *42*, 2592.
[28] C. Kocabas, S. H. Hur, A. Gaur, M. A. Meitl, M. Shim, J. A. Rogers, *Small* **2005**, *1*, 1110.
[29] Y. Diao, B. C.-K. Tee, G. Giri, J. Xu, D. H. Kim, H. A. Becerril, R. M. Stoltenberg, T. H. Lee, G. Xue, S. C. B. Mannsfeld, Z. Bao, *Nat. Mater.* **2013**, *12*, 665.
[30] M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, P. Avouris, *ACS Nano* **2008**, *2*, 2445.
[31] L. Huang, X. Cui, G. Dukovic, S. P. O Brien, *Nanotechnology* **2004**, *15*, 1450.
[32] K. Iakoubovskii, N. Minami, A. Karthigeyan, *J. Mater. Chem.* **2012**, *22*, 4716.
[33] B. Park, I.-G. Bae, Y. H. Huh, *Sci. Rep.* **2016**, *6*, 19485.
[34] J. Huang, R. Fan, S. Connor, P. Yang, *Angew. Chem., Int. Ed.* **2007**, *46*, 2414.
[35] S. Kang, T. Kim, S. Cho, Y. Lee, A. Choe, B. Walker, S. J. Ko, J. Y. Kim, H. Ko, *Nano Lett.* **2015**, *15*, 7933.
[36] Y.-H. Kim, J.-S. Heo, T.-H. Kim, S. Park, M.-H. Yoon, J. Kim, M. S. Oh, G.-R. Yi, Y.-Y. Noh, S. K. Park, *Nature* **2012**, *489*, 128.
[37] J. Kim, M.-G. Kim, J. Kim, S. Jo, J. Kang, J.-W. Jo, W. Lee, C. Hwang, J. Moon, L. Yang, Y.-H. Kim, Y.-Y. Noh, J. Yun Jaung, Y.-H. Kim, S. Kyu Park, *Sci. Rep.* **2015**, *5*, 14520.
[38] A. Nish, J.-Y. Hwang, J. Doig, R. J. Nicholas, *Nat. Nanotechnol.* **2007**, *2*, 640.
[39] P. Wei, J. H. Oh, G. Dong, Z. Bao, *J. Am. Chem. Soc.* **2010**, *132*, 8852.
[40] B. D. Naab, S. Guo, S. Olthof, E. G. B. Evans, P. Wei, G. L. Millhauser, A. Kahn, S. Barlow, S. R. Marder, Z. Bao, *J. Am. Chem. Soc.* **2013**, *135*, 15018.
[41] P. Wei, N. Liu, H. R. Lee, E. Adijanto, L. Ci, B. D. Naab, J. Q. Zhong, J. Park, W. Chen, Y. Cui, Z. Bao, *Nano Lett.* **2013**, *13*, 1890.

