18

Vernier caliper

18.1 6 in CALIPER

A typical linear plate-counting system is illustrated by L.S. Starrett's model 723 vernier caliper (Figure 18.1).

This device uses sine-cosine pickup, coarse plate counting logic, and analog interpolation between plates to provide a resolution of 0.0001". The 723 is a general purpose digital-output LCD-display 6 in caliper, with a small electronics module 2 × 0.6 × 1.4", and it is specified at one year battery life, with two small silver-zinc cells used for power. A two-chip circuit is used, with a 5 μm CMOS ASIC for both drive and demodulation, using switched capacitor methods, and a 4 bit microprocessor handles math and display.

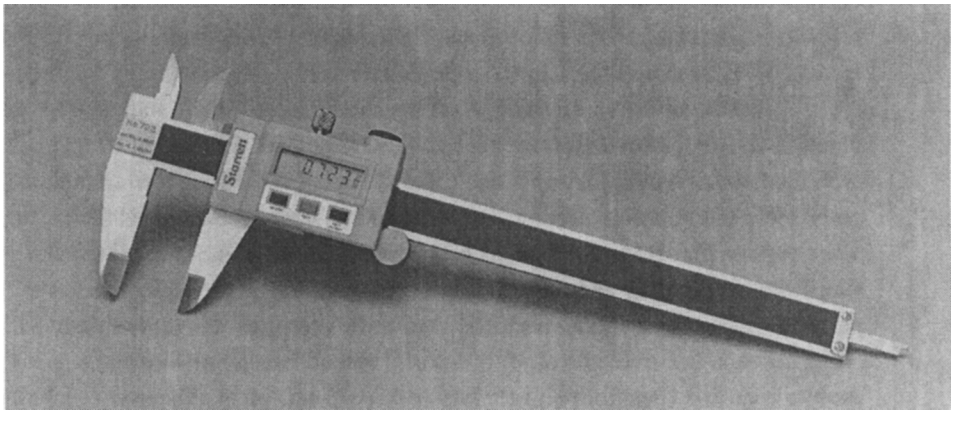

Figure 18.1 Starrett model 723 (U.S. patent 614,818, L. K. Baxter and R. J. Buehler, assigned to L. S. Starrett Co.)

The model 723 uses capacitive sensing to achieve the high resolution and good battery life. It uses multiple plates on 0.1 in centers, with a digital coarse plate counter keeping track of the position of the slider on the 60 plates and an analog sin-cos fine position sense for the 0.1% resolution. Its plate geometry is shown in Figure 18.2.

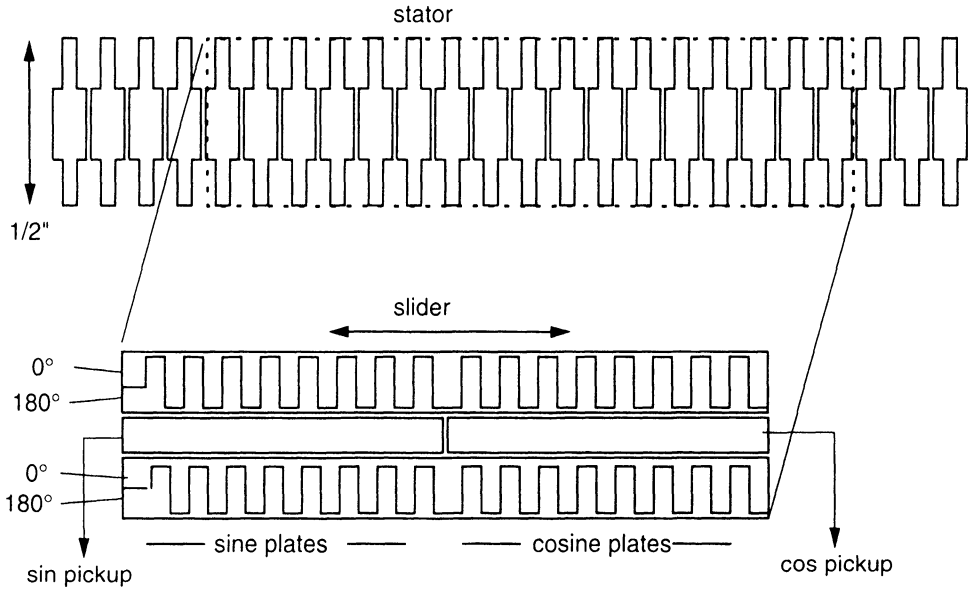

Figure 18.2 Starrett 723 plate geometry

A partial section of stator is shown. The 6 in long stator is fabricated from 1/32 in FR-4 printed circuit board with 1 oz copper and a laminated 0.006 in glass-epoxy cover layer. It is glued in a channel of the stainless steel caliper bar.

The slider plate is 1/16 in FR-4 printed circuit board stock. In operation, it slides on top of the stator as shown, covering 17 of the stator plates with a small air gap. The outside plates of the slider are driven by a 3 V p-p 50 kHz CMOS signal at 0° and at 180°. One section of slider plates picks up a sine (or, more accurately, a rounded triangle) signal. The other section, the cosine section, is displaced 0.025 in. The stator plates underneath the sine plates on the slider will then, by capacitive coupling to the slider sine plates, assume a signal which varies as approximately sine (position), that is, a square wave at 50 kHz is picked up whose amplitude describes a sine waveform as the slider is moved, with one cycle for each 0.1 in of travel. The stator plates underneath the cosine slider plates will assume a cosine (position) signal. The center section of the slider is composed of two pickup plates, one of which picks up, by capacitive coupling, the signal of the sine stator plates, while the other picks up the cosine signal. The pickup plates feed high-impedance guarded amplifiers. The block diagram of the 723 is a typical multiplate system, as shown in Figure 18.3.

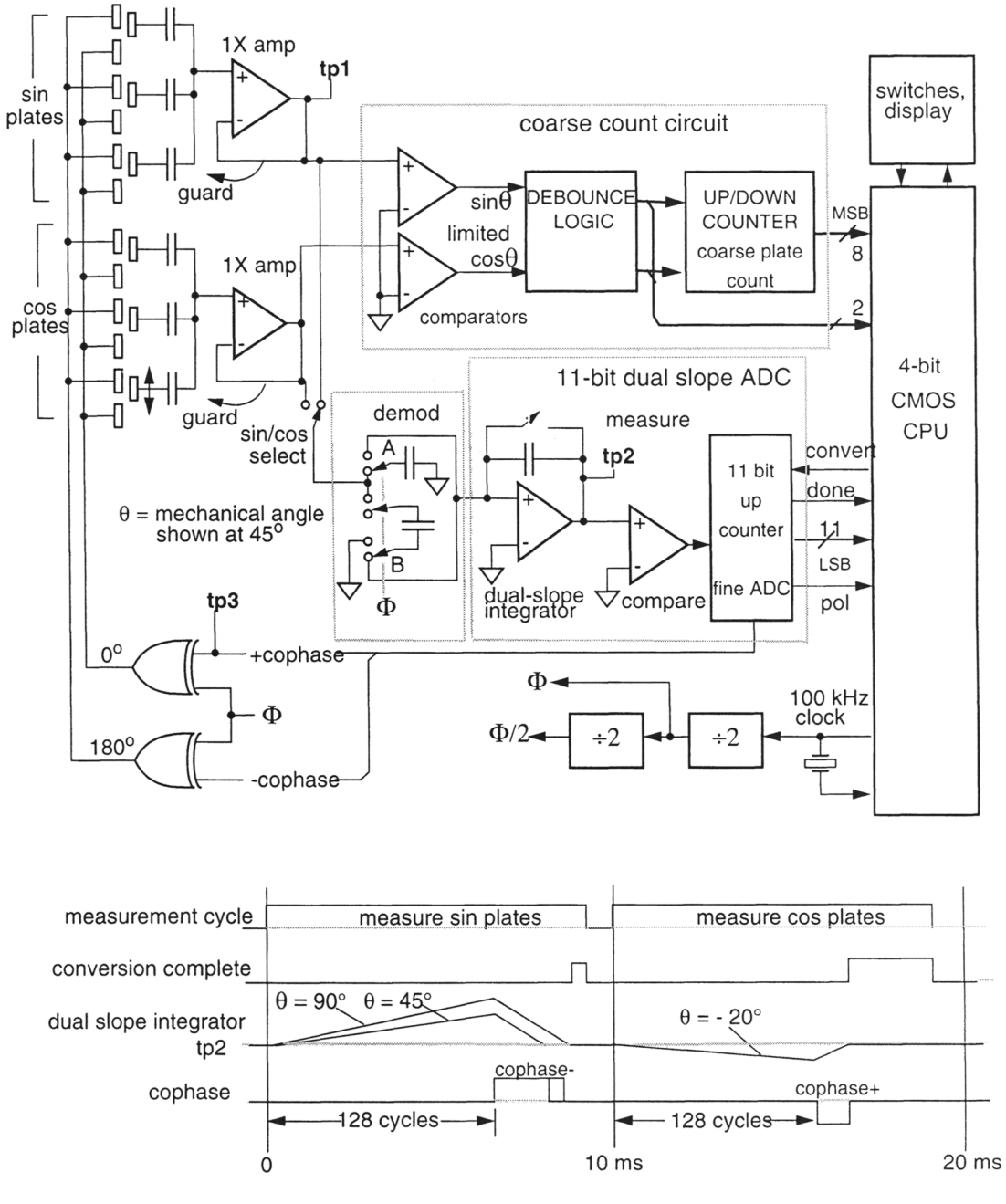

Figure 18.3 Starrett 723 block diagram

18.2 CIRCUIT DESCRIPTION

1x amplifier

Six of the sine plates are shown in the block diagram, coupling through the small 0.85 pF capacitance of the pickup plates to the input amplifier. A high-impedance 1× CMOS amplifier is used, with its output at *tp*1 fed back to guard the pickup. This guard totally surrounds the pickup plate and its connection to the input amplifier, and is connected to the two pins on the amplifier adjacent to the input pin to null out almost all of the capacitance to ground which would otherwise severely attenuate the signal. A small unguarded capacitance on the chip causes about a 35% signal amplitude loss which is compensated by the demodulation circuit.

The amplifier output signal at *tp*1 shows the 50 kHz modulation at a mechanical angle θ of 45° (Figure 18.4).

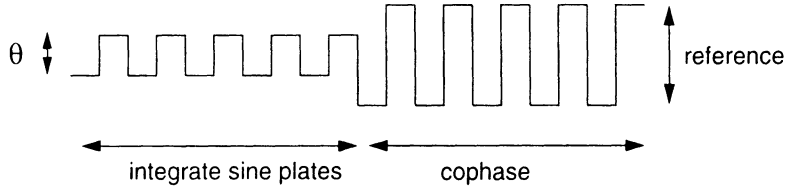

Figure 18.4 Amplifier output signal

The first segment at an amplitude θ changes with mechanical position in the range of 2 V p-p at 50 kHz 0° to 2 V p-p at 180°. The second segment at a reference amplitude results from driving both 0° and 180° sine plates with an identical (either 0° or 180°) signal when the cophase command is issued so that a full-scale reference output is produced. This is similar to the 90° modulation discussed in Chapter 10, except the 90° signal is further modulated by a higher frequency (50 kHz) carrier for this application.

Coarse plate count

The coarse plate count is implemented by squaring the sin and cos input signals with two comparators and determining phase with a *D*-type flip-flop clocked with 100 kHz. The flip-flop output will be a one for mechanical angles between 0° and 180° and a zero for 180° to 360°. After processing by the debounce logic of Section 8.3, the debounced output signals control an up/down counter which keeps track of coarse position.

Demodulator

The sine and cosine plates are alternately selected at about a 100 Hz rate. The chosen plate's signal is sampled (when the clock square wave is a one level) onto a small holding capacitor by demodulation switch *A*, and applied to the input of the dual-slope integrator when the clock is a zero. Similarly, switch *B* samples the input signal when the clock is a zero, and applies the sample capacitor with reverse polarity to the input of the dual-slope integrator. This is a switched capacitor implementation of a conventional synchronous push-pull demodulator followed by an integrator.

Dual-slope integrator

The integrator output, as shown in the timing diagram on Figure 18.3, will slowly increase with a small fixed positive mechanical angle θ to a voltage $K\theta$. After 128 clock cycles, a timer will change the drive signals 0° and 180° so they are both at 0°. This produces a mechanical-angle-independent full-slope discharge of the dual-slope integrator which continues until the integrator reaches zero and a comparator terminates the measurement cycle. During this "cophase +" discharge, the ADC counts clock pulses; full-scale voltage $K\theta$ on the integrator takes exactly 128 clock cycles to discharge to zero, and smaller voltages take proportionately less time. The cophase signal, then, has a time duration proportional to the magnitude of the voltage from the sine plates. It feeds the count enable input of an 11 bit counter which is clocked by 100 kHz. Negative mechanical inputs produce a negative-going slope on the integrator, and during cophase time the cophase term is active, resulting in a full-scale charge of the integrator to zero and a negative sign on the ADC output. This type of integrator is used for digital voltmeter applications, and is insensitive to component drift provided only that an accurate timebase is used.

18.2.1 CMOS ASIC

Sensor interfacing is handled by a CMOS semi-custom integrated circuit, or ASIC (Application-specific Semi-custom Integrated Circuit). This circuit, with a chip size of 3 × 4 mm, uses p- and n-channel MOSFETs from a standard array part with connections done by final-level metallization. This array also provides MOS capacitors in small values and diffused resistors. Macrocells have been characterized by the vendor for amplifiers and logic functions.

The ASIC's advantages are very low device interelectrode capacitance and low power consumption. Stable, small-value MOS capacitors and relatively unstable resistors make it more suited for switched capacitance circuits than conventional resistor-transistor circuits.

18.3 PROBLEMS

Several problems were encountered during design verification.

Wandering baseline

The coarse count comparators were originally designed with a simple circuit, shown above. In operation, the coarse plate count often made errors which were traced to a wandering baseline of the 1× amplifier output signal (Figure 18.5). With a very high impedance resistor (or, in this case, back-to-back high impedance FETs), small static charges could swing the amplifier DC level by 500–1000 mV. This effect was repaired by a change in logic: instead of comparing the signal to zero, one half-cycle of the signal was stored on a small MOS capacitor and compared to the second half of the signal.

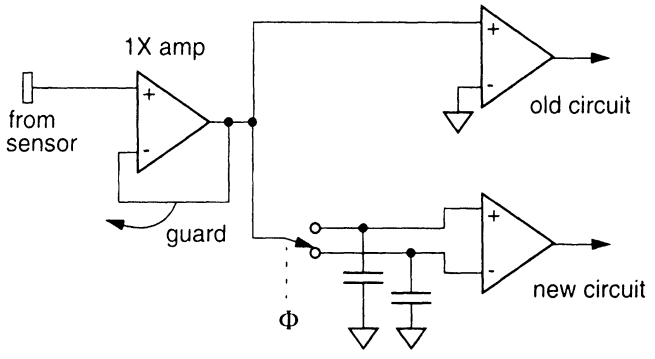

Figure 18.5 Starrett 723, fix for wandering baseline

Static charge

Static charge was a major problem. Static charge effects were not seen early in the design, which was started in the spring, as spring and summer seasons in New England tend to be humid and humidity masks static charge. In the winter, however, the humidity drops and static charge can become a problem. In the 723, the stator plates were covered with a thin layer of glass-epoxy laminate for protection, and this layer could easily pick up a charge after being rubbed on cloth. This charge could discharge through the small air gap to the slider plates and cause an error in the coarse plate count. As the caliper has no way of sensing absolute position, this coarse count error becomes a 0.050 in dimensional error.

Luckily, the effect is short and occurs during only one clock pulse. The repair was to add logic to detect a single comparator output bit which was of the opposite polarity of each of its neighbors, and reset it to its two neighbors' value (Figure 18.6).

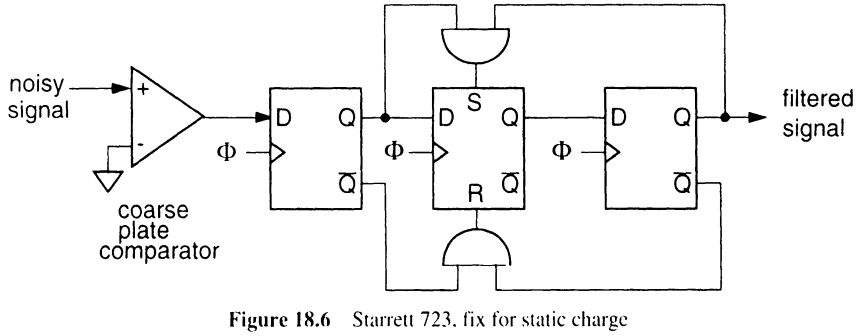

Figure 18.6 Starrett 723, fix for static charge

Parametric capacitance variation

The CMOS ASIC uses p-n diodes from its inputs to the power rails to protect against electrostatic discharge damage; these diodes have the typical variation of capacitance with reverse bias which is caused by the depletion area width becoming modulated by input voltage. The effect on the circuit is a capacitance at the pickup amplifier input which is modulated by the signal. This effect is a fraction of a pF, but as the pickup capacity is also a fraction of a pF, the signal amplitude is modulated in a nonlinear curve (Figure 18.7).

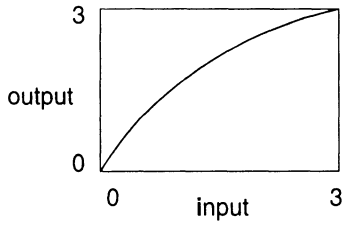

Figure 18.7 Parametric capacitance nonlinearity

For this chip, the p-n diode to the positive rail has the most effect; as the input voltage approaches the positive rail, the capacitance of this diode increases and the signal amplitude compresses.

Nontriangular sine and cosine waveforms

With zero capacitor plate spacing, or with ideal no-fringe-effects capacitors, the interpolation between plates would be ideal triangular waveforms, and the interpolation value could be easily determined by the methods of Section 8.1.1. In practice, the triangle is rounded by fringe effects and the sine and cosine waveforms are not equal value (Figure 18.8).

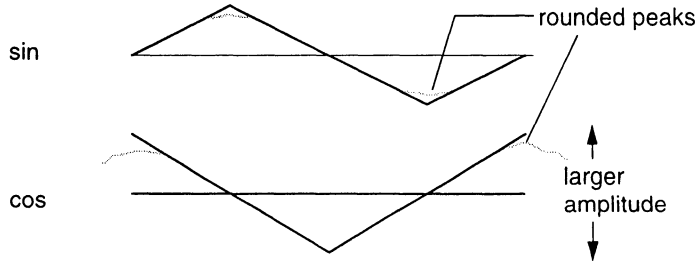

Figure 18.8 Sine and cosine signal inaccuracy

Table lookup

The effects of the shape of the triangular signals and the nonlinearity caused by parametric capacitance variation are both corrected using a lookup table whose entries are empirically determined. As the geometry of the plates and the physical size of the p-n diodes are both stable, the table results apply quite well to different units in production, with no trimming for individual variations needed.