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ULTRA LOW-POWER MEMS-BASED RADIOS FOR WBAN

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> It is in your power to withdraw yourself whenever you desire. Perfect tranquility within consists in the good ordering of the mind, the realm of your own. Think of the universal power, of which thou has a very small portion; and of universal time, of which a short and indivisible interval has been assigned to thee; and of that which is fixed by destiny, and how small a part of it thou art.
>
> Marcus Aurelius, *Meditations*

12.1 INTRODUCTION TO BODY AREA NETWORKS

Non communicable diseases (NCD) such as cardiovascular disease, diabetes, and cancer are the leading causes of global mortality today, accounting for around two-thirds of total deaths per year [1]. Further, data show that nearly 80% of the deaths by the NCDs occur in middle and low income countries which impose a large economic and social burden on the already under-staffed health-care systems [2]. This is further exacerbated by the fact that the population of people above the age of 60 is expected to rise to 1.2 billion or 15 % of the global population by the year 2025 [3]. Since the treatment of NCDs is expensive, prevention of these diseases in people with high risk factors by better and more accurate early diagnostics becomes important.

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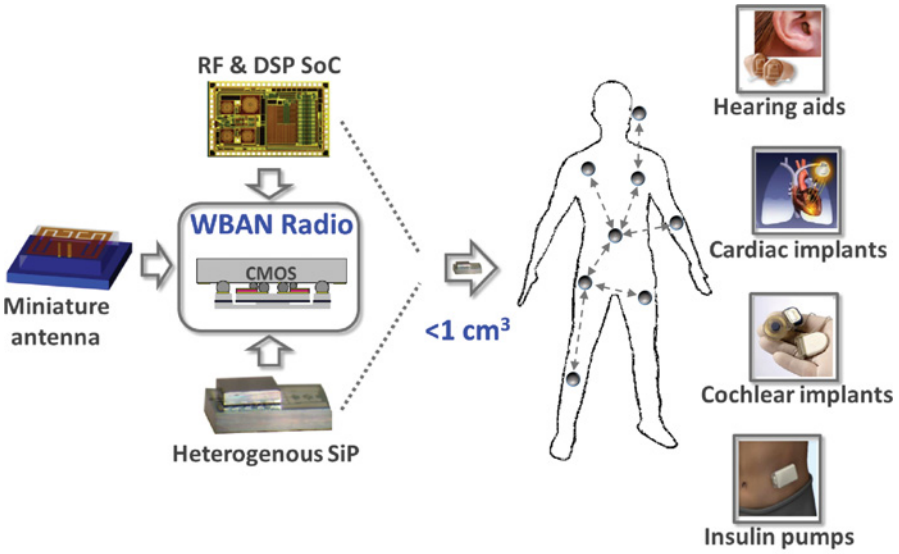

FIGURE 12.1 A typical WBAN system.

This requires a constant monitoring of various physiological parameters to enable an early detection of the onset of symptoms. Therefore, to alleviate the pressure on the health-care systems, there is a need for remote data collection from patients. Fortunately, wearable monitoring systems offer a low cost solution for this issue. These monitoring systems consist of an agglomeration of sensors that monitor various physiological parameters. In addition to this, these systems also usually utilize a wireless radio (since wired systems are expensive and cumbersome) to connect to the data collection hub for further analysis. Taken together, the sensors and the radio form what is known as a wireless body area network (WBAN). According to [4] *"A Wireless Body Area Network consists of small, intelligent devices attached on or implanted in the body which are capable of establishing a wireless communication link. These devices provide continuous health monitoring and real-time feedback to the user or medical personnel"* (Figure 12.1). There has been a rapid increase in the proliferation of these WBAN devices in the recent times with almost 1.7 million of these units being sold worldwide in 2012. This figure is projected to go up further and reach almost 18.2 million units by the year 2017 as shown in Figure 12.2 [5]. Due to this ever increasing presence, much research has been done in this field to improve and optimize the WBANs. Owing to their wearable/implantable nature, these BANs have a unique set of requirements unlike the normal wireless sensor networks (WSN). These requirements are detailed in the following section.

12.2 WBAN REQUIREMENTS

- The power consumption of the WBAN should be in the order of few tens of μW to ensure battery autonomy of such systems.

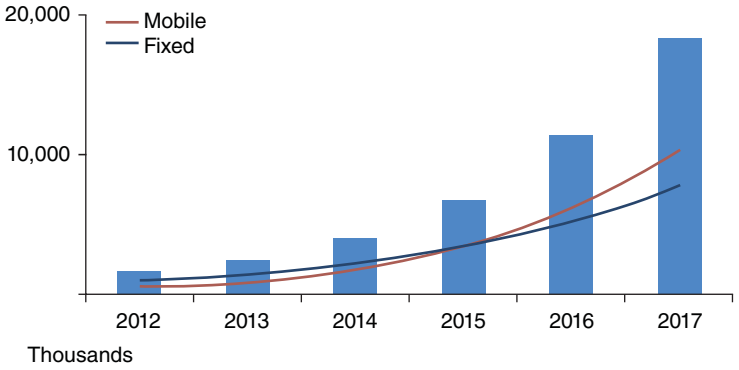

FIGURE 12.2 Projection of Global Health WBAN Shipments (2012–2017).

- WBAN devices should be very small in size of maximum 1 cm^3 in volume.
- They should have low output power to avoid any potential health concerns.
- The communication in some of these nodes which involve implantable devices occur through the human body which is a lossy medium that should be taken into consideration. Moreover, the fact that human body may be in motion should also be taken into account.
- Finally, strict security mechanisms are needed to ensure confidentiality of the patient's data.

12.3 LIMITATIONS OF CONVENTIONAL RADIOS FOR WBAN SYSTEMS

In the above list of WBAN requirements, the first point is of particular importance, since the size of the system is limited, which greatly constrains the energy sources. The main source of the power dissipation in the WBAN systems is the radio required to communicate with the data collection hub. To illustrate this point, let a hypothetical ultra low-powered radio that requires only 10 μW for nominal operation be utilized by the BAN. If such radio uses a CR2032 button cell battery (20 mm diameter and 3.2 mm thickness which amounts to around 1 cm^3) that provides about 225 mAh as an energy source, the battery life time can be calculated to be around 2.5 years. In case of further miniaturization of the battery, this lifetime will decrease even further, as in the case when a V335 battery providing 5 mAh is used for the same radio. This battery is expected to last only 20 days with the radio consuming 10 μW of power. Therefore, it is imperative to keep the power dissipation of radios used in WBANs as low as possible in order to extend the energy autonomy. Taking advantage of the fact that the average data that the WBAN needs to communicate are in the order of a few kb/s, the power reduction of the radios is accomplished by duty cycling. Duty cycling involves data transfer via radios capable of achieving high data rates, so that they communicate short bursts of data at this high rate and are asleep the rest of the

time. Any increase in the data rate capability of these radios serves to reduce the time which they are active, thus leading to lower duty-cycle ratios and subsequently lower energy dissipation. But any such data rate increase poses many design challenges, especially in the frequency synthesizer part, due to the fact that the data rate is invariably linked to the synthesizer design. For instance, in the case of conventional phase locked loop (PLL)-based synthesizers, the data rate is directly proportional to the loop bandwidth. Therefore, any increase in data rate will also require an increase of the loop bandwidth which comes at a cost of increased quantization noise (QN) due to the Sigma-Delta modulator (SDM) appearing at the PLL output [6]. Many techniques have been suggested in the literature to reduce the impact of the SDM QN at the output of the PLL [7, 8]. Even though this reduction of the SDM QN would prima facie appear to help increasing the transmitter (TX) data rate, in reality it solves only a part of the problem. This is because of the fact that the PLL-based synthesizers accrue a constant energy overhead due to the frequency reference (which, in most cases consist of a crystal oscillator (XO). This is due to the reason that the XO has a long startup time, during which it has a significant power consumption. In addition, the settling time of the PLL also contributes significantly to the energy overhead of the system. This energy overhead therefore reduces the impact of any increase in data rate for reducing power consumption by increasing the rate of duty cycling. Therefore, it is necessary to look for an architecture that circumvents this energy overhead of the frequency synthesizer, thereby making a migration to higher peak data rates more effective. Apart from this overhead problem of the crystal oscillators, for applications requiring ultra miniaturized radio like cochlear implants, the quartz crystal remains one of the bulkiest part, preventing the introduction of a radio link in the ear canal. Therefore, there is a need to find an alternative to the crystal which not only can startup fast, but also is small so that it can be used in miniaturized systems. But before going into the potential solutions to the bulky crystal, there is a need to derive a figure-of-merit (FoM) that takes into account the energy overhead. This is due to the fact that the conventional FoM which calculates the energy spent per bit communicated (Energy/bit) does not address the energy overhead and is therefore of little use in Ultra Low Powered (ULP) duty-cycled systems.

12.4 COMPARISON METRICS FOR ULP RADIOS

The derivation of the energy metric here follows the work of [9] by assuming a ULP system which has to maintain a mean data rate of MDR (bit/s). The time taken for this system to communicate K bits of data is $T_d(s) = K/MDR$. If the system employs a radio capable of a peak data rate of PDR(bit/s), then it can be duty cycled with a ratio $DC = MDR/PDR$. The packet rate of the system is given by $R_p(packets/s) = MDR/L$ where L is the length of each packet.The duration of each packet is then $D_p(s) = L/PDR$. If this radio consumes a peak power of $P_p(W)$ while in operation, then the energy spent for communicating K bits of data is given by $E_c(J) = T_d \cdot R_p \cdot D_p \cdot P_p$ (communication energy). In addition, if the radio dissipates

a power of $P_{st}(W)$ during wake-up, the overhead energy spent during each wake-up cycle will be $E_{oh}(J) = P_{st} \cdot T_w$, where $T_w(s)$ is the wake-up time of the radio (which is usually dominated by the frequency synthesizer wake-up time). In a PLL-based radio, the energy wasted during the settling time of the synthesizer also adds to this overhead ($E_{settle}(J) = P_p \cdot T_{settle}$). Subsequently, the energy wasted as overhead during the communication of K data bits is $E_{oh,tot}(J) = T_d \cdot R_p \cdot (E_{oh} + E_{settle})$. Then, the overall energy spent by the system for communicating K bits of data is $E_{p,tot}(J) = E_c + E_{oh,tot}$.

Useful Energy Threshold To illustrate the application of the above-derived FoM, let a WBAN communicating 10 kbit/s on average be assumed. Now let the radio used in the system utilize the state-of-the-art (SOTA) transmitters given by [10] and [11] which have a peak operational power dissipation (P_p) of 5.4 mW and are capable of a peak data rate (PDR) of 2 Mbit/s. To achieve the MDR of 10 kbit/s, the system can be duty cycled with a ratio of $DC = 0.5\%$. If the packet length is fixed to be $L = 32$ bytes, then the packet rate is calculated as $R_p = 40$ packets/s and the duration of each packet is $D_p = 125$ μs. If the data transmitted by the system is assumed to be $K = 10$ kb, then $T_d = 1$ s and the mean energy dissipated for communication is $E_c = 47$ μJ. If such a BAN employs a PLL-based radio for its radio, then the system will have a long wake-up time owing to the XO (typically $T_w = 1$ ms) and a high start-up power dissipation (P_{st}) of around 1 mW which worsens the $E_{p,tot}$ FoM. Coming to the energy overhead, due to its long startup time, the XO is usually left permanently on during which time it consumes 50–100 μW of power. Therefore the energy overhead for the transmission of 10 kb of data is ($E_{oh,tot} = 50$–100 μJ) which is higher than the energy spent to communicate. Even if a duty cycling of the XO along with the TX is pursued, based on the 1 ms startup time and 0.5 mW power, the energy overhead is 20 μJ (40 packets/s). In addition to this, assuming a best case PLL settling time of around 20 μs, the energy overhead due to the PLL will be around 4.3 μJ. This is shown in Figure 12.3 which graphically explains the aforementioned energy dissipation calculations. Thus, the total energy dissipated in the best case is then $E_{p,tot} = 51.3$ μJ. If the system uses a CR2032 button cell battery (225 mAh) as its power source, this energy dissipation translates to a battery lifetime of 200 days or about 4.4 days when a V335 (5 mAh) battery is used. This very small lifetime deters the use of button cell powered autonomous wearable/implantable nodes. An important conclusion that can be drawn from the figures presented above is that, the energy wasted as overhead during each transmit cycle is almost equal to the communication energy. As the data rate of the transmitter is increased further, the communication energy keeps decreasing and at a certain point, the overhead takes over as the dominant energy sink of the system. This crossover point (called useful energy threshold or UET) shown in Figure 12.4 represents an important point for duty-cycled applications. This is due to the fact that any data rate increase which brings E_c below this UET has a limited impact on the system efficiency due to the larger energy overhead. Therefore, in order to increase the UET, there is a need to reduce the energy overhead of the system by means of reducing its startup time.

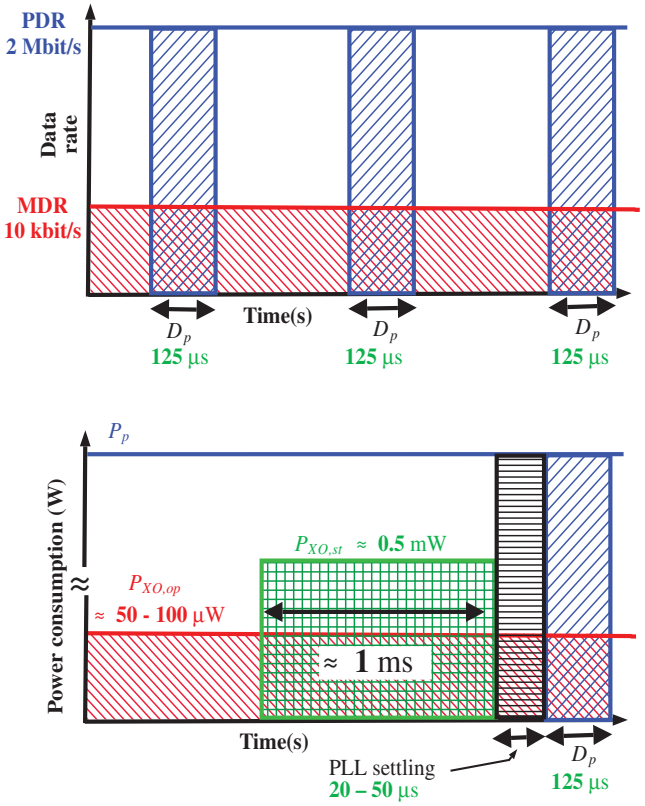

FIGURE 12.3 PLL-based transmitter duty cycling showing crystal oscillator startup overhead.

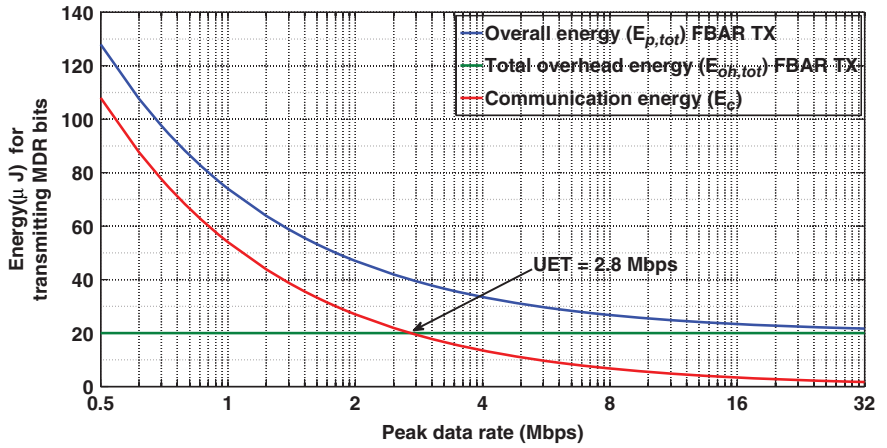

FIGURE 12.4 Energy dissipation break-up of a 10 kbit/s ULP system using the TX in [10]. *Source:* Wong et al. 2013 [10]. Reproduced with permission of IEEE.

12.5 MEMS RESONATORS—A SOLUTION TO BULKY CRYSTALS

MEMS resonators are an attractive alternative to the bulky quartz crystals due to their extremely small size with about 100 times smaller form factor. Among these micromachined resonators, a class of resonators called Bulk Acoustic Wave (BAW) resonators are of particular interest at RF, since they provide a stable frequency reference in the GHz range. Using such resonators, the loop-based synthesizer (PLL) employing crystal oscillator reference can be replaced by a loop- free, almost fully digital synthesizers which not only can startup in μs, but also avoid the latency due to the settling of the PLL. In addition, the high Q of the BAW resonators also makes them suitable for bandpass filters at RF with sharp roll off characteristics.

12.5.1 BAW Resonators

BAW resonators have found widespread use in duplexers due to their small size, high rejection, and low insertion loss [12]. They consist of a piezoelectric material (typically AlN) sandwiched between two electrodes as shown in Figure 12.5. When an electric field is applied between these electrodes, it causes mechanical deformation of the piezoelectric material. This results in an acoustic wave that travels in the direction of the thickness of the piezoelectric film for a particular orientation of electric field. The acoustic wave is reflected back at the film interface with the acoustic insulation layer due to impedance mismatch. When the thickness of the film equals an integer multiple of half wavelength, a standing wave is created by the forward travelling wave and the reflected wave. This acoustic wave in turn modifies the electric field distribution inside the piezoelectric film which changes the electrical impedance of the device. Thus the electrical impedance of the resonator changes with frequency [13]. Based on the nature of the acoustic insulator, the BAW resonators are classified into (a) Thin-Film Bulk Acoustic Resonators (FBAR) and (b) Solidly Mounted Resonators (SMR). While in an FBAR, the air interface serves as the acoustic insulator, the SMR employs Bragg mirrors made up of alternating layers of high and

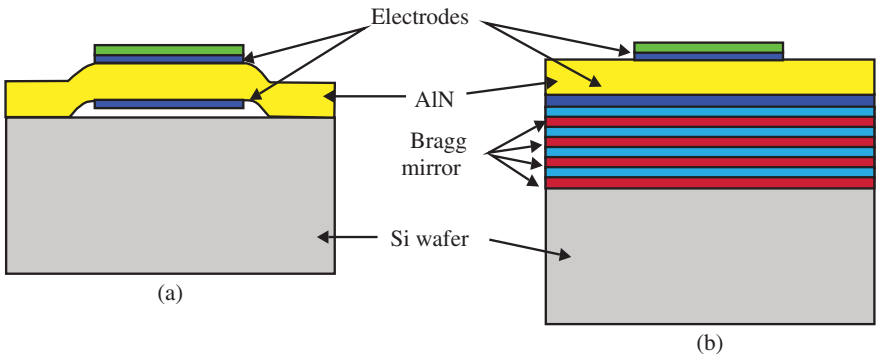

FIGURE 12.5 Cross section of BAW resonators: (a) FBAR, (b) SMR.

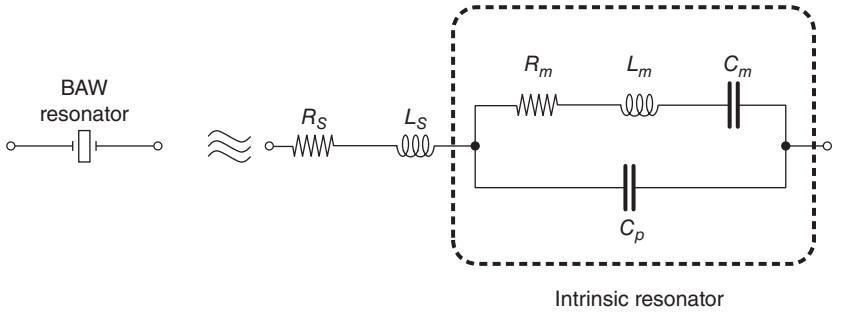

FIGURE 12.6 Butterworh-Van Dyke equivalent circuit of the BAW resonator.

low acoustic impedance. The thickness of the acoustic impedance layers must be designed with specified thickness such that there is a complete reflection of the acoustic waves into the device. The electrical equivalent of the BAW resonator is given by the Butterworth-Van Dyke model (Figure 12.6) and is similar to that of a quartz crystal [14]. It consists of a series Resistor-Inductor-Capacitor (RLC) network along with a parallel capacitance. In addition, there are parasitic resistances and inductances associated with the access connections. The intrinsic resonator thus has two resonance frequencies, one corresponding to the series RLC branch (series resonance) and the other corresponding to the total resonator itself (parallel or anti-resonance). The relation between these frequencies is given by

$$\omega_s = \frac{1}{\sqrt{L_m C_m}} \tag{12.1a}$$

$$\omega_p = \omega_s \sqrt{1 + \frac{C_m}{C_p}} \tag{12.1b}$$

The main performance parameters of the FBAR are the effective electromechanical coupling coefficient k_{eff} and the Q factor which specifies the energy loss in the resonator material. The coupling coefficient determines the energy conversion efficiency between acoustic and electrical domains or in other words is the ratio of the current in the motional branch (series branch) to the parallel branch. The relationship between this coupling coefficient and the resonance frequencies is given by [13]

$$k_{eff}^2 = \frac{\pi^2}{4} \left(\frac{\omega_p - \omega_s}{\omega_p} \right). \tag{12.2}$$

Thus, the coupling coefficient determines the interval of the resonance frequencies and therefore the tenability of the FBAR. Typical values of the coupling coefficient for an FBAR is about a few % and typical values of Q are in the range of 500–1000. Thus, the product $M = K \cdot Q_m$ (K is the ratio of the motional and the parallel

capacitances i.e., C_m/C_p) is the figure-of-merit of a BAW resonator which needs to be maximized to improve the performance. Even though either of FBAR or SMR can be utilized in the design of the radio, the work presented in this chapter is based on FBAR and both the terms FBAR and BAW resonator will be used interchangeably henceforth in this chapter.

12.6 FBAR-BASED RADIOS

As mentioned in the previous sections, PLL-free radios based on FBARs have fast startup which aids in reducing the energy overhead in the case of WBANs. In addition, $Q-$ *boosted* FBARs serve as excellent band-pass filters at GHz frequencies. Both these properties of the FBAR have been taken advantage of in the radio presented in this chapter. Owing to different design methodologies, the design of the Transmitter (TX) and the Receiver (RX) have been dealt with separately.

12.7 FBAR-BASED TX ARCHITECTURE

In order to reduce the TX E_{oh}, an alternative method of frequency synthesis was proposed by Flatscher et al. [15] based on an FBAR. This method takes advantage of the fact that the FBAR has a very small startup time (a few μs) and hence less energy is wasted during each wake-up sequence. The modulation is performed by simply varying the digitally controlled oscillator (DCO) frequency (frequency shift keying - FSK). The main problem of the circuit presented in [15] is that it is confined to addressing a few channels owing to the limited frequency tuning range of the FBAR (a few MHz). A simple way to solve this problem is to divide down the FBAR Digitally Controlled Oscillator (DCO) local oscillator (LO) signal (f_{LO}) to generate an Intermediate Frequency (IF). The LO and the IF can then be up-converted ($f_{RF} = f_{LO} + f_{IF}$) to get the desired carrier frequency which is then power amplified and transmitted. Even this method of mixing does not enable this architecture to cover all the frequencies in a band like the 2.4 GHz ISM. Therefore, in order to circumvent the issue of limited channel addressing, the divider used to generate the IF has been implemented as a Phase Switching Divider (PSD) with a division step of 0.2 that further reduces the tuning range required on the FBAR to cover all channels in the band of interest.

Figure 12.7 shows the proposed PLL-free up-conversion transmitter architecture. It consists of an FBAR DCO generating the LO signal, which is then divided by a PSD to produce the desired IF signal, i.e., $f_{IF} = f_{LO}/N$. The LO and the IF are then fed to a mixer which up-converts these signals ($f_{RF} = f_{LO} + f_{IF}$) followed by a single-ended class-C PA doing the final amplification. The centre frequency of the FBAR is chosen such that the spurs due to IF harmonics fall outside the band of interest while also being able to address all the channels in the given band. For instance, with the band of interest in this case being f_{RF} = 2.36–2.5 GHz and the channel to be addressed is at 2.36 GHz, if f_{LO} is chosen to be greater than or equal to 2.22 GHz, the

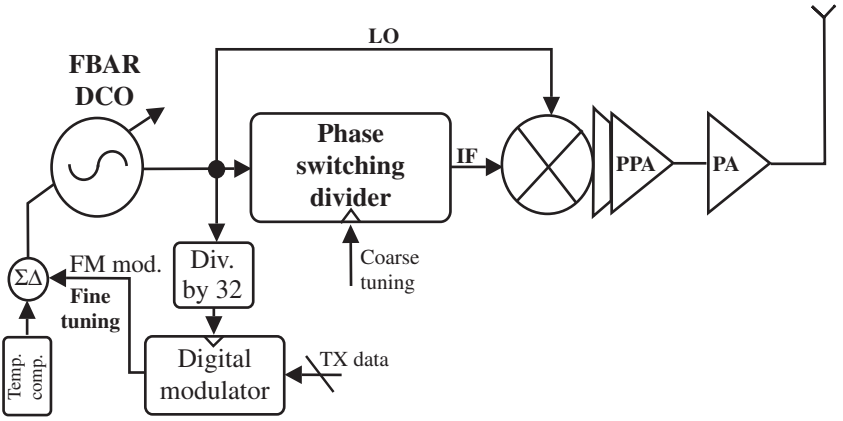

FIGURE 12.7 PLL-free up-conversion TX architecture.

second harmonic IF spur will be located at frequencies ≤ 2.5 GHz which is within the ISM band. Therefore the constraint on the LO is given by $f_{LO} < 2.2$ GHz. The other extreme is having an LO frequency far away from the wanted band. The drawback of this is as follows: greater the frequency difference between the LO and the wanted band, the higher the frequency of the IF signal will be. The IF is produced by the PSD which utilizes the IF itself as a clock (asynchronous feedback) for its state machines. Therefore, a high IF would result in more power dissipation in the PSD. Based on these constraints, a frequency of 2.2 GHz was chosen for the FBAR DCO. The DCO output is also divided by 32 to serve as a clock for a digital modulator that performs FSK by varying the DCO frequency.

12.7.1 FBAR DCO

Temperature compensated FBAR DCOs provide a highly stable reference at RF frequencies. These DCOs achieve an excellent phase noise performance along with low-power consumption [16] which is the main reason for choosing them for this TX architecture. The transistor level schematic of an FBAR DCO is shown in Figure 12.8. The DCO is implemented using a complementary structure in order to halve the power dissipation and reduce the flicker noise up-conversion. It consists of two cross-coupled pairs providing negative conductance to compensate for the energy loss in the FBAR. To avoid the latch-up of the circuit at startup, the cross-coupled pairs are AC coupled at their sources [17]. Furthermore, two common mode feedback (CMFB) transistors are implemented below the NMOS cross-coupled pair. To control the amplitude of the circuit while also ensuring a fast and reliable start up, an amplitude regulation loop (M_5–M_7) has been designed. This amplitude regulation loop is based on the concept of a proportional-to-absolute-temperature (PTAT) current [18]. A bank of 31 pairs of depletion/inversion MOS capacitors coarsely tune the DCO. Coarse tuning is also accomplished by changing the division ratio of the

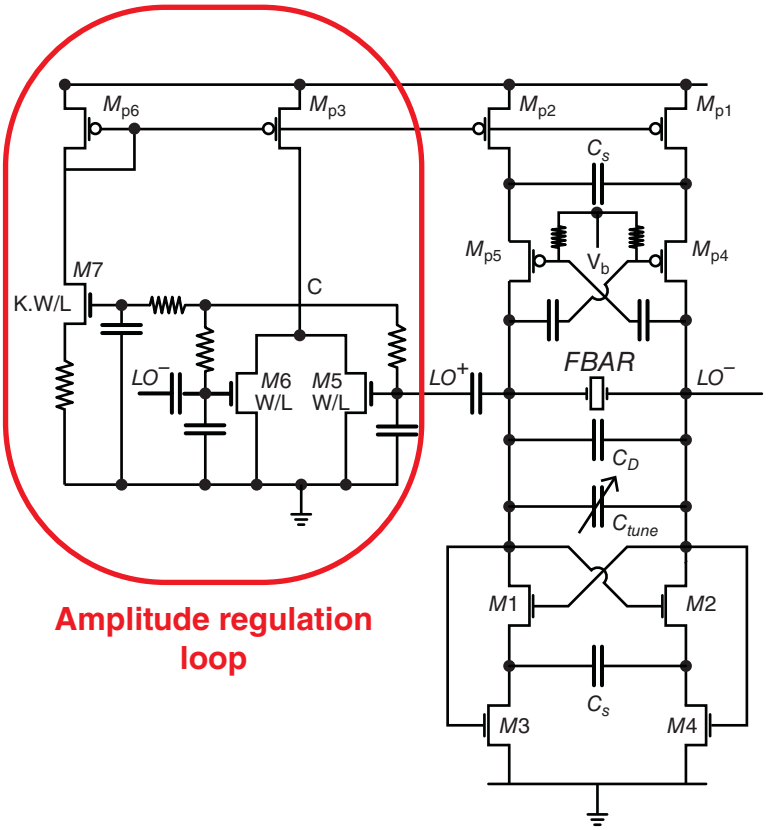

FIGURE 12.8 Schematic of the FBAR DCO.

PSD. The DCO also has three other MOS capacitances driven by the output of a 7-bit, second − order ΔΣ modulator enabling fine tuning. While the upper limit of the tuning range is limited by the resonator itself (a few MHz), the DCO has been designed to achieve a tuning resolution of around 0.9 ppm. Speaking of tuning, there exists a condition on the maximum DCO tuning range that must be satisfied for this architecture such that all the frequency channels within the particular band can be addressed. This condition is given as follows:

$$\Delta f_t = \frac{\Delta \cdot f_{LO}}{N_L^2 + (\Delta + 1) N_L + \Delta}, \tag{12.3}$$

where N_L is the lowest division ratio required for IF generation (which corresponds to the highest IF, provided low-side injection) and Δ is the division ratio step. With the f_{LO} being 2.2 GHz based on the power dissipation versus IF second harmonic tradeoff as mentioned in the previous section, the lowest division ratio N_L is 7.33 (for $f_{RF} = 2.5$ GHz and $f_{IF} = 300$ MHz). If a divider with a step size $\Delta = 1$ is used,

the tuning range required to address all the channels according to equation (12.3) is $\Delta f_t = 31.6$ MHz or $\Delta f_t/f_{LO} = 14.4‰$. This is impossible to achieve for an FBAR, thus making this architecture unsuitable for multi-channel communication [15]. To circumvent this problem, the PSD with $\Delta = 0.2$ is used which decreases the tuning range needed to a more relaxed value of $\Delta f_t = 7$ MHz or $\Delta f_t/f_{LO} = 3.18‰$. This FBAR tuning along with the modulation index (MI) required on the transmit side for a successful demodulation by the receiver also sets the limit on the Maximum Achievable Data Rate (MADR) of the system (irrespective of single or multi-channel addressing). If the condition of all channel addressing is imposed on this, then if the maximum tuning range of the FBAR is given as TR (in‰) and the tuning required to compensate for the process and voltage variations is PV (in ‰) ($\simeq 1‰$ [19]), the tuning remaining for modulation after accounting for Δf_t is

$$\Delta f_m = (TR - PV) * f_{LO} - \Delta f_t. \tag{12.4}$$

Then the MADR with All Channel Coverage (MADR-ACC) is given by

$$MADR - ACC = \frac{\Delta f_m}{MI}. \tag{12.5}$$

Any attempt to achieve data rates above this limit will see that the communication is restricted to a few channels.

12.7.2 Phase Switching Divider

The PSD implemented here was originally implemented to reduce the QN at the output of a fractional-N PLL [20]. The PSD block diagram is shown in Figure 12.9. It is made up of a five stage ring oscillator (ILRO) that is injection locked to the FBAR DCO. This ring oscillator produces five phases at the LO frequency that are spaced $0.2/f_{LO}$ apart. The PSD also consists of a finite state machine (FSM) that produces the select signals with each of them corresponding to a phase signal from the ILRO. The select signals are resynchronized using the edges of the phase signals following which the multiplication of the select signal and its phase occurs in a phase combiner. The resulting signals are then summed together using OR gates. This summed signal is then fed to an integer divider that is set to divide by the nearest integer of the division ratio required. The output of this integer divider is the wanted IF signal which also clocks the FSM. Further information about the implementation of this PSD is given in [20].

12.7.3 Mixer, Power Amplifier Stage, and Digital Baseband

The mixer is implemented as a single-balanced Gilbert cell with resonant load at 2.44 GHz followed by a push-pull preamplifier-buffer (PPA) which performs differential to single-ended conversion. The final power amplifier consists of a single-ended cascoded output stage and a resonant interface between the PPA and PA as shown in Figure 12.10. The integrated digital baseband contains an FSK modulator with

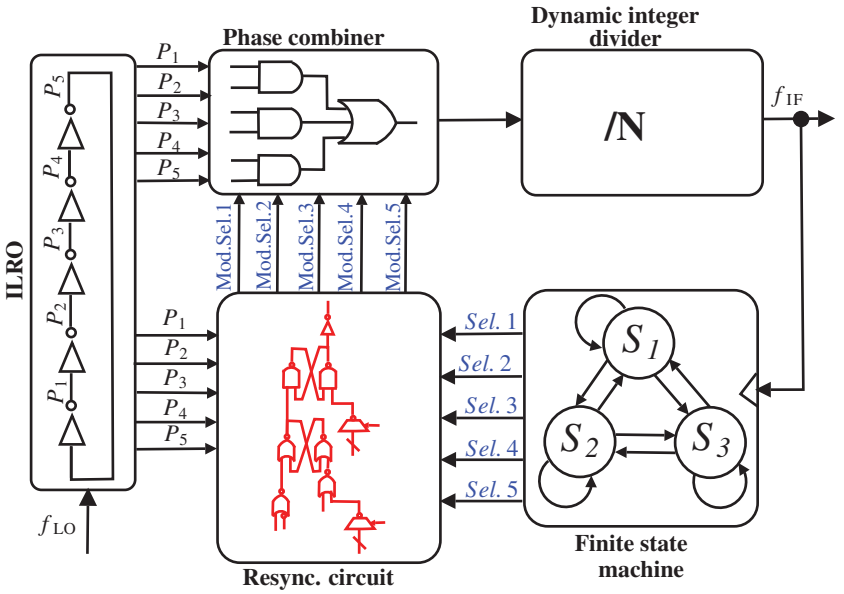

FIGURE 12.9 Phase switching divider.

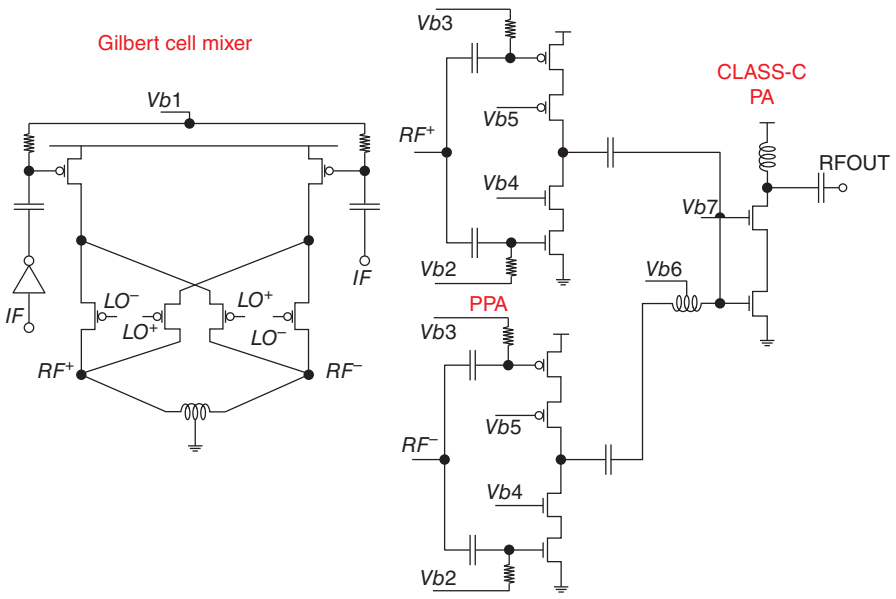

FIGURE 12.10 RF frontend mixer, PPA, and PA.

programmable pulse shape and modulation index, data rate selection, Manchester coding along with a high speed SPI interface. The input to the FSK modulator is the desired TX data pattern that is programmable via an SPI interface and can be set to a random sequence for the purpose of modulation analysis.

12.8 TRANSMITTER MEASUREMENT RESULTS

The structurally compensated (with SiO_2) FBAR used for this setup was measured to have a frequency sensitivity of −6.5 ppm/°C or 814 ppm over the temperature range −40 to 85°C. Further details about the SiO_2 compensation of the FBAR and its packaging can be found in [21]. To further improve the frequency stability, a three-points calibration scheme was employed [22] which reduced this large deviation to ±20 ppm over the entire range as shown in Figure 12.11. The maximum tuning of the FBAR DCO was measured to be 4.9‰. Accounting for FBAR PV variations (PV = 1‰) [19] and $\Delta f_t/f_{LO} = 3.18‰$ leaves $\Delta f_M/f_{LO} = 0.72‰$ for modulation. From equation (12.5), this translates to MADR-ACC of 3 Mbit/s at an MI of 0.5 in the range of 2.36—2.5 GHz. But if the focus is only on the 2.4—2.48 GHz ISM band or the other wing bands alone, then the f_{LO} frequency can be chosen to be 2.29 GHz so that the spur due to the IF second harmonic is outside the band. In this case, the tuning range required reduces to 0.99‰ resulting in an MADR-CC of 12 Mbit/s (2 FSK). Even though the MADR-CC is limited, specific channels can still be addressed at higher data rates. For this, the digital baseband of the implemented TX supports data rate up to 16 Mbit/s (4 FSK with 8 MS/s) and the eye diagrams corresponding to the different data rates are given in Figure 12.13, which show a trend of decreasing modulation accuracy with increasing data rates. Finally, the phase noise of the DCO shown in Figure 12.12 gives the value of −128 dBc/Hz at a frequency offset of 100 kHz and a

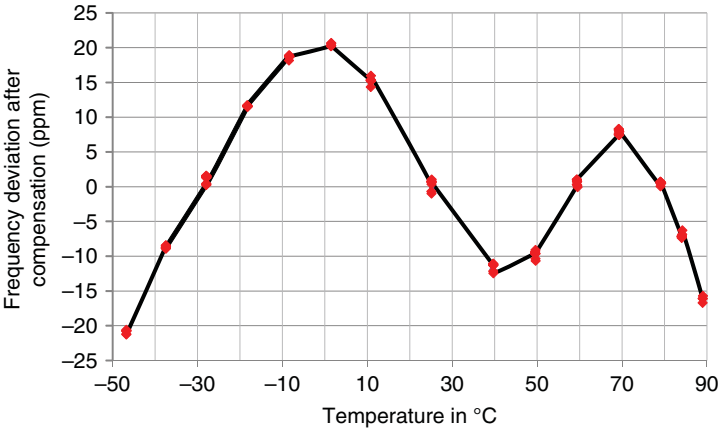

FIGURE 12.11 Measured FBAR DCO frequency stability versus temperature.

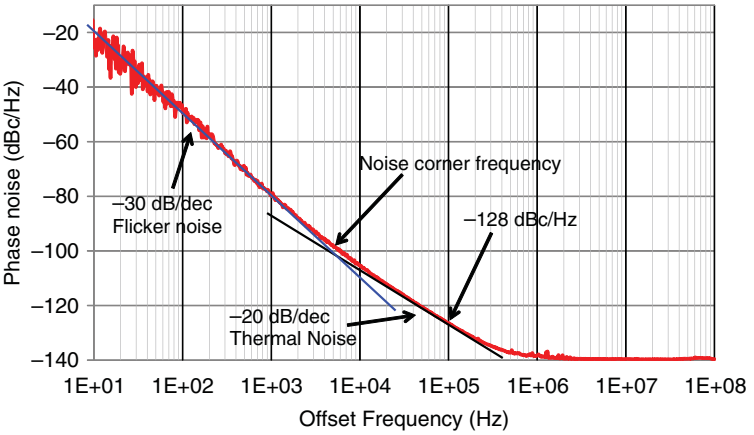

FIGURE 12.12 Measured phase noise of the FBAR DCO.

flicker to thermal noise corner frequency of 5 kHz. This value is also the phase noise of the carrier signal at low offset frequencies (due to injection locking).

The maximum output power of the Transmitter is −1 dBm which meets the Bluetooth-Smart requirements [23] (Figure 12.14). The spurs in the wideband output spectrum (Figure 12.15) mainly occur due to four mechanisms namely: (a) the fractional division step of the PSD (=0.2) causing spurs at multiples of $0.2 * f_{IF}$ offset, (b) clock feedthrough spurs located at multiples of $f_{LO}/32$ offset, (c) LO feedthrough,

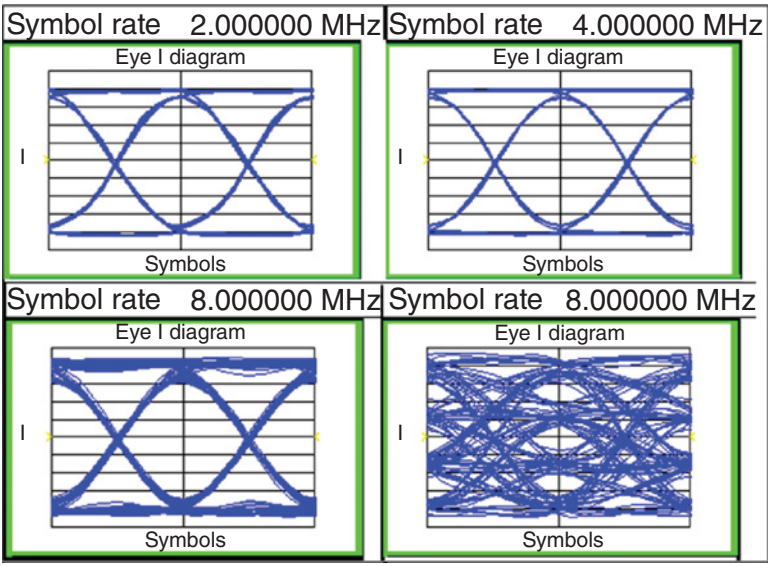

FIGURE 12.13 Eye diagrams for GFSK at various data rates *viz.* (a) 1 Mbit/s, (b) 2 Mbit/s, (c) 8 Mbit/s, (d) 16 Mbit/s, (8 MSps — 4FSK).

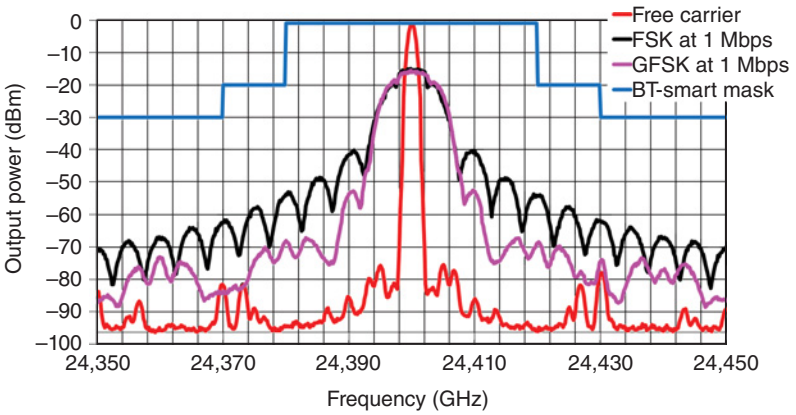

FIGURE 12.14 Close-in spectrum showing free carrier, FSK, and GFSK.

and (d) IF second harmonic. While the spurs due to both LO feedthrough and IF second harmonic are at −29 dBc, the fractional spurs due to the divider step are at least 47 dB below the carrier. The clock feedthrough spurs are at least −70 dBc as shown in Figure 12.15.

The dynamic operation of the TX is shown in Figure 12.16 which depicts the time domain TX output measured at 1 Mbit/s FSK with a modulation index of 0.5. The current profile shows that the TX takes only 5 μs to start transmission after wake-up. The wake-up times of the individual blocks are given as follows: 2 μs for the FBAR DCO, 2 μs for the PA, and 3 μs for the modulator. The PA and the modulator can be started at the same time after which the sample data pattern "0110 1010" can be seen on the frequency versus time plot. The TX can be turned off in 3 μs while channel switching also can be performed in just 3 μs. This frequency agility is one of the main

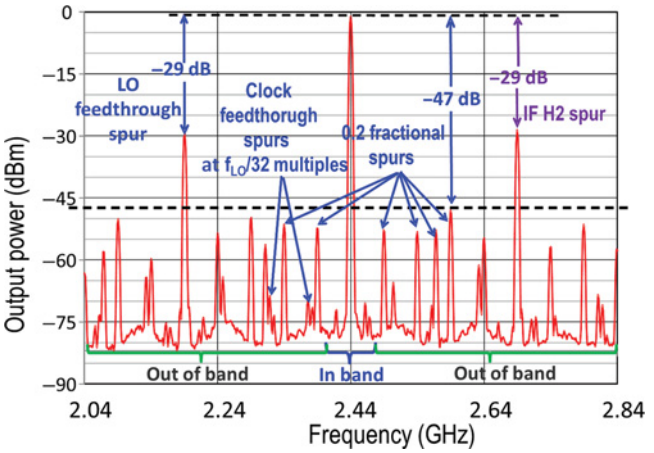

FIGURE 12.15 Wide-band spectrum showing the spurious characteristics.

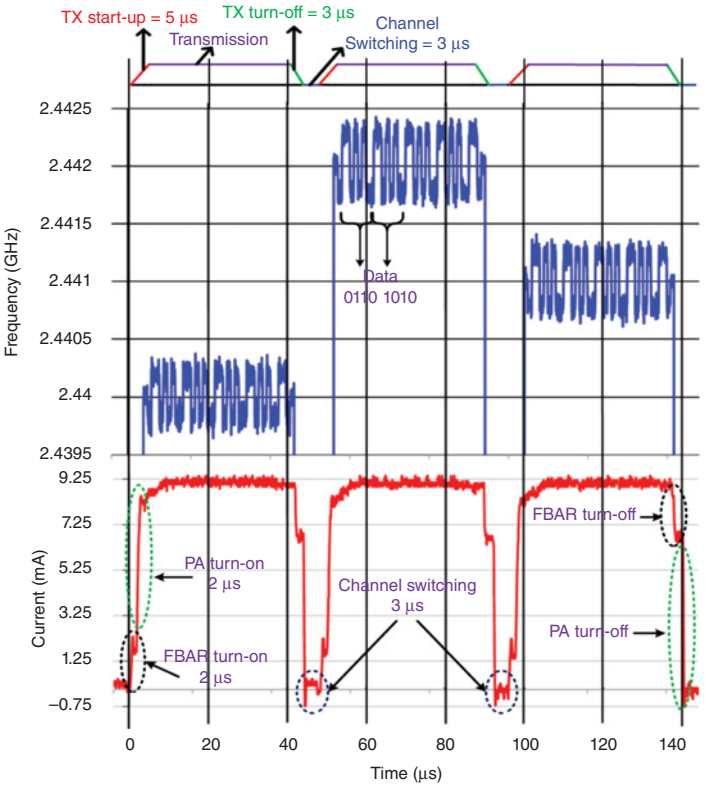

FIGURE 12.16 Frequency agility of the TX showing FSK data (top) and TX current profile (bottom) showing the startup/channel switching times.

advantages of this TX since it allows us to perform frequency hopping to any channel within the band in a span of 3 µs, while still being a narrow-band system.

The TX consumes 9.2 mA from a 1.2 V supply with the power breakdown shown in Figure 12.17. The power consumption during the 5 µs startup phase takes the following trajectory: Initially, the FBAR DCO starts during which time it consumes 2.5 mA, followed by a ramping up of the current due to the PA startup during the next 3 µs till the peak current is reached. To find an approximation for the startup energy overhead, the area under the current profile (Figure 12.16) was calculated and multiplied with the supply voltage to give the energy dissipation as $E_{oh} = 18$ nJ. At this juncture, it is imperative to note that this synthesizer does not suffer from the settling time that plagues the PLL-based synthesizer. Now, if this TX is implemented in the 10 kbit/s WBAN system described in Section 12.4 with L = 32 bytes and K = 10 kb, at a peak data rate of 16 Mbit/s this translates to the total startup energy dissipation $E_{oh,tot} = 0.72$ µJ. The duration of each packet in this system is $D_p = 16$ µs and consequently, the energy dissipated in communication is now $E_c = 7$ µJ. Therefore, the total energy FoM is $E_{p,tot} = 7.72$ µJ. A comparison of this TX with the

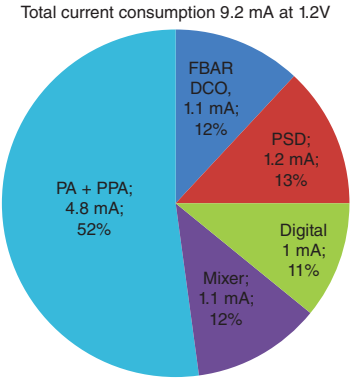

FIGURE 12.17 TX power consumption breakdown.

PLL-based SOTA TX at different peak data rates can be seen in Figure 12.18 from which the following conclusions can be drawn.

- The FBAR-based TX shows a 34 reduction in the startup energy overhead figures due to the very fast startup of the FBAR DCO and the absence of the synthesizer settling time.
- Due to this small startup overhead, the UET of the FBAR-based TX is 187.5 Mbit/s as opposed to 2.8 Mbit/s for PLL-based transmitter.
- The PLL-based TX performs slightly better at lower peak data rates due to the fact that the power spent for communication is much higher at these data rates. Since the PLL-based TX has lower peak power dissipation, this is an expected result.

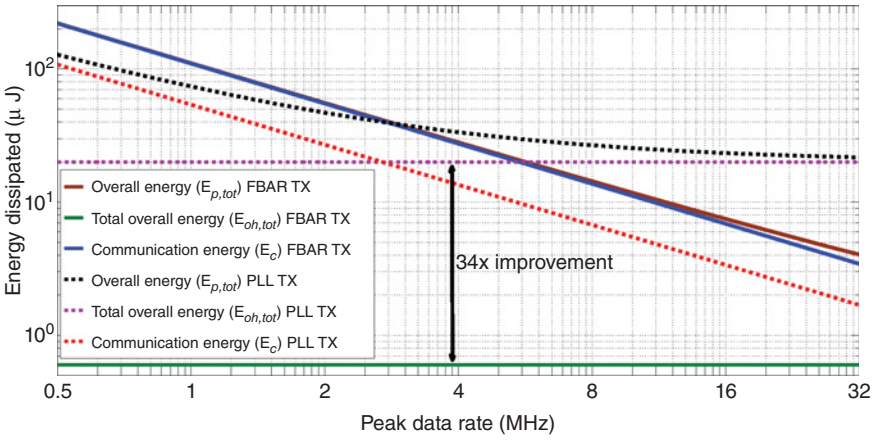

FIGURE 12.18 Variation of the energy dissipation with peak data rate in PLL-based SOTA TX and FBAR TX.

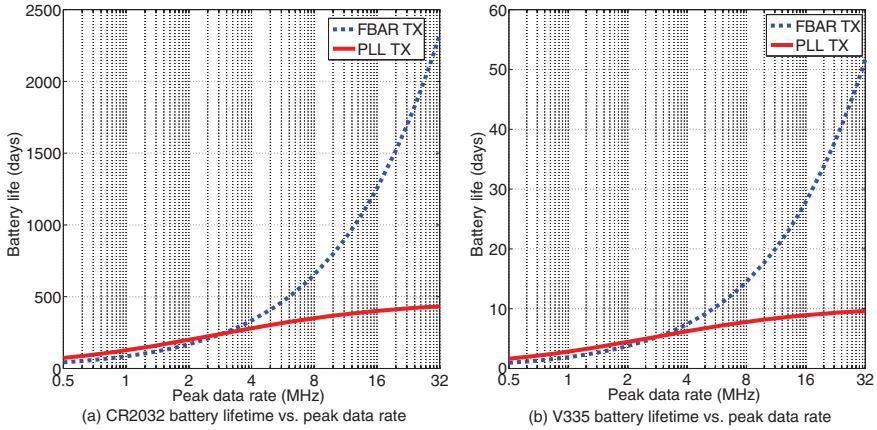

FIGURE 12.19 (a) Variation of lifetime of CR2032 battery with increasing data rate, (b) variation of lifetime of V335 battery with increasing data rate.

- At higher peak data rates, the longevity of the FBAR-based TX operating from a fixed power source such as a CR2032 battery is much more (Figures 12.19a and 12.19b) than that of the PLL-based TX due to its reduced overhead $E_{oh,tot}$. For instance, if under the assumption that the SOTA TX can be extended to operate at 16 Mbit/s peak data rate with the same power (5.4 μW), the FBAR-based TX outperforms the PLL-based SOTA TX by having a 3 times longer (1254 days vs. 400 days) battery life. But if the transmitters are operated at their maximum capable peak data rates (16 Mbit/s for FBAR TX and 2 Mbit/s for PLL TX), then the FBAR-based TX outperforms the PLL-based TX by a factor 7 in battery lifetime.

The performance comparison of this transmitter with other works of literature is shown in Table 12.1. The chip microphotograph given in Figure 12.20 shows the PLL-free, FBAR-based TX and the circuit of [20].

TABLE 12.1 Performance comparison with prior literature.

Parameter	[10]	[11]	[15]	This work
Peak data rate	2 Mbit/s	1 Mbit/s	50 kbit/s	16 Mbit/s
Modulation	FSK/PSK	FSK/PSK	FSK	FSK
I_{dc}(mA)	4.5	8.9	6.0	9.2
V_{DD}(V)	1.2	1.0	1.8	1.2
TX output power	0 dBm	0 dBm	1 dBm	−1 dBm
Startup time	40 μs	N/A	2 μs	5 μs
DCO PN (dBc/Hz)	−112 at 1 M	−87 at 130 k	−126 at 1 M	−121 at 100 k
Energy efficiency	2.7 nJ/b	6.5 nJ/b	144 nJ/b	0.7 nJ/b
$E_{st,tot}$ FoM	67 μJ	89 μJ	N/A	7.5 μJ
Technology	90 nm	130 nm	130 nm	65 nm

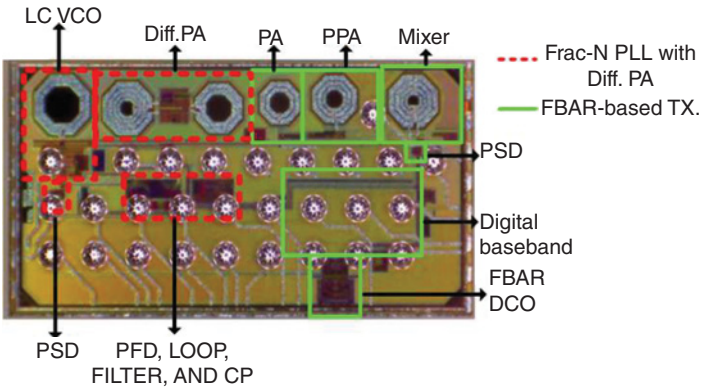

FIGURE 12.20 FBAR-based transmitter chip microphotograph.

12.9 SUMMARY OF THE FBAR-BASED TX

A PLL-free transmitter architecture based on an FBAR to reduce the startup energy overhead in duty-cycled low-power systems has been presented. Utilizing a PSD injection locked to the FBAR DCO to generate the IF thereby overcoming the limited frequency tuning of the FBAR, this TX can address all channels in the frequency range of 2.36–2.5 GHz. The FBAR also gives the TX the ability to start in just 5 μs, enabling this TX architecture to achieve a significant reduction in energy dissipation (a 7x reduction in the ULP example mentioned) at its MADR as compared to SOTA TX. In addition, the provision to switch channels in just 3 μs despite being a narrowband system makes this transmitter an attractive proposition for ULP systems.

12.10 RECEIVER ARCHITECTURE

A receiver which makes the best use of the low phase noise of the FBAR DCO signal and eliminates the need for a PLL to address multiple channels is presented in this section. As shown in the block diagram of Figure 12.21, the receiver utilizes the intrinsic high Q of the FBAR in the RF front-end to provide in-band interferer rejection and in the frequency synthesis to provide clocks with high spectral purity. The PLL-free approach involving integer dividers, and the sub-sampling–based down-conversion, makes the receiver easily scalable for implementing it in an advanced deep sub-micron process.

The received RF signal from the antenna is pre-filtered and then fed differentially to the LNA. The LNA amplifies the RF signal and this amplified signal is fed to the input of an Amplifier-Mixer-Filter (AMF) cell which performs channel selection and filtering. The AMF cell can either be loaded with an FBAR full-lattice [24] or a FBAR pseudo-lattice [25] to provide narrow-band filtering at RF or at a super-high intermediate frequency (IF). This filtering can be used as an anti-aliasing filter to

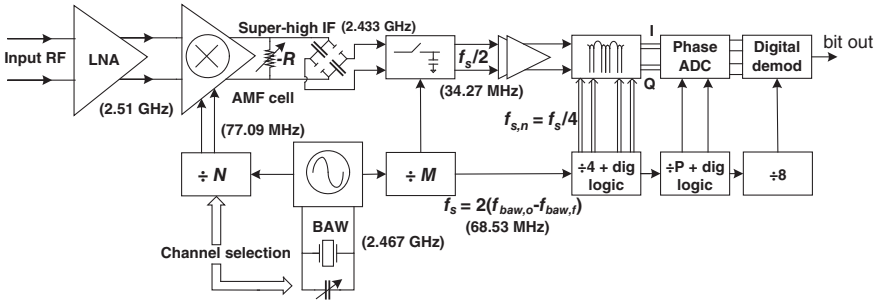

FIGURE 12.21 MEMS-based PLL-free sub-sampling receiver architecture. High Q FBARs are used in the channel selection filter and in the oscillator. The typical values of frequencies along the receiver chain are given in the parentheses.

support direct sampling of the input signal at RF. Further the use of a sub-sampling mixer provides discrete time filtering and this improves the overall filtering of the receiver chain. The signal converted to baseband in quadrature by the mixer is fed to a phase ADC and then to a digital demodulator to obtain the digital outputs. As it can be seen in Figure 12.21, the synthesis involves only a chain of integer dividers to provide the various clocks required in the chain.

12.10.1 Frequency Synthesis: The Integer-*N* Approach

Instead of running the FBAR DCO at a fixed frequency as in [26], if some frequency tuning is enabled by adding a switchable capacitor array across the resonator, then let us assume that the center frequency of each channel (which can be arbitrary) in the required band can be expressed as,

$$f_{rf,ch,n} = (f_{fbar,o} - \Delta f_n) \cdot \left(1 + \frac{1}{P_n}\right), \tag{12.6}$$

where $f_{fbar,o}$ is the intrinsic FBAR DCO frequency, Δf_n is the frequency tuning on the FBAR DCO.

$$P_n = N_l, (N_l + 1), (N_l + 2) \ldots N_h, \quad \text{where } N_l, N_h \text{ are integers.} \tag{12.7}$$

With no tuning ($\Delta f_n = 0$), the biggest step size (occurs for the lowest integer) is given by,

$$f_{step} = f_{fbar,o} \cdot \left(\frac{1}{N_l} - \frac{1}{N_l + 1}\right) = \frac{f_{fbar,o}}{N_l \cdot (N_l + 1).} \tag{12.8}$$

The step size reduces as N_l increases but the value of N_h that can be tolerated depends on image reject pre-filter characteristic. In a similar scenario (but the channel

selection is done at IF) [26], N_l and N_h are chosen to be 15 and 30 with $f_{fbar,o}$ at 2.32 GHz.

To address any arbitrary frequency in the band of interest with integer division, there is a compulsive need for tuning the FBAR oscillator. The minimum tuning required depends on the biggest step size defined in equation (12.8). The minimum tuning required is decided by the relationship defined as,

$$(f_{fbar,o} - \Delta f_{min}) \cdot \left(1 + \frac{1}{N_l}\right) = f_{fbar,o} \cdot \left(1 + \frac{1}{N_l + 1}\right), \tag{12.9}$$

which when simplified results in,

$$\Delta f_{min} = \frac{f_{fbar,o}}{(N_l + 1)^2} = f_{step} \cdot \left(\frac{N_l}{N_l + 1}\right). \tag{12.10}$$

For nominal values of $f_{fbar,o}$ at 2.32 GHz and minimum value of 15 for N [26], the minimum tuning required is 9.06 MHz (0.4%). This is a reasonable requirement which can be achieved by adding a switched capacitor array across the FBAR in the DCO [27]. If N_h and N_l are the maximum and minimum integer division ratios respectively, then the range of frequencies that can be addressed by a single FBAR DCO and a set of integer dividers is given by,

$$(f_{fbar,o} - \Delta f_{min}) \cdot \left(1 + \frac{1}{N_h}\right) \leq f_{ch} \leq f_{fbar,o} \cdot \left(1 + \frac{1}{N_l}\right). \tag{12.11}$$

Similar to [26], N_h gets fixed by the pre-filter used for image rejection. For respective nominal values of N_l, N_h, $f_{fbar,o}$, and Δf_{min} at 15, 30, 2.32 GHz and 9.06 MHz, the range of frequencies that can be addressed is 86.7 MHz which is sufficient for covering the whole 2.4 GHz ISM band (80 MHz wide).

Sub-Sampling Clock Synthesis It is clear that with down-conversion by mixing in two steps, any arbitrary channel can be selected and down-converted to baseband. However, to preserve the frequency/phase-modulated information of the signal, there is a need for quadrature down-conversion to baseband. This requires generating quadrature either in the signal path or in the LO. By integer division, quadrature clocks can be generated only when the division ratio is even [28]. This additional constraint of even integer division results in the requirement of a higher tuning range on the FBAR DCO. To alleviate these issues, we choose a sub-sampling–based down-conversion approach for translating the filtered channel to baseband in quadrature. The critical anti-alias filtering needed to support this approach is readily provided by the FBAR channel selection filter.

If $f_{rf,ch,n}$ is the wanted channel frequency, it is selected by down-converting it to the peak frequency of the FBAR pseudo-lattice in the AMF cell. In other words,

$$f_{rf,ch,n} = f'_{fbar,f} + \frac{f'_{fbar,o}}{P_n}, \quad \text{with } P_n \text{ being an integer.} \tag{12.12}$$

In equation (12.12) $f'_{fbar,o}$ is the FBAR DCO frequency with frequency tuning and similarly $f'_{fbar,f}$ is the peak frequency of the AMF cell with tuning which are given by,

$$f'_{fbar,o} = f_{fbar,o} - \Delta f_o \quad \text{and} \quad f'_{fbar,f} = f_{fbar,f} - \Delta f_f. \tag{12.13}$$

If this filtered channel has to be down-converted (in two steps) to baseband in quadrature by sampling with differential clocks obtained by integer division of the FBAR DCO signal, then the initial sampling rate f_s can be shown to be given by [24],

$$f_s = \frac{f'_{fbar,o}}{m} = \frac{2f'_{fbar,f}}{2k-1}, \quad \text{with} \quad m, k = 1, 2, 3 \ldots . \tag{12.14}$$

It is clear from equation(12.14) that, the intrinsic anti-resonant frequencies of the FBARs used in the DCO ($f_{fbar,o}$) and in the filter ($f_{fbar,f}$) have to be different and the offset between these is at a minimum when $m = k$ in equation (12.14). Small offsets between the anti-resonant frequencies can be easily generated by depositing an oxide layer on the electrodes [29]. When the offset is minimum, the frequencies $f'_{fbar,o}$ and $f'_{fbar,f}$ are related as,

$$f'_{fbar,f} = \left(1 - \frac{1}{2m}\right) \cdot f'_{fbar,o}, \quad m = 1, 2, 3 \ldots . \tag{12.15}$$

Using equation (12.15) in equation (12.12), we get,

$$f_{rf,ch,n} = f'_{fbar,o} \cdot \left(1 + \frac{1}{P_n} - \frac{1}{2m}\right). \tag{12.16}$$

On the similar lines of the previous discussion, the minimum tuning required on the FBAR DCO ($\Delta f_{o,min}$) to address any arbitrary frequency in the band of interest is,

$$\Delta f_{o,min} = \frac{f_{fbar,o}}{(N_l+1)^2 - \frac{N_l \cdot (N_l+1)}{2m}}. \tag{12.17}$$

The tuning required (12.17) is similar to that in equation (12.10). For nominal values of $f_{fbar,o}$, N_l and m to be 2.4, 15 and 15 GHz respectively, the tuning required

is 9.68 MHz (0.4%) which is a feasible requirement [27]. Similarly from equation (12.15) the tuning (Δf_f) required in the AMF cell is given by

$$\Delta f_f = \left(1 - \frac{1}{2m}\right) \cdot \Delta f_o, \quad m = 1, 2, 3 \ldots . \tag{12.18}$$

Further, with minimum difference between the intrinsic anti-resonant frequencies of the resonators used in the DCO and in the AMF cell, the sampling rate in equation (12.14) can be simplified as,

$$f_s = 2 \cdot (f'_{fbar,o} - f'_{fbar,f}). \tag{12.19}$$

Taking nominal values for the intrinsic anti-resonant frequencies $f_{fbar,o}$ and $f_{fbar,f}$ at 2.4 GHz and 2.32 GHz respectively, the sampling rate is 160 MHz with $m = 15$. The range of frequencies that can be addressed with this approach is

$$f'_{fbar,o} \cdot \left(1 + \frac{1}{N_h} - \frac{1}{2m}\right) \leq f_{ch} \leq f_{fbar,o} \cdot \left(1 + \frac{1}{N_l} - \frac{1}{2m}\right). \tag{12.20}$$

Taking the minimum and maximum integer division ratios for the channel selection LO to be 15 and 30 respectively, the range of frequencies that can be addressed with the sub-sampling approach is 89.68 -MHz which exceeds the bandwidth of the 2.4 GHz ISM band.

12.10.2 FBAR-Based RF Front-End

The RF front-end comprises of an LNA and an AMF cell as shown in Figure 12.21. A current reuse topology with g_m boosting is used for the LNA [25]. The AMF cell (see Figure 12.27) also involves current reuse to facilitate low-power consumption. Before going into the details of this cell, we shall first have a look at the load of this cell, which is an FBAR-based pseudo-lattice.

FBAR -Based Pseudo-Lattice Network The FBAR impedance has a peak at DC (capacitive at DC) and the DC offset or flicker noise arising from the transconductance stage get amplified and this causes a concern when the wanted signal is brought down to DC by sampling as these unwanted DC components are still present at DC (by sampling). This problem is partly alleviated in [24] by discrete time filtering which provides null at DC to attenuate the unwanted components before the signal down-conversion. Further, the absence of ideal bandpass filtering increases the effective noise bandwidth and which in-turn increases the amount of noise folding owing to sampling-based down-conversion [30, 31].

An FBAR pseudo-lattice structure as in [25] can be used (see Figure 12.22) to circumvent the issues in the previous paragraph. The term *pseudo* is used as the structure involves both FBARs and capacitors and differs from the FBAR lattice structures used in [32], [33], where only FBARs in the form of a lattice are used to provide wide band

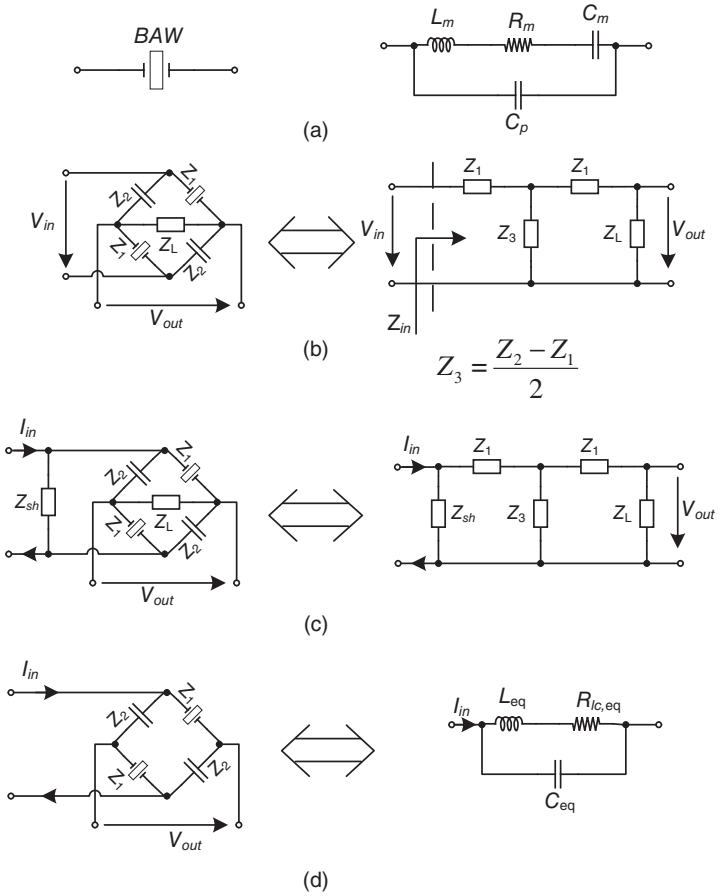

FIGURE 12.22 (a) FBAR equivalent model; FBAR-based lattice (b) with voltage input, (c) with current input. (d) The pseudo-lattice can be replaced by an LC equivalent with Q equal to that of the FBARs used in the lattice.

filtering. The pseudo-lattice comprises of two matched FBARs (Z_1) and two matched capacitances (Z_2) as shown.

The FBAR pseudo-lattice is not suitable for voltage inputs [25]. For a current input, the lattice provides a trans-impedance given by,

$$Z_{tran} = \frac{V_{out}}{I_{in}} = \frac{Z_L \cdot (Z_2 - Z_1)}{Z_1 + Z_2 + 2Z_L}, \text{with } Z_{sh} \to \infty. \tag{12.21}$$

The magnitude plot of the trans-impedance as given in equation (12.21) is shown in Figure 12.23. As it can be seen it results in an ideal bandpass response similar to the one with voltage input. However, the peak of the trans-impedance is at the anti-resonant frequency of the matched FBARs used in the pseudo-lattice and the

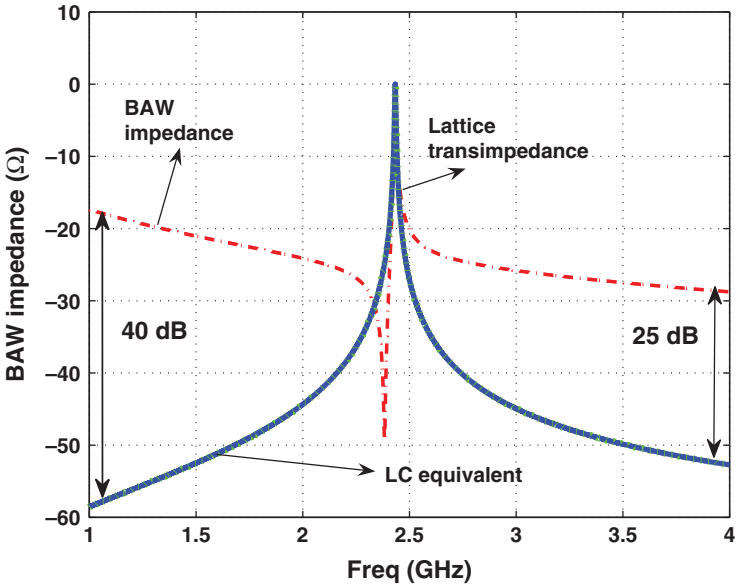

FIGURE 12.23 Normalized frequency plots of the FBAR impedance, trans-impedance of the FBAR pseudo-lattice. The pseudo-lattice significantly improves the rejection especially at far frequencies from the center frequency.

bandwidth of this filtering response is equal to that of the FBAR which depends on the Q of the resonator. It can be seen that the rejection provided by the FBAR pseudo-lattice is far superior compared to a single FBAR especially at frequencies far away from the center (peak) frequency. The FBAR pseudo-lattice can be modeled with an LC tank equivalent as shown in Figure 12.22 with the inductor L_{eq}, capacitor C_{eq}, and loss in the inductor $R_{lc,eq}$ given by

$$L_{eq} = L_m, \quad C_{eq} = \frac{1}{\omega_p^2 L_{eq}}, \quad \text{and} \quad R_{lc,eq} = R_m, \tag{12.22}$$

where ω_p is the anti-resonant frequency of the FBAR.

Bandwidth Tuning in the Lattice The intrinsic bandwidth of the lattice filter might not be sufficient for the targeted narrow-band standard. In [24], a solution is proposed to boost the Q of the FBAR by adding negative conductance across the resonator and without burning additional power. However in the lattice, two FBARs are used and compensation has to be provided to both the resonators to boost the Q and decrease the bandwidth. If a shunt impedance Z_{sh} is added in parallel with the current source as shown in Figure 12.22c, the trans-impedance is given by

$$Z_{tran} = \frac{Z_{sh} Z_L \cdot (Z_2 - Z_1)}{(Z_{sh} + Z_L) \cdot (Z_1 + Z_2) + 2 \cdot (Z_1 Z_2 + Z_{sh} Z_L)}. \tag{12.23}$$

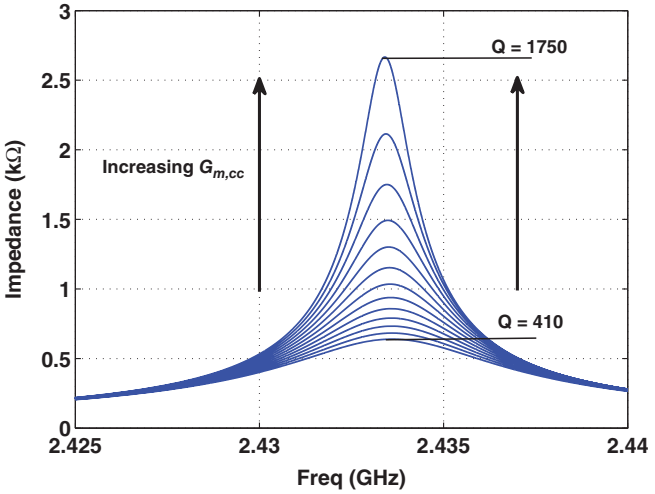

FIGURE 12.24 Q boosting of the FBAR pseudo-lattice by adding a negative conductance across it.

If Z_{sh} is a negative conductance $(-G_{m,cc}/2)$, then it can be shown that this negative conductance partially compensates for the losses in the resonators and thus boosts the Q of the filter and reduces its bandwidth. This phenomenon is similar to that in the Q-enhanced FBAR [24]. The bandwidth reduction and Q-boosting of the pseudo-lattice trans-impedance by adding a negative conductance is plotted in Figure 12.24. It is clear from the figure that the maximum impedance (impedance at the peak frequency) increases with the amount of compensation added. The critical conductance is the conductance which completely compensates for the losses in the resonators of the lattice and makes it to oscillate. This critical conductance is evaluated by equating the trans-admittance $(1/Z_{tran})$ to zero. In other words, equating the denominator of the expression in equation (12.23) to zero, we get

$$Z_{sh} = -\frac{Z_L \cdot (Z_1 + Z_2) + 2Z_1 Z_2}{Z_1 + Z_2 + 2Z_L} = -Z_{in}. \tag{12.24}$$

Without any load, it can be shown that the Z_{in} is given by $(Z_1 + Z_2)/2$. The peak of the trans-impedance (defined in equation (12.23) is at the anti-resonant frequency of the FBARs used in the lattice. The impedance of these resonators at the anti-resonant frequency is resistive [34] and is given by

$$R_p = (KQ_m)^2 \cdot R_m. \tag{12.25}$$

So, Z_{in} at ω_p becomes

$$Z_{in} \cong \frac{R_p}{2} - \frac{j}{2 \cdot \omega_p \cdot C_{ltc}}. \tag{12.26}$$

Owing to intrinsically high Q of the FBARsand large capacitance C_{ltc}, the imaginary part of Z_{in} in equation (12.26) is negligible compared to R_p and the critical transconductance $G_{m,cc,max}$ can be shown to be given by

$$G_{m,cc,max} \cong \frac{4}{R_p}. \tag{12.27}$$

This critical conductance is twice that in the case of compensating a single FBAR [24]. This is justified because in the case of the lattice, two FBARs are used and the losses in both the resonators need to be compensated which requires more (negative) conductance.

The bandwidths of the filtering responses for various levels of compensation ($G_{m,cc}$) are evaluated numerically and variation of the bandwidth with the negative shunt conductance is plotted in Figure 12.25. In the plot the negative conductance is normalized to the maximum conductance as defined in equation (12.27) and the bandwidth is normalized to the bandwidth of the lattice filter without any compensation added across it. As seen in the plot, the bandwidth varies linearly with the increase in the negative conductance and can be expressed mathematically as

$$f_{bw,eq} = f_{bw,max} \cdot (1 - g_{m,cc}), \tag{12.28}$$

where $g_{m,cc}$ is the normalized conductance and is given by

$$g_{m,cc} = \frac{G_{m,cc}}{G_{m,cc,max}} \cong \frac{G_{m,cc}R_p}{4}. \tag{12.29}$$

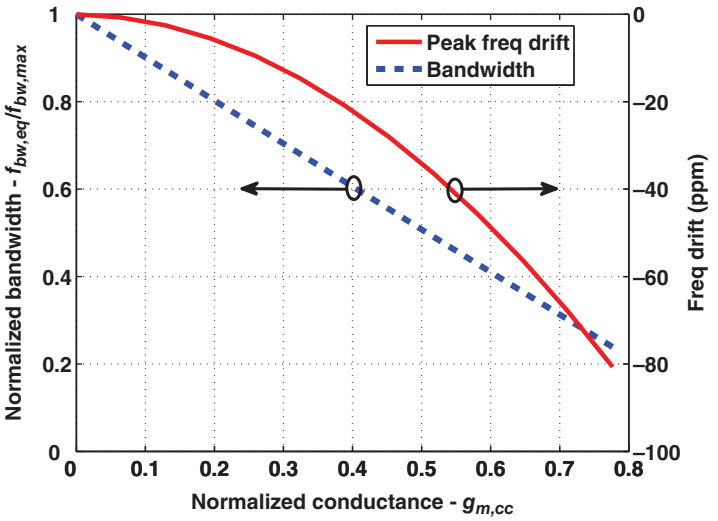

FIGURE 12.25 Bandwidth variation and the peak frequency drift with the addition of the negative conductance to boost the Q.

Adding negative conductance across the lattice not only reduces the bandwidth of the filter by boosting the Q, but also slightly drifts the peak frequency as seen in Figure 12.24. The variation of the peak frequency from the intrinsic anti-resonant frequency of the FBARs in the pseudo-lattice is plotted in Figure 12.25. The drift is very small compared to the anti-resonant frequency. For example, a bandwidth reduction by a factor of 2, the drift is around 50 ppm for an anti-resonant frequency of 2.433 GHz, which corresponds to a frequency drift of 120 kHz. This frequency drift owing to the shunt negative conductance becomes significant when the receiver is operated for very narrow-band standards where the channel bandwidth is a few hundred kHz.

Frequency Tuning in the Lattice The anti-resonant frequency of the FBAR can be tuned by adding a capacitance across it [24]. Similarly, adding a capacitance (Z_L) across the output terminals of the pseudo-lattice shifts the peak frequency of its trans-impedance. This can be observed from the expression for the trans-impedance in equation (12.23). By evaluating the peak frequency numerically (using the expression in equation (12.23) and taking $Z_L = 1/(j\omega C_L)$), the peak frequency tuning of the lattice is plotted in Figure 12.26. The peak frequency drift for a single FBAR is also shown in the plot. It can be seen that a certain amount of drift in the peak frequency of the pseudo-lattice requires approximately twice the capacitance required for drifting the peak frequency of a single FBAR by the same amount. The pseudo-lattice is a symmetrical structure, in that interchanging the FBARs with the capacitances and vice versa does not alter the performance of the lattice. So, addition of the load capacitance (Z_L) has similar impact on both the FBARs and on the capacitances. In other words, if the addition of capacitance C_L induces a capacitance ΔC in

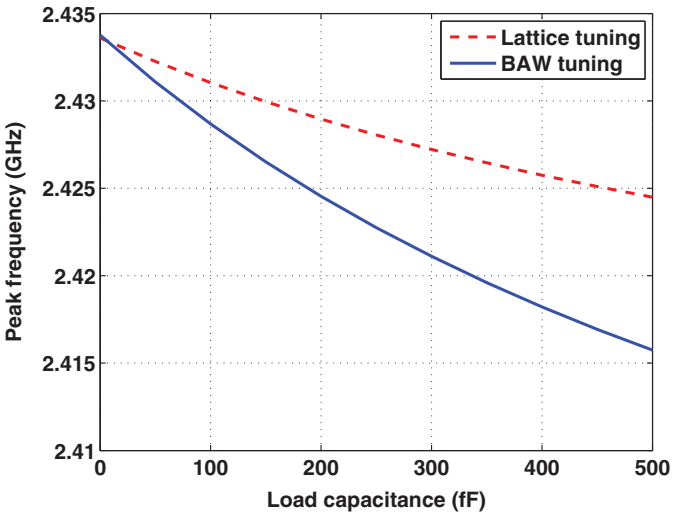

FIGURE 12.26 The peak frequency drift by adding capacitance for (a) single FBAR, (b) FBAR pseudo-lattice.

parallel with the FBARs, it induces a capacitance exactly equal to ΔC in parallel with the capacitors C_{ltc}. So at DC, the impedance of the FBARs and the capacitances in the pseudo-lattice is $(C_m + C_p + \Delta C)$ and thus results in an ideal bandpass response similar to that in an LC tank. As before, the inductance of the equivalent LC tank remains the same at L_m and the capacitance accounting for the frequency tuning can be empirically evaluated and can be expressed as

$$C_{eq,tune} \cong \frac{C_m \cdot (2C_p + C_L)}{2C_p + C_L + 2C_m}. \tag{12.30}$$

The AMF Cell The use of the FBARs in a pseudo-lattice structure significantly improves the selectivity compared to the use of a single resonator. However, this has to be complemented with a low-power transconductance stage which drives the pseudo-lattice so that the performance of the channel selection filter is highly efficient. In [24], a low-power solution called the AMF cell is proposed for the transconductance stage which employs current reuse to perform amplification, mixing, and Q-boosting of the FBAR used as the load. In this work too, the AMF cell is used but instead of a single FBAR, the FBAR pseudo-lattice is used. The AMF cell schematic is shown in Figure 12.27. It is a pseudo-differential structure with cascode transistors used for

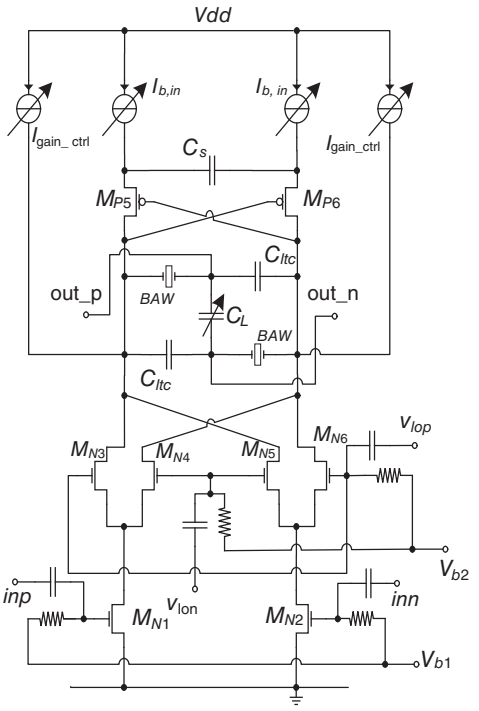

FIGURE 12.27 AMF cell with FBAR pseudo-lattice load: a low-power solution to perform channel selection and filtering at RF.

mixing. A CMFB structure (not shown) is used to set the DC voltage at the drains of the mixing transistors.

The input RF signal amplified by the LNA is fed to the AMF cell which performs channel selection and filtering. The input transistors $M_{N,1}$ and $M_{N,2}$ convert this to current (with transconductance $G_{m,in}$) which is then mixed with a low-frequency LO by the transistors $M_{N,3}$–$M_{N,6}$. This is then filtered by the FBAR pseudo-lattice placed at the drains of these mixing transistors. The Q-boosting of the lattice is provided by the PMOS cross-coupled pairs $M_{P,5}$ and $M_{P,6}$, with $G_{m,cc}$ being the transconductance of each of them. A switched capacitor array (C_L) which is digitally controlled is used as a load in the lattice to provide frequency tuning to the filter as shown in Figure 12.27. Capacitor C_s is added to ensure that the sources of the cross-coupled pair are at AC ground. To decouple the gain and the bandwidth settings, two parallel current sources (I_{gain_ctrl}) are added as in [24]. The mixing transistors are hard switched and the conversion gain of the AMF cell is given by

$$A_{conv} = \frac{2}{\pi} \cdot G_{m,in} \cdot |Z_{tran}|, \tag{12.31}$$

with $Z_{sh} = -G_{m,cc}/2$ in Z_{tran} as defined in equation (12.23).

Significance of the Capacitors C_{ltc} in the Lattice So far, we have seen that choosing two matched capacitances with a value of $C_{ltc} = C_m + C_p$, with C_m and C_p determined by the matched FBARs used in the pseudo-lattice, an ideal bandpass response similar to that of a high-Q LC tank is obtained. The term $(Z_2 - Z_1)$ in the numerator of the expression for the trans-impedance is the reason for a zero at the frequency where impedance of the FBAR Z_1 is equal to that of the capacitor $C_{ltc}(Z_2)$. At DC, these impedances are purely capacitive and equal to $(C_m + C_p)$. This is the reason for choosing a value of $(C_m + C_p)$ for the capacitances used in the pseudo-lattice and this results in a response similar to that in an LC tank with null at DC. If the capacitors C_{ltc} are tuned, then based on the impedance of these capacitors and the FBAR, a null appears at a particular frequency where all the impedances in the pseudo-lattice are exactly equal.

To better understand this phenomenon, consider the lattice network shown in Figure 12.28. When matched FBARs and matched capacitors are used, and without a load the input current divides into equal parts and flows through branches of the lattice as shown. So, the differential output voltage across the output terminals of the lattice is given by

$$V_{out} = \left(\frac{I_{in}}{2} \cdot Z_1 + V_X\right) - \left(\frac{I_{in}}{2} \cdot Z_2 + V_X\right) = \frac{I_{in}}{2} \cdot (Z_1 - Z_2). \tag{12.32}$$

It is evident from equation (12.32) that at the frequency where $Z_1 = Z_2$, the differential voltage is zero. The presence of a load does not affect this zero as already validated by the expression in equation (12.23). This property is attractive as it helps in rejecting out any strong interferer at any frequency which affects the performance

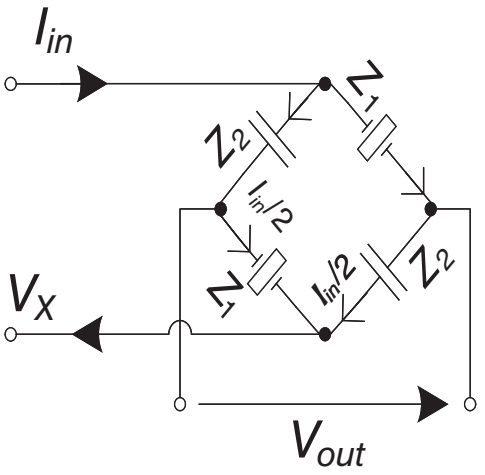

FIGURE 12.28 Significance of the capacitors C_{ltc} in the pseudo-lattice. By tuning these capacitors, the null can be positioned to reject any strong interferer.

of the receiver. This property can also be exploited to reduce the LO feedthrough arising from the mismatches in the mixing transistors. The flicker noise/DC offsets from the input pair and from the LNA preceding the AMF cell get up-converted to the frequency of the channel selection LO and can be rejected out by tuning appropriately the capacitance C_{ltc}. The simulated AMF cell response with different values of C_{ltc} is shown in Figure 12.29. It can be seen from this figure that, the peak of the

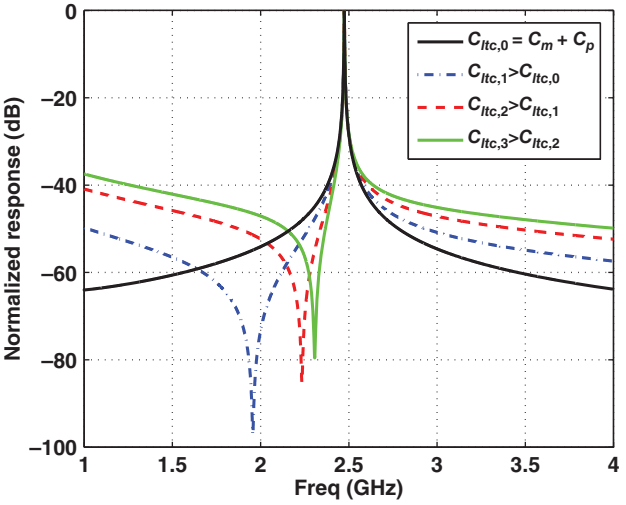

FIGURE 12.29 Simulated responses of the AMF cell with different values of C_{ltc}.

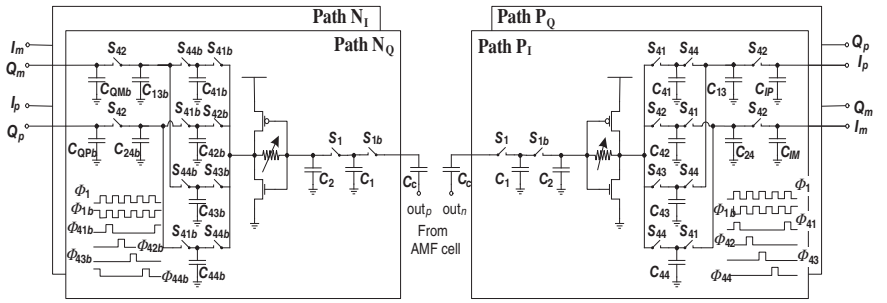

FIGURE 12.30 Quadrature two-stage sub-sampling down-conversion mixer. The second stage also provides discrete time filtering and decimates the sampling rate.

frequency response remains the same irrespective of the tuning of C_{ltc} and only the position of the null varies. This is an attractive property which allows rejecting out an strong unwanted signal without affecting the wanted signal.

12.10.3 Quadrature Sub-Sampling Mixer

The selected and filtered channel at the output of the AMF cell has to be down-converted to baseband in quadrature. Sampling the filtered signal at $f'_{fbar,f}$ by a clock with frequency of f_s as defined in equation (12.14) translates it to an intermediate frequency of $f_s/2$. This has to be further down-converted to baseband which requires the second stage of sampling. The two-stage sub-sampling mixer is shown in Figure 12.30. As seen, the differential outputs from the AMF cell are AC coupled to the sampling mixer. Four identical mixing circuits are placed, two on each side of the differential outputs of the AMF cell. This is done to make sure that the pseudo-lattice always sees a constant load on both the sides when either of the phases of the sampling clock ϕ_1 or ϕ_{1b} are high. To improve the overall conversion gain of the receiver, self-biased inverter-based amplifiers are placed between the two stages of the sub-sampling mixer as shown in the Figure 12.30.

The first stage of the sampling mixer has initial sampling switch clocked at a rate of f_s followed by another which removes the track component. The samples at $f_s/2$ are fed to the inverter-based amplifier and the small signal current is integrated on to the capacitors $C_{41(b)} - C_{44(b)}$ when the corresponding switches $S_{41(b)} - S_{44(b)}$ are turned on as shown in Figure 12.31. It is clear from Figure 12.30 that this integration is done periodically for a duration of $T_s/2$ which results in a windowed integration response (taking the bias resistance R_b to be large compared to the impedance of the capacitor C_{4x}) given by [35]

$$|H_{WI}(f)| = \frac{G_m}{2f_s C_{4x}} \cdot \left| \frac{sin(\pi f/2f_s)}{(\pi f/2f_s)} \right|. \tag{12.33}$$

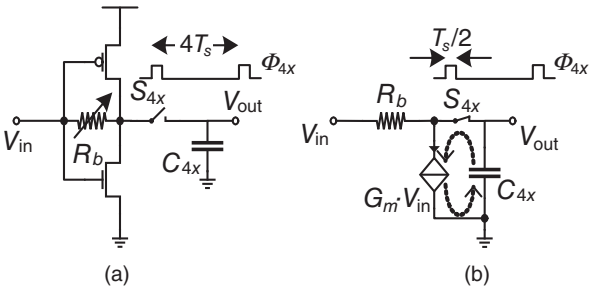

FIGURE 12.31 (a) Inverter-based IF amplifier, (b) small signal model – windowed integration.

The windowed integration results in a *sinc* response as shown in Figure 12.32. The response has nulls at all even multiples of f_s (resulting from the integration for a duration of $T_s/2$). This helps in reducing the amount of noise folding resulting from the second stage of sampling as in [35]. It is clear from the various phases of the clocks used, that the first sample from the initial sampling mixer is read out to the capacitor $C_{41(b)}$, second to $C_{42(b)}$, third to $C_{43(b)}$, fourth to $C_{44(b)}$, fifth again to capacitor $C_{41(b)}$, and so on. This periodically repeats and at the end of every cycle, the charges on capacitors $C_{41(b)}$, $C_{43(b)}$ are added and total charge is read out to capacitor $C_{13(b)}$. Similarly, capacitors $C_{42(b)}$ and $C_{44(b)}$ read out to capacitor $C_{24(b)}$. The charges from these capacitors are read out differentially as shown. To synchronize the reading out of the samples, a pair of switched capacitors driven by clock ϕ_{42} are added as shown. This way, out of 4 samples, a single sample is produced which results in re-sampling at a rate of $f_s/4$. So, this translates the channel at $f_s/2$ to baseband in quadrature. In this

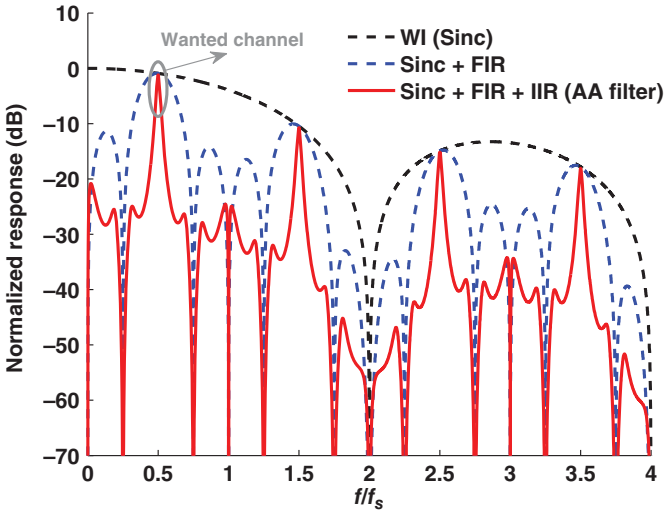

FIGURE 12.32 Filtering in the sub-sampling mixer.

process of the second down-conversion, the sampling mixer decimates the sampling rate which reduces the power consumed by the ADC. The adding of alternate samples and taking out a differential output results in an FIR response which is given by

$$H_{FIR}(z_1) = (1 + z_1^{-2}) - (z_1^{-1} + z_1^{-3}), \quad \text{with} \quad z_1 = e^{j2\pi f T_s}. \tag{12.34}$$

The capacitors in both the stages of the sampling mixer are not reset and the charge redistribution among the various capacitors in the mixer results in an IIR effect. It can be shown that the total IIR response is given by

$$|H_{iir}| = |H_{iir,1}||H_{iir,2}|, \tag{12.35}$$

$$\text{where,} \quad |H_{iir,1}(z_1)| = \frac{C_1}{C_2} \cdot \left| \frac{1}{1 - \alpha_1 \cdot z_1^{-1}} \right| \tag{12.36}$$

$$\text{and} \quad |H_{iir,2}(z)| = \frac{\alpha_2 C_a}{C_o} \left| \frac{1}{X(z)} \right| \quad \text{with,} \tag{12.37}$$

$$\begin{aligned} X(z) = M(z) \cdot (1 - \alpha_2\alpha_3 z^{-1} + \alpha_2^2 z^{-1} - z^{-1}) + \\ \alpha_2\alpha_3 \cdot ((M(z) + 1) \cdot (1 - \alpha_2) \cdot z^{-2} - z^{-1}), \end{aligned} \tag{12.38}$$

$$M(z) = \frac{1 - (1 - \alpha_3) \cdot z^{-1}}{1 - \alpha_3} \quad \text{and} \quad z = e^{j8\pi f T_s}. \tag{12.39}$$

The capacitor ratios are given by,

$$\begin{aligned} \alpha_1 &= \frac{C_2}{C_1 + C_2}, \quad \alpha_2 = \frac{C_{13(b)}}{2C_{41(b)} + C_{13(b)}} \quad \text{and} \\ \alpha_3 &= \frac{C_{13(b)}}{C_{13(b)} + C_{IP(QMb)}} = \frac{C_{24(b)}}{C_{24(b)} + C_{IM(QPb)}}. \end{aligned} \tag{12.40}$$

The second stage of the sampling mixer also requires an anti-alias filter as it re-samples at a rate of $f_{s,n} = f_s/4$. However, an interesting feature of the sampling mixer is that the second stage of the mixer has inherent anti-alias filtering functionality which prevents the unwanted signals from aliasing into the signal of interest. The windowed integration, the FIR filtering, and the IIR filtering combined together form the built-in anti-alias filtering for the second stage of the mixer, whose response is shown in Figure 12.32. As seen, the anti-alias filtering has nulls at every multiple of the new sampling rate $f_{s,n}$ except at those which are odd multiples of $f_s/2$ where the wanted signal is present. These nulls arising from the FIR filtering prevent the unwanted signals from aliasing into the signal of interest in the second stage of

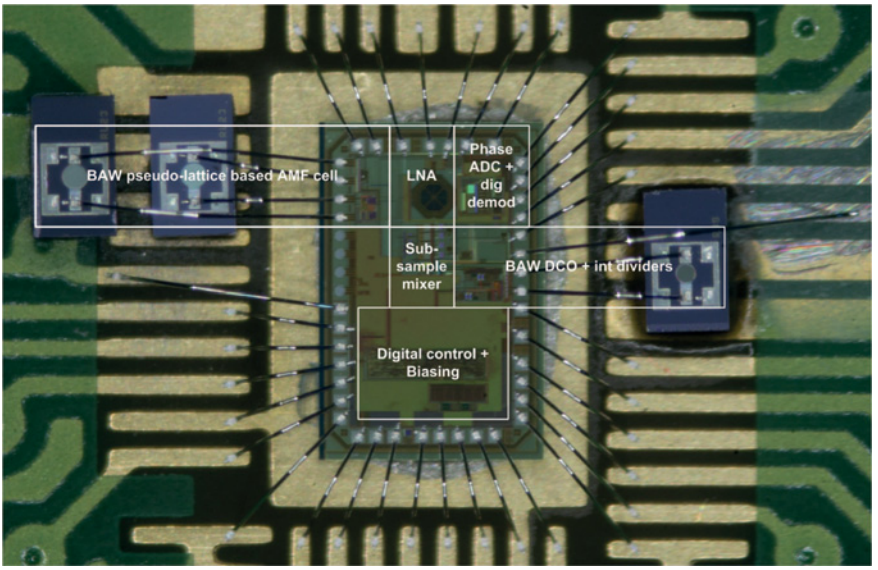

FIGURE 12.33 Chip microphotograph of the receiver. For a color version of this figure, see the color plate section.

the sampling mixer. However, it should be noted that these nulls are as a result of the differential output in the mixer and so reject only the signals at these frequencies and do not attenuate the noise.

This way the two-stage sub-sampling mixer down-converts the filtered channel to baseband in quadrature. The second stage provides discrete time filtering and feeds the down-converted samples to a phase Analog to Digital Converter (ADC) [36] at a decimated rate to reduce the power consumption of the ADC. A digital demodulator for Binary Frequency Shift Keying (BFSK) modulation scheme provides the demodulated bit out.

12.10.4 Receiver Measurement Results

The chip microphotograph of the multi-channel receiver is shown in Figure 12.33. The FBARs used for the channel filter (pseudo-lattice) and for the oscillator are wire bonded to the test chip. The complete receiver including the frequency synthesis consumes 5.94 mA current from a 1.8 V supply. The current breakdown is given in Table 12.2. The FBAR DCO without any additional capacitance (for tuning) works at 2.467 GHz and consumes 1.21 mA. A maximum tuning of 8.95 MHz is observed on the DCO and the current consumption for this maximum tuning is 1.74 mA. The FBAR DCO current consumption can be reduced when a complementary current reuse structure is used as in [37]. The AMF cell with the FBAR pseudo-lattice load peaks at 2.433 GHz with no additional tuning capacitance. The intrinsic Q of the FBARs used is around 400. This Q is boosted in the AMF cell to provide bandwidths down to 1 MHz ($Q = 2430$). The AMF cell consumes 1.08 mA with no

TABLE 12.2 Power consumption, $V_{DD} = 1.8$ V.

Block	Current (mA)
LNA	1.5
FBAR DCO	1.21
AMF cell	1.08
IF amplifier	4×0.1
Dividers, buffers, ADC, demodulator	1.75
Total	5.94

additional capacitance and for the maximum tuning it increases by 0.35 mA. The initial sampling rate is 68.5 MHz which is accordance with equation (12.19), while the decimated sampling rate is at 17.12 MHz.

Filtering in the Receiver The filtering responses (simulated and measured) of the AMF cell for various frequency tuning settings are shown in Figure 12.34. The maximum conversion gain of the RF front-end including the LNA and the AMF cell is 30.4 dB. The overall filtering response of the receiver including the AMF cell and the discrete time filtering is shown in Figure 12.35. A rejection of around 50 dB is measured at an offset of 15 MHz from the center frequency. The overall conversion gain of the receiver from RF to baseband is measured to be 46.2 dB.

Owing to the mismatches between the mixing transistors in the AMF cell, the large-amplitude, low-frequency channel selection clock feeds through to the output

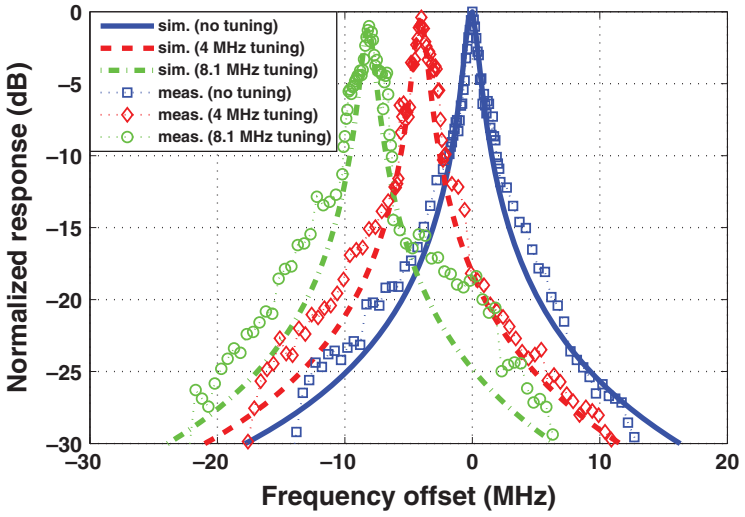

FIGURE 12.34 FBAR pseudo-lattice–based AMF cell filtering response with different tuning settings. A maximum tuning of 8.1 MHz is observed for the AMF cell. The plot is normalized to 30.4 dB which corresponds to the maximum gain with no tuning.

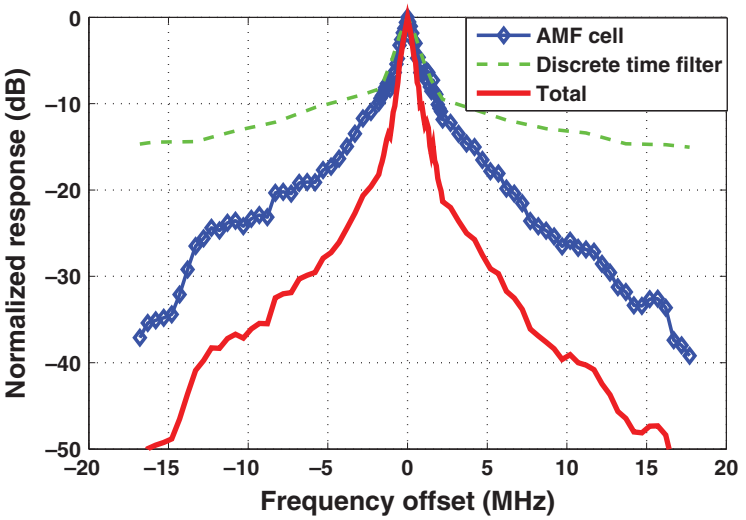

FIGURE 12.35 Overall measured response (normalized to 46.2 dB) of the receiver.

and appears close to the wanted signal after down-conversion by sub-sampling. It should be noted here that the DC offset or flicker noise from the LNA and from the input transistors of the AMF cell also get up-converted to the same frequency of the LO used for channel selection. As mentioned previously, this issue is solved by tuning the pseudo-lattice by the capacitances C_{ltc} so as to place the null at the required frequency. This attenuates the unwanted signal arising from LO feedthrough by 20 dB.

TABLE 12.3 Performance comparison.

Parameter	[38]	[39]	[40]	This work
Technology	130 nm CMOS	65 nm CMOS	65 nm CMOS	0.18 μm CMOS
Input frequency	2.4–2.48 GHz	2.4–2.7 GHz	1.8–2 GHz	2.5–2.63 GHz
Filter bandwidth	1 MHz	5/10/20 MHz	4 MHz	1–6 MHz
Maximum gain	—	30 dB	55.8 dB	46.2 dB
Noise figure	—	4.8 dB	2.8 dB	8.6 dB
Third Order Intercept (IIP3)	−15 dBm	−27 dBm	−8.4 dBm[a]	−38.7 dBm[b]
Sensitivity	−83 dBm[c]	—	—	−78 dBm[d]
Power Cons.	61.5 mW	77.6 mW	25.2 mW[e]	10.69 mW

[a] 10 MHz, 20 MHz.
[b] ±500 kHz.
[c] A bluetooth receiver, so the data rate is taken to be 1 Mbit/s.
[d] Data rate of 268 kbit/s.
[e] Does not include ADC and DBB.

12.11 SUMMARY OF THE FBAR-BASED RX

A novel way to perform channel selection and filtering at RF using FBARs has been presented herein. The FBAR pseudo-lattice filter limits the noise bandwidth which prevents noise folding, a major drawback in sampling receivers. The sub-sampling mixer provides discrete time filtering which complements the channel filter and improves the overall performance of the receiver. Employing current reuse in the LNA and in the AMF cell helps in achieving a low-power solution. A PLL-free approach for addressing multiple channels (arbitrary frequency) in the band of interest is presented. The use of integer dividers and sampling-based down-conversion helps in easy scalability to deep sub-micron processes.

12.12 CONCLUSION

MEM resonators (FBAR) prove superior to quartz crystals for building ULP WBAN systems owing to their fast wake-up which serves to reduce the energy overhead in the frequency synthesizer. In addition, they provide $high - Q$ band-pass filtering at RF which aids in channel selection. Combined with their very small size (form factor) as opposed to the bulky quartz crystals, they prove to be an ideal fit for implantable/wearable wireless sensor nodes.

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