11

Switched capacitor techniques

Capacitive transducer circuits which are built on conventional printed circuit boards can use standard analog design techniques, but designs for implementation on silicon are best done with switched capacitor circuits using analog discrete-time approaches, as accurate resistors are unavailable on silicon. MOS technology has become the most widely used silicon fabrication technique, suitable for large-scale digital circuits with 10^6 transistors as well as small application-specific ICs for mixed analog and digital functions. MOS transistors also make excellent switches, and switched capacitor implementations of analog circuits for capacitive sensors offer an excellent combination of accuracy, low production cost, and integration with digital and computer logic circuits. This chapter is an introduction to switched capacitor technology. For an in-depth treatment, read *Switched Capacitor Circuits* by Allen and Sánchez-Sinencio [1984].

11.1 ALTERNATE DESIGN TECHNIQUES

11.1.1 Digital signal processing

DSP (digital signal processing) techniques are becoming more popular as powerful DSP microcomputers are becoming available for low cost. With a DSP implementation, the low-level signal from the sensor electrodes is lowpass filtered, digitized to the required precision and at the required sampling rate, and input to a DSP computer for processing. The output digital stream is converted back to a continuous analog signal, if needed, with a DAC (digital-to-analog converter) and an output reconstruction filter. DSP techniques are accurate and capable of handling complex algorithms, but development time and power consumption are unfavorable, and more silicon area is usually needed.

If a local computer is needed for other purposes and has some unused cycles, the DSP method may be best. A very rough estimate of instructions-per-second compute power for capacitive sensor processing can be made:

- Assume the frequency response needed from the transducer is f_C
- Choose $10 f_C$ for the sensor clock f_S, except f_S should be greater than 10 kHz or so to keep capacitive reactances in a reasonable range
- Each half-cycle of f_S may need this processing:

1. interrupt
2. input sample value
3. demodulate by inverting alternate half cycles
4. filter by averaging both half-cycle values
5. output sample at f_S rate
6. return from interrupt

Assuming the desired computation precision is handled by a single CPU instruction, this calculation may require 20–30 instructions at a rate of $2f_S$. At 10 kHz, this is 0.4–0.6 MIPS (million instructions per second), well within the range of almost all processors. Adding other signal processing such as AGC or more complex filtering will double or triple the MIPS required.

DSP computers suited for this use are available from Analog Devices, ATT, Texas Instruments, and many other manufacturers, for prices starting at about $15. They handle 16 or 32 bit fixed point or floating point number crunching, and excel at the multiply-and-accumulate operations needed for digital signal processing. While a general purpose 8 bit microcomputer may be limited to 1–5 MIPS, DSP computers are 10–100 times faster and provide more precise math.

11.1.2 Charge coupled devices, bucket brigade devices

Other silicon implementations which can be considered are CCDs (charge coupled devices) and bucket brigade devices, but these can have a poor signal-to-noise ratio and are high volume solutions only, perhaps 1M units, as tooling expenses are high. Also, postfilter antialiasing requirements are more stringent as the sampling rate is closer to the maximum input frequency [Davis, 1979].

11.1.3 Packaged switched capacitor filters

Active filters built with switched capacitor circuits are available from several manufacturers. National's MF4, MF6, etc., are typical examples. They are packaged in 14–20 pin ICs and sell for less than $10. Their advantages are:

- Up to 12 pole filter complexity
- Input frequency range 0.1 Hz–100 kHz
- Frequency response proportional to clock frequency
- Frequency accuracy to ± 0.3% typ
- Dynamic range of 83 dB
- Low voltage, low current power requirements
- Gain accuracy ± 0.15%

These devices can build allpass, highpass, lowpass, bandpass, or band reject filters with manufacturer-selected or user-selected filter response choice. An advantage over continuous analog implementations is the ease and accuracy of tuning the response frequency by adjusting the clock. This is somewhat complicated by the necessity of providing an input antialias filter which will cover the range of clock tuning, but as the clock is usually 25 to 100 times the filter response frequency, the input antialias filter will be simple and may not need to be tuned. A disadvantage, common to all switched-capacitor circuits, is the limited frequency response. As the clock may be a high multiple of the maximum signal frequency, the signal is limited to the low hundreds of kHz.

Some of these devices are noisy compared to continuous-time realizations; this parameter should be checked carefully for sensitive applications.

11.2 COMPONENT ACCURACY

Capacitive sensor circuits use several types of components: operational amplifiers, switches, resistors, and capacitors. Of these components, the resistors and capacitors have the most effect on circuit accuracy, as amplifiers and CMOS switches are available which are quite accurate. With conventional PC board construction, accurate discrete components are available, but when converting a design to silicon, the designer must be aware of tolerance limitations. An *RC* circuit's frequency response varies as the product of two component types with poor absolute accuracy, while a switched capacitor filter with an accurate clock varies as the ratio of similar components, capacitors, so that absolute precision is unimportant and the ratio is controlled by very precise and repeatable photolithography. With silicon implementations, probably the worst case is for large value *RC* time constants which might be used in a low frequency active filter. As an example, for a 10 kHz filter, a resistor of 100 kΩ and a capacitor of 159 pF could be used. These two components would take up 500 mil^2 of silicon and have a tolerance of 50% and a temperature coefficient of almost 0.2%/°C. With a switched capacitor equivalent, the (ratio) tolerance improves by a factor of 500 to 0.1% and the temperature coefficient improves to better than 25 ppm/°C.

11.2.1 MOS vs. bipolar processes

Either MOS or bipolar processing can be used for capacitive sensor processing circuits. Bipolar processes produce superior high gain, high frequency bipolar transistors, while MOS (metal oxide semiconductors) processes make high input impedance transistors and very accurate switches. In general, for low power consumption and low frequency applications (below 1 MHz), MOS processes will be superior; for higher frequencies, bipolar transistors and g_m-C filters can be used. MOS (or JFET) transistors have considerably more $1/f$ noise than bipolar transistors which can be a negative factor for baseband systems, but capacitive sensors typically use an excitation frequency which is above the 2–20 kHz $1/f$ corner of low noise MOS transistors.

11.2.2 BiCMOS process

BiCMOS processes combine bipolar and CMOS transistors on the same chip, and have been developed for digital and memory applications, particularly to provide a low impedance, high current output buffer with small area. As the process moves into the mainstream, it has been adopted for improved analog circuit designs.

The most obvious improvement is the use of bipolar emitter-follower buffers for driving output pins or low impedance on-chip circuits. Bipolar transistors have a lower and more predictable voltage drop, smaller size, and higher bandwidth with capacitive loading.

The commonly used differential-cascode connection for operational amplifiers is improved if PMOS input transistors, contributing near-zero input current and lower $1/f$ noise than NMOS, are followed by a differential common-base bipolar n-p-n pair [Wooley, 1990]. A drawback for high impedance sensors is the increased size and increased parasitic capacitance of PMOS relative to NMOS transistors, so with an excitation frequency higher than the $1/f$ corner frequency of NMOS, NMOS may be preferred. Either polarity of MOS is preferable to bipolar for high slew rate and low input current, as input-stage bias current can be increased for MOS to increase input-stage slew rate (generally the limiting slew rate for the complete amplifier) without the accompanying penalty of higher input bias current found with bipolar transistors.

Other circuits which are improved with BiCMOS are reference voltages (band gap references) and temperature-dependent voltage generation using the well-known accurate temperature dependence of the forward voltage drop of similar diodes with dissimilar forward current. These circuits can be also built with a small performance degradation using standard CMOS processing, as the low gain, low frequency response parasitic bipolar substrate transistors can be pressed into service as diodes.

11.2.3 MOS vs. discrete component accuracy

Tables 11.1 and 11.2 compare the accuracy of MOS components with discrete components. The discrete devices were chosen to represent the highest available precision.

Table 11.1 Component accuracy, NMOS [Allen et al., p. 560; Colclaser, p. 237]

Component	Relative accuracy	Absolute accuracy	Voltage coef., ppm/V	Temp. coef., ppm/°C	Range of values
Poly-to-poly capacitor	0.1%	3%	−30	+25	0.15–0.2 pF/mil^2
MOS capacitor	0.1% (10 μm)	3%	−20	+25	0.25–0.3 pF/mil^2
Diffused resistor	2% (5 μm) 0.23% (50 μm)	±50%	−200	+1500	10±2 Ω/□
Polysilicon resistor	2% (5 μm)	±50%	--	+1500	60 Ω/□
Ion implanted resistor	2% (5 μm) 0.15% (50 μm)	--	−800	+400	500–20 kΩ/□
FET resistor	4%	±25%	Voltage dependent	--	10 k–100 kΩ

Table 11.2 Component accuracy, discrete [Mazda, pp. 12-19, 13-8; also various manufacturers' data sheets]

Component	Relative accuracy	Absolute accuracy	Voltage coef., ppm/V	Temp. coef., ppm/°C	Range of values
Resistor, carbon film	1%	1%	250	±500	1 Ω – 1 MΩ
Resistor, metal film	0.1%	0.1%	0	±5	10 Ω – 1 MΩ
Resistor, wire-wound, Cu/Ni	0.05%	0.05%	0	+20	1 Ω – 1 kΩ
Capacitor, mica	1%	1%	0	±60	1 pF – 0.02 μF
Capacitor, poly-styrene	2%	2%	0	−150 ±60	20 pF – 0.1 μF
Capacitor, npo ceramic	5%	5%	0	0 ±30	10 pF – 0.01 μF

11.3 SAMPLED SIGNALS

Generally switched capacitor circuits sample a continuous analog input signal at a constant high frequency. As capacitive sensors usually use a high frequency clock to excite the sense electrodes and the sensor output is a clock-frequency variable amplitude signal, when using switched capacitor circuits to demodulate capacitive sensors, the sensor clock is a natural choice for the switched capacitor clock. The sampling process is shown in the time domain (Figure 11.1).

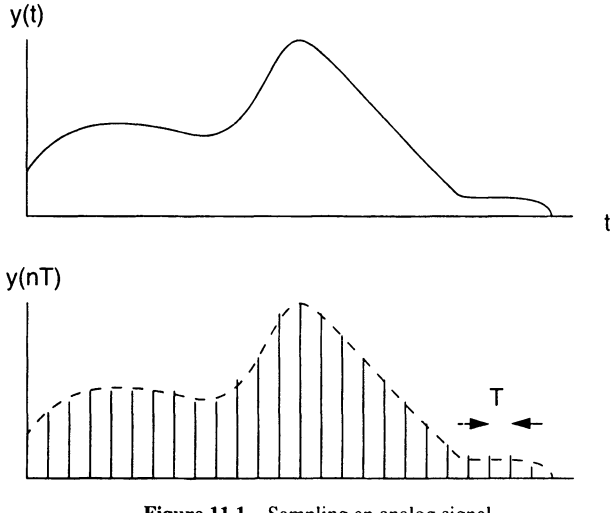


Figure 11.1 Sampling an analog signal

If the sampling frequency f_S (equal to $1/T$) is considerably higher than the maximum frequency of the analog input signal $y(t)$, say 4–10 times higher, the sampling process can be simply modeled as a delay of $T/2$ seconds without introducing serious errors. If, however, the input analog signal has frequency components which are higher than $f_S/2$, the signal cannot be completely recovered, and "aliasing" components are produced which may cause inaccuracies. This is the well-known sampling theorem, which is discussed in any book on digital signal processing [Bellanger, 1984, or Lynn et al., 1989]. Aliasing can be avoided by using a lowpass filter or a bandpass filter to remove high frequency input signals. These filters are also useful to remove unwanted interfering signals such as clocks which couple from other circuits in a system. Without attention, these clocks can alias down to low frequency signals which may be demodulated to a slowly varying signal offset.

If the sampling frequency is high compared to the maximum input frequency, classical AC analysis techniques will produce approximately correct results. If not, z-transform analysis should be used. The z transform is

$$Y(z) = \sum_{n=0}^{\infty} y(n) z^{-n} \tag{11.1}$$

A sampled input signal $y(n)$ is converted from an equation in time to an equation in the complex variable z.

The z transform is similar to the Fourier transform

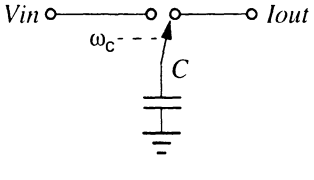
$$S(f) = \sum_{n=-\infty}^{\infty} y(n) e^{-j2\pi f n T} \tag{11.2}$$

If a z transform analysis of a system is available, the frequency response of the system to a periodic waveform can be determined by replacing z by $e^{j2\pi fT}$.

The z transform is an essential analysis tool for digital signal processing, and the texts cited above or other DSP texts can be consulted for more information.

11.4 FILTERS

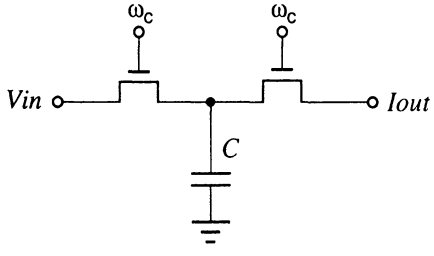
Switched capacitor filters substitute a switched capacitor



for a resistor. The input voltage, *Vin*, is sampled onto a small holding capacitor C during half of the square wave clock ω_c and discharged into a load impedance during the second

half of the clock. The current *Iout* will be proportional to $CVin \times \omega_c$, and the circuit behaves like a resistor of value $1/C$. Note that the clock waveform does not need to be square; some designers use a highly asymmetric rectangular clock waveform to simplify output reconstruction filters.

MOS transistors can substitute for the switch



Propagation delay is added in the drive circuits so that ω_c and $\overline{\omega}_c$ have a slight underlap to protect against both transistors being momentarily on at the same time, causing a large current spike.

11.4.1 Lowpass filter, *RC*

A simple lowpass filter section (Figure 11.2)

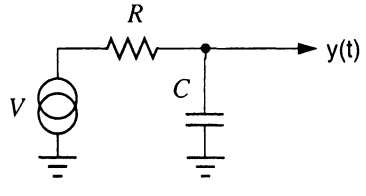
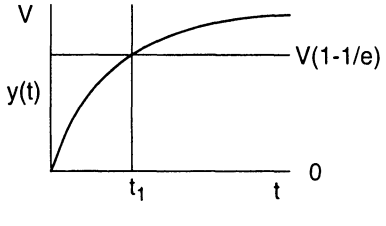


Figure 11.2 *RC* lowpass filter

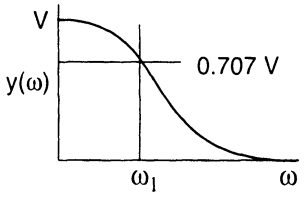
has the familiar exponential response vs. time, with a *V*-volt step input



$$y(t) = V\left(1 - e^{-\frac{t}{RC}}\right) \qquad 11.3$$

$$t_1 = \frac{1}{RC}$$

and its frequency response, with a V-volt frequency sweep input, is



$$|y(\omega)| = \frac{V}{|1 + j\omega RC} \tag{11.4}$$

$$\omega_1 = \frac{1}{RC}$$

11.4.2 Lowpass filter, switched capacitor

A switched capacitor equivalent of the RC lowpass filter is shown in Figure 11.3.

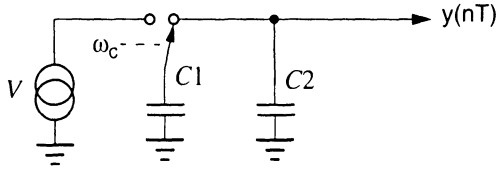
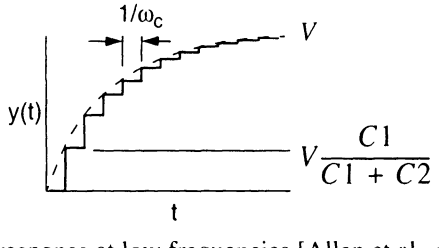
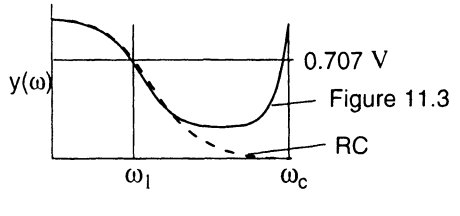


Figure 11.3 Switched capacitor lowpass filter

It has a similar exponential response vs. time



and a similar frequency response at low frequencies [Allen et al., p. 57]



$$|y(\omega)| = \frac{V}{\left[1 + 2\frac{C2}{C1}\left(1 + \frac{C2}{C1}\right)(1 - \cos\omega T)\right]^{1/2}} \tag{11.5}$$

$$\omega_1 = \frac{1}{T\left(1 + \dfrac{C2}{C1}\right)}$$

$$\omega_c = \frac{1}{T} \qquad 11.6$$

The switched capacitor lowpass filter can be designed to match the frequency response of the *RC* lowpass filter. Assume an *RC* filter with $\omega_1 = 20$ rad/s. First, a sampling frequency ω_c is chosen to be much larger than ω_1, say 5–25 times larger. We will use 500 rad/s. Then the values $C1$ and $C2$ are chosen so that

$$\frac{C2}{C1} = \frac{\omega_c}{\omega_1} - 1$$

which calculates as 3.98. The absolute value of $C1$ and $C2$ can be any convenient number for the chosen fabrication process. The accuracy of this method was verified by numerical methods and plotted in Figure 11.4.

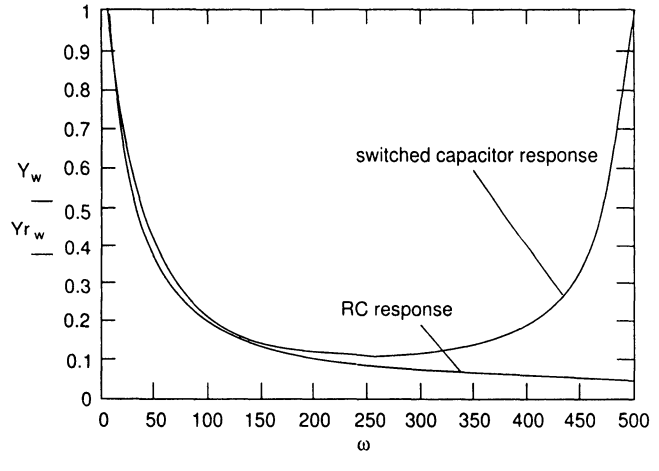


Figure 11.4 Comparison of switched capacitor lowpass to *RC* lowpass

This shows the expected good match at low frequencies and the poor performance when the input frequency approaches the sampling frequency. In most circuits, of course, an input lowpass (antialias) filter will be used and will reject frequencies above about 250 rad/s.

11.5 INTEGRATOR

Another circuit which works well with switched capacitor implementation is the integrator shown in Figure 11.5.

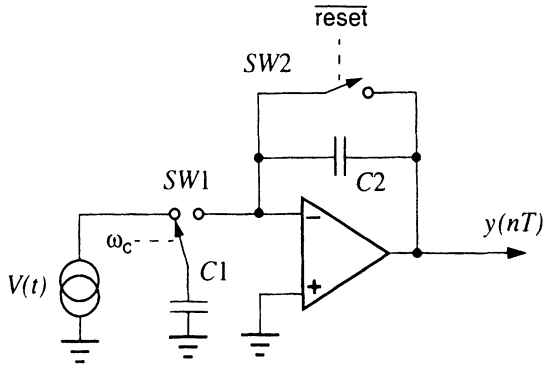


Figure 11.5 Switched capacitor integrator

Switch *SW2* is closed briefly at the beginning of the integration to discharge *C2*, then opened, and with each cycle of ω_c a charge packet equal to VC_1 is dumped into the inverting input of the amplifier. With a low-input-current amplifier, this charge is 100% transferred to *C2*. The voltage on *C2* is equal to the output voltage, and is

$$V_{C2} = \frac{Q}{C2} = \sum_{n=0}^{\infty} \frac{V_n \cdot C1}{C2} \qquad 11.7$$

V_n is the value of V at each sample time $1/\omega_c$. With a constant ω_c this circuit implements a sampled-data integrator with a gain of $C1/C2$.

11.6 INSTRUMENTATION AMPLIFIER

Switched capacitor circuits make a very effective instrumentation amplifier for converting differential signals with added DC into a single-ended signal [Allen et al., p. 81] (Figure 11.6).

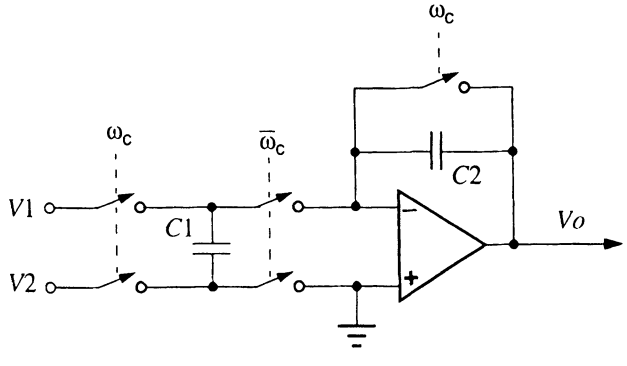


Figure 11.6 Switched capacitor instrumentation amplifier

During the first half-cycle of clock, the difference between input voltage $V1$ and $V2$ is impressed on $C1$ and $C2$ is zeroed. During the second half cycle, $C1$ is discharged into $C2$ which assumes a voltage

$$V_o = \frac{C1}{C2}(V1 - V2) \qquad 11.8$$

with a half-clock-cycle delay. V_o alternates with half-clock segments of 0 V, so a sample and hold circuit may be needed to remove the clock-frequency pulses. An advantage of this circuit over traditional discrete designs is that the common mode rejection is better; an integrated switched capacitor instrumentation amplifier is available from Linear Technology in a 16-pin package, the LTC1043, with a common mode rejection ratio of 120 dB and a maximum clock rate of 5 MHz.

Differential integrator

In the circuit above, if capacitor $C2$ is much larger than $C1$ and the switch which zeros $C2$ is turned on less frequently, the same circuit becomes a differential integrator. $C2$ is zeroed at the beginning of a measurement cycle, then $C1$ is switched many times to accumulate input voltage samples in $C2$. No output sample-and-hold function is needed with this use.

11.7 DEMODULATOR

The synchronous demodulator often used to demodulate a capacitive sensor which was shown in Chapter 4 (Figure 4.5) is repeated here (Figure 11.7). This demodulator can be integrated simply, using a switched capacitor circuit (Figure 11.8).

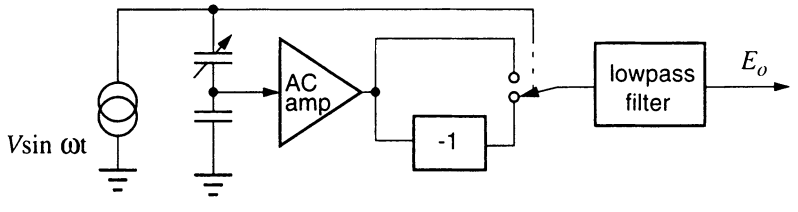


Figure 11.7 Synchronous demodulator

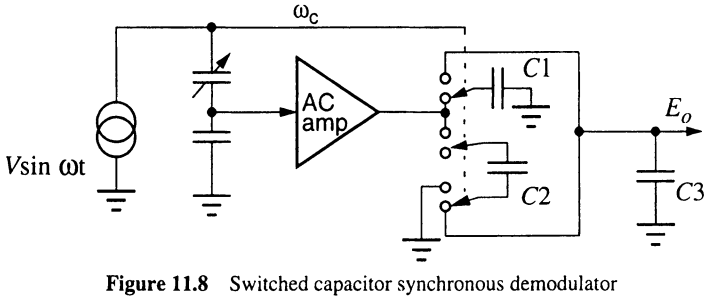


Figure 11.8 Switched capacitor synchronous demodulator

The gain is proportional to $C1/C3$ for positive half cycles of ω_c and proportional to $C2/C3$ for negative half cycles. Usually $C1 = C2$ and $C3 > C2$ to produce a lowpass response and the lowpass frequency is determined by $C3$ as above (Figure 11.3). E_o is a discontinuous-time baseband signal.

11.8 SWITCHED CAPACITOR CIRCUIT COMPONENTS

11.8.1 Switch

The lowpass switched capacitor circuit (Figure 11.3) works with an approximately square-wave clock, ω_c. When the switch is in the left position a charge $Q = C1 \times V$ is accumulated in $C1$. The switch then transfers most of the charge to the (usually) larger capacitor, $C2$. The first step size is $VC1/(C1+C2)$, and as $C2$ charges toward V, proportionately less charge is transferred to produce a decaying exponential.

As in all switched capacitor circuits, the accuracy of the switch is critical. ON resistance, Rds_{ON}, and injected charge, Q_I, are the most important parameters for integrated switches; with discrete MOS switches or packaged integrated switch arrays (CD4066 or DG401, as examples), the leakage current must also be considered.

The switch can be fabricated with small-geometry n-channel MOSFETs for integrated designs. Table 11.3 lists the circuit parameters when 5 μm silicon rules are used.

Table 11.3 Component parameters for switched capacitor lowpass

Component	Parameters	Performance
n-FET, silicon, 5 μm rules	Rds_{ON} = 2–10 kΩ Q_I = 0.05 pC I_S (off) = 0.2 pA	dv/dt = 0.02 V/s in hold circuit
FET switch, discrete, D444	Rds_{ON} = 85 Ω Q_I = 5 pC I_S (off) = 10 pA	dv/dt = 1 V/s in hold circuit
$C1$	1 pF	total charge = 5 pC @ 5 V
$C2$	10 pF	charge time @ 2000 Ω = 60 ns

A small-geometry integrated FET works well with the small capacitance values available on silicon. The ON resistance at 2 kΩ is low enough to charge the large 10 pF capacitor in less than 60 ns. Q_I, the injected charge, is the small packet of charge which is transferred to the negative supply with each switch transition and should be considerably less than the charge stored on $C1$ for good accuracy.

With the silicon FET the injected charge is 1% of $C1$'s charge. The discrete FET injected charge is equal to $C1$'s charge, so this FET would be hopelessly inaccurate when

used with this small capacitor. With a discrete capacitor in the 100–1000 pF range, however, the discrete switch is capable of good results.

11.8.2 Operational Amplifiers

The operational amplifier for silicon implementation may be a MOS type with the following equivalent circuit [Allen et al., pp. 691, 695] (Figure 11.9).

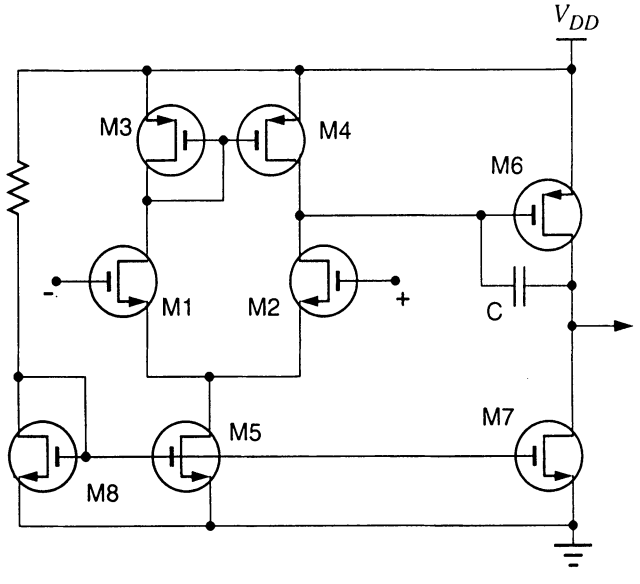


Figure 11.9 MOS amplifier equivalent circuit

The amplifier uses the standard differential-input amplifier, *M*1-*M*2-*M*5, which contributes high differential gain and low common mode gain. Its load is the high impedance Wilson current source *M*3 and *M*4, and *M*6 buffers and further amplifies the signal. The capacitor *C*, sometimes with a series resistor, shapes the amplifier response to a –6 dB/octave rolloff for stability, and the value of *C* is adjusted to the closed loop gain of the amplifier for best frequency response. The voltage gain *A*, if the input pair *M*1 and *M*2 are identical, is

$$A = \frac{g_{m2}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds6} + g_d}$$

$$g_m = \sqrt{2\mu C_{ox}(W/L)I_D} \qquad 11.9$$

$$g_{ds} = \lambda I_D$$

The transconductance g_m is a function of μ, the surface mobility of electrons or holes, C_{ox}, the gate oxide capacitance per unit area, and the FET's channel width *W* and length *L*. The channel conductance g_{ds} (the reciprocal of channel resistance) depends on λ, the channel length modulation factor determined by the particular CMOS process used, and the drain

current I_D. A SPICE analysis of this amplifier shows the characteristics listed in Table 11.4.

Table 11.4 MOS operational amplifier characteristics

Gain, Av	5000
*R*out	500 kΩ
Unity gain bandwidth	1 MHz
Phase margin, no load	75°
Input offset voltage	10 mV
Power consumption	2.5 mW
Power supply rejection ratio	82 dB
Common mode rejection ratio	80 dB
Slew rate with C_L = 10 pF	10 V/μs

To achieve this performance, the width-to-length ratios of the FETs are customized, from a small geometry 10/10 input FET to larger 100/10 (100 μm width, 10 μm length) output FETs. These characteristics are similar to packaged operational amplifiers, except the gain is considerably lower and the output resistance is considerably higher for the MOS implementation, but neither of these compromises causes too much trouble with integrated switched capacitor circuits. DC gain is not critical in circuits where the signal is modulated on a 20 kHz carrier, and the gain at 20 kHz is limited to 50× by the 6 dB/octave compensation and the unity gain bandwidth. The high value of output resistance for the MOS circuit, 500 kΩ, would be awkward in a packaged amplifier, but the amplifier is typically driving very high impedances if it is used on-chip; an amplifier which drives signals off-chip would need an additional buffer for lower output impedance.

Bi-MOSFET amplifier

A low noise, low input capacitance integrated amplifier can be built with bipolar-MOS processes, using MOS input stages and bipolar outputs. This combination gives high input impedance, near-zero current noise, and low output impedance for driving low impedance loads, capacitive loads, or driving off-chip. A bi-MOS amplifier designed for biological probes [Takahashi et al., 1994] was optimized for high input impedance and low input capacitance; it is described in this paragraph.

MOSFETs are noisier than bipolar transistors or JFETs, but input-referred noise voltages of 15 nV/$\sqrt{\text{Hz}}$ can be achieved with p-channel FETs and current noise is very low. Current noise is normally a problem only when a MOSFET input needs to be brought out to a bonding pad; the usual diode protection for electrostatic discharge can contribute much higher current noise than the amplifier. The Bi-MOS amplifier uses a p-channel MOSFET input differential amplifier, a p-MOS second stage, and a Darlington bipolar output stage. The design challenge is to achieve low noise with low input capacitance.

For the BiFET amplifier input circuit transistors, transconductance and midband noise decrease by *W/L* while capacitance is minimized by reducing *WL*, so a high *W/L* ratio of 50 is chosen. A capacitance of 6 pF and a spot noise of 38 nV/$\sqrt{\text{Hz}}$ is achieved well into the $1/f$ region at 280 Hz. Additional information on FET noise is found in Section 12.1.2.

11.9 ACCURACY

11.9.1 Capacitor ratios

Switched capacitor circuits have two very favorable characteristics for silicon implementations. The gain, for most circuits, is proportional to the ratio of capacitors. Capacitor ratios are the most stable parameter available on an integrated circuit, as seen in Table 11.1, and rival the stability of *RC* products available in precision discrete components.

11.9.2 Amplifier accuracy

Amplifier input offset voltage accuracy can be excellent, contributing at worst a few mV of DC offset. Most sensitive capacitive sensor circuits amplify the signal while it is modulated on the carrier frequency, so the DC offset is unimportant except at the final demodulator stage. For integrated amplifiers as above, the relatively low gain compared to packaged ICs may contribute to small changes in gage factor and imperfect cancellation of stray capacitance for guard circuits.

11.9.3 Parasitics

The MOS capacitor uses SiO_2, glass, as a dielectric. This is one of the most stable and least lossy dielectrics available. Parasitic capacitors are formed, however, with the typical MOS capacitor construction.

The silicon oxide isolation and passivation layer forms the dielectric for the MOS capacitor. Isolation from the substrate is done with the usual n^+ diffusion, forming a reverse biased diode and also acting as a reasonably low-resistivity bottom plate. The top plate is the aluminum interconnect metallization. Both top and bottom plates will add a small parasitic capacitance, C_T and C_B, to the capacitor C (Figure 11.10).

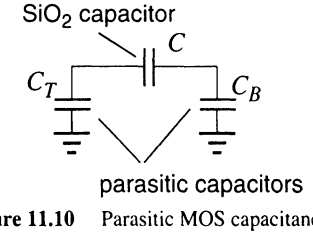


Figure 11.10 Parasitic MOS capacitances

The effect of these capacitors is usually to just slightly increase another circuit capacitor value. Suppose, for example, C_T and C_B are considered in the demodulation circuit above (Figure 11.8). Considering $C1$, C_B is shorted and C_T simply adds to $C1$. For $C2$, C_T is charged by the amplifier but does not contribute to the output, while C_B adds to $C3$. For $C3$, C_T adds its capacitance and C_B is shorted and does not contribute to the output. If

the MOS capacitor value is adjusted downward by a few percent to compensate for the parasitics; no other circuit effects will be seen. C_B's value ranges from 5–20% of the total [Allen et al., p. 397], while C_T is between 0.1 and 1%.

11.9.4 Charge injection

A small packet of charge is injected into a MOS switch with each clock edge. It is caused by small voltage-dependent parasitic capacitances from gate to source and drain electrodes, and varies from 5 pC for discrete circuits to 0.005–0.05 pC for small-geometry IC switches, as shown in Table 11.3. Uncompensated charge injection can be a serious source of error; for ICs, sample and hold errors in the range of 5–50 mV are typical. The amount of charge injection usually increases as switching speed increases, and also varies with the DC bias point. Several techniques can be used to minimize this charge. A simulation of charge-injection errors in a D/A converter using a variety of circuit techniques to minimize and compensate for injection errors [Willingham et al., 1990] shows an improvement of about 500×. Actual circuits will not achieve this level of performance, but the simulation shows that performance is limited by component tolerance and not by systematic design flaws.

Dummy switches

A dummy switch can be connected in a way that injects an equal and opposite quantity of charge. A simple circuit with C_S representing the signal input port and C_L the output shows the effects of charge injection. An unwanted voltage step is seen at the output (Figure 11.11).

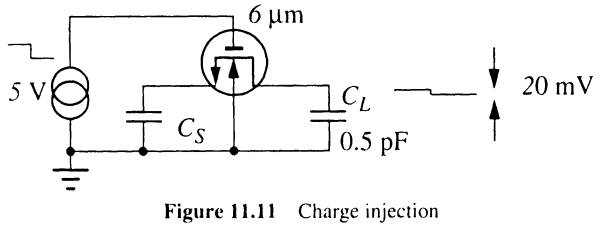


Figure 11.11 Charge injection

With typical 3 µm self-aligned p-well n-channel FETs, the injected charge at a DC level of 2.5 V is 0.01 pC which causes a voltage step (from $Q = CV$) of 20 mV in a 0.5 pF capacitor. If an inverted clock is used to drive a half-sized dummy transistor (Figure 11.12)

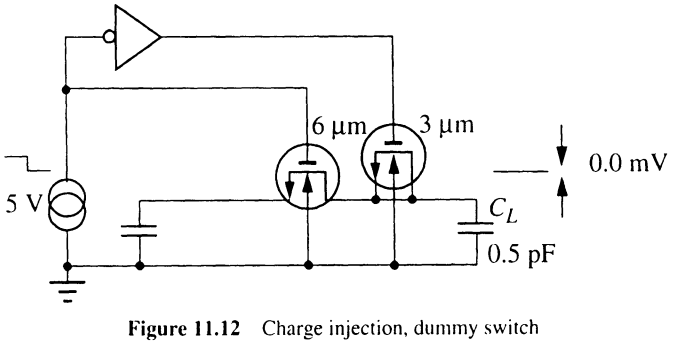


Figure 11.12 Charge injection, dummy switch

the injected charge can, in theory, be exactly nulled. A 3 μm wide transistor with an inverted drive for charge injection compensation is used in parallel with the 6 μm working switch in Figure 11.11. With the normal symmetric transistor, the gate-to-drain capacitance is the same as the gate-to-source capacitance, and only the gate-to-drain capacitance of the working switch contributes to charge injection if the source C_S is respectably low impedance, hence the 2:1 ratio. But two effects mitigate the success of this effort: if clock rise and fall times are slow or if the logic inverter has finite delay, half-size transistors (or, more accurately, half width-to-length-ratio transistors) are not optimal; the size can be adjusted to be somewhat smaller for improved performance. Also, as the parasitic capacitors are voltage-dependent, the exact ratio also depends on the threshold voltage [Eichenberger, 1990] and should also be adjusted to the signal input voltage. With a large input signal swing, all factors cannot be accommodated at once.

Subtraction

Another method [Martin, 1982] can null charge injection more accurately by subtraction in circuits where an operational amplifier is used. The integrator in Figure 11.5 is redrawn with individual MOS switches in Figure 11.13.

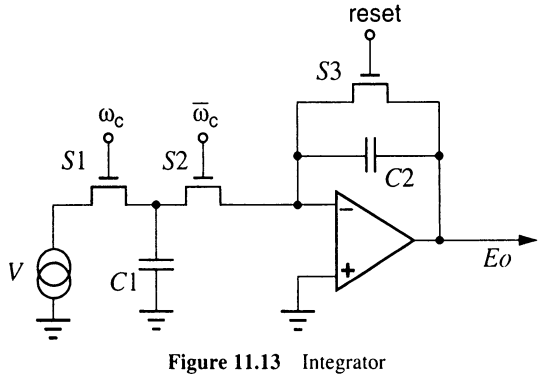


Figure 11.13 Integrator

Transistor *S*1 will pull some charge from *C*1 when it is shut off, and transistor *S*2 will inject charge into *C*1 and *C*2. These effects can be compensated with a similar circuit feeding the noninverting input, as shown in Figure 11.14 on page 193.

11.10 BALANCED DIFFERENTIAL-INPUT DEMODULATOR

A balanced circuit which features:

- Linearization of 1/spacing dependence
- Reference capacitors to compensate environmental effects
- Differential processing to minimize charge injection

has been described [Schnatz et al., 1992] for use with a pressure transducer, but it demonstrates excellent techniques for accurate switched-capacitor demodulation for any type of

sensor. The transducer described has a measured nonlinearity of less than 0.4% from pressure input to voltage output. Its block diagram is shown in Figure 11.15.

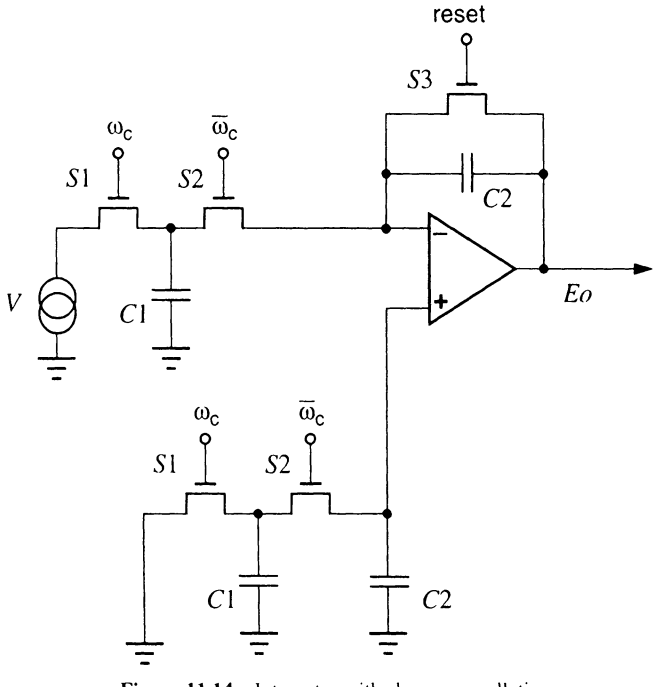


Figure 11.14 Integrator with charge cancellation

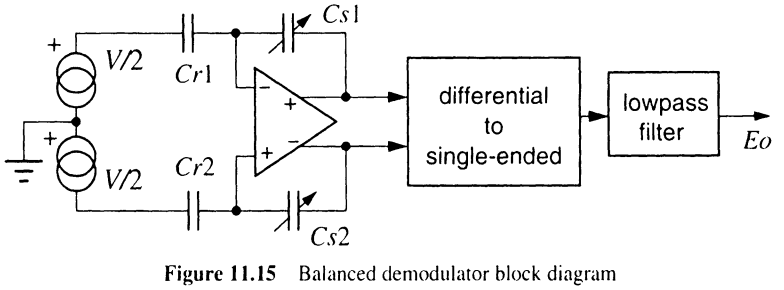


Figure 11.15 Balanced demodulator block diagram

The sense capacitor is divided into two equal capacitors, $Cs1$ and $Cs2$, and a reference capacitor Cr in close physical proximity is divided into two equal capacitors, $Cr1$ and $Cr2$. The output voltage is

$$E_o = V \cdot \frac{Cr}{Cs}$$

which is linear for spacing-variable capacitors; if Cs is an area-variable capacitor, its position can be interchanged with Cr. The circuits are implemented using switched capacitor techniques (Figure 11.16).

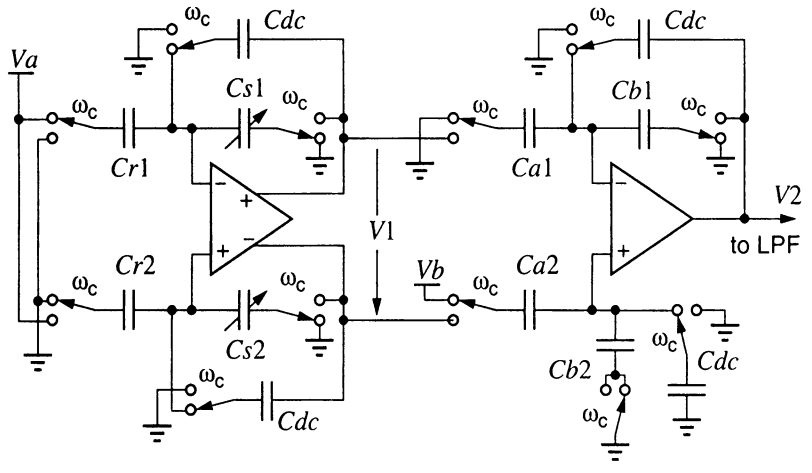


Figure 11.16 Balanced demodulator circuit

All switches are shown in the $\omega_c = 1$ position. The first stage produces a differential DC output voltage with amplitude proportional to the plate spacing. With $\omega_c = 1$, *Cr*1 is charged to *Va*, *Cs*1 is discharged, and *Cdc* holds the previous output voltage sample; *Cr*2, etc., do the same with negative polarity. When ω_c switches to 0, *Cr*1's charge is transferred to *Cs*1 and *Cdc* is charged to the output voltage. The exact value of *Cdc* is unimportant, except it must be large enough to handle worst case leakage currents without excessive droop and small enough to charge fully in one cycle of clock. The amplifier output takes the value $V1 = -2VaCr/Cs$; uncompensated voltage drops, interfering signals, charge injection, and leakage current effects appear as a common mode voltage. Appropriate small delays must be added to the ω_c signals to avoid simultaneous conduction.

The following stage is the switched capacitor version of the standard four-resistor instrumentation amplifier; its common mode rejection is equal to the matching of the capacitor ratios and can be 40 dB with careful processing. This stage cancels the unwanted common mode voltage component of *V*1 and adds an adjustable DC offset, *Vb*, if needed. *Ca*1 and *Ca*2 are nominally equal, as are *Cb*1 and *Cb*2; the dummy switch connected to *Cb*2 compensates for the charge injected by the switch connected to *Cb*1. If the amplifier is to produce an output centered around a displaced value, *Vb* is adjusted appropriately; otherwise *Vb* can be zero. This stage can also add gain as needed to establish the gage factor; its gain is *Ca/Cb*. The overall transfer function is

$$V2 = \frac{Ca}{Cb}\left(2Va\frac{Cr}{Cs} - Vb\right) \qquad 11.10$$

11.11 ALTERNATE BALANCED DEMODULATOR

Using the instrumentation amplifier above (Figure 11.6) and simplifying the input stage, a simplified balanced demodulator is as shown in Figure 11.17.

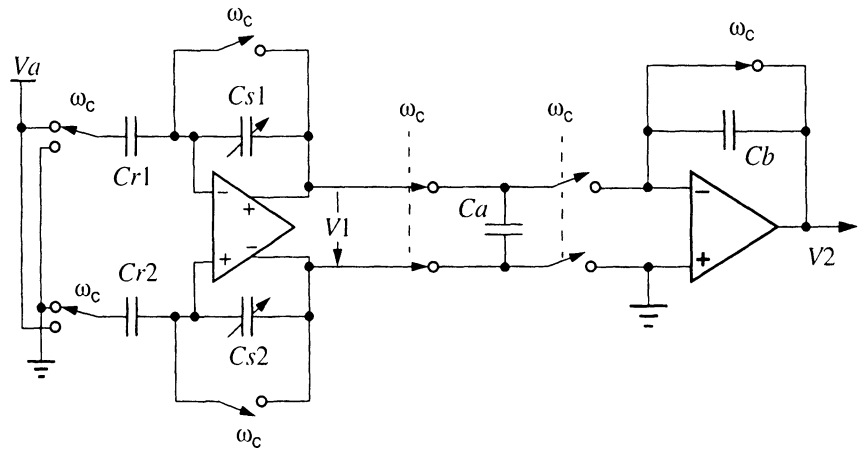


Figure 11.17 Alternate balanced demodulator

Again, all switches are shown in the $\omega_c = 1$ position. The first stage output $V1$ is an amplitude-modulated square wave rather than the discrete-time analog signal shown in Figure 11.16. The variable capacitors $Cs1$ and $Cs2$ are shorted with $\omega_c = 0$, and with $\omega_c = 1$ the fixed charge impressed upon the reference capacitors $Cr1$ and $Cr2$ is transferred to $Cs1$ and $Cs2$. $V1$ is picked up by Ca when $\omega_c = 1$ and its charge is transferred to Cb with $\omega_c = 0$ to complete the balanced-to-single-ended conversion. The common-mode rejection of this circuit is excellent as it is not dependent on component matching. The $Ca - Cb$ circuit will need charge injection compensation for maximum accuracy as shown in Figure 11.12, and the square wave output can be converted to DC with a sample and hold, a low-pass filter, or the same Cdc switching shown in Figure 11.16. This circuit will need more power to bias the operational amplifiers, as higher slew rate is needed than the previous circuit to handle the square wave output signals. The overall circuit gain is

$$V2 = -\frac{Ca}{Cb}\left(2Va\frac{Cr}{Cs}\right) \qquad 11.11$$