Unleash Innovation

N5 tsmc Chip Integration Checker (tCIC) User Guide

v1.1_0_2a

DTP/TSMC

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- The tCIC/user-guide are used to support Top designer to check guideline rules in APR phase to prevent DRC violations when doing chip-integration
- The tCIC/user-guide are valid for the following assumptions:
  - Process-Milestone-Library: N5 v1.1
  - TSMC POR SRAM: N5 v1.1
  - DRM version: T-N05-CL-DR-014 v1.1
- Please note that the tCIC/user-guide represent a “diagram-in-time” and are subject to change if any of the above assumptions are modified
- For any questions regarding this tCIC/user-guide, please contact your TSMC technical support person

Guideline Content Update History

tCIC Version	Release Date	Corresponding Guideline Version	Update History
v0.5_0_1a	09/06/2019	v0.5_0_1	1. First Release 2. Copy from N5 v1.0_0_2a tCIC package
v0.9_0_1a	12/13/2019	v0.9_0_1	1. Support Boundary Controlled H280P57 APR Block 2. Add H280P57 BC APR block relate rules : DBLK.H210P51.EN.4.1.5:FG112, DBLK.H210P51.EN.4.2.4:FG112, DBLK.H210P51.S.4.1.3, DBLK.H210P51.S.4.2.3, DBLK.EN.4.1.5:ALP76, DBLK.EN.4.2.4:ALP76, DBLK.H280P57.EN.4.1.5:NOBC, DBLK.H280P57.EN.4.1.5:BC, DBLK.H280P57.EN.4.2.4:NOBC. DBLK.H280P57.EN.4.2.4:BC, DBLK.H280P57.S.4.1.3, DBLK.H280P57.S.4.2.3, DBLK.S.7.1.1, DBLK.S.7.2.1, DBLK.S.9.1.6, DBLK.S.9.1.7, DBLK.S.9.1.8, DBLK.S.9.1.9, DBLK.S.9.2.6, DBLK.S.9.2.7, DBLK.S.9.2.8, DBLK.S.9.2.9, DBLK.H280P57.R.8.3 3. Update spec of TOP.EN.4.1.4, 4. Remove DBLK.H210P51.EN.1.2:ALP76 5. Separate :NOBC and :BC guideline on DBLK.*.EN.4.1*, DBLK.*.EN.4.2* 6. Separate :NOBC and :BC guideline on DBLK.H280P57*.W.* 7. Update DBLK.H280P57.S.3.1.1 DBLK.H280P57.S.3.2.1, DBLK.S.8.1, DBLK.S.8.1.3, DBLK.8.2, DBLK.8.2.4, DBLK.S.8.2.5 guidelines for v0.9 FP type SRAM design 8. Add LUP.R.1* related rules

Guideline Content Update History

tCIC Version	Release Date	Corresponding Guideline Version	Update History
v0.9_0_2a	06/12/2020	v0.9_0_2	1. Update spec of DBLK.H210P51.S.3.2.2, DBLK.H210P51.S.3.2.3, DBLK.H280P57.S.3.2.1 2. Update spec of DBLK.R.3.2, DBLK.H280P57.R.3.1, DBLK.H280P57.R.3.3, DBLK.H280P57.R.3.4, DBLK.R.9, DBLK.H280P57.R.9.1, DBLK.H280P57.R.9.2, DBLK.H280P57.R.9.3 3. Add DBLK.H210P51.R.8.1:BC, DBLK.H210P51.R.8.2:BC, DBLK.H280P57.R.8.1:BC, DBLK.H280P57.R.8.2:BC, DBLK.H210P51.R.5, DBLK.H280P57.R.5 4. Rename DBLK.H280P57.S.3_Forbidden to DBLK.H280P57.EN.3 5. Add DBLK.S.8.2.6 / DBLK.RBLK.EN.3.1.1.M2, DBLK.RBLK.EN.3.2.1.M2, DBLK.H210P51.S.3.2.2, DBLK.R.7.1.2 6. Update spec of DBLK.H210P51.S.3.2.2, DBLK.R.7.1.1, DBLK.R.7.1.2
v1.1_0_1a	08/14/2020	v1.1_0_1	1. Add eFuse related guidelines

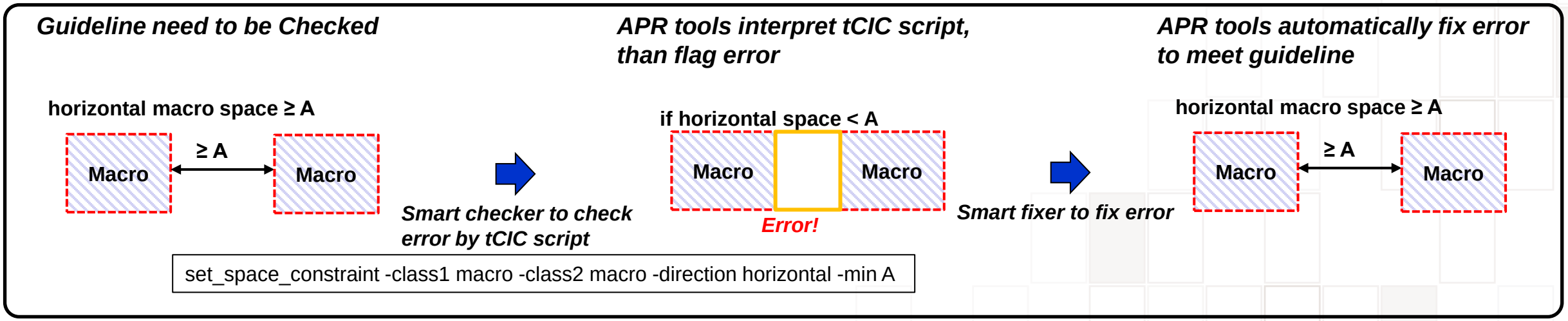
Guideline Content Update History

tCIC Version	Release Date	Corresponding Guideline Version	Update History
v1.1_0_2a	12/25/2020	v1.1_0_2	1. Relax Pin/Track Alignment block for non-BC APR Blocks, update DBLK.H210P51.W.1.1:FG28_ALP76, DBLK.H210P51.W.2.1:FG28_ALP76, DBLK.H210P51.W.3.1:FG28_ALP76, DBLK.H210P51.EN.4.1:FG28_ALP76, DBLK.H210P51.W.1.1:FG112_ALP76, DBLK.H210P51.W.2.1:FG112_ALP76, DBLK.H210P51.W.3.1:FG112_ALP76, DBLK.H210P51.EN.4.1:FG112_ALP76, DBLK.H210P51.EN.4.1.1:FG112_ALP76, DBLK.H280P57.W.1.1:ALP76, DBLK.H280P57.W.2.1:ALP76, DBLK.H280P57.W.3.1:ALP76, DBLK.H280P57.EN.4.1.4:ALP76 2. Tighten BC block location, update DBLK.H210P51.EN.4.1.2:BC, DBLK.H210P51.EN.4.1.3:FG112_BC 3. Update DBLK.R.9.1, DBLK.H280P57.R.9.1, DBLK.H280P57.R.9.2. delete DBLK.H280P57.R.9.3 4. Update DBLK.LUP.R.1, add DBLK.LUP.R.2 5. Update name of TSMC_SRAM_ROM → TSMC_ROM to meet guideline 6. Update CIP supported variable and rules 7. Add page of tCIC Auto-Fixing Hint: Sanity Rules Check

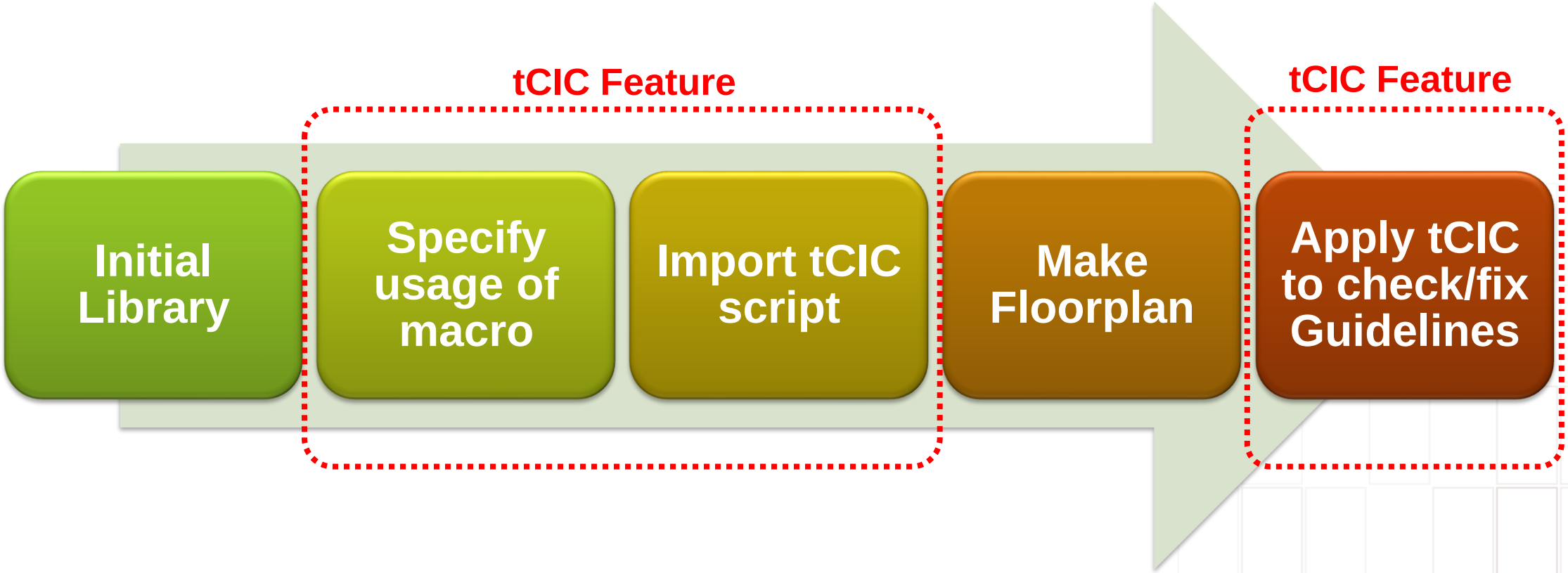
tCIC Overview

- tCIC is a flow to check/fix geometry guidelines among objects in chip integration
  - Object includes core region, macro routing blockage, and etc.
  - tCIC script is a set of TCL commands to express guidelines
  - tCIC script is generated based on Chip Integration Design Guideline
- Major APR tools can support tCIC script to check and floorplan easily and automatically
  - Innovus
  - ICC2

tCIC working Concept



Usage Model of tCIC

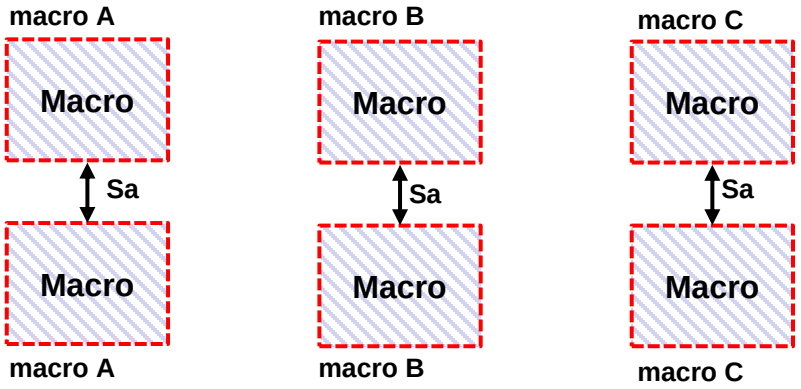


Usage of tCIC Package

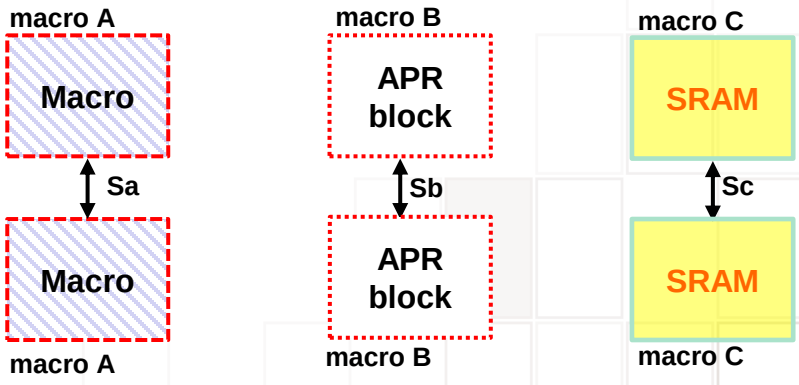
- tCIC package includes
  - Macro usage manager: utility to specify macro as TSMC SRAM or APR block
  - tCIC global script: Main tCIC global script
- tCIC script describe ground guidelines of macro, and special guidelines related to APR block and TSMC SRAM
  - User need to specify macro usage for correct checking
  - tCIC recognizes TSMC SRAM or APR block by specified "usage" of each macro
  - IPs w/o specified "usage", tCIC will check IPs by macro guidelines

Specify Usage of Macro is Necessary for Correct Checking

w/o specify macro usage, tCIC check every macro by ground rule (Sa)



User specify macro B as APR-block and macro C as SRAM, tCIC checks macro B and C by APR-block ground rule (Sb) and SRAM ground rule (Sc) individually, instead of macro ground rule (Sa)



Content of Package

Path	Filename	Content
Innovus	tCIC_macro_usage_manager_N5_General_v1d1_0_2a_Official_12252020.tcl	Macro usage manager for Innovus
	tCIC_N5_General_v1d1_0_2a_Official_12252020.tcl	tCIC main rule script
	tCIC_description_N5_General_v1d1_0_2a_Official_12252020.tcl	Rule description file to map constraint name and guideline
	tCIC_set_cip_variables_N5_General_v1d1_0_2a_Official_12252020.tcl	Customize IP guideline configuration file
	run_tcic.tcl	Example script of running tCIC in Innovus
ICC2	tCIC_macro_usage_manager_N5_General_v1d1_0_2a_Official_12252020.tcl.e	Macro usage manager for ICC2
	tCIC_N5_General_v1d1_0_2a_Official_12252020.tcl.e	tCIC main rule script
	tCIC_description_N5_General_v1d1_0_2a_Official_12252020.tcl.e	Rule description file to map constraint name and guideline
	tCIC_set_cip_variables_N5_General_v1d1_0_2a_Official_12252020.tcl	Customize IP guideline configuration file
	run_tcic.tcl	Example script of running tCIC in ICC2

N5 tCIC Package and Usage (Innovus)

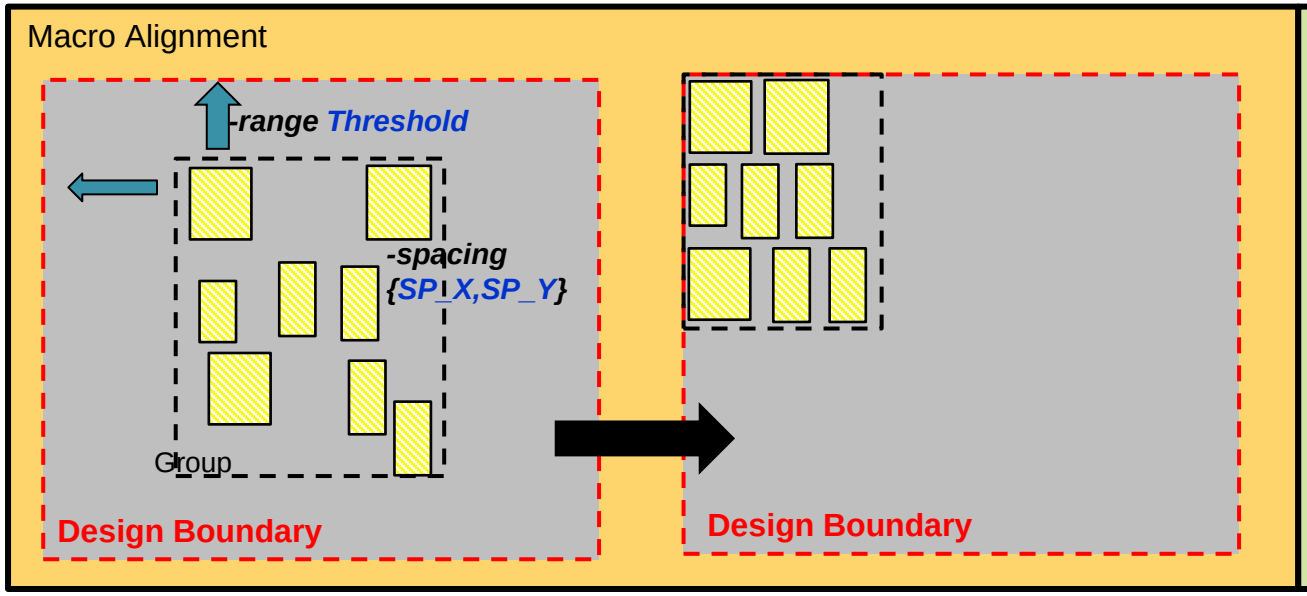
- **Tool version : Innovus 20.13-e011 or later version**
- **Put package in run directory then follow procedure below**

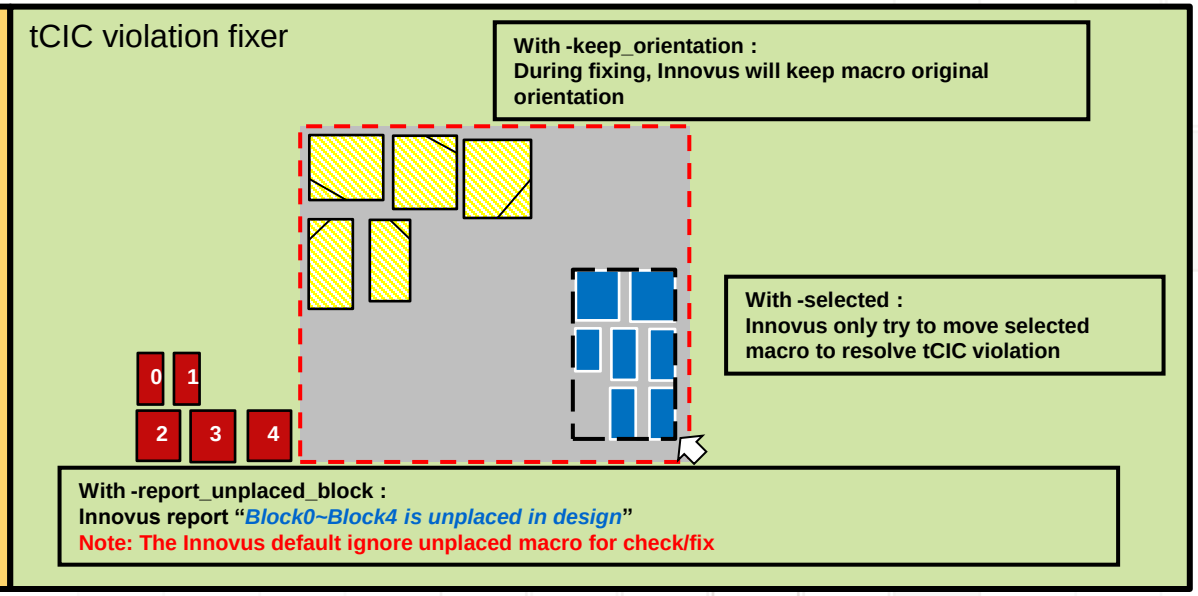
	Step	Procedure	Command
Checker	**1**	source macro usage manager script	source tCIC_macro_usage_manager_N5_General_v1d1_0_2a_Official_12252020.tcl
	2	If design is chip top:	tCIC_set_fullchip_mode 1
		specify design cell type (default is H210P51)	tCIC_set_design_cell_type H210P51 (Support key word: H210P51/H280P57)
		If design include FG112 APR block:	tCIC_set_FG112_mode 1
		If design need to align P76 tracks in chip top:	tCIC_set_align_p76_track_mode 1
		If design is boundary controlled block:	tCIC_set_boundary_controlled_block_mode 1
		If boundary cell type is common well (CW):	tCIC_set_boundary_cell_style CW
		If boundary row cell type is NROW, use following command (default is PROW type)	tCIC_set_boundary_row_cell_style NROW
		Set top layer of DTCD/ICOVL (top My layer, default 10 for 1P14M)	tCIC_set_max_DTCD_layer 10
		specify macro usage (example: set APR blocks)	tCIC_specify_macro_usage -usage APR_BLOCK_H210P51_FG28 -macro [list <APR block names>] ….
	3	Convert tCIC script to Innovus native format	convert_tCIC_to_ufc -input_files "tCIC_description_N5_General_v1d1_0_2a_Official_12252020.tcl tCIC_N5_General_v1d1_0_2a_Official_12252020.tcl" -ufc_file tcic.ufc
	4	cutRow before apply tCIC check	cutRow
	5	apply tCIC check	check_ufc tcic.ufc [-report_unplaced_block] #Specified option to report list of unplaced macro in design [-include_all_rules] #Specified option to report all rules be checked [-report_file check.rpt] #Specified option to write out summary report

Optional Setting

N5 tCIC Package and Usage (Innovus)

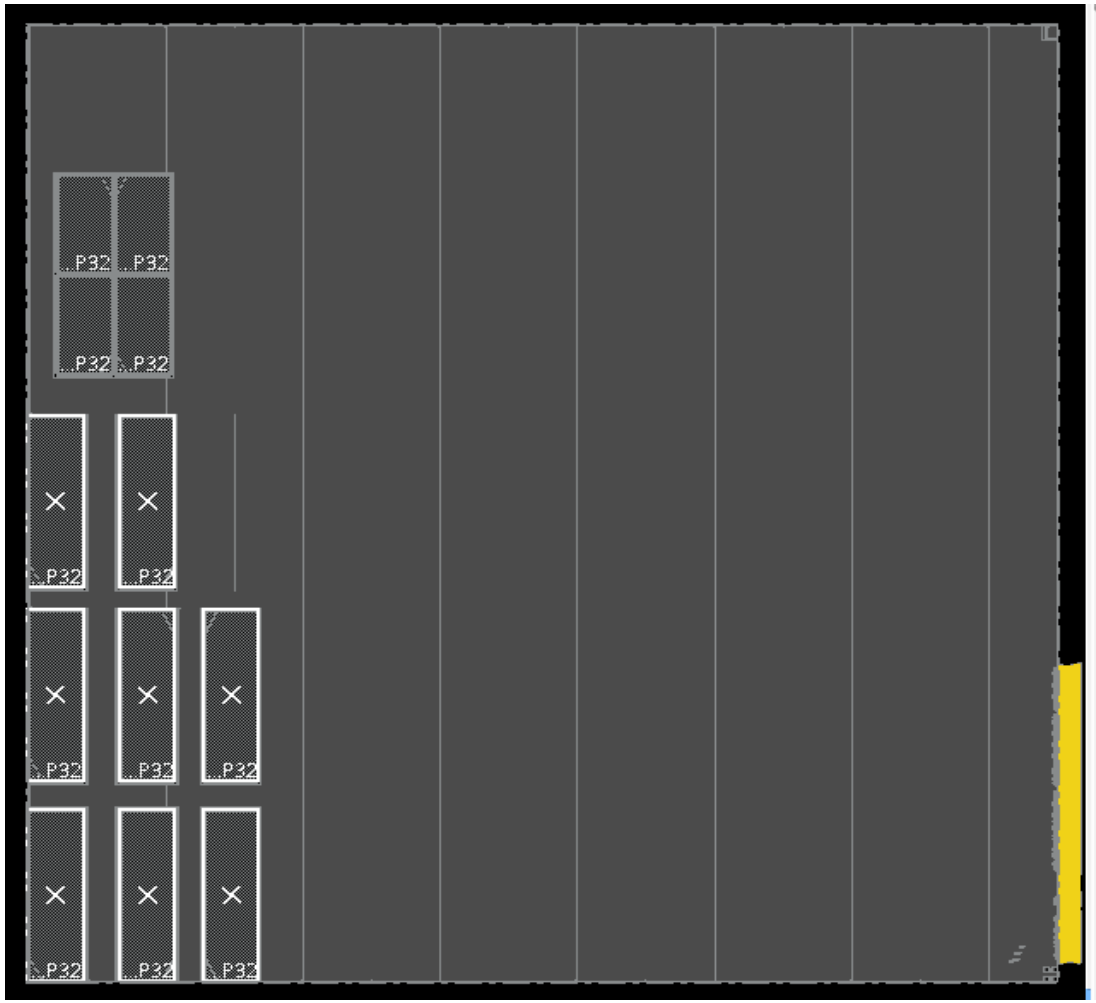
	Step	Procedure	Command
Fixer	**1**	Define macro group **(optional)**	createInstGroup *Group* -members { *Macro_Instance_list* }
	2	Macro boundary/channel alignment **(optional)**	align_macros -groups *Group* \ -ref {core constraint local} \ #Do NOT change this option -range *Threshold* \ #Specified space threshold to snap group on boundary -spacing { *SP_X SP_Y* } #Specified the channel space of macro in group
	3	Macro legalization to resolve tCIC violation	fix_floorplan -file "tCIC_description_N5_General_v1d1_0_2a_Official_12252020.tcl tCIC_N5_General_v1d1_0_2a_Official_12252020.tcl" -type tcic \ [-selected] #Specified option to fix selected Macro only [-keep_orientation] #Specified option to forbid tool change macro orientation during fix [-report_unplaced_block] #Specified option to report list of unplaced macro in design [-report_file fix.rpt] #Specified option to write out summary report

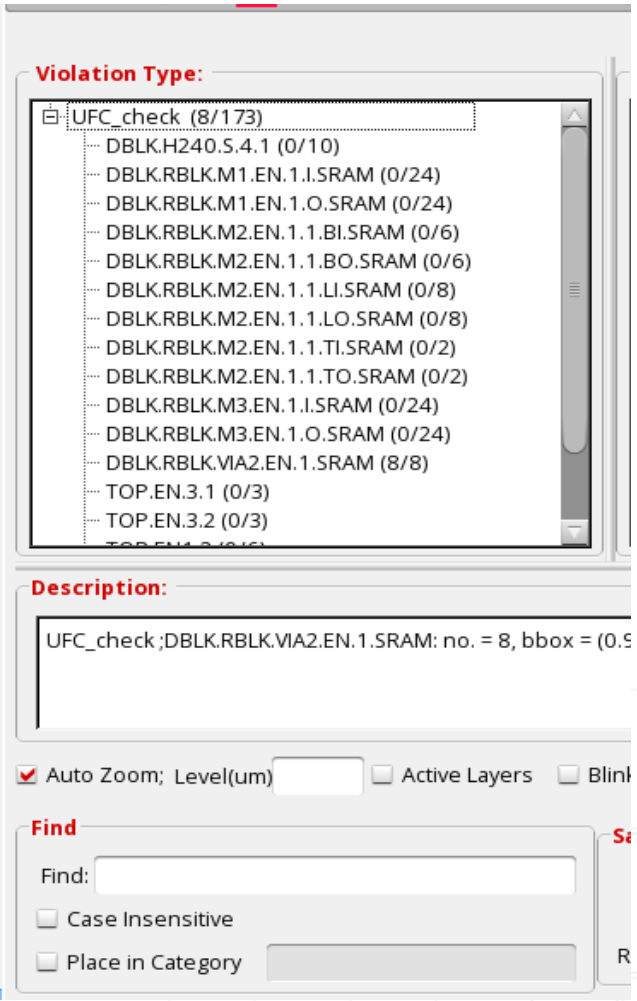




Floorplan Error Flag by tCIC (Innovus)

tCIC example result by Innovus





N5 tCIC Package and Usage (ICC2)

- **Tool version : ICC2 Q-2019.12-SP5-VAL-20201208 or later version**
- **Put package in run directory then follow procedure below**

	Step	Procedure	Command
Checker	**1**	source macro usage manager script	source tCIC_macro_usage_manager_N5_General_v1d1_0_2a_Official_12252020.tcl.e
	2	If design is chip top:	tCIC_set_fullchip_mode 1
		specify design cell type (default is H210P51)	tCIC_set_design_cell_type H210P51 (Support key word: H210P51/H280P57)
		If design include FG112 APR block:	tCIC_set_FG112_mode 1
		If design need to align P76 tracks in chip top:	tCIC_set_align_p76_track_mode 1
		If design is boundary controlled block:	tCIC_set_boundary_controlled_block_mode 1
		If boundary cell type is common well (CW):	tCIC_set_boundary_cell_style CW
		If boundary row cell type is NROW, use following command (default is PROW type)	tCIC_set_boundary_row_cell_style NROW
		Set top layer of DTCD/ICOVL (top My layer, default 10 for 1P14M)	tCIC_set_max_DTCD_layer 10
		specify macro usage (example: set APR blocks)	tCIC_specify_macro_usage -usage APR_BLOCK_H210P51_FG28 -macro [list <APR block names>] ….
	3	Synopsys recommended option of ICC2 P-2019.03-SP5 or later version	set_app_options -name plan.floorplan_rule.honor_all_from_objects_for_halo_rule -value true set_app_options -name plan.floorplan_rule.must_enclose_level -value 1
	4	ICC2 option to ignore unplace macro check	set_app_options -name plan.floorplan_rule.ignore_unplaced_macros -value true
	5	apply tCIC check	apply_tsmc_floorplan_constraints \ -filename tCIC_N5_General_v1d1_0_2a_Official_12252020.tcl.e -user_description tCIC_description_N5_General_v1d1_0_2a_Official_12252020.tcl.e check_floorplan_rules -err_view Error_tCIC
	6	Use error browser to open *Error_tCIC.err* file to show violation on GUI	

Optional Setting

N5 tCIC Package and Usage (ICC2)

	Step	Procedure	Command
Fixer	**1**	Define macro group **(optional)**	create_bound -name *Group* set group_macros { *Macro_Instance_list* } add_to_bound *Group* $group_macros
	2	Macro boundary/channel alignment **(optional)**	align_macros \ [-macros *macro_list*] | [-group *macro_group*] # List of macro instances to align [-reference_macro *macro_inst*] # Macro instance to help determine alignment [-boundary_threshold {*Threshold_X Threshold_Y* }] # Specify space threshold to snap group on boundary [-channel_size { *SP_X SP_Y* }] # Try to use this spacing between macros if possible [-abutment_threshold { *Abut_TH_X Abut_TH_Y* }] # Specify threshold spacing to trigger macros abut [-abutment_distance {*Abut_SP_X Abut_SP_Y* }] # Specify space of macro virtual abutment [-optimize_orientations] #Enable macro orientation change to get best chance for abutment
	3	Macro legalization to resolve tCIC violation	fix_floorplan_rules \ [-file *fix.tcl*] # Output script to replay fixing [-bbox {{x1 y1} {x2 y2}}] # Floorplan fixing only apply on specified window

Required Setting	Suggested number	Notice
Threshold_X / Threshold_Y	N/A	Design dependent value. User can adjust this value to optimize fixing result. If *Threshold_X (Threshold_Y)* ≥ 1/2 Block size, all macro will be moved to edge
SP_X / SP_Y	≥0.663 / ≥0.560	0.663/0.560 setting just let fixer meet N5 guideline. Larger number is suggested for preventing routing congestion around macro
Abut_TH_X / Abut_TH_Y	≥0.663 / ≥0.560	0.663/0.560 setting just let fixer abut macro which not able to meet spacing requirement. Larger number will enable more aggressive fixing
Abut_SP_X / Abut_SP_Y	0.153 / 0, or 0.051 / 0	If macro group contain TSMC POR SRAM, Abut_SP_X = 0.153 is required. For other case, set Abut_SP_X as 0.051

N5 tCIC Package and Usage (ICC2)

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Macro Alignment

-boundary_threshold {*Threshold_X Threshold_Y*}

Ref.

-reference_macro *macro_inst*
To specify anchor point of macro shift

-channel_size {*SP_X SP_Y*}

-macros *macro_list* -group *macro_group*

Design Boundary

Ref.

-abutment_threshold {*Threshold_X Threshold_Y* }
When channel space <= threshold, tool try to do macro abutment

-abutment_distance {*SP_X SP_Y*}
Specified the target space <= distance when tool try to do macro abutment

-optimize_orientations
Option to allow tool change macro orientation to get better change to abut macros

Design Boundary

Design Boundary

tCIC violation fixer

{x2,y2}

{x1,y1}

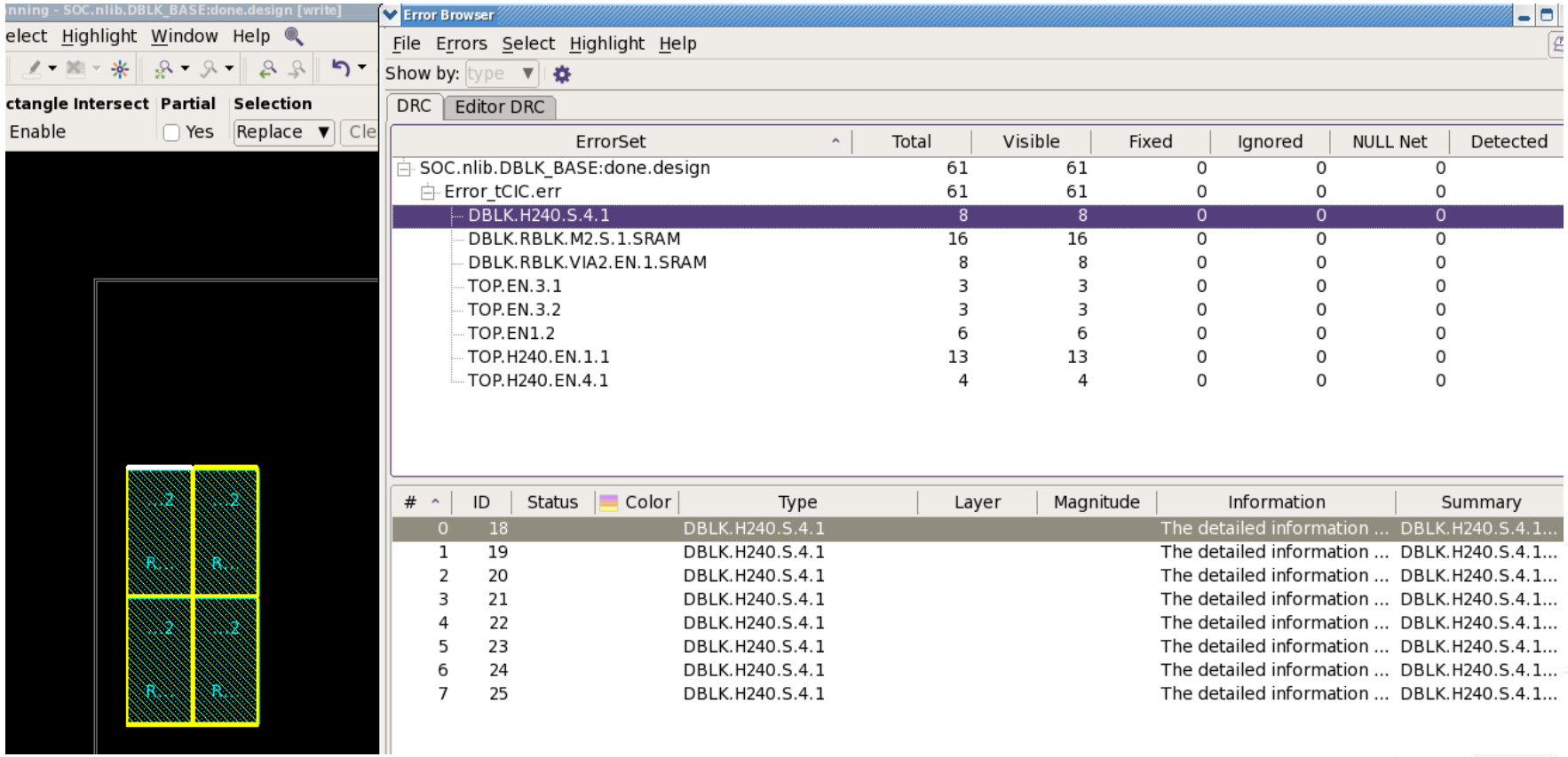
With -file fix.tcl : ICC2 output executed command to monitor database change or use to reproduce results

Fix.tcl

With -bbox {x1 y1 x2 y2}:
ICC2 try to resolve tCIC violation on macro inside bbox

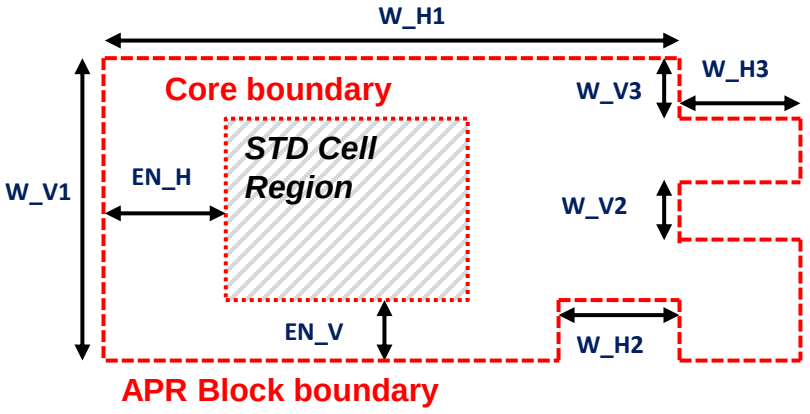
Floorplan Error Flag by tCIC (ICC2)

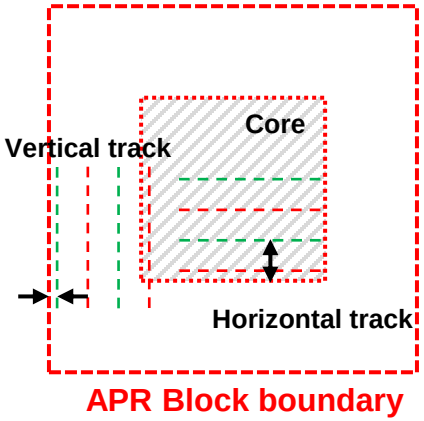
tCIC example result by ICC2

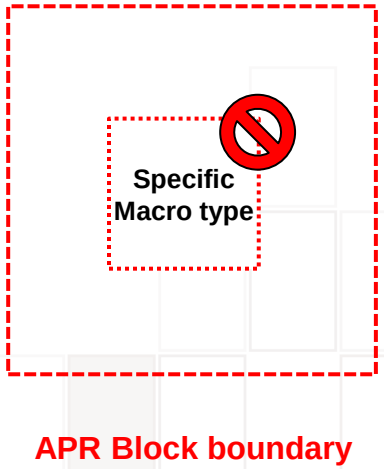


tCIC Auto-Fixing Hint: Sanity Rules Check

- To ensure quality of tCIC auto-fixing, TSMC recommend to solve following rule violations by manually before fixing
  - APR Block boundary width and height
  - APR Block boundary to Core boundary distance
  - Routing track
  - Forbidden macro in design







Detail Information (1)

- **Following macro usage are used in tCIC script**

Usage	Meaning
APR_BLOCK_H210P51_FG28	APR block contains only TSMC SRAM or fin grid 28nm macro
APR_BLOCK_H210P51_FG112	APR block contains FG112 APR block or FG112 Macro
APR_BLOCK_H210P51_FG28_BC	APR block that all edges are covered by boundary cell, only TSMC SRAM or fin grid 28nm macro
APR_BLOCK_H210P51_FG112_BC	APR block that all edges are covered by boundary cell, and contains FG112 APR block or FG112 Macro
APR_BLOCK_H280P57	APR block built by H280P57 cell and APR techfile, for H280P57 APR Block related guidelines
APR_BLOCK_H280P57_BC	APR block use H280P57 STD cell and core offset is 0 (3nm in horizontal direction)
MACRO_FG112	macro contain macro with FB_10, such macro will be placed on 112nm grid in Y-axis
TSMC_SRAM_POR	TSMC POR SRAM, this type of SRAM must be surrounded by core, or mirror abut itself
TSMC_SRAM_FP	TSMC SRAM, this type of SRAM can be placed alone w/o abutting core
TSMC_ROM	TSMC ROM, this tCIC usage **must** be used with TSMC_SRAM_POR or TSMC_SRAM_FP
TSMC_SRAM_P2	SRAM with M3 pins in middle, this tCIC usage **must** be used with TSMC_SRAM_POR or TSMC_SRAM_FP
MACRO_EFUSE	TSMC eFuse IP that require 5um KOZ
MACRO_ESD_C1	TSMC ESD Clamp that require 5.6μm KOZ
MACRO_ESD_C2	TSMC ESD Clamp that require 3.6μm KOZ
MACRO_ESD_C3	TSMC ESD Clamp that require 2.6μm KOZ
MACRO_BEOL_ONLY	Macro only contains BEOL layers. ex.bump macro. All fin-grid or PO-grid related guidelines are not checking on this type
DTCD	Reserved Keywords
ICOVL	Reserved Keywords
ICOVL_2	Reserved Keywords

tCIC Usage by SRAM Type

- **Following Table shows tCIC usage by SRAM type and default name**

SRAM Type	Default Cell Name	tCIC Usage
SPSB SRAM	ts1n5psb{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts1n5psb{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP
SPMB SRAM	ts1n5pmb{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts1n5pmb{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP
2PRF	ts6n5p{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts6n5p{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP
UHD2PRF	ts6n5p{vt}b{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts6n5p{vt}b{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP
ROM	ts3n5p{vt}a{depth}x{width}m{mux}{seg}bz{o}{d}_*	TSMC_SRAM_POR + **TSMC_ROM**
	ts3n5p{vt}a{depth}x{width}m{mux}{seg}bz{o}{d}y_*	TSMC_SRAM_FP + **TSMC_ROM**
HDSPSB SRAM	ts1n5psb{vt}b{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts1n5psb{vt}b{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP
HDSPMB SRAM	ts1n5pmb{vt}b{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts1n5pmb{vt}b{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP
HSSP SRAM	ts1n5phs{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts1n5phs{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP

tCIC Usage by SRAM Type

- **Following Table shows tCIC usage by SRAM type and default name**

SRAM Type	Default Cell Name	tCIC Usage
L1CACHE	ts5n5pl1{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*	TSMC_SRAM_POR
	ts5n5pl1{vt}a{depth}x{width}m{mux}**wf**_*	TSMC_SRAM_POR + **TSMC_SRAM_P2**
	ts5n5pl1{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}y_*	TSMC_SRAM_FP

Remark: excepted content in { }

{ }	Expected Content
{vt}	svt lvt ulvt
{depth}	[0..9]
{width}	[0..9]
{mux}	[0..9]
{seg}	s f
{w}	Empty or w
{h}	Empty or h
{o}	Empty or o
{d}	Empty or d
{cp}	Empty or cp

Example:
ts1n5psb{vt}a{depth}x{width}m{mux}{seg}{w}bz{h}{o}{d}{cp}_*
=> ts1n5psblvta128x32m16swbz_*

Detail Information (2)

- Following functions are included in macro usage manager script
  - tCIC_report_optional_setting
    - report all option setting
  - tCIC_set_fullchip_mode <switch>
    - when switch is 1, tCIC will check floorplan in full-chip mode
    - Guidelines only be checked when switch is on : TOP.*
    - Guidelines only be checked when switch is off : DBLK.*
  - tCIC_set_align_p76_track_mode <switch>
    - when switch is 1, tCIC will check floorplan with spec for P76 track Alignment
    - Guideline only check when switch is on: *ALP76*
  - tCIC_set_FG112_mode <switch> [Option only effective when cell_type is H210P51]
    - when switch is 1, tCIC will check floorplan with spec for FG112 design
    - Guidelines only be checked when switch is on: *FG112*
    - Guidelines only be checked when switch is off: *FG28*
  - tCIC_set_boundary_controlled_block_mode <switch>
    - when switch is 1, tCIC will check floorplan with spec for boundary controlled block design
    - Guidelines only be checked when switch is on : *BC*
    - Guidelines only be checked when switch is off : *NOBC*

Detail Information (3)

- Following functions are included in macro usage manager script
  - tCIC_set_design_cell_type <cell_type>
    - Guidelines only be checked when cell_type is H210P51 : TOP.H210P51* / DBLK.H210P51.* / CORE.H210P51.*
    - Guidelines only be checked when cell_type is H280P57 : TOP.H280P57* / DBLK.H280P57.* / CORE.H280P57.*
  - tCIC_set_boundary_cell_style <cell_style>
    - Only two switch supported, DEF (default) and CW (for common well type boundary cell)
    - Guidelines only be checked when cell_style is CW : *BDRYCW
  - tCIC_set_boundary_row_cell_style <cell_style> [Option only effective when cell_type is H280P57]
    - Only two switch supported, PROW (default) and NROW (for NROW type boundary cell)
    - Guidelines only be checked when cell_style is PROW : DBLK.H280P57.EN.5.1.M2_PROW
    - Guidelines only be checked when cell_style is NROW : DBLK.H280P57.EN.5.1.M2_NROW

Detail Information (4)

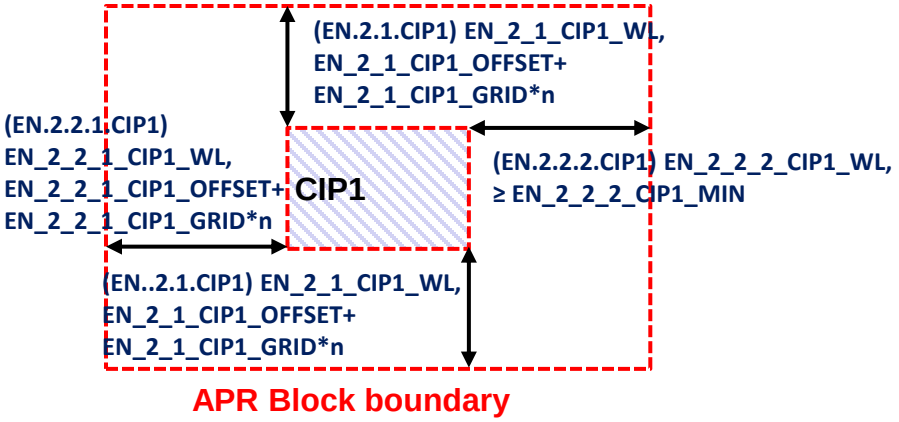
- Following functions are included in macro usage manager script
  - tCIC_reset_macro_usage <macro_list>
    - remove all usage of <macro_list>, if <macro_list> is empty, remove usage of all macro
  - tCIC_report_macro_usage
    - report macro of each usage
  - tCIC_specify_macro_usage -usage <usage_list> -macro <macro_list>
    - specify usages of macro in <macro_list>
  - tCIC_get_macro_by_usage <usage_list>
    - return macro list of all usage in <usage_list>
  - tCIC_rename_metal_layer <layer_index> <layer_name>
    - Rename default metal layer used in checker (M1 to top My layer)
    - Report current layer mapping by using command without argument
    - Command need apply before “apply_tsmc_floorplan_constraints” / “convert_tCIC_to_ufc”

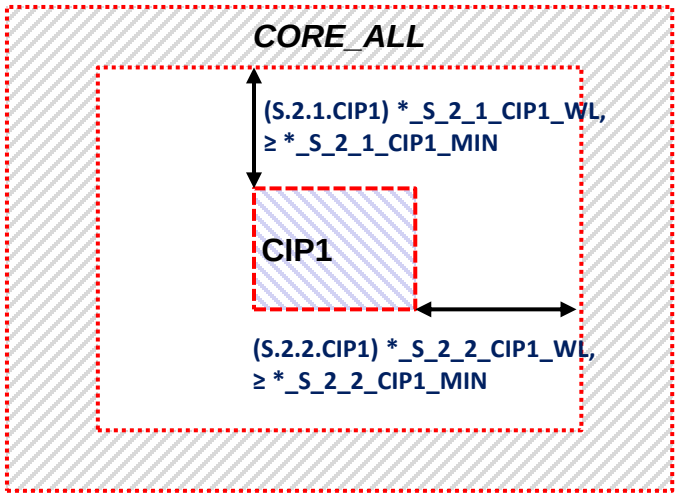
Customized IP Guideline

- tCIC script provide 5 slots for IP with user configurable rules
  - User can apply usage “CUSTOMIZE_IP1 ~ CUSTOMIZE_IP5” to required macro
- Following table list all rule codes and brief meaning

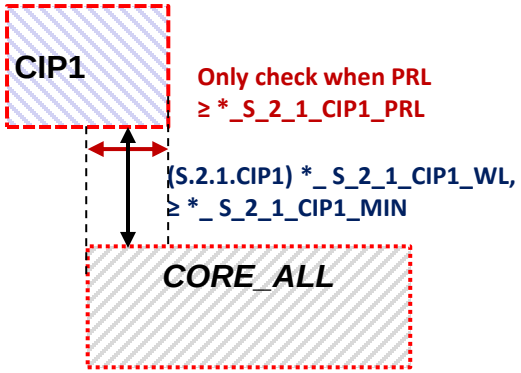
Space to		Block Boundary	STD Cell	Other Macro	Macro_nonLg3	Macro in same Customize IP group	Identical macro	Identical macro, Mirrored
Customized IP1	V	DBLK.EN.2.1.CIP1	DBLK.*.S.2.1.CIP1	DBLK.S.5.1.CIP1	DBLK.S.5.1.1.CIP1	DBLK.S.5G.1.CIP1	DBLK.S.5I.1.CIP1	DBLK.S.5M.T.CIP1 DBLK.S.5M.B.CIP1
	H	DBLK.EN.2.2.CIP1	DBLK.*.S.2.2.CIP1	DBLK.S.5.2.CIP1	DBLK.S.5.2.1.CIP1	DBLK.S.5G.2.CIP1	DBLK.S.5I.2.CIP1	DBLK.S.5M.L.CIP1 DBLK.S.5M.R.CIP1
Customized IP2	V	DBLK.EN.2.1.CIP2	DBLK.*.S.2.1.CIP2	DBLK.S.5.1.CIP2	DBLK.S.5.1.1.CIP2	DBLK.S.5G.1.CIP2	DBLK.S.5I.1.CIP2	DBLK.S.5M.T.CIP2 DBLK.S.5M.B.CIP2
	H	DBLK.EN.2.2.CIP2	DBLK.*.S.2.2.CIP2	DBLK.S.5.2.CIP2	DBLK.S.5.2.1.CIP2	DBLK.S.5G.2.CIP2	DBLK.S.5I.2.CIP2	DBLK.S.5M.L.CIP2 DBLK.S.5M.R.CIP2
Customized IP3	V	DBLK.EN.2.1.CIP3	DBLK.*.S.2.1.CIP3	DBLK.S.5.1.CIP3	DBLK.S.5.1.1.CIP3	DBLK.S.5G.1.CIP3	DBLK.S.5I.1.CIP3	DBLK.S.5M.T.CIP3 DBLK.S.5M.B.CIP3
	H	DBLK.EN.2.2.CIP3	DBLK.*.S.2.2.CIP3	DBLK.S.5.2.CIP3	DBLK.S.5.2.1.CIP3	DBLK.S.5G.2.CIP3	DBLK.S.5I.2.CIP3	DBLK.S.5M.L.CIP3 DBLK.S.5M.R.CIP3
Customized IP4	V	DBLK.EN.2.1.CIP4	DBLK.*.S.2.1.CIP4	DBLK.S.5.1.CIP4	DBLK.S.5.1.1.CIP4	DBLK.S.5G.1.CIP4	DBLK.S.5I.1.CIP4	DBLK.S.5M.T.CIP4 DBLK.S.5M.B.CIP4
	H	DBLK.EN.2.2.CIP4	DBLK.*.S.2.2.CIP4	DBLK.S.5.2.CIP4	DBLK.S.5.2.1.CIP4	DBLK.S.5G.2.CIP4	DBLK.S.5I.2.CIP4	DBLK.S.5M.L.CIP4 DBLK.S.5M.R.CIP4
Customized IP5	V	DBLK.EN.2.1.CIP5	DBLK.*.S.2.1.CIP5	DBLK.S.5.1.CIP5	DBLK.S.5.1.1.CIP5	DBLK.S.5G.1.CIP5	DBLK.S.5I.1.CIP5	DBLK.S.5M.T.CIP5 DBLK.S.5M.B.CIP5
	H	DBLK.EN.2.2.CIP5	DBLK.*.S.2.2.CIP6	DBLK.S.5.2.CIP5	DBLK.S.5.2.1.CIP5	DBLK.S.5G.2.CIP5	DBLK.S.5I.2.CIP5	DBLK.S.5M.L.CIP5 DBLK.S.5M.R.CIP5

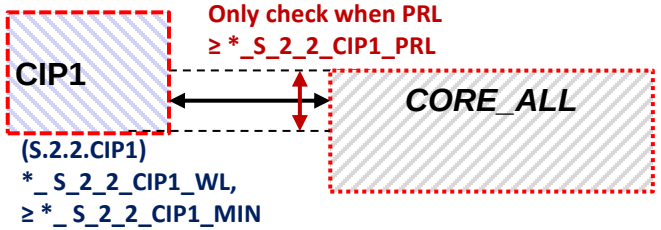
Customized IP Guideline

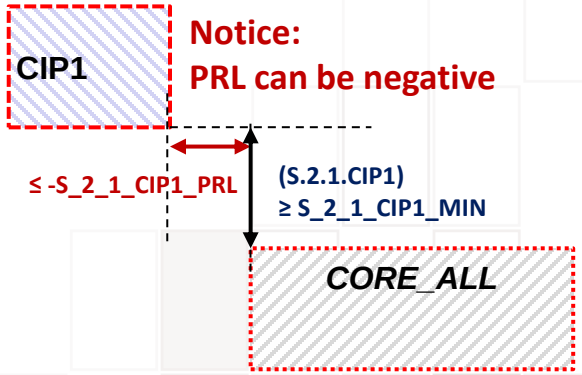




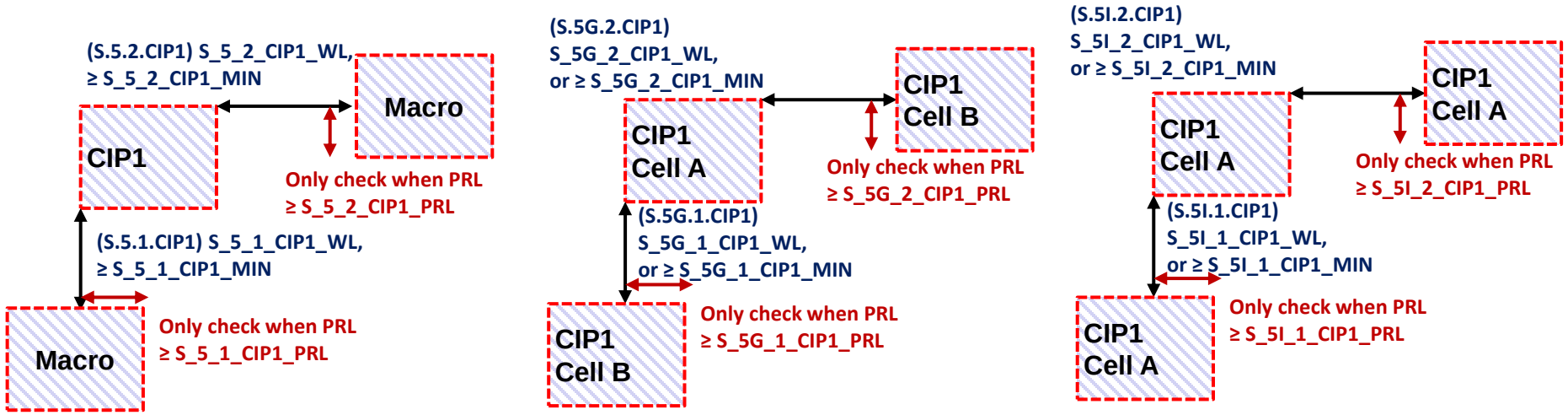
- If grid is not required in DBLK.EN rules, it can be set as 0.0005 (database grid)
- PRL setting exist for all spacing rules. Negative PRL means spacing still checked in corner to corner condition
- Recommend to set PRL of vertical spacing as -(MIN horizontal spacing-0.0005)





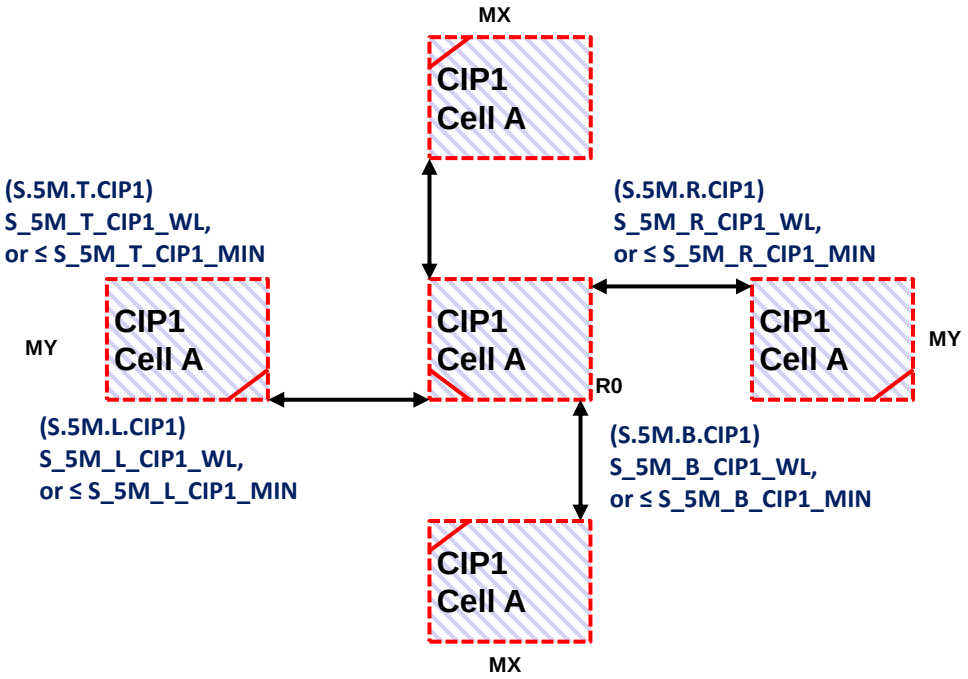


Customized IP Guideline

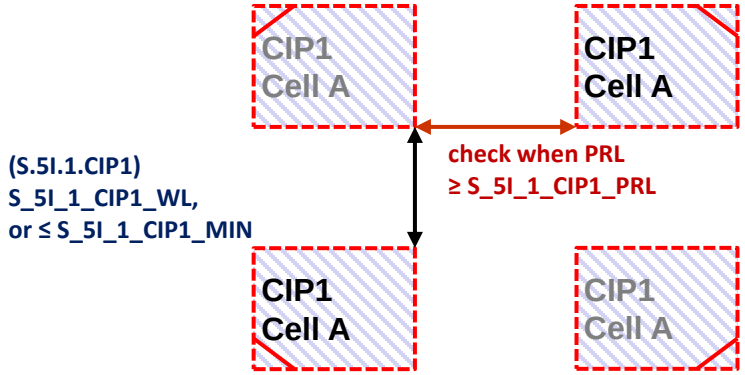


- WHITE_LIST setting exists in DBLK.S.5.* / DBLK.S.5G.* / DBLK.S.5I.* / DBLK.S.5M.* to allow abutment.
  If WHITE_LIST is not required, it can be set identical as MIN.
- Only one number is allowed in WHITE_LIST
- If smaller spacing is only allowed in identical + mirror condition (DBLK.S.5M.*), PRL setting in DBLK.S.5I.* should be adjusted to prevent overkill IP at diagonal corner

Customized IP Guideline



- PRL setting also exists in DBLK.S.5M.* rules
- tCIC can automatically follow macro rotation, for example, if a CIP1 macro flip vertically (MX), DBLK.S.5M.T.CIP1 will check spacing from lower side of macro



- IP at diagonal corner may be flagged by DBLK.S.5I.* rules, if PRL is not adjusted well

Customized IP Guideline

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.EN.2.1.CIP1	BOUNDARY_ALL enclosure CUSTOMIZE_IP1 in vertical direction	**EN.2.1.CIP1**	=	EN_2_1_CIP1_WL, EN_2_1_CIP1_OFF+ EN_2_1_CIP1_GRID*n μm
DBLK.EN.2.2.1.CIP1	BOUNDARY_ALL enclosure left edge of CUSTOMIZE_IP1 in horizontal direction	**EN.2.2.1.CIP1**	=	EN_2_2_1_CIP1_WL, EN_2_2_1_CIP1_OFF+ EN_2_2_1_CIP1_GRID*n μm
DBLK.EN.2.2.2.CIP1	BOUNDARY_ALL enclosure right edge of CUSTOMIZE_IP1 in horizontal direction	**EN.2.2.2.CIP1**	=	EN_2_2_2_CIP1_WL, ≥EN_2_2_2_CIP1_MIN μm
DBLK.H210P51.S.2.1.CIP1	CUSTOMIZE_IP1 to H210P51 STD cell region spacing in vertical direction (PRL≥ H210P51_S_2_1_CIP1_PRL μm)	**S.2.1.CIP1**	=	H210P51_S_2_1_CIP1_WL, ≥H210P51_S_2_1_CIP1_MIN μm
DBLK.H210P51.S.2.2.CIP1	CUSTOMIZE_IP1 to H210P51 STD cell region spacing in horizontal direction (PRL≥H210P51_S_2_2_CIP1_PRL μm)	**S.2.2.CIP1**	=	H210P51_S_2_2_CIP1_WL, ≥H210P51_S_2_2_CIP1_MIN μm
DBLK.H280P57.S.2.1.CIP1	CUSTOMIZE_IP1 to H280P57 STD cell region spacing in vertical direction (PRL≥ H280P57_S_2_1_CIP1_PRL μm)	**S.2.1.CIP1**	=	H280P57_S_2_1_CIP1_WL, ≥H280P57_S_2_1_CIP1_MIN μm
DBLK.H280P57.S.2.2.CIP1	CUSTOMIZE_IP1 to H280P57 STD cell region spacing in horizontal direction (PRL≥H280P57_S_2_2_CIP1_PRL μm)	**S.2.2.CIP1**	=	H280P57_S_2_2_CIP1_WL, ≥H280P57_S_2_2_CIP1_MIN μm

Customized IP Guideline

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.S.5.1.CIP1	Spacing from CUSTOMIZE_IP1 to MACRO in vertical direction (PRL≥ S_5_1_CIP1_PRL μm)	**S.5.1.CIP1**	=	S_5_1_CIP1_WL, ≥S_5_1_CIP1_MIN μm
DBLK.S.5.2.CIP1	Spacing from CUSTOMIZE_IP1 to MACRO in horizontal direction (PRL≥ S_5_2_CIP1_PRL μm)	**S.5.2.CIP1**	=	S_5_2_CIP1_WL, ≥S_5_2_CIP1_MIN μm
DBLK.S.5G.1.CIP1	Spacing of CUSTOMIZE_IP1 in vertical direction (PRL≥ S_5G_1_CIP1_PRL μm), except two CUSTOMIZE_IP1 are identical and placed in mirror direction	**S.5G.1.CIP1**	=	S_5G_1_CIP1_WL, ≥S_5G_1_CIP1_MIN μm
DBLK.S.5G.2.CIP1	Spacing of CUSTOMIZE_IP1 in horizontal direction (PRL≥ S_5G_2_CIP1_PRL μm), except two CUSTOMIZE_IP1 are identical and placed in mirror direction	**S.5G.2.CIP1**	=	S_5G_2_CIP1_WL, ≥S_5G_2_CIP1_MIN μm
DBLK.S.5I.1.CIP1	Spacing of CUSTOMIZE_IP1 in vertical direction (PRL≥ S_5I_1_CIP1_PRL μm) , when two CUSTOMIZE_IP1 are identical, except two CUSTOMIZE_IP1 are placed in mirror direction	**S.5I.1.CIP1**	=	S_5I_1_CIP1_WL, ≥S_5I_1_CIP1_MIN μm
DBLK.S.5I.2.CIP1	Spacing of CUSTOMIZE_IP1 in horizontal direction (PRL≥ S_5I_2_CIP1_PRL μm), when two CUSTOMIZE_IP1 are identical, except two CUSTOMIZE_IP1 are placed in mirror direction	**S.5I.2.CIP1**	=	S_5I_2_CIP1_WL, ≥S_5I_2_CIP1_MIN μm
DBLK.S.5M.B.CIP1	Spacing of bottom edge of CUSTOMIZE_IP1 in vertical direction (PRL≥ S_5M_B_CIP1_PRL μm), when two CUSTOMIZE_IP1 are identical and placed in mirror direction	**S.5M.B.CIP1**	=	S_5M_B_CIP1_WL, ≥S_5M_B_CIP1_MIN μm
DBLK.S.5M.T.CIP1	Spacing of top edge of CUSTOMIZE_IP1 in vertical direction (PRL≥ S_5M_T_CIP1_PRL μm), when two CUSTOMIZE_IP1 are identical and placed in mirror direction	**S.5M.T.CIP1**	=	S_5M_T_CIP1_WL, ≥S_5M_T_CIP1_MIN μm
DBLK.S.5M.L.CIP1	Spacing of left edge of CUSTOMIZE_IP1 in horizontal direction (PRL≥ S_5M_L_CIP1_PRL μm), when two CUSTOMIZE_IP1 are identical and placed in mirror direction	**S.5M.L.CIP1**	=	S_5M_L_CIP1_WL, ≥S_5M_L_CIP1_MIN μm
DBLK.S.5M.R.CIP1	Spacing of right edge of CUSTOMIZE_IP1 in horizontal direction (PRL≥ S_5M_R_CIP1_PRL μm), when two CUSTOMIZE_IP1 are identical and placed in mirror direction	**S.5M.R.CIP1**	=	S_5M_R_CIP1_WL, ≥S_5M_R_CIP1_MIN μm

Customized IP Guideline

Guideline No.	Replaced Guideline
DBLK.EN.2.1.CIP1	DBLK.EN.2.1
DBLK.EN.2.2.1.CIP1	DBLK.EN.2.2.1
DBLK.EN.2.2.2.CIP1	DBLK.EN.2.2.2
DBLK.H210P51.S.2.1.CIP1	DBLK.H210P51.S.2.1
DBLK.H210P51.S.2.2.CIP1	DBLK.H210P51.S.2.2
DBLK.H280P57.S.2.1.CIP1	DBLK.H280P57.S.2.1
DBLK.H280P57.S.2.2.CIP1	DBLK.H280P57.S.2.2
DBLK.S.5.1.CIP1	DBLK.S.5.1
DBLK.S.5.2.CIP1	DBLK.S.5.2
DBLK.S.5G.1.CIP1	DBLK.S.5.1.1.CIP1
DBLK.S.5G.2.CIP1	DBLK.S.5.2.1.CIP1
DBLK.S.5I.1.CIP1	DBLK.S.5G.1.CIP1
DBLK.S.5I.2.CIP1	DBLK.S.5G.2.CIP1
DBLK.S.5M.B.CIP1	DBLK.S.5I.1.CIP1
DBLK.S.5M.T.CIP1	DBLK.S.5I.1.CIP1
DBLK.S.5M.L.CIP1	DBLK.S.5I.2.CIP1
DBLK.S.5M.R.CIP1	DBLK.S.5I.2.CIP1

Default Value of CIP Variables

Rule	Variable	Value
DBLK.H210P51.S.2.1.CIP1	H210P51_S_2_1_CIP1_WL	0.560
	H210P51_S_2_1_CIP1_MIN	0.560
	H210P51_S_2_1_CIP1_PRL	-0.6625
DBLK.H210P51.S.2.2.CIP1	H210P51_S_2_2_CIP1_WL	0.663
	H210P51_S_2_2_CIP1_MIN	0.663
	H210P51_S_2_2_CIP1_PRL	-0.5595
DBLK.H280P57.S.2.1.CIP1	H280P57_S_2_1_CIP1_WL	0.784
	H280P57_S_2_1_CIP1_MIN	0.784
	H280P57_S_2_1_CIP1_PRL	-0.9685
DBLK.H280P57.S.2.2.CIP1	H280P57_S_2_2_CIP1_WL	0.969
	H280P57_S_2_2_CIP1_MIN	0.969
	H280P57_S_2_2_CIP1_PRL	-0.7835

Rule	Variable	Value
DBLK.EN.2.1.CIP1	EN_2_1_CIP1_WL	0.560
	EN_2_1_CIP1_OFF	0.560
	EN_2_1_CIP1_GRID	0.028
DBLK.EN.2.2.1.CIP1	EN_2_2_1_CIP1_WL	0.714
	EN_2_2_1_CIP1_OFF	0.714
	EN_2_2_1_CIP1_GRID	0.102
DBLK.EN.2.2.2.CIP1	EN_2_2_1_CIP1_WL	0.714
	EN_2_2_1_CIP1_MIN	0.714
DBLK.S.5.1.CIP1	S_5_1_CIP1_WL	0.560
	S_5_1_CIP1_MIN	0.560
	S_5_1_CIP1_PRL	-0.6625
DBLK.S.5.2.CIP1	S_5_2_CIP1_WL	0.663
	S_5_2_CIP1_MIN	0.663
	S_5_2_CIP1_PRL	-0.5595
DBLK.S.5G.1.CIP1	S_5G_1_CIP1_WL	0.560
	S_5G_1_CIP1_MIN	0.560
	S_5G_1_CIP1_PRL	-0.6625
DBLK.S.5G.2.CIP1	S_5G_2_CIP1_WL	0.663
	S_5G_2_CIP1_MIN	0.663
	S_5G_2_CIP1_PRL	-0.5595

Rule	Variable	Value
DBLK.S.5I.1.CIP1	S_5I_1_CIP1_WL	0.560
	S_5I_1_CIP1_MIN	0.560
	S_5I_1_CIP1_PRL	-0.6625
DBLK.S.5I.2.CIP1	S_5I_2_CIP1_WL	0.663
	S_5I_2_CIP1_MIN	0.663
	S_5I_2_CIP1_PRL	-0.5595
DBLK.S.5M.B.CIP1	S_5M_B_CIP1_WL	0.560
	S_5M_B_CIP1_MIN	0.560
	S_5M_B_CIP1_PRL	-0.6625
DBLK.S.5M.T.CIP1	S_5M_T_CIP1_WL	0.560
	S_5M_T_CIP1_MIN	0.560
	S_5M_T_CIP1_PRL	-0.6625
DBLK.S.5M.L.CIP1	S_5M_L_CIP1_WL	0.663
	S_5M_L_CIP1_MIN	0.663
	S_5M_L_CIP1_PRL	-0.5595
DBLK.S.5M.R.CIP1	S_5M_R_CIP1_WL	0.663
	S_5M_R_CIP1_MIN	0.663
	S_5M_R_CIP1_PRL	-0.5595

Customized IP Guideline Configuration

- To modify user define guidelines, please edit file “set_cip_variables.tcl” in package
  - Content in package align all Customize IP rules as well as general macro
- User can use tCIC_set_cip_variable command to configure spec of required rules
  - Syntax: tCIC_set_cip_variable <rule_key> <value>
    <rule_key> are keyword of spec, <value> is the number of spec
  - Ex. tCIC_set_cip_variable S_5_1_CIP1_MIN 0.56 means:
    set min. spacing of DBLK.S.5.1.CIP1 to 0.56 μm
  - Available <rule_key> is listed in guideline diagram

```
# DBLK.S.5.1.CIP1
# min. PRL to trigger vertical spacing checking from Customize IP1 to other macro
tCIC_set_cip_variable S_5_1_CIP1_PRL -0.6625
# min. vertical spacing from Customize IP1 to other macro
tCIC_set_cip_variable S_5_1_CIP1_MIN 0.56
```

Rule key denote min. spacing of DBLK.S.5.1.CIP1

Set value to 0.56

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N5 tCIC Supported Chip-Integration Design Guideline

DTP/TSMC

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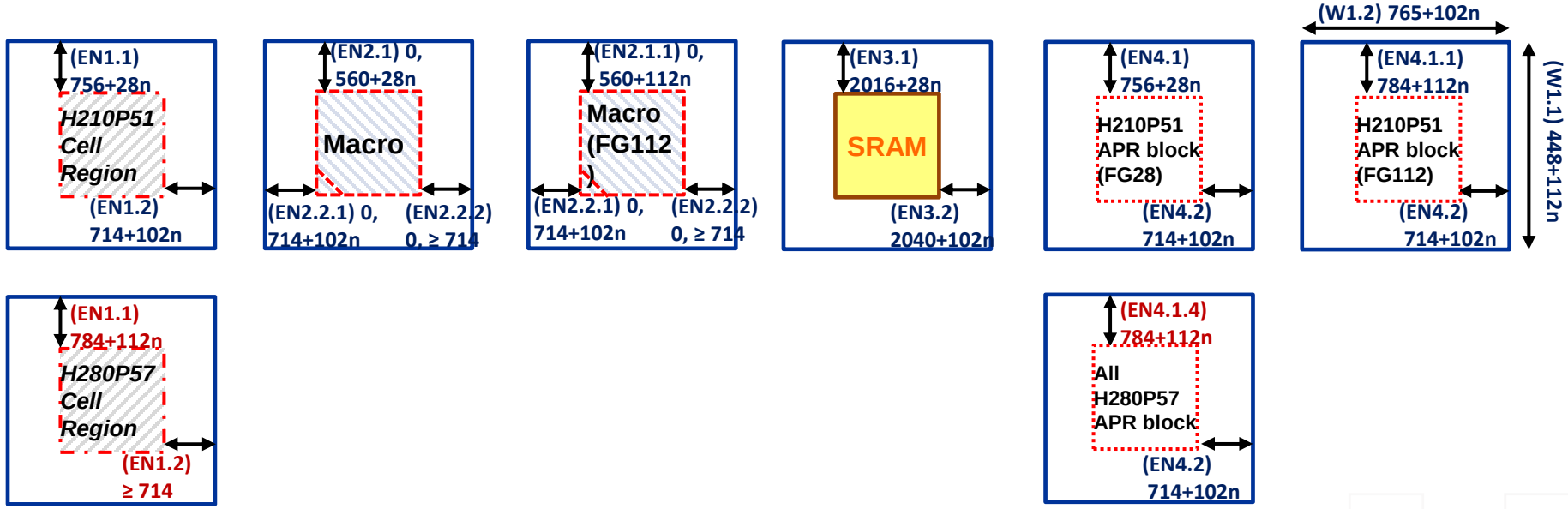
APR Top Design

Chip-integration Design Guideline for APR (General Section for H210P51 and H280P57)

- Common APR Design Guidelines

APR Top Design



APR Top Design

Guideline No.	Equivalent G.L. in APR Block	Guideline Description	Label	Op.	Rule
TOP.H210P51.EN.1.1	DBLK.H210P51.EN.1.1:*	Chip_Boundary enclosure H210P51 STD cell region in vertical direction	EN1.1	=	0.756+0.028*n µm
TOP.H280P57.EN.1.1	DBLK.H280P57.EN.1.1:*	Chip_Boundary enclosure H280P57 STD cell region in vertical direction	EN1.1	=	0.784+0.112*n µm
TOP.H210P51.EN.1.2	DBLK.H210P51.EN.1.2:*	Chip_Boundary enclosure H210P51 STD cell region in horizontal direction	EN1.2	=	0.714+0.102*n µm
TOP.H280P57.EN.1.2	DBLK.H280P57.EN.1.2:*	Chip_Boundary enclosure H280P57 STD cell region in horizontal direction	EN1.2	≥	0.714 µm
TOP.EN.2.1	DBLK.EN.2.1	Chip_Boundary enclosure Macro in vertical direction	EN2.1	=	0, 0.560+0.028*n µm
TOP.EN.2.1.1	DBLK.EN.2.1.1:*	Chip_Boundary enclosure Fin Grid 112nm Macro in vertical direction	EN2.1.1	=	0, 0.560+0.112*n µm
TOP.EN.2.2.1	DBLK.EN.2.2.1	Chip_Boundary enclosure left edge of Macro in horizontal direction	EN2.2.1	=	0, 0.714+0.102*n µm
TOP.EN.2.2.2	DBLK.EN.2.2.2	Chip_Boundary enclosure right edge of Macro in horizontal direction	EN2.2.2	=	0, ≥0.714 µm
TOP.EN.3.1	DBLK.EN.3.1	Chip_Boundary enclosure TSMC SRAM in vertical direction	EN3.1	=	2.016+0.028*n µm
TOP.EN.3.2	DBLK.EN.3.2	Chip_Boundary enclosure TSMC SRAM in horizontal direction	EN3.2	=	2.040+0.102*n µm

- **In Chip-integration, APR block design guidelines should be applied except some guidelines which have equivalent top guidelines shown in table above**

APR Top Design

Guideline No.	Equivalent G.L. in APR Block	Guideline Description	Label	Op.	Rule
TOP.EN.4.1	DBLK.*.EN.4.1:* DBLK.*.EN.4.1.2:*	Chip_Boundary enclosure H210P51 APR Block with Fin Grid 28nm in vertical direction	EN4.1	=	0.756+0.028*n µm
TOP.EN.4.1.1	DBLK.*.EN.4.1.1:* DBLK.*.EN.4.1.3:*	Chip_Boundary enclosure H210P51 APR Block with Fin Grid 112nm in vertical direction	EN4.1.1	=	0.784+0.112*n µm
TOP.EN.4.1.4	DBLK.*.EN.4.1.4:* DBLK.*.EN.4.1.5:*	Chip_Boundary enclosure all H280P57 APR block in vertical direction	EN4.1.1	=	0.784+0.112*n µm
TOP.EN.4.2	DBLK.*.EN.4.2:* DBLK.*.EN.4.2.2:* DBLK.*.EN.4.2:4:* DBLK.*.EN.4.2:5:*	Chip_Boundary enclosure APR block in horizontal direction	EN4.2	=	0.714+0.102*n µm
TOP.W.1.1	DBLK.*.W.1.1:*	Chip_Boundary width in vertical direction	W1.1	=	0.448+0.112*n µm
TOP.W.1.2	DBLK.*.W.1.2.*	Chip_Boundary width in horizontal direction	W1.2	=	0.765+0.102*n µm

- **In Chip-integration, APR block design guidelines should be applied except some guidelines which have equivalent top guidelines shown in table above**

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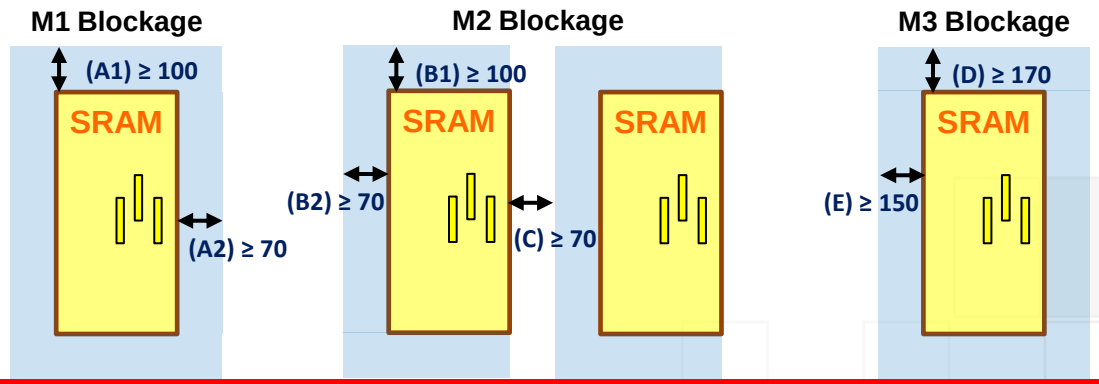
APR Routing Blockage

Chip-integration Design Guideline for PnR
General Section for H210P51 and H280P57

- **Placement**

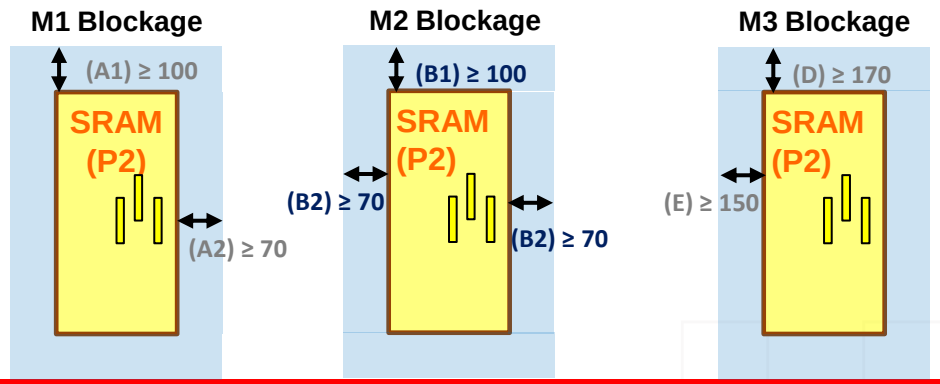
Guidelines of Routing Blockage in APR Block (TSMC SRAM)

Guideline No.	Description	Label	Op.	Rule
DBLK.RBLK.EN.3.1.M1	Width of 0-spacing M1 routing blockage surrounding TSMC SRAM in vertical direction. All TSMC SRAM should be surrounded by 0-sapcing M1 routing blockage	A1	≥	0.1000 µm
DBLK.RBLK.EN.3.2.M1	Width of 0-spacing M1 routing blockage surrounding TSMC SRAM in horizontal direction. All TSMC SRAM should be surrounded by 0-sapcing M1 routing blockage	A2	≥	0.0700 µm
DBLK.RBLK.EN.3.1.M2	Width of 0-spacing M2 routing blockage surrounding TSMC SRAM in vertical direction. All TSMC SRAM should be surrounded by 0-sapcing M2 routing blockage except pin side (except TSMC SRAM Pin Type 2)	B1	≥	0.1000 µm
DBLK.RBLK.EN.3.2.M2	Width of 0-spacing M2 routing blockage surrounding TSMC SRAM in array side. (except TSMC SRAM Pin Type 2)	B2	≥	0.0700 µm
DBLK.RBLK.S.3.2.M2	Space from TSMC SRAM pin side to 0-spacing M2 routing blockage (except TSMC SRAM Pin Type 2)	C	≥	0.0700 µm
DBLK.RBLK.EN.3.1.M3	Width of 0-spacing M3 routing blockage surrounding TSMC SRAM in vertical direction. All TSMC SRAM should be surrounded by 0-sapcing M3 routing blockage	D	≥	0.1700 µm
DBLK.RBLK.EN.3.2.M3	Width of 0-spacing M3 routing blockage surrounding TSMC SRAM in horizontal direction. All TSMC SRAM should be surrounded by 0-sapcing M3 routing blockage	E	≥	0.1500 µm



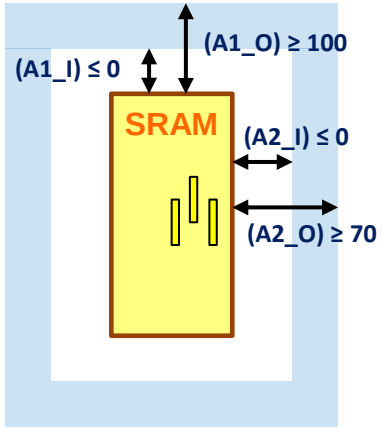
Guidelines of Routing Blockage in APR Block (TSMC SRAM Pin Type 2)

Guideline No.	Description	Label	Op.	Rule
DBLK.RBLK.EN.3.1.M1	Width of 0-spacing M1 routing blockage surrounding TSMC SRAM in vertical direction. All TSMC SRAM should be surrounded by 0-sapcing M1 routing blockage	A1	≥	0.1000 µm
DBLK.RBLK.EN.3.2.M1	Width of 0-spacing M1 routing blockage surrounding TSMC SRAM in horizontal direction. All TSMC SRAM should be surrounded by 0-sapcing M1 routing blockage	A2	≥	0.0700 µm
DBLK.RBLK.EN.3.1.1.M2	Width of 0-spacing M2 routing blockage surrounding TSMC SRAM Pin Type 2 in vertical direction. All TSMC SRAM Pin Type 2 should be surrounded by 0-sapcing M2 routing blockage	B1	≥	0.1000 µm
DBLK.RBLK.EN.3.2.1.M2	Width of 0-spacing M2 routing blockage surrounding TSMC SRAM Pin Type 2 in horizontal direction. All TSMC SRAM Pin Type 2 should be surrounded by 0-sapcing M2 routing blockage	B2	≥	0.0700 µm
DBLK.RBLK.EN.3.1.M3	Width of 0-spacing M3 routing blockage surrounding TSMC SRAM in vertical direction. All TSMC SRAM should be surrounded by 0-sapcing M3 routing blockage	D	≥	0.1700 µm
DBLK.RBLK.EN.3.2.M3	Width of 0-spacing M3 routing blockage surrounding TSMC SRAM in horizontal direction. All TSMC SRAM should be surrounded by 0-sapcing M3 routing blockage	E	≥	0.1500 µm

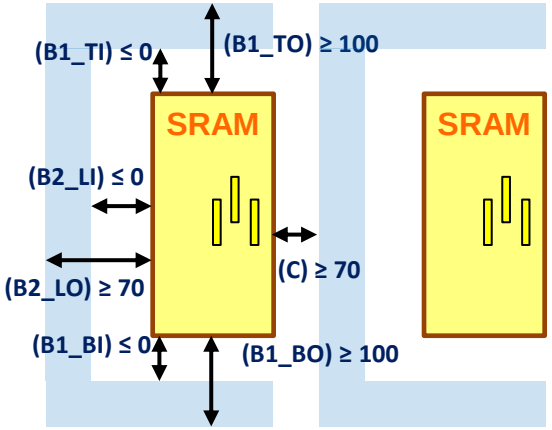


Guidelines of Routing Blockage in APR Block (Rules in tCIC)

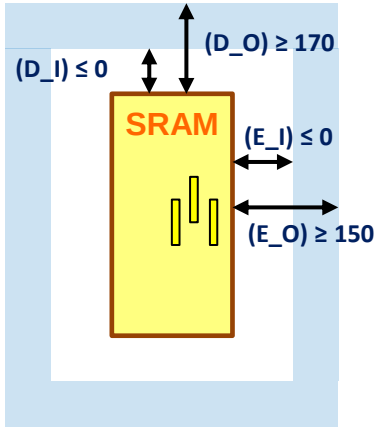
M1 Blockage



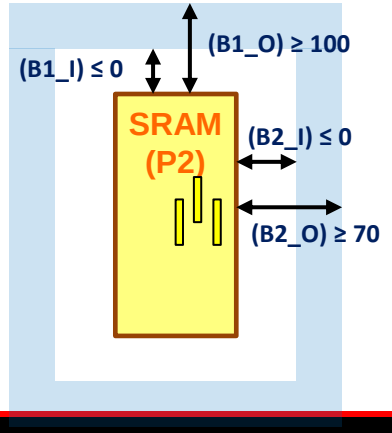
M2 Blockage



M3 Blockage



M2 Blockage



Guidelines of Routing Blockage in APR Block (Rules in tCIC)

Guideline No.	Description	Label	Op.	Rule
DBLK.RBLK.EN.3.1.M1_I	Distance from Inside edge of 0-spacing M1 routing blockage to TSMC SRAM in vertical direction	A1_I	≤	0 µm
DBLK.RBLK.EN.3.1.M1_O	Distance from outside edge of 0-spacing M1 routing blockage to TSMC SRAM in vertical direction	A1_O	≥	0.100 µm
DBLK.RBLK.EN.3.2.M1_I	Distance from Inside edge of 0-spacing M1 routing blockage to TSMC SRAM in horizontal direction	A2_I	≤	0 µm
DBLK.RBLK.EN.3.2.M1_O	Distance from outside edge of 0-spacing M1 routing blockage to TSMC SRAM in horizontal direction	A2_O	≥	0.070 µm
DBLK.RBLK.EN.3.1.M2_TI	Distance from Inside edge of 0-spacing M2 routing blockage to top edge of TSMC SRAM in vertical direction (except TSMC SRAM Pin Type 2)	B1_TI	≤	0 µm
DBLK.RBLK.EN.3.1.M2_TO	Distance from outside edge of 0-spacing M2 routing blockage to top edge of TSMC SRAM in vertical direction (except TSMC SRAM Pin Type 2)	B1_TO	≥	0.100 µm
DBLK.RBLK.EN.3.1.M2_BI	Distance from Inside edge of 0-spacing M2 routing blockage to bottom edge of TSMC SRAM in vertical direction (except TSMC SRAM Pin Type 2)	B1_BI	≤	0 µm
DBLK.RBLK.EN.3.1.M2_BO	Distance from outside edge of 0-spacing M2 routing blockage to bottom edge of TSMC SRAM in vertical direction (except TSMC SRAM Pin Type 2)	B1_BO	≥	0.100 µm
DBLK.RBLK.EN.3.2.M2_LI	Distance from Inside edge of 0-spacing M2 routing blockage to left edge of TSMC SRAM in horizontal direction (except TSMC SRAM Pin Type 2)	B2_LI	≤	0 µm
DBLK.RBLK.EN.3.2.M2_LO	Distance from outside edge of 0-spacing M2 routing blockage to left edge of TSMC SRAM in horizontal direction (except TSMC SRAM Pin Type 2)	B2_LO	≥	0.070 µm
DBLK.RBLK.S.3.2.M2	Space from TSMC SRAM pin side to 0-spacing M2 routing blockage (except TSMC SRAM Pin Type 2)	C	≥	0.070 µm
DBLK.RBLK.EN.3.1.M3_I	Distance from Inside edge of 0-spacing M3 routing blockage to TSMC SRAM in vertical direction	D_I	≤	0 µm
DBLK.RBLK.EN.3.1.M3_O	Distance from outside edge of 0-spacing M3 routing blockage to TSMC SRAM in vertical direction	D_O	≥	0.170 µm
DBLK.RBLK.EN.3.2.M3_I	Distance from Inside edge of 0-spacing M3 routing blockage to TSMC SRAM in horizontal direction	E_I	≤	0 µm
DBLK.RBLK.EN.3.2.M3_O	Distance from outside edge of 0-spacing M3 routing blockage to TSMC SRAM in horizontal direction	E_O	≥	0.150 µm
DBLK.RBLK.EN.3.1.1.M2_I	Distance from Inside edge of 0-spacing M2 routing blockage to TSMC SRAM Pin Type 2 in vertical direction	B1_I	≤	0 µm
DBLK.RBLK.EN.3.1.1.M2_O	Distance from outside edge of 0-spacing M2 routing blockage to TSMC SRAM Pin Type 2 in vertical direction	B1_O	≥	0.100 µm
DBLK.RBLK.EN.3.2.1.M2_I	Distance from Inside edge of 0-spacing M2 routing blockage to TSMC SRAM Pin Type 2 in horizontal direction	B2_I	≤	0 µm
DBLK.RBLK.EN.3.2.1.M2_O	Distance from outside edge of 0-spacing M2 routing blockage to TSMC SRAM Pin Type 2 in horizontal direction	B2_O	≥	0.070 µm

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Latch-up Prevention Guideline around OD Injector

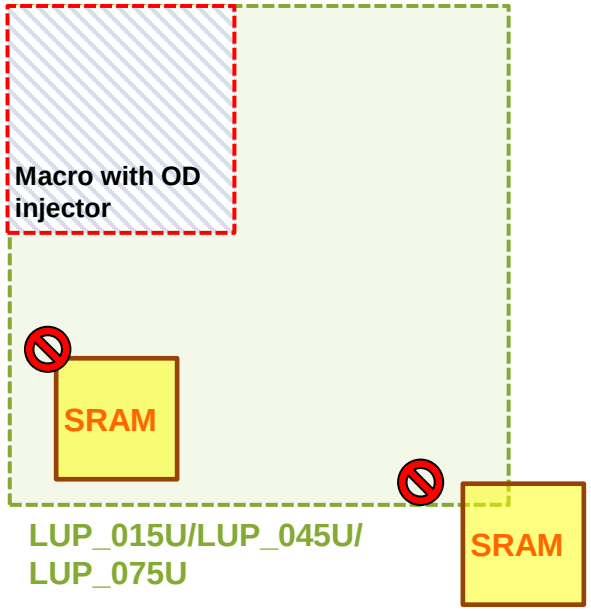
Chip-integration Design Guideline for PnR General Section for H210P51 and H280P57

- Placement

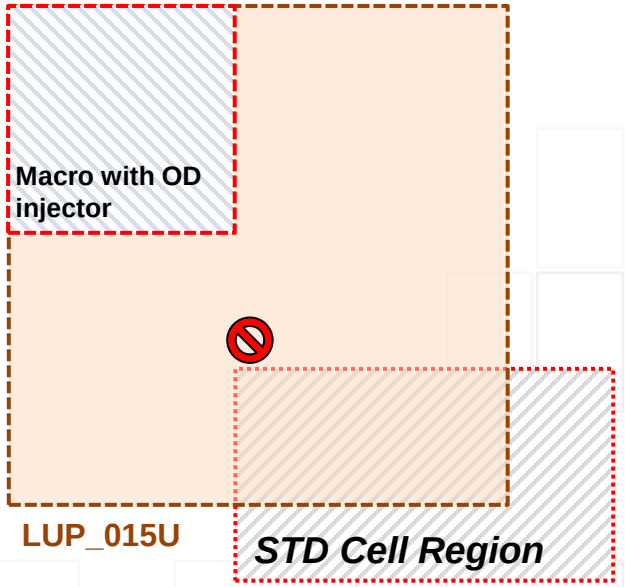
Implementation Guideline Around OD injector

Guideline No.	Description	Label	Op.	Rule
DBLK.LUP.R.1	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_015U, LUP_015U_P, LUP_015U_N LUP_045U, LUP_075U, LUP_045U_18V, LUP_075U_18V, LUP_045U_15V, LUP_075U_15V, LUP_045U_IHIA, LUP_075U_IHIA, LUP_045U_18V_IHIA, LUP_075U_18V_IHIA, LUP_045U_15V_IHIA, LUP_075U_15V_IHIA			
DBLK.LUP.R.2	Forbid STD Cell Region overlap with following LUP marker layers: LUP_015U, LUP_015U_P, LUP_015U_N,			

DBLK.LUP.R.1



DBLK.LUP.R.2



Implementation Guideline Around OD injector (tCIC Rule Codes)

Guideline No.	Description	Label	Op.	Rule
DBLK.LUP.R.1_LUP_015U	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_015U			
DBLK.LUP.R.1_LUP_015U_P	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_015U_P			
DBLK.LUP.R.1_LUP_015U_N	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_015U_N			
DBLK.LUP.R.1_LUP_045U	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_045U			
DBLK.LUP.R.1_LUP_075U	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_075U			
DBLK.LUP.R.1_LUP_045U_18V	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_045U_18V			
DBLK.LUP.R.1_LUP_075U_18V	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_075U_18V			
DBLK.LUP.R.1_LUP_045U_15V	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_045U_15V			
DBLK.LUP.R.1_LUP_075U_15V	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_075U_15V			
DBLK.LUP.R.1_LUP_045U_IHIA	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_045U_IHIA			
DBLK.LUP.R.1_LUP_075U_IHIA	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_075U_IHIA			
DBLK.LUP.R.1_LUP_045U_18V_IHIA	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_045U_18V_IHIA			
DBLK.LUP.R.1_LUP_075U_18V_IHIA	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_075U_18V _IHIA			
DBLK.LUP.R.1_LUP_045U_15V_IHIA	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_045U_15V_IHIA			
DBLK.LUP.R.1_LUP_075U_15V_IHIA	Forbid TSMC SRAM overlap with following LUP marker layers: LUP_075U_15V_IHIA			
DBLK.LUP.R.2_LUP_015U	Forbid STD Cell Region overlap with following LUP marker layers: LUP_015U			
DBLK.LUP.R.2_LUP_015U_P	Forbid STD Cell Region overlap with following LUP marker layers: LUP_015U_P			
DBLK.LUP.R.2_LUP_015U_N	Forbid STD Cell Region overlap with following LUP marker layers: LUP_015U_N			

Unleash Innovation

TSMC ESD Clamp Guideline

Chip-integration Design Guideline for PnR
General Section for H210P51 and H280P57

- **Placement**

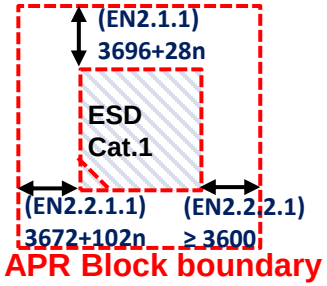
Guidelines of TSMC ESD Clamp

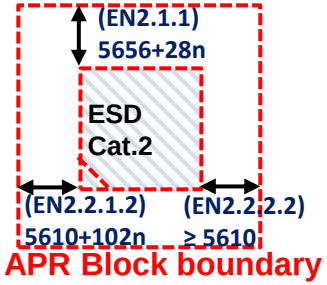
- **TSMC ESD Clamp are separated into 3 groups**
  - **Cat.1 / Cat.2 / Cat.3 with different keep out zone requirement**
  - **Required KOZ: Cat.2 > Cat.1 > Cat.3**

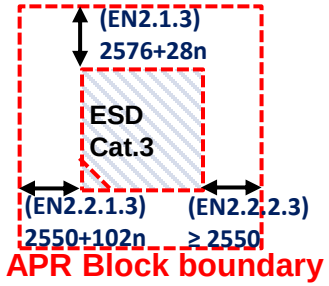
Table of TSMC ESD Clamp Macro & Guideline usage

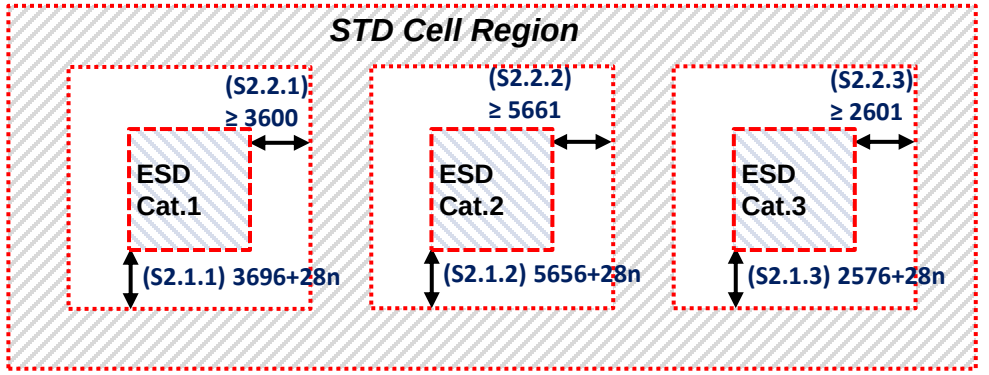
Macro Name	ESD Macro type in Guideline
ESD_PCLAMP_1V8_N1_H	ESD Clamp Category 2
ESD_PCLAMP_CORE_CDM_N1_V	ESD Clamp Category 1
ESD_PCLAMP_CORE_N1_H	ESD Clamp Category 2
ESD_PCLAMP_CORE_N1_V	ESD Clamp Category 1
ESD_PCLAMP_IO_P1_H	ESD Clamp Category 2
ESD_PCLAMP_IO_P1_V	ESD Clamp Category 2
ESD_PCLAMP_3V3_P1_V_M*	ESD Clamp Category 3

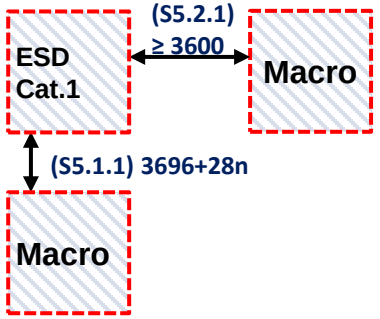
Guidelines of TSMC ESD Clamp

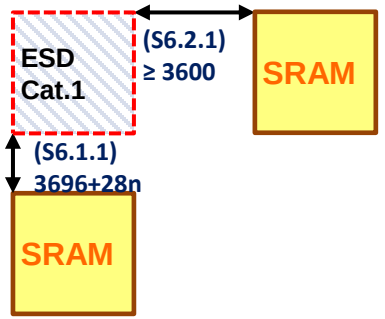


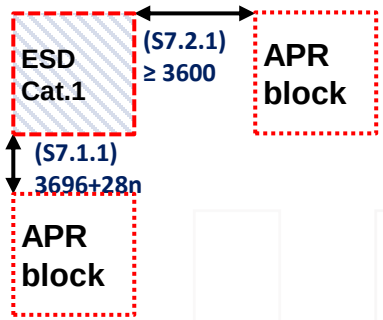


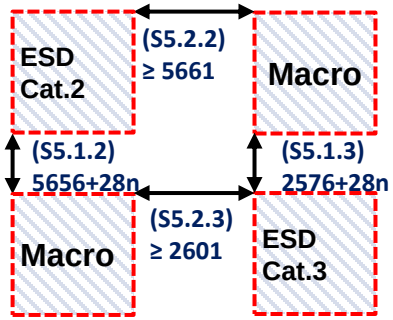


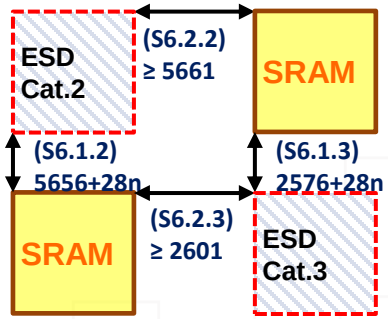


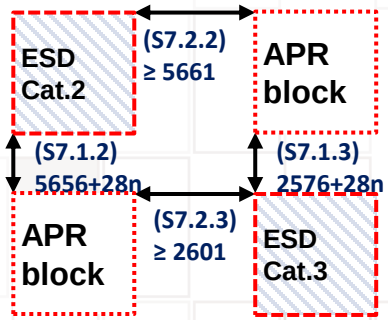












Guidelines of TSMC ESD Clamp

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.EN.2.1.ESD_C1	Block edge enclosure TSMC ESD Clamp Category 1 in vertical direction	**EN2.1.1**	=	3.696+0.028*n µm
DBLK.EN.2.1.ESD_C2	Block edge enclosure TSMC ESD Clamp Category 2 in vertical direction	**EN2.1.1**	=	5.656+0.028*n µm
DBLK.EN.2.1.ESD_C3	Block edge enclosure TSMC ESD Clamp Category 3 in vertical direction	**EN2.1.1**	=	2.576+0.028*n µm
DBLK.EN.2.2.1.ESD_C1	Block edge enclosure Left edge of TSMC ESD Clamp Category 1 in horizontal direction	**EN2.2.1.1**	=	3.672+0.102*n µm
DBLK.EN.2.2.1.ESD_C2	Block edge enclosure Left edge of TSMC ESD Clamp Category 2 in horizontal direction	**EN2.2.1.2**	=	5.610+0.102*n µm
DBLK.EN.2.2.1.ESD_C3	Block edge enclosure Left edge of TSMC ESD Clamp Category 3 in horizontal direction	**EN2.2.1.3**	=	2.550+0.102*n µm
DBLK.EN.2.2.2.ESD_C1	Block edge enclosure Right edge of TSMC ESD Clamp Category 1 in horizontal direction	**EN2.2.2.1**	≥	3.600 µm
DBLK.EN.2.2.2.ESD_C2	Block edge enclosure Right edge of TSMC ESD Clamp Category 2 in horizontal direction	**EN2.2.2.2**	≥	5.610 µm
DBLK.EN.2.2.2.ESD_C3	Block edge enclosure Right edge of TSMC ESD Clamp Category 3 in horizontal direction	**EN2.2.2.3**	≥	2.550 µm
DBLK.S.2.1.ESD_C1	TSMC ESD Clamp Category 1 to STD cell region spacing in vertical direction (PRL>-3.6µm)	**S2.1.1**	=	3.696+0.028*n µm
DBLK.S.2.1.ESD_C2	TSMC ESD Clamp Category 2 to STD cell region spacing in vertical direction (PRL>-5.661µm)	**S2.1.2**	=	5.656+0.028*n µm
DBLK.S.2.1.ESD_C3	TSMC ESD Clamp Category 3 to STD cell region spacing in vertical direction (PRL>-2.601µm)	**S2.1.3**	=	2.576+0.028*n µm
DBLK.S.2.2.ESD_C1	TSMC ESD Clamp Category 1 to STD cell region spacing in horizontal direction (PRL>-3.696µm)	**S2.2.1**	≥	3.600 µm
DBLK.S.2.2.ESD_C2	TSMC ESD Clamp Category 2 to STD cell region spacing in horizontal direction (PRL>-5.656µm)	**S2.2.2**	≥	5.661 µm
DBLK.S.2.2.ESD_C3	TSMC ESD Clamp Category 3 to STD cell region spacing in horizontal direction (PRL>-2.576µm)	**S2.2.3**	≥	2.601 µm
DBLK.S.5.1.ESD_C1	Spacing from Macro to TSMC ESD Clamp Category 1 in vertical direction (PRL>-3.6µm)	**S5.1.1**	=	3.696+0.028*n µm
DBLK.S.5.1.ESD_C2	Spacing from Macro to TSMC ESD Clamp Category 2 in vertical direction (PRL>-5.661µm)	**S5.1.2**	=	5.656+0.028*n µm
DBLK.S.5.1.ESD_C3	Spacing from Macro to TSMC ESD Clamp Category 3 in vertical direction (PRL>-2.601µm)	**S5.1.3**	=	2.576+0.028*n µm
DBLK.S.5.2.ESD_C1	Spacing from Macro to TSMC ESD Clamp Category 1 in horizontal direction (PRL>-3.696µm)	**S5.2.1**	≥	3.600 µm
DBLK.S.5.2.ESD_C2	Spacing from Macro to TSMC ESD Clamp Category 2 in horizontal direction (PRL>-5.656µm)	**S5.2.2**	≥	5.661 µm
DBLK.S.5.2.ESD_C3	Spacing from Macro to TSMC ESD Clamp Category 3 in horizontal direction (PRL>-2.576µm)	**S5.2.3**	≥	2.601 µm

Guidelines of TSMC ESD Clamp

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.S.6.1.ESD_C1	Spacing from TSMC SRAM to TSMC ESD Clamp Category 1 in vertical direction (PRL>-3.6μm)	**S6.1.1**	=	3.696+0.028*n μm
DBLK.S.6.1.ESD_C2	Spacing from TSMC SRAM to TSMC ESD Clamp Category 2 in vertical direction (PRL>-5.661μm)	**S6.1.2**	=	5.656+0.028*n μm
DBLK.S.6.1.ESD_C3	Spacing from TSMC SRAM to TSMC ESD Clamp Category 3 in vertical direction (PRL>-2.601μm)	**S6.1.3**	=	2.576+0.028*n μm
DBLK.S.6.2.ESD_C1	Spacing from TSMC SRAM to TSMC ESD Clamp Category 1 in horizontal direction (PRL>-3.696μm)	**S6.2.1**	≥	3.600 μm
DBLK.S.6.2.ESD_C2	Spacing from TSMC SRAM to TSMC ESD Clamp Category 2 in horizontal direction (PRL>-5.656μm)	**S6.2.2**	≥	5.661 μm
DBLK.S.6.2.ESD_C3	Spacing from TSMC SRAM to TSMC ESD Clamp Category 3 in horizontal direction (PRL>-2.576μm)	**S6.2.3**	≥	2.601 μm
DBLK.S.7.1.ESD_C1	Spacing from APR block to TSMC ESD Clamp Category 1 in vertical direction (PRL>-3.6μm)	**S7.1.1**	=	3.696+0.028*n μm
DBLK.S.7.1.ESD_C2	Spacing from APR block to TSMC ESD Clamp Category 2 in vertical direction (PRL>-5.661μm)	**S7.1.2**	=	5.656+0.028*n μm
DBLK.S.7.1.ESD_C3	Spacing from APR block to TSMC ESD Clamp Category 3 in vertical direction (PRL>-2.601μm)	**S7.1.3**	=	2.576+0.028*n μm
DBLK.S.7.2.ESD_C1	Spacing from APR block to TSMC ESD Clamp Category 1 in horizontal direction (PRL>-3.696μm)	**S7.2.1**	≥	3.600 μm
DBLK.S.7.2.ESD_C2	Spacing from APR block to TSMC ESD Clamp Category 2 in horizontal direction (PRL>-5.656μm)	**S7.2.2**	≥	5.661 μm
DBLK.S.7.2.ESD_C3	Spacing from APR block to TSMC ESD Clamp Category 3 in horizontal direction (PRL>-2.576μm)	**S7.2.3**	≥	2.601 μm

Unleash Innovation

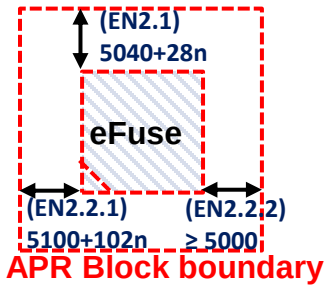
TSMC eFuse Guideline

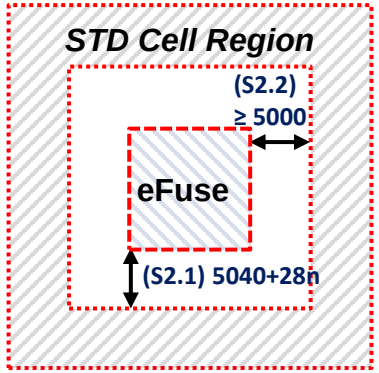
Chip-integration Design Guideline for PnR
General Section for H210P51 and H280P57

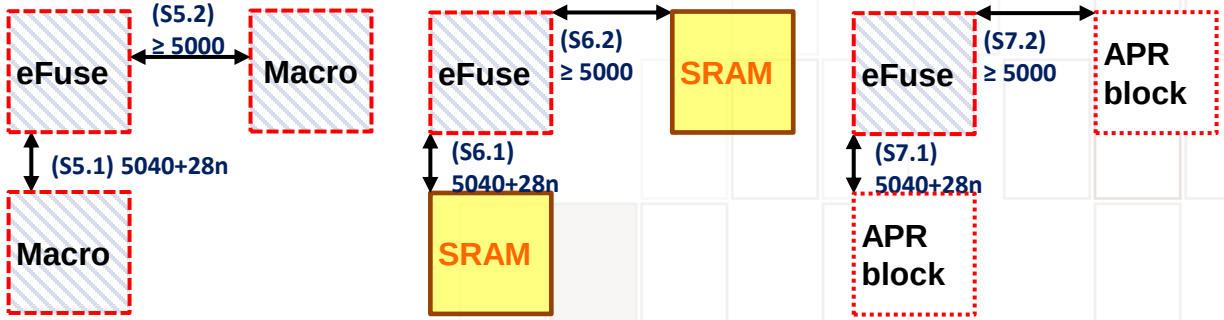
- **Placement**

Guidelines of TSMC eFuse

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.EN.2.1.EFUSE	Block edge enclosure TSMC eFuse in vertical direction	**EN2.1**	=	5.040+0.028*n µm
DBLK.EN.2.2.1.EFUSE	Block edge enclosure Left edge of TSMC eFuse in horizontal direction	**EN2.2.1**	=	5.100+0.102*n µm
DBLK.EN.2.2.2.EFUSE	Block edge enclosure Right edge of TSMC eFuse in horizontal direction	**EN2.2.2**	≥	5.000 µm
DBLK.S.2.1.EFUSE	TSMC eFuse to STD cell region spacing in vertical direction (PRL>-5µm)	**S2.1**	=	5.040+0.028*n µm
DBLK.S.2.2.EFUSE	TSMC eFuse to STD cell region spacing in horizontal direction (PRL>-5.04µm)	**S2.2**	≥	5.000 µm
DBLK.S.5.1.EFUSE	Spacing from Macro to TSMC eFuse in vertical direction (PRL>-5µm)	**S5.1**	=	5.040+0.028*n µm
DBLK.S.5.2.EFUSE	Spacing from Macro to TSMC eFuse in horizontal direction (PRL>-5.04µm)	**S5.2**	≥	5.000 µm
DBLK.S.6.1.EFUSE	Spacing from TSMC SRAM to TSMC eFuse in vertical direction (PRL>-5µm)	**S6.1**	=	5.040+0.028*n µm
DBLK.S.6.2.EFUSE	Spacing from TSMC SRAM to TSMC eFuse in horizontal direction (PRL>-5.04µm)	**S6.2**	≥	5.000 µm
DBLK.S.7.1.EFUSE	Spacing from APR block to TSMC eFuse in vertical direction (PRL>-5µm)	**S7.1**	=	5.040+0.028*n µm
DBLK.S.7.2.EFUSE	Spacing from APR block to TSMC eFuse in horizontal direction (PRL>-5.04µm)	**S7.2**	≥	5.000 µm







Unleash Innovation

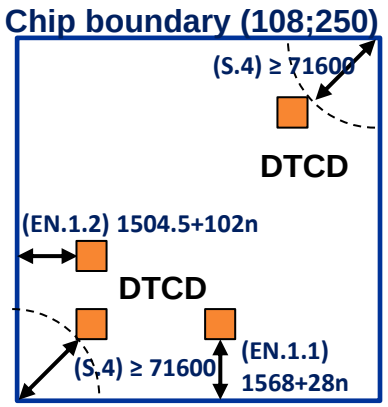
DTCD/ICOVL Insertion

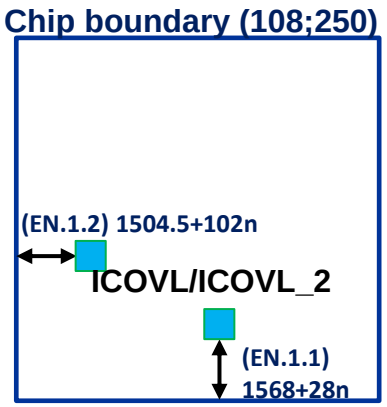
Chip-integration Design Guideline for PnR
General Section for H210P51 and H280P57

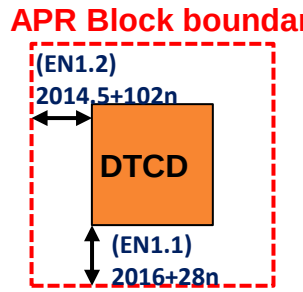
- Reliability & Manufacturing

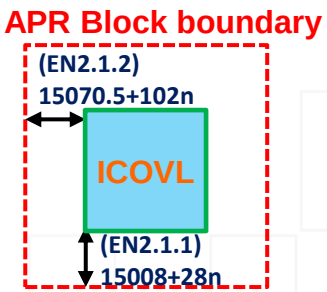
Guideline of DTCD/ICOVL for Chip-Int.

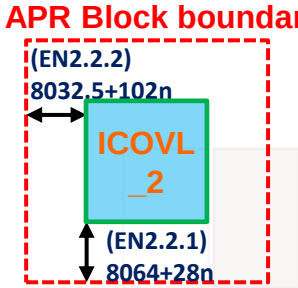
Guideline No.	Equivalent G.L. in Block Level	Guideline Description	Label	Op.	Rule
TOP.DTCD.EN.1.1	DBLK.DTCD.EN.1.1 DBLK.DTCD.EN.2.1.1 DBLK.DTCD.EN.2.2.1	Chip_Boundary enclosure DTCD/ICOVL/ICOVL_2 in vertical direction	**EN.1.1**	=	1.568+0.028*n µm
TOP.DTCD.EN.1.2	DBLK.DTCD.EN.1.2 DBLK.DTCD.EN.2.1.2 DBLK.DTCD.EN.2.2.2	Chip_Boundary enclosure DTCD/ICOVL/ICOVL_2 in horizontal direction	**EN.1.2**	=	1.5045+0.102*n µm
TOP.DTCD.S.4		Spacing of DTCD to corner of chip_boundary	**S.4**	≥	71.600 µm











Guideline of DTCD for IP

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.DTCD.EN.1.1	APR Block edge enclosure DTCD in vertical direction	**EN1.1**	=	2.016+0.028*n μm
DBLK.DTCD.EN.1.2	APR Block edge enclosure DTCD in horizontal direction	**EN1.2**	=	2.0145+0.102*n μm
DBLK.DTCD.EN.2.1.1	APR Block edge enclosure ICOVL in vertical direction	**EN2.1.1**	=	15.008+0.028*n μm
DBLK.DTCD.EN.2.1.2	APR Block edge enclosure ICOVL in horizontal direction	**EN2.1.2**	=	15.0705+0.102*n μm
DBLK.DTCD.EN.2.2.1	APR Block edge enclosure ICOVL_2 in vertical direction	**EN2.2.1**	=	8.064+0.028*n μm
DBLK.DTCD.EN.2.2.2	APR Block edge enclosure ICOVL_2 in horizontal direction	**EN2.2.2**	=	8.0325+0.102*n μm

Diagram of DTCD /ICOVL Guidelines

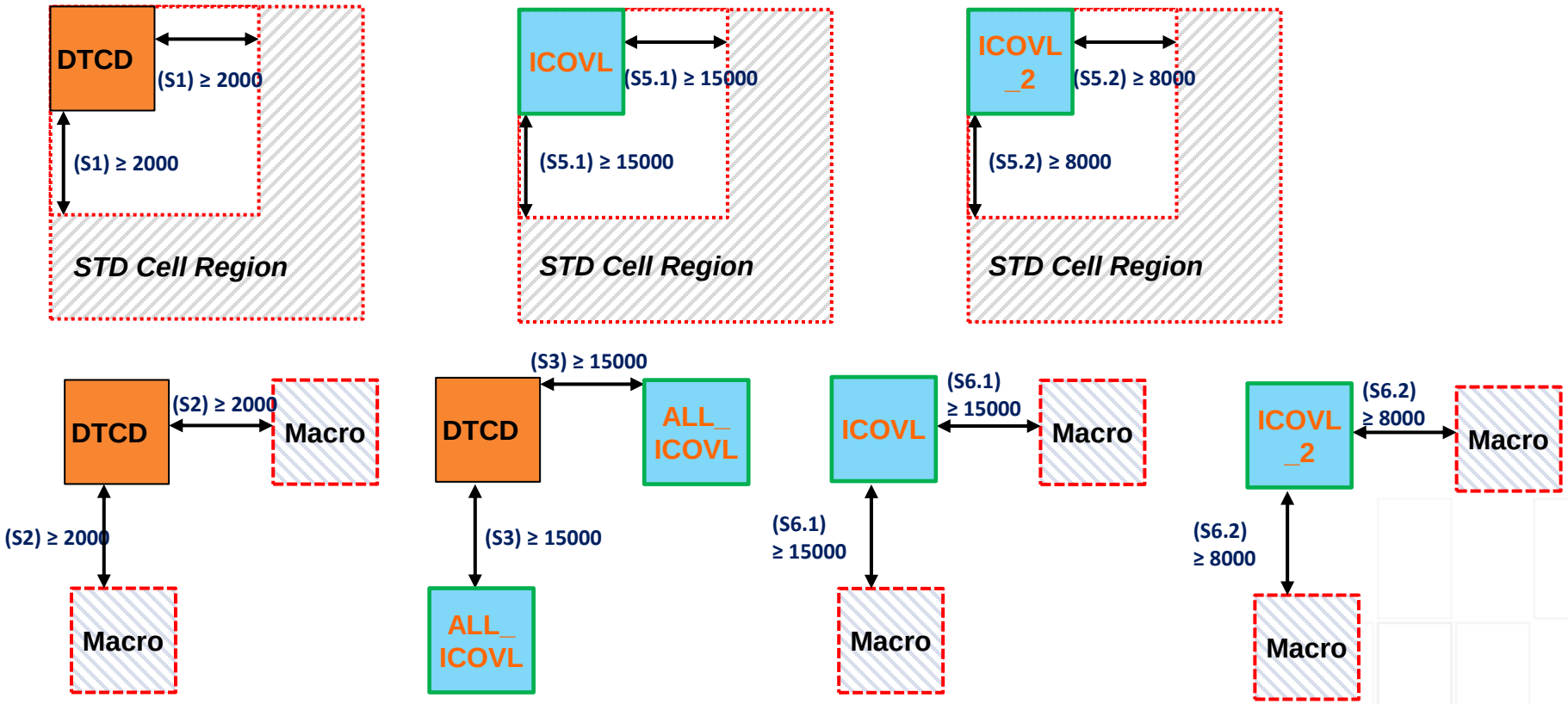


Diagram of DTCD /ICOVL Guidelines

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.DTCD.S.1	Spacing of DTCD to STD cell region	S1	≥	2.000 µm
DBLK.DTCD.S.2	Spacing of DTCD to Macro	S2	≥	2.000 µm
DBLK.DTCD.S.3	Spacing of DTCD to ICOVL/ICOVL_2	S3	≥	15.000 µm
DBLK.DTCD.S.5.1	Spacing of ICOVL to STD cell region	S5.1	≥	15.000 µm
DBLK.DTCD.S.5.2	Spacing of ICOVL_2 to STD cell region	S5.1	≥	8.000 µm
DBLK.DTCD.S.6.1	Spacing of ICOVL to Macro	S6.2	≥	15.000 µm
DBLK.DTCD.S.6.2	Spacing of ICOVL_2 to Macro	S6.2	≥	8.000 µm
DBLK.DTCD.EN.3.1	Metal routing blockage enclosure DTCD. All DTCD should be surrounded by 0-spacing Metal routing blockage n M1,Mx,Mxb, Mxd, Mxe, Mya, Myb, My layers	EN.3.1	≥	1.000 µm
DBLK.DTCD.EN.3.2	Metal routing blockage enclosure ICOVL/ICOVL_2. Any ICOVL/ICOVL_2 should be surrounded by 0-spacing Metal routing blockage on M1,Mx,Mxb, Mxd, Mxe, Mya, Myb, My layers	EN.3.2	≥	8.000 µm

Unleash Innovation

Chip-integration Design Guideline for APR

Specific Section for H210P51

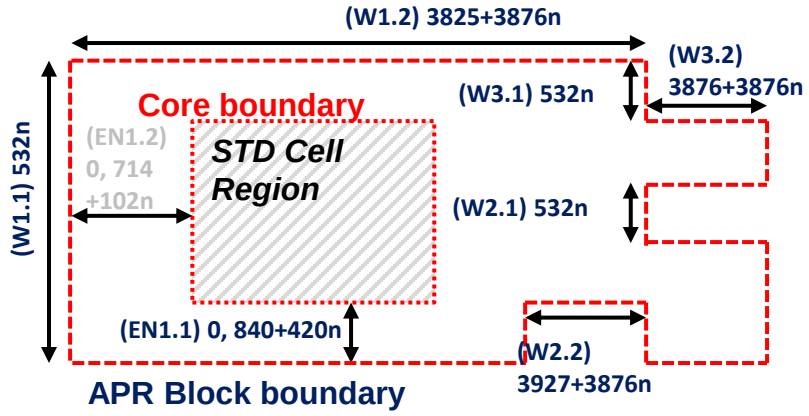
Unleash Innovation

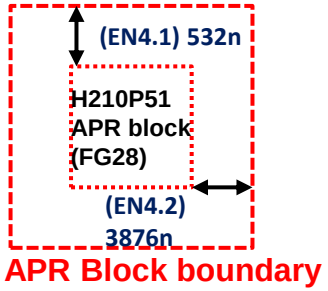
P76 Track Alignment

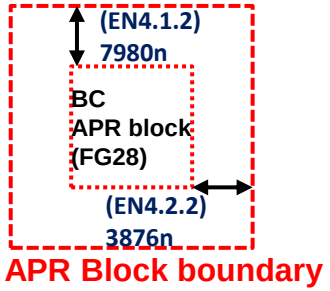
Chip-integration Design Guideline for APR
Specific Section for H210P51

- Track and Row

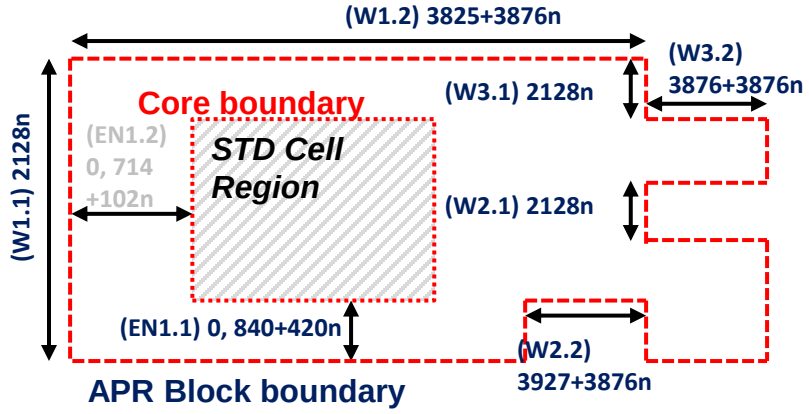
Guideline of Track Alignment (H210P51 FG28)

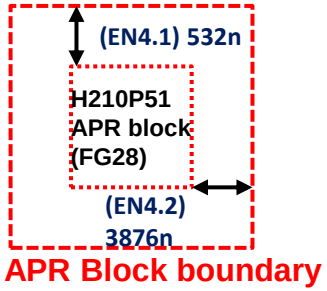


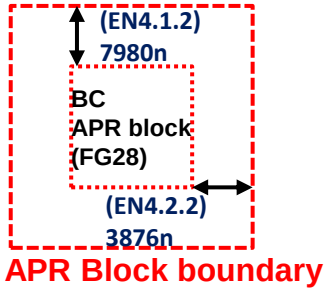


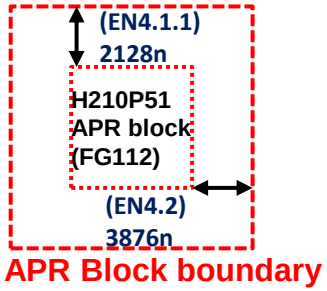


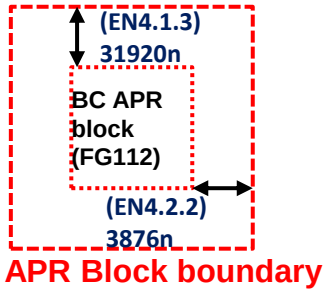
Guideline of Track Alignment (H210P51 FG112)



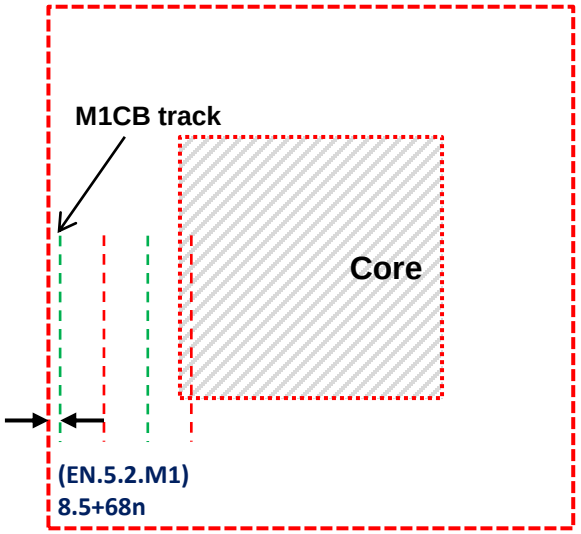


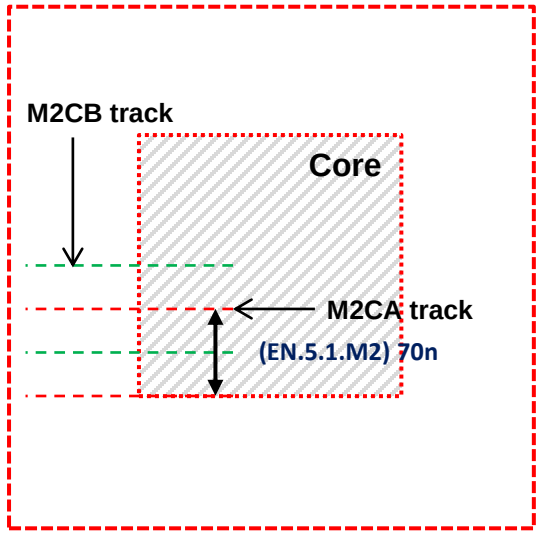


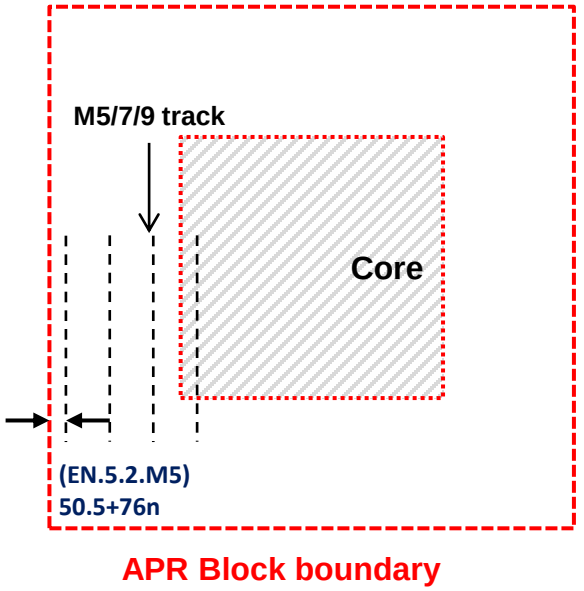


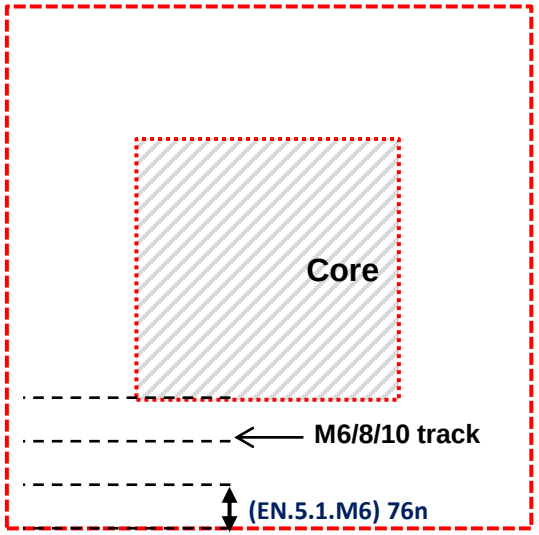


Guideline of Track Alignment (H210P51)









Guideline of Track Alignment (H210P51 FG28)

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.W.1.1:FG28_ALP76	Width of H210P51 APR Block with Fin Grid 28nm in vertical direction	**W1.1**	=	0.532*n µm
DBLK.H210P51.W.1.2:ALP76	Width of H210P51 APR Block in horizontal direction	**W1.2**	=	3.825+3.876*n µm
DBLK.H210P51.W.2.1:FG28_ALP76	Vertical edge length of H210P51 APR Block with Fin Grid 28nm between two consecutive 270-270 degree corners	**W2.1**	=	0.532*n µm
DBLK.H210P51.W.2.2:ALP76	Horizontal edge length of H210P51 APR block between two consecutive 270-270 degree corners	**W2.2**	=	3.927+3.876*n µm
DBLK.H210P51.W.3.1:FG28_ALP76	Vertical edge length of H210P51 APR Block with Fin Grid 28nm between two consecutive 90-270 degree corners	**W3.1**	=	0.532*n µm
DBLK.H210P51.W.3.2:ALP76	Horizontal edge length of H210P51 APR block between two consecutive 90-270 degree corners	**W3.2**	=	3.876+3.876*n µm
DBLK.H210P51.EN.1.1:ALP76	In H210P51 APR block, Block edge enclosure H210P51 STD cell region in vertical direction	**EN1.1**	=	0, 0.840+0.420*n µm
DBLK.H210P51.EN.4.1:FG28_ALP76	In H210P51 APR block, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 28nm in vertical direction	**EN4.1**	=	0.532*n µm
DBLK.H210P51.EN.4.1.2:FG28_ALP76	In H210P51 APR block, Block edge enclosure BC H210P51 APR block with Fin Grid 28nm in vertical direction	**EN4.1.2**	=	7.980*n µm
DBLK.H210P51.EN.4.2:ALP76	In H210P51 APR block, Block edge enclosure H210P51 APR block w/o Boundary Controlled in horizontal direction	**EN4.2**	=	3.876*n µm
DBLK.H210P51.EN.4.2.2:ALP76	In H210P51 APR block, Block edge enclosure Boundary Controlled H210P51 APR block in horizontal direction	**EN4.2.2**	=	3.876*n µm

Guideline of Track Alignment (H210P51 FG28 & FG112)

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.EN.5.1.M2	In H210P51 APR block, Core enclosure horizontal M2CA track in vertical direction	**EN.5.1.M2**	=	0.070*n μm
DBLK.EN.5.1.M6:ALP76	Block boundary enclosure horizontal M6 track in vertical direction	**EN.5.1.M6**	=	0.076*n μm
DBLK.EN.5.1.M8:ALP76	Block boundary enclosure horizontal M8 track in vertical direction	**EN.5.1.M6**	=	0.076*n μm
DBLK.EN.5.1.M10:ALP76	Block boundary enclosure horizontal M10 track in vertical direction	**EN.5.1.M6**	=	0.076*n μm
DBLK.H210P51.EN.5.2.M1	In H210P51 APR block, Block boundary enclosure vertical M1CB track in horizontal direction	**EN.5.2.M1**	=	0.0085+0.068*n μm
DBLK.EN.5.2.M5:ALP76	Block boundary enclosure vertical M5 track in horizontal direction	**EN.5.2.M5**	=	0.0505+0.076*n μm
DBLK.EN.5.2.M7:ALP76	Block boundary enclosure vertical M7 track in horizontal direction	**EN.5.2.M5**	=	0.0505+0.076*n μm
DBLK.EN.5.2.M9:ALP76	Block boundary enclosure vertical M9 track in horizontal direction	**EN.5.2.M5**	=	0.0505+0.076*n μm

Guideline of Track Alignment (H210P51 FG112)

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.W.1.1:FG112_ALP76	Width of H210P51 APR Block with Fin Grid 112nm in vertical direction	W1.1	=	2.128*n µm
DBLK.H210P51.W.1.2:ALP76	Width of H210P51 APR Block in horizontal direction	W1.2	=	3.825+3.876*n µm
DBLK.H210P51.W.2.1:FG112_ALP76	Vertical edge length of H210P51 APR Block with Fin Grid 112nm between two consecutive 270-270 degree corners	W2.1	=	2.128*n µm
DBLK.H210P51.W.2.2:ALP76	Horizontal edge length of H210P51 APR Block between two consecutive 270-270 degree corners	W2.2	=	3.927+3.876*n µm
DBLK.H210P51.W.3.1:FG112_ALP76	Vertical edge length of H210P51 APR Block with Fin Grid 112nm between two consecutive 90-270 degree corners	W3.1	=	2.128*n µm
DBLK.H210P51.W.3.2:ALP76	Horizontal edge length of H210P51 APR Block between two consecutive 90-270 degree corners	W3.2	=	3.876+3.876*n µm
DBLK.H210P51.EN.1.1:ALP76	In H210P51 APR block, Block edge enclosure H210P51 STD cell region in vertical direction	EN1.1	=	0, 0.840+0.420*n µm
DBLK.H210P51.EN.4.1:FG112_ALP76	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1	=	0.532*n µm
DBLK.H210P51.EN.4.1.1:FG112_ALP76	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure Non-BC H210P51 H210P51 APR Block with Fin Grid 112nm in vertical direction	EN4.1.1	=	2.128*n µm
DBLK.H210P51.EN.4.1.2:FG112_ALP76	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1.2	=	7.980*n µm
DBLK.H210P51.EN.4.1.3:FG112_ALP76	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.3	=	31.92*n µm
DBLK.H210P51.EN.4.2:ALP76	In H210P51 APR block, Block edge enclosure H210P51 APR block w/o Boundary Controlled in horizontal direction	EN4.2	=	3.876*n µm
DBLK.H210P51.EN.4.2.2:ALP76	In H210P51 APR block, Block edge enclosure Boundary Controlled H210P51 APR block in horizontal direction	EN4.2.2	=	3.876*n µm

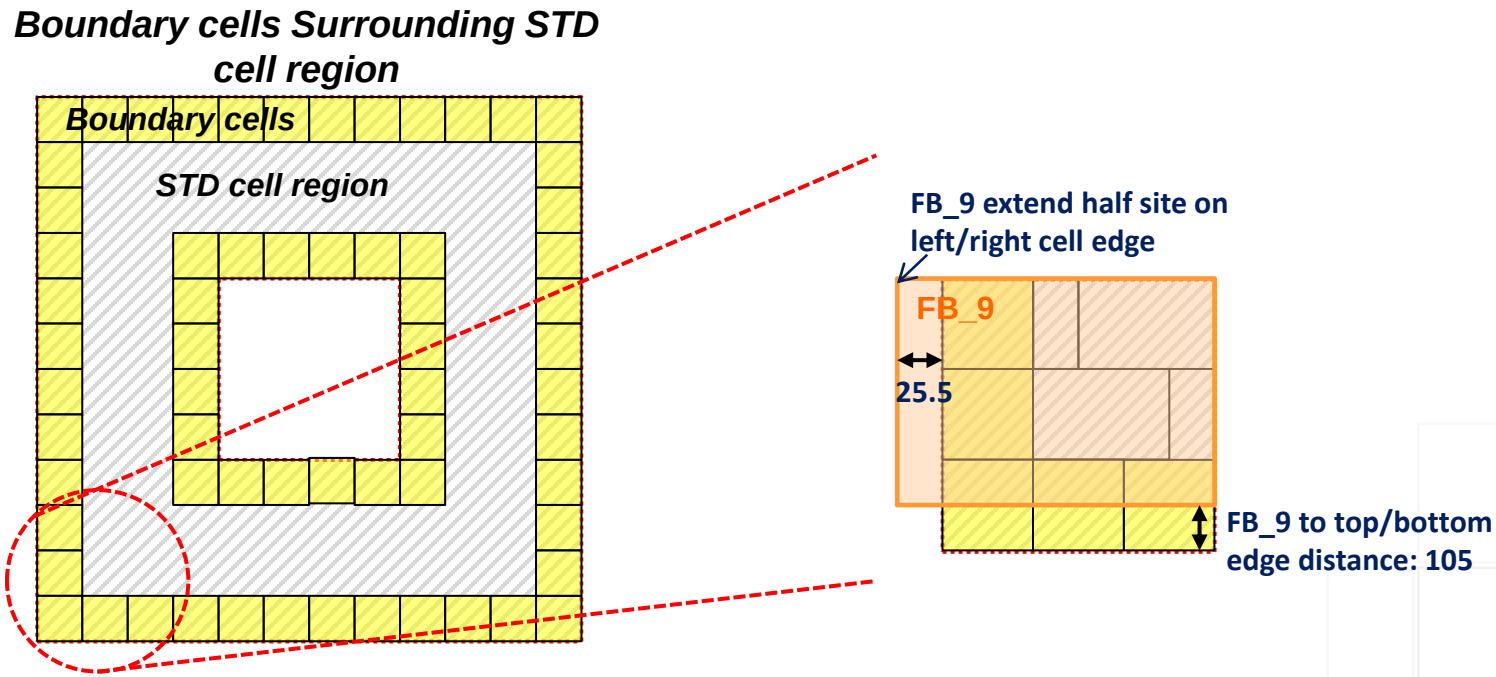
Unleash Innovation

H210P51 STD-Cell Region

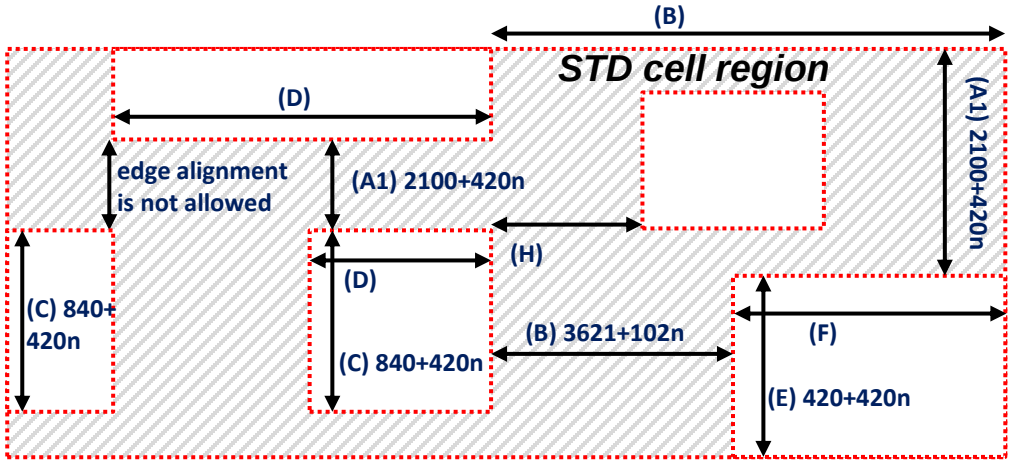
Chip-integration Design Guideline for APR
Specific Section for H210P51

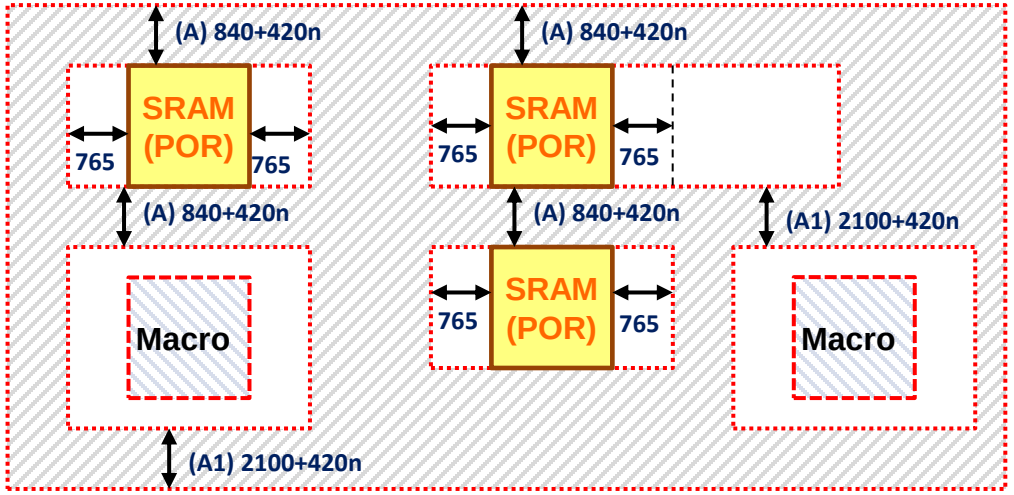
- Dimension and Enclosure

H210P51 APR Block: FB_9 Region



H210P51 APR Block: STD Cell Region





Rule	Label	Boundary Cell Type	
		IW (Default)	CW
Width	(B)	3.621+0.102*n	3.111+0.102*n
Hole width	(D)	0.969+0.102*n	0.969+0.102*n
Jog length	(F)	1.020+0.102*n	0.714+0.102*n
Concave width	(H)	3.621+0.102*n	3.111+0.102*n

IW: Isolated NWELL boundary cell
CW: Common NWELL boundary cell

H210P51 APR Block: STD Cell Region

Default Guideline

Guideline No.	Guideline Description	Label	Op.	Rule
CORE.R.1	Boundary cell must surrounded on all edges of STD cell region	-		
CORE.H210P51.W.1.1	Width of H210P51 STD cell region in vertical direction	A	=	0.840+0.420*n µm
CORE.H210P51.W.1.1.1	Width of H210P51 STD cell region in vertical direction, if both side of STD cell region do not touch {TSMC POR SRAM size 0.765um in horizontal direction}	A1	=	2.100+0.420*n µm
CORE.H210P51.W.1.2	Width of H210P51 STD cell region in horizontal direction	B	=	3.621+0.102*n µm
CORE.H210P51.W.2.1	Vertical edge length of H210P51 STD cell region between two consecutive 270-270 degree corners	C	=	0.840+0.420*n µm
CORE.H210P51.W.2.2	Horizontal edge length of H210P51 STD cell region between two consecutive 270-270 degree corners	D	=	0.969+0.102*n µm
CORE.H210P51.W.3.1	Vertical edge length of H210P51 STD cell region between two consecutive 90-270 degree corners	E	=	0.420+0.420*n µm
CORE.H210P51.W.3.2	Horizontal edge length of H210P51 STD cell region between two consecutive 90-270 degree corners	F	=	1.020+0.102*n µm
CORE.H210P51.W.4.2	Concave corner to concave corner width of H210P51 STD cell region in horizontal direction	H	=	3.621+0.102*n µm

Guideline Change when using CW (common well) type boundary Cells

Guideline No.	Guideline Description	Label	Op.	Rule
CORE.H210P51.W.1.2:BDRYCW	Width of H210P51 STD cell region in horizontal direction	B	=	3.111+0.102*n µm
CORE.H210P51.W.2.2:BDRYCW	Horizontal edge length of H210P51 STD cell region between two consecutive 270-270 degree corners	D	=	0.969+0.102*n µm
CORE.H210P51.W.3.2:BDRYCW	Horizontal edge length of H210P51 STD cell region between two consecutive 90-270 degree corners	F	=	0.714+0.102*n µm
CORE.H210P51.W.4.2:BDRYCW	Concave corner to concave corner width of H210P51 STD cell region in horizontal direction	H	=	3.111+0.102*n µm

Unleash Innovation

H210P51 APR Block Design

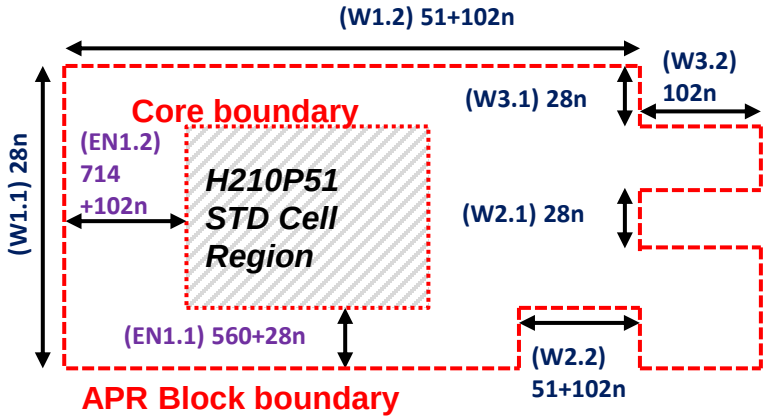
Chip-integration Design Guideline for APR Specific Section for H210P51

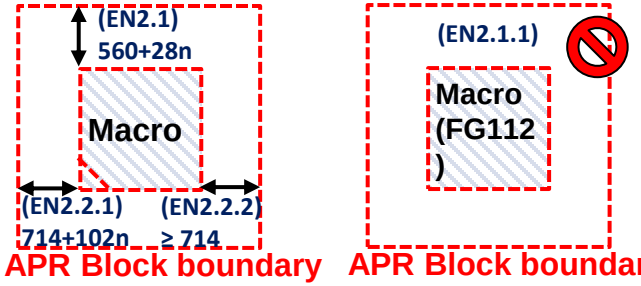
- H210P51 APR Block Design

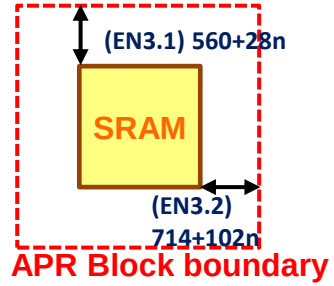
About FG28, FG112 and Boundary Controlled APR Block

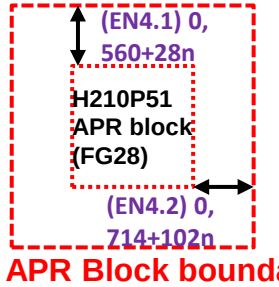
- APR Block using H210P51 cells have 4 kinds of variation
  - FG28 w/o Boundary Controlled (Guideline Baseline)
  - FG28 with Boundary Controlled
  - FG112 w/o Boundary Controlled
  - FG112 with Boundary Controlled
- Difference between FG28/FG112
  - FG28: FB_10 (H280P57 cells) cannot be used in any sub-block or macro
  - FG112: Allow FB_10 (H280P57 cells) inside sub-block or macro
- Difference of “Boundary Controlled”
  - STD cell region and APR Block (Boundary Controlled only) can abut block boundary
  - However, Block edge must be fully covered by boundary cell (except 1CPP gap)
- Guideline code end with :FG28 / :FG112 denote rule only effect in FG28 or FG112 APR Block
- Guidelines code end with “:NOBC / :BC” denote rule only effect in typical or boundary controlled APR Block
- Chip Top Design is considered as FG112 and NOBC

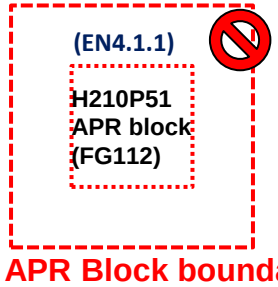
H210P51 APR Block Design Baseline (FG28, Non Boundary Controlled)

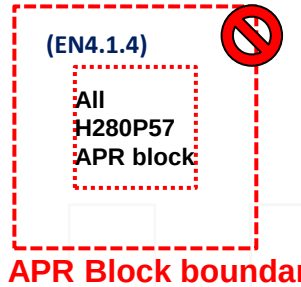


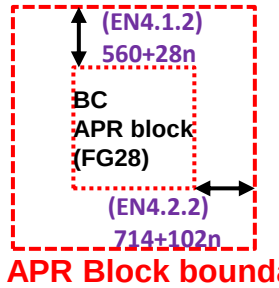


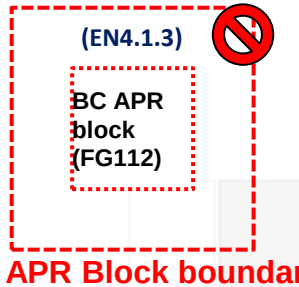






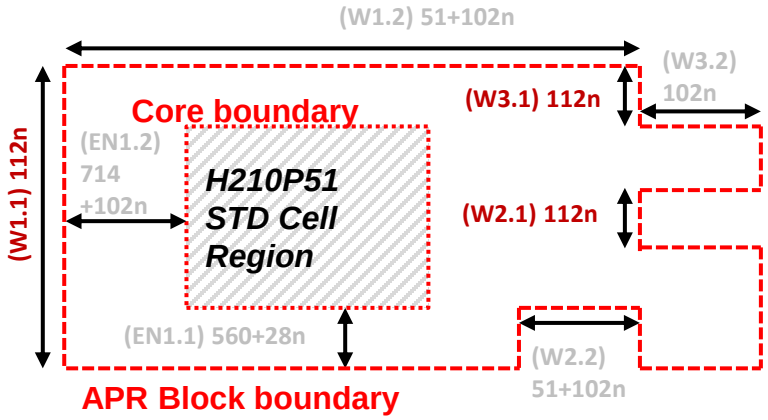


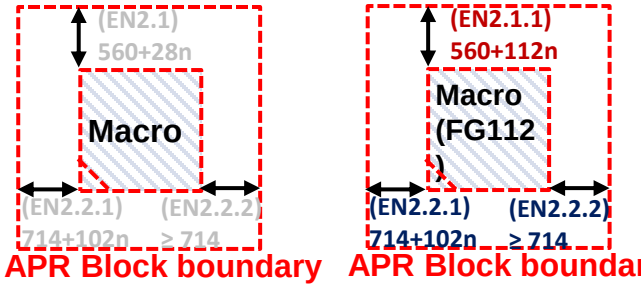


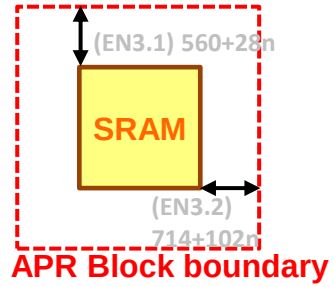


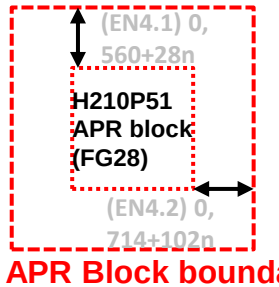
Notice:
Blue labels: common or FG28 guidelines
Red labels: FG112 guidelines
Purple Labels: Non-BC guidelines
Green labels: BC guidelines

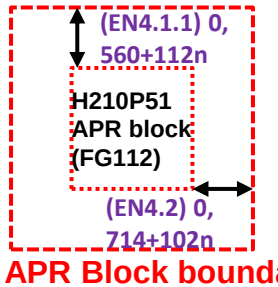
H210P51 APR Block Design Guidelines (FG112, Non Boundary Controlled)

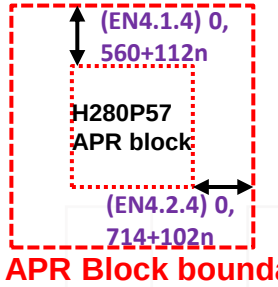


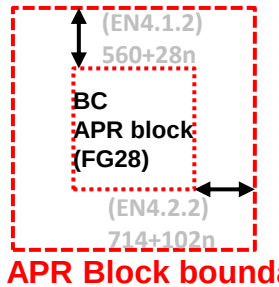


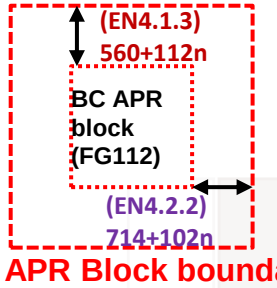


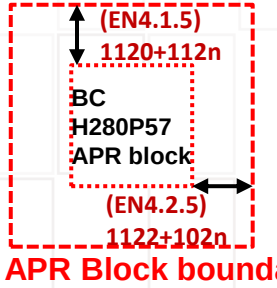






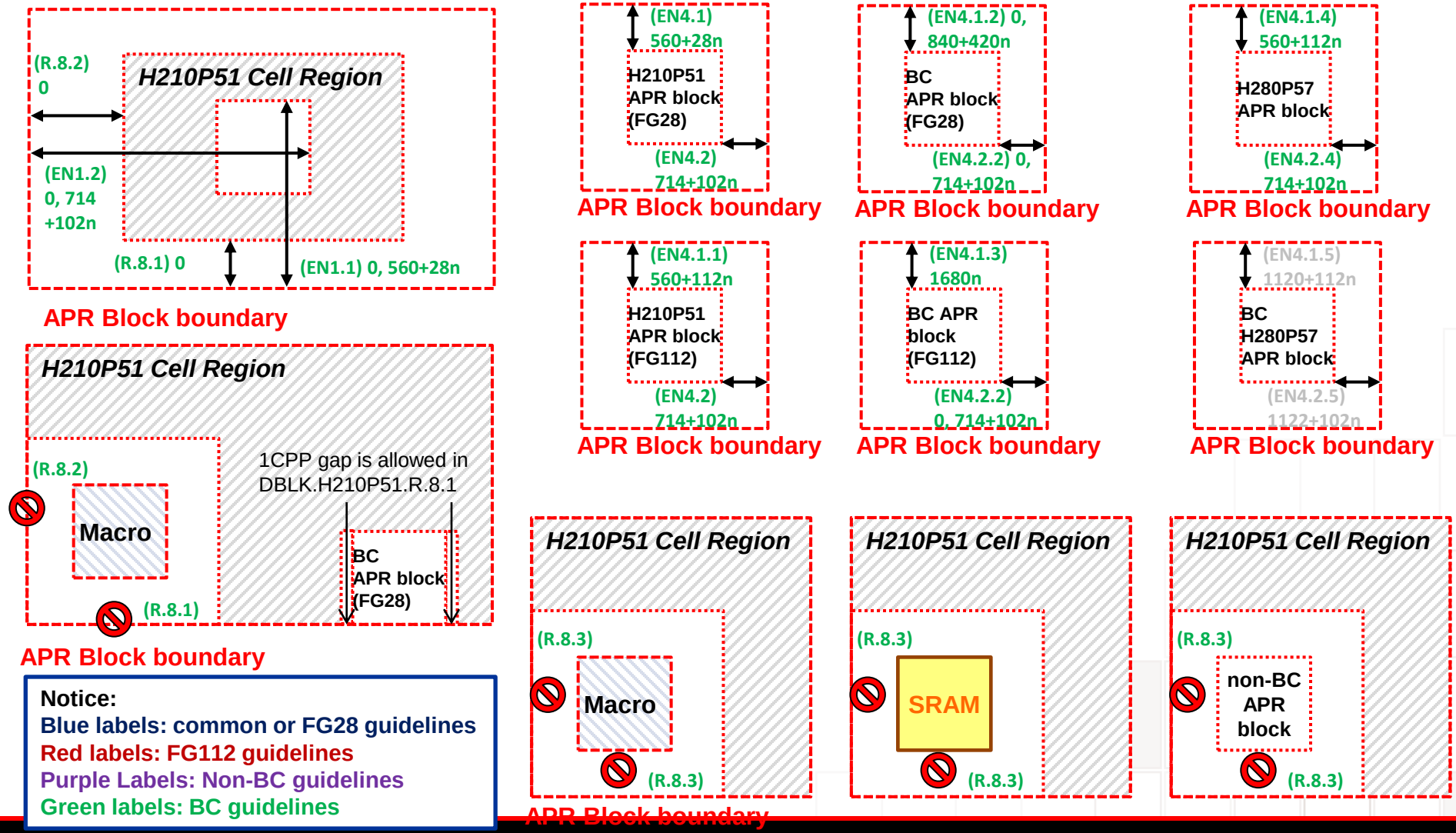






Notice:
Blue labels: common or FG28 guidelines
Red labels: FG112 guidelines
Purple Labels: Non-BC guidelines
Green labels: BC guidelines

H210P51 APR Block Design Guidelines (Boundary Controlled)



Notice:
Blue labels: common or FG28 guidelines
Red labels: FG112 guidelines
Purple Labels: Non-BC guidelines
Green labels: BC guidelines

H210P51 APR Block Design

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.W.1.1:FG28	Width of H210P51 APR Block with Fin Grid 28nm in vertical direction	W1.1	=	0.028*n µm
DBLK.H210P51.W.1.1:FG112	Width of H210P51 APR Block with Fin Grid 112nm in vertical direction	W1.1	=	0.112*n µm
DBLK.H210P51.W.1.2	Width of H210P51 APR Block in horizontal direction	W1.2	=	0.051+0.102*n µm
DBLK.H210P51.W.2.1:FG28	Vertical edge length of H210P51 APR Block with Fin Grid 28nm between two consecutive 270-270 degree corners	W2.1	=	0.028*n µm
DBLK.H210P51.W.2.1:FG112	Vertical edge length of H210P51 APR Block with Fin Grid 112nm between two consecutive 270-270 degree corners	W2.1	=	0.112*n µm
DBLK.H210P51.W.2.2	Horizontal edge length of H210P51 APR block between two consecutive 270-270 degree corners	W2.2	=	0.051+0.102*n µm
DBLK.H210P51.W.3.1:FG28	Vertical edge length of H210P51 APR Block with Fin Grid 28nm between two consecutive 90-270 degree corners	W3.1	=	0.028*n µm
DBLK.H210P51.W.3.1:FG112	Vertical edge length of H210P51 APR Block with Fin Grid 112nm between two consecutive 90-270 degree corners	W3.1	=	0.112*n µm
DBLK.H210P51.W.3.2	Horizontal edge length of H210P51 APR block between two consecutive 90-270 degree corners	W3.2	=	0.102*n µm
DBLK.H210P51.EN.1.1:NOBC	In H210P51 APR block w/o Boundary Controlled, Block edge enclosure H210P51 STD cell region in vertical direction	EN1.1	=	0.560+0.028*n µm
DBLK.H210P51.EN.1.1:BC	In Boundary Controlled H210P51 APR block, Block edge enclosure H210P51 STD cell region in vertical direction	EN1.1	=	0, 0.560+0.028*n µm
DBLK.H210P51.EN.1.2:NOBC	In H210P51 APR block w/o Boundary Controlled, Block edge enclosure H210P51 STD cell region in horizontal direction	EN1.2	=	0.714+0.102*n µm
DBLK.H210P51.EN.1.2:BC	In Boundary Controlled H210P51 APR block, Block edge enclosure H210P51 STD cell region in horizontal direction	EN1.2	=	0, 0.714+0.102*n µm
DBLK.EN.2.1	Block edge enclosure Macro in vertical direction	EN2.1	=	0.560+0.028*n µm
DBLK.H210P51.EN.2.1.1:FG28	Fin Grid 112nm Macro is not allowed in H210P51 APR Block with Fin Grid 28nm			
DBLK.H210P51.EN.2.1.1:FG112	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure Fin Grid 112nm Macro in vertical direction	EN2.1.1	=	0.560+0.112*n µm
DBLK.EN.2.2.1	Block edge enclosure Left edge of Macro in horizontal direction	EN2.2.1	=	0.714+0.102*n µm
DBLK.EN.2.2.2	Block edge enclosure Right edge of Macro in horizontal direction	EN2.2.2	≥	0.714 µm
DBLK.EN.3.1	Block edge enclosure TSMC SRAM in vertical direction	EN3.1	=	0.560+0.028*n µm
DBLK.EN.3.2	Block edge enclosure TSMC SRAM in horizontal direction	EN3.2	=	0.714+0.102*n µm

H210P51 APR Block Design

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.EN.4.1:NOBC	In H210P51 APR block w/o Boundary Controlled, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1	=	0, 0.560+0.028*n µm
DBLK.H210P51.EN.4.1:BC	In Boundary Controlled H210P51 APR block, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1	=	0.560+0.028*n µm
DBLK.H210P51.EN.4.1.1:FG28	Non-BC H210P51 APR block with Fin Grid 112nm is not allowed in H210P51 APR Block with Fin Grid 28nm			
DBLK.H210P51.EN.4.1.1:FG112_NOBC	In Non-BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.1	=	0, 0.560+0.112*n µm
DBLK.H210P51.EN.4.1.1:FG112_BC	In BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.1	=	0.560+0.112*n µm
DBLK.H210P51.EN.4.1.2:NOBC	In H210P51 APR block w/o Boundary Controlled, Block edge enclosure BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1.2	=	0.560+0.028*n µm
DBLK.H210P51.EN.4.1.2:BC	In Boundary Controlled H210P51 APR block, Block edge enclosure BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1.2	=	0, 0.840+0.420*n µm
DBLK.H210P51.EN.4.1.3:FG28	BC H210P51 APR block with Fin Grid 112nm is not allowed in Non-BC H210P51 APR block with Fin Grid 28nm			
DBLK.H210P51.EN.4.1.3:FG112_NOBC	In Non-BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.3	=	0.560+0.112*n µm
DBLK.H210P51.EN.4.1.3:FG112_BC	In BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.3	=	1.680*n µm
DBLK.H210P51.EN.4.1.4:FG28	All H280P57 APR block is not allowed in H210P51 APR Block with Fin Grid 28nm			
DBLK.H210P51.EN.4.1.4:FG112_NOBC	In Non-BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure H280P57 APR block in vertical direction	EN4.1.4	=	0, 0.560+0.112*n µm
DBLK.H210P51.EN.4.1.4:FG112_BC	In BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure H280P57 APR block in vertical direction	EN4.1.4	=	0.560+0.112*n µm
DBLK.H210P51.EN.4.1.5:FG112	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure Boundary Controlled H280P57 APR block in vertical direction	EN4.1.5	=	1.120+0.112*n µm

H210P51 APR Block Design

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.EN.4.2:NOBC	In H210P51 APR block w/o Boundary Controlled, Block edge enclosure H210P51 APR block w/o Boundary Controlled in horizontal direction	EN4.2	=	0, 0.714+0.102*n µm
DBLK.H210P51.EN.4.2:BC	In Boundary Controlled H210P51 APR block, Block edge enclosure H210P51 APR block w/o Boundary Controlled in horizontal direction	EN4.2	=	0.714+0.102*n µm
DBLK.H210P51.EN.4.2.2:NOBC	In H210P51 APR block w/o Boundary Controlled, Block edge enclosure Boundary Controlled H210P51 APR block in horizontal direction	EN4.2.2	=	0.714+0.102*n µm
DBLK.H210P51.EN.4.2.2:BC	In Boundary Controlled H210P51 APR block, Block edge enclosure Boundary Controlled H210P51 APR block in horizontal direction	EN4.2.2	=	0, 0.714+0.102*n µm
DBLK.H210P51.EN.4.2.4:FG112_NOBC	In Non-BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure H280P57 APR block in horizontal direction	EN4.2.4	=	0, 0.714+0.102*n µm
DBLK.H210P51.EN.4.2.4:FG112_BC	In BC H210P51 APR block with Fin Grid 112nm, Block edge enclosure H280P57 APR block in horizontal direction	EN4.2.4	=	0.714+0.102*n µm
DBLK.H210P51.EN.4.2.5:FG112	In H210P51 APR Block with Fin Grid 112nm, Block edge enclosure Boundary Controlled H280P57 APR block in horizontal direction	EN4.2.5	=	1.122+0.102*n µm
DBLK.H210P51.R.8.1:BC	In Boundary Controlled H210P51 APR block, empty area cannot touch horizontal block edges (Rule checks block enclosure **Checked_Empty_Area_H210P51** in vertical direction >0) Definition of Checked_Empty_Area_H210P51: **Checked_Empty_Area_H210P51** = Block NOT { { { H210P51 STD cell region OR Boundary Controlled H210P51 APR Block } size 0.0255 in horizontal direction} OR Macro }	R.8.1		
DBLK.H210P51.R.8.2:BC	In Boundary Controlled H210P51 APR block, empty area cannot touch vertical block edges (Rule checks block enclosure **Checked_Empty_Area_H210P51** in horizontal direction >0) Definition of Checked_Empty_Area_H210P51: Please refer to DBLK.H210P51.R.8.1:BC	R.8.2		
DBLK.H210P51.R.8.3:BC	In Boundary Controlled H210P51 APR block, macro, TSMC SRAM and APR block w/o Boundary Controlled must be surrounded by H210P51 STD cell region	R.8.3		

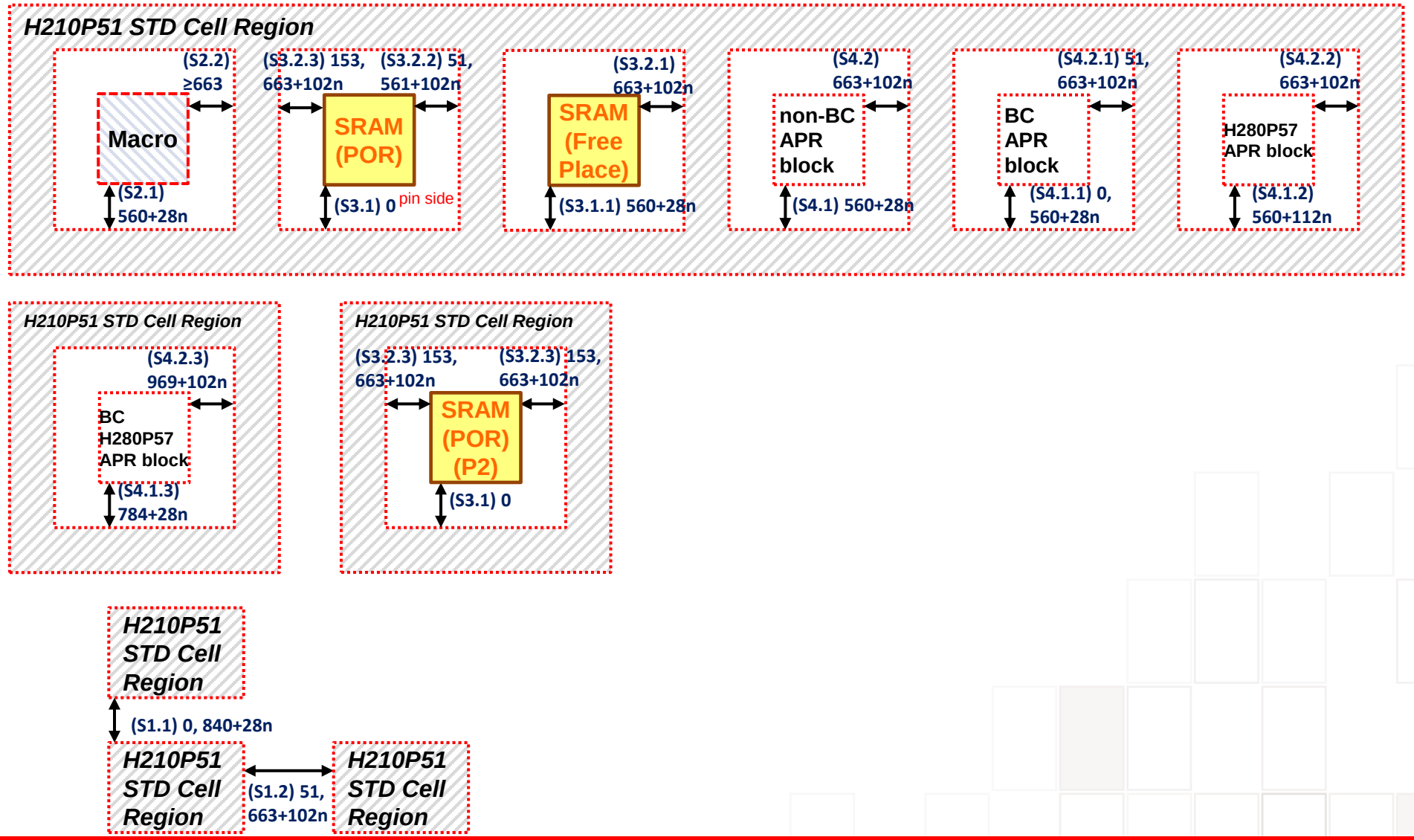
Unleash Innovation

H210P51 Spacing

Chip-integration Design Guideline for APR
Specific Section for H210P51

- **Placement**

H210P51 APR Block Design



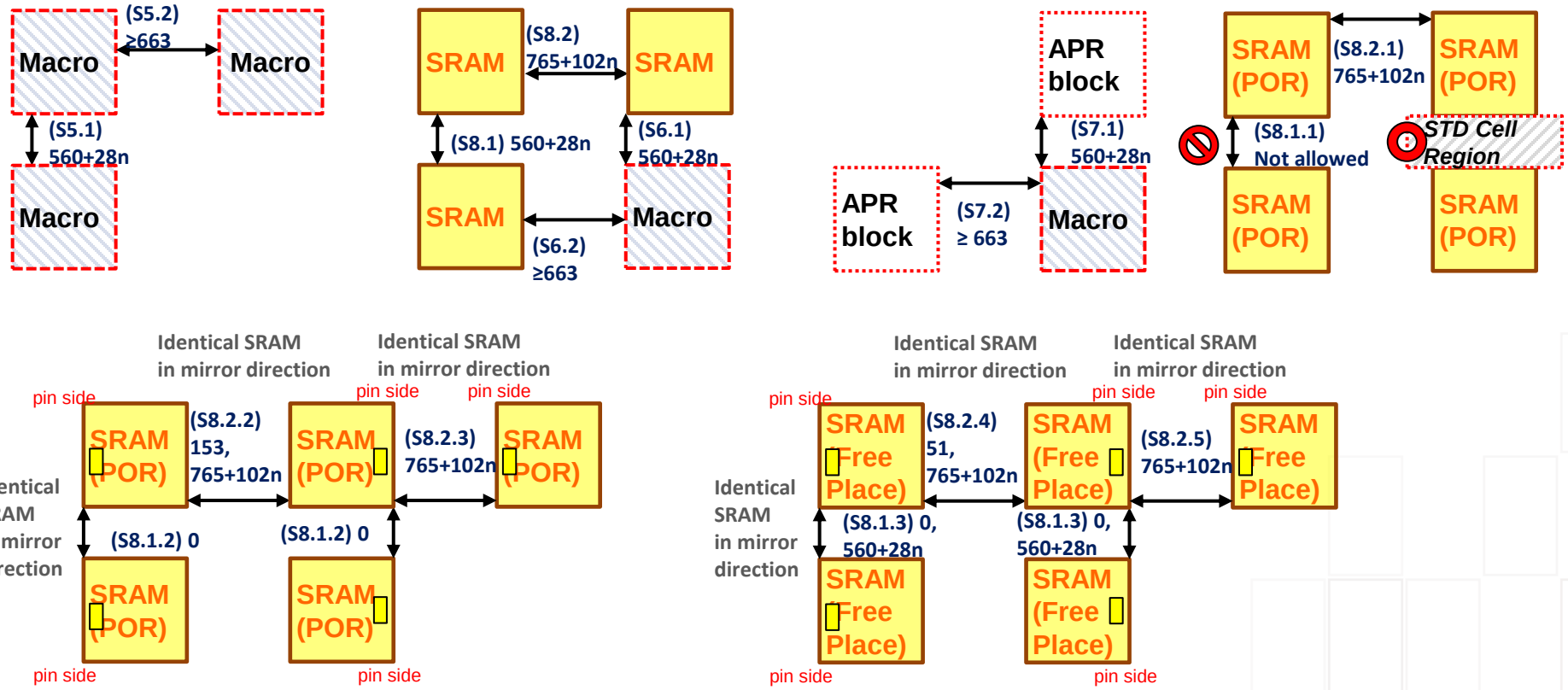
H210P51 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.S.1.1	Spacing of H210P51 STD cell region in vertical direction (PRL≥-0.663μm)	**S1.1**	=	0, 0.840+0.028*n μm
DBLK.H210P51.S.1.2	Spacing of H210P51 STD cell region in horizontal direction (PRL≥-0.84μm)	**S1.2**	=	0.051, 0.663+0.102*n μm
DBLK.H210P51.S.2.1	Macro to H210P51 STD cell region spacing in vertical direction (PRL>-0.663μm)	**S2.1**	=	0.560+0.028*n μm
DBLK.H210P51.S.2.2	Macro to H210P51 STD cell region spacing in horizontal direction (PRL>-0.560μm)	**S2.2**	≥	0.663 μm
DBLK.H210P51.S.3.1	TSMC POR SRAM to H210P51 STD cell region spacing in vertical direction (PRL≥0μm), except another TSMC POR SRAM in between	**S3.1**	=	0 μm
DBLK.H210P51.S.3.1.1	TSMC free placement SRAM to H210P51 STD cell region spacing in vertical direction (PRL>-0.663μm)	**S3.1.1**	=	0.560+0.028*n μm
DBLK.H210P51.S.3.2.1	TSMC free placement SRAM to H210P51 STD cell region spacing in horizontal direction (PRL>-0.560μm)	**S3.2.1**	=	0.663+0.102*n μm
DBLK.H210P51.S.3.2.2	Pin side of TSMC POR SRAM [except TSMC SRAM Pin Type 2] to H210P51 STD cell region spacing in horizontal direction (PRL≥0μm)	**S3.2.2**	=	0.051, 0.561+0.102*n μm
DBLK.H210P51.S.3.2.2.1	Right side of TSMC POR SRAM [is TSMC SRAM Pin Type 2] to H210P51 STD cell region spacing in horizontal direction (PRL≥0μm)	**S3.2.2.1**	=	0.153, 0.663+0.102*n μm
DBLK.H210P51.S.3.2.3	Array side of TSMC POR SRAM to H210P51 STD cell region spacing in horizontal direction (PRL≥0μm)	**S3.2.3**	=	0.153, 0.663+0.102*n μm

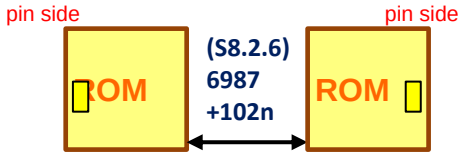
H210P51 APR Block: Spacing

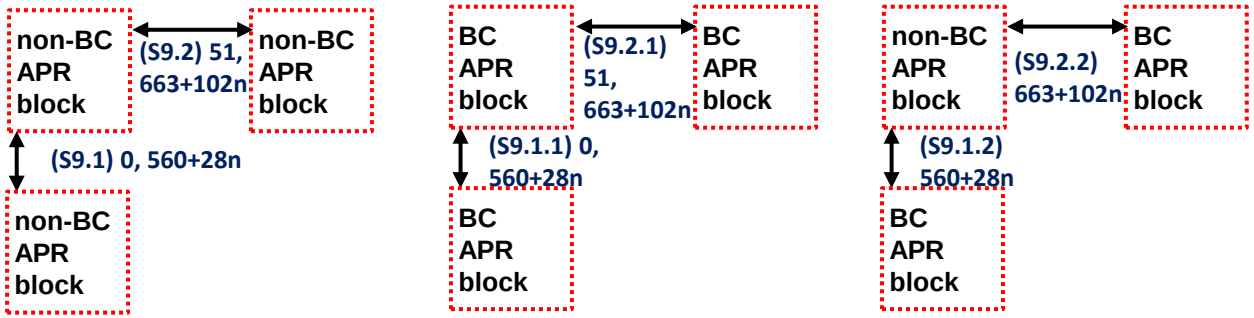
Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H210P51.S.4.1	H210P51 APR block w/o Boundary Controlled to H210P51 STD cell region spacing in vertical direction (PRL > -0.663μm)	S4.1	=	0.560+0.028*n μm
DBLK.H210P51.S.4.1.1	Boundary Controlled H210P51 APR Block to H210P51 STD cell region spacing in vertical direction (PRL > -0.663μm)	S4.1.1	=	0, 0.560+0.028*n μm
DBLK.H210P51.S.4.1.2	H280P57 APR block to H210P51 STD cell region spacing in vertical direction (PRL > -0.663μm)	S4.1.2	=	0.560+0.028*n μm
DBLK.H210P51.S.4.1.3	Boundary Controlled H280P57 APR block to H210P51 STD cell region spacing in vertical direction (PRL > -0.969μm)	S4.1.3	=	0.784+0.028*n μm
DBLK.H210P51.S.4.2	H210P51 APR block w/o Boundary Controlled to H210P51 STD cell region spacing in horizontal direction (PRL > -0.560μm)	S4.2	=	0.663+0.102*n μm
DBLK.H210P51.S.4.2.1	Boundary Controlled H210P51 APR Block to H210P51 STD cell region spacing in horizontal direction (PRL > -0.560μm)	S4.2.1	=	0.051, 0.663+0.102*n μm
DBLK.H210P51.S.4.2.2	H280P57 APR block to H210P51 STD cell region spacing in horizontal direction (PRL > -0.560μm)	S4.2.2	=	0.663+0.102*n μm
DBLK.H210P51.S.4.2.3	Boundary Controlled H280P57 APR block to H210P51 STD cell region spacing in horizontal direction (PRL > -0.784μm)	S4.2.3	=	0.969+0.102*n μm

H210P51 APR Block: Spacing



H210P51 APR Block: Spacing





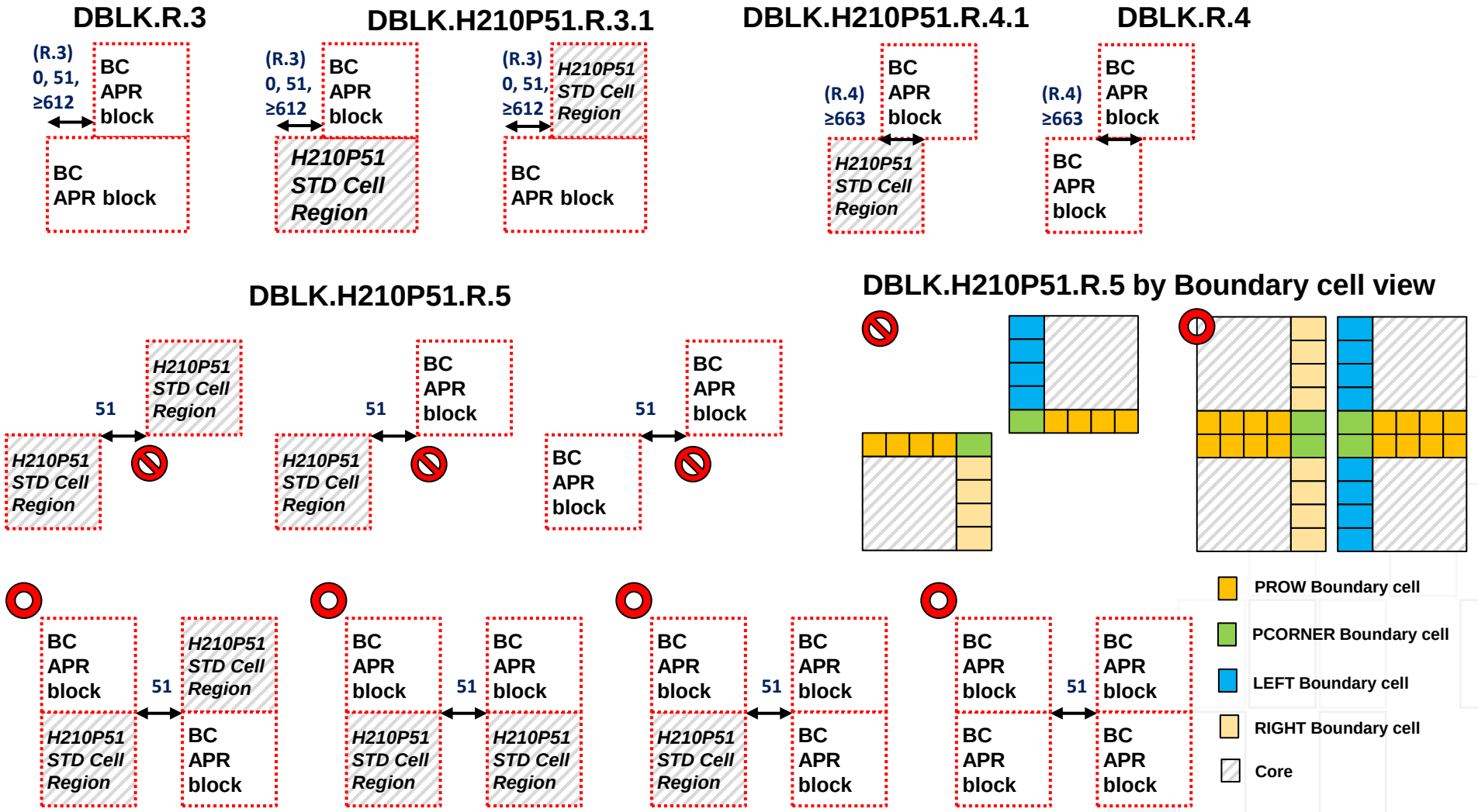
H210P51 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.S.5.1	Spacing from Macro to Macro in vertical direction (PRL>-0.663µm)	**S5.1**	=	0.560+0.028*n µm
DBLK.S.5.2	Spacing from Macro to Macro in horizontal direction (PRL>-0.560µm)	**S5.2**	≥	0.663 µm
DBLK.S.6.1	Spacing from TSMC SRAM to Macro in vertical direction (PRL>-0.663µm)	**S6.1**	=	0.560+0.028*n µm
DBLK.S.6.2	Spacing from TSMC SRAM to Macro in horizontal direction (PRL>-0.560µm)	**S6.2**	≥	0.663 µm
DBLK.S.7.1	Spacing from APR block to Macro in vertical direction (PRL>-0.663µm)	**S7.1**	=	0.560+0.028*n µm
DBLK.S.7.2	Spacing from APR block to Macro in horizontal direction (PRL>-0.560µm)	**S7.2**	≥	0.663 µm
DBLK.S.8.1	Spacing of TSMC SRAM in vertical direction (PRL>-0.765µm), except: 1. Both TSMC SRAM are TSMC POR SRAM 2. Both TSMC SRAM are identical TSMC Free Placement SRAM, with mirrored orientation	**S8.1**	=	0.560+0.028*n µm
DBLK.S.8.1.1	Spacing of TSMC POR SRAM in vertical direction is not allowed, except STD cell region in between (PRL >-0.051µm)	**S8.1.1**		
DBLK.S.8.1.2	Spacing of a pair of mirrored, identical TSMC POR SRAM in vertical direction, except STD cell region in between (PRL >-0.051µm)	**S8.1.2**	=	0 µm
DBLK.S.8.1.3	Spacing of a pair of mirrored, identical TSMC Free Placement SRAM in vertical direction, except STD cell region in between (PRL >-0.765µm)	**S8.1.3**	=	0, 0.560+0.028*n µm
DBLK.S.8.2	Spacing of TSMC SRAM in horizontal direction (PRL >-0.560µm), except: 1. Both TSMC SRAM are TSMC POR SRAM 2. Both TSMC SRAM are identical TSMC Free Placement SRAM, with mirrored orientation	**S8.2**	=	0.765+0.102*n µm
DBLK.S.8.2.1	Spacing of TSMC POR SRAM in horizontal direction (PRL >0µm), except condition of DBLK.S.8.2.2	**S8.2.1**	=	0.765+0.102*n µm
DBLK.S.8.2.2	Array side spacing of a pair of mirrored, identical TSMC POR SRAM in horizontal direction (PRL >0µm)	**S8.2.2**	=	0.153, 0.765+0.102*n µm
DBLK.S.8.2.3	Pin side spacing of a pair of mirrored, identical TSMC POR SRAM in horizontal direction (PRL >0µm)	**S8.2.3**	=	0.765+0.102*n µm
DBLK.S.8.2.4	Array side spacing of a pair of mirrored, identical TSMC Free Placement SRAM in horizontal direction (PRL >-0.560µm)	**S8.2.4**	=	0.051, 0.765+0.102*n µm
DBLK.S.8.2.5	Pin side spacing of a pair of mirrored, identical TSMC Free Placement SRAM in horizontal direction (PRL >-0.560µm)	**S8.2.5**	=	0.765+0.102*n µm

H210P51 APR Block: Spacing

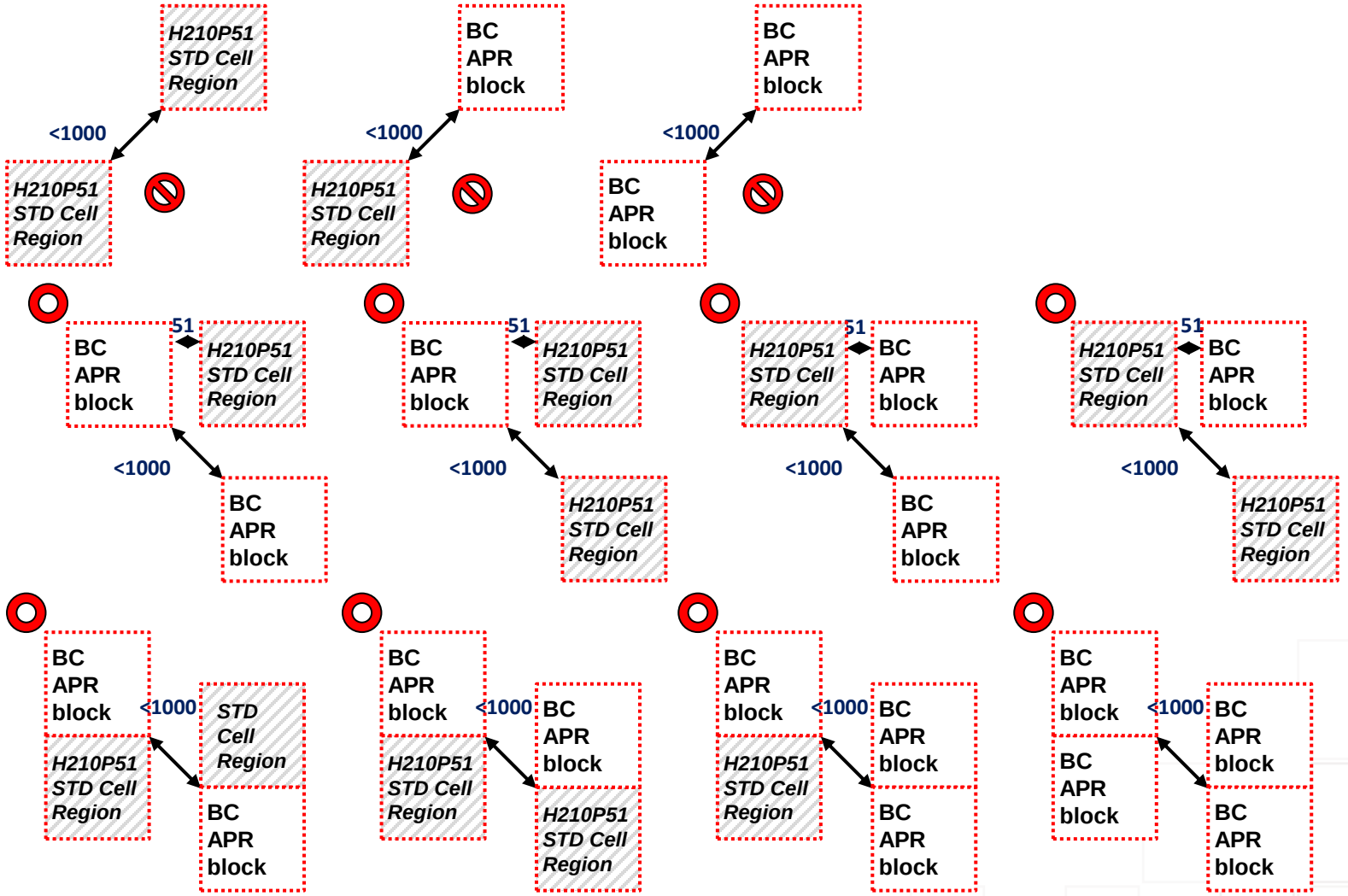
Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.S.8.2.6	Array side spacing of TSMC ROM in horizontal direction (PRL >0μm)	**S8.2.6**	=	6.987+0.102*n μm
DBLK.S.9.1	Spacing of H210P51 APR block w/o Boundary Controlled vertical direction (PRL> -0.663μm)	**S9.1**	=	0, 0.560+0.028*n μm
DBLK.S.9.1.1	Spacing of Boundary Controlled H210P51 APR Block in vertical direction (PRL>-0.663μm)	**S9.1.1**	=	0, 0.560+0.028*n μm
DBLK.S.9.1.2	Spacing from Boundary Controlled H210P51 APR Block to H210P51 APR block w/o Boundary Controlled in vertical direction (PRL>-0.663μm)	**S9.1.2**	=	0.560+0.028*n μm
DBLK.S.9.2	Spacing of APR block w/o Boundary Controlled in horizontal direction (PRL>-0.560μm)	**S9.2**	=	0.051, 0.663+0.102*n μm
DBLK.S.9.2.1	Spacing of Boundary Controlled H210P51 APR Block in horizontal direction (PRL>-0.560μm)	**S9.2.1**	=	0.051, 0.663+0.102*n μm
DBLK.S.9.2.2	Spacing from Boundary Controlled H210P51 APR Block to H210P51 APR block w/o Boundary Controlled in horizontal direction (PRL>-0.560μm)	**S9.2.2**	=	0.663+0.102*n μm

H210P51 APR Block: Spacing



H210P51 APR Block: Spacing

DBLK.H210P51.R.5.1



H210P51 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.R.3	Project length difference between horizontal edges of Boundary Controlled H210P51 APR Block when vertical abutting	**R.3**	=	0, 0.051, ≥0.612 µm
DBLK.H210P51.R.3.1	Project length difference between horizontal edges of H210P51 STD cell region and Boundary Controlled H210P51 APR Block when vertical abutting	**R.3.1**	=	0, 0.051, ≥0.612 µm
DBLK.R.4	Overlap width of vertical abutting Boundary Controlled H210P51 APR Block	**R.4**	≥	0.663 µm
DBLK.H210P51.R.4.1	Overlap width of vertical abutting H210P51 STD cell region and Boundary Controlled H210P51 APR Block	**R.4.1**	≥	0.663 µm
DBLK.H210P51.R.5	Forbid point touch (horizontal spacing 0.051 µm, PRL =0) of 2 H210P51 STD cell region, or Boundary Controlled H210P51 APR Block, except 4 point touch (tCIC check spacing of **Checked_Empty_Area_H210P51** ≥ 0.001 µm, PRL ≥ -0.001 µm)			
DBLK.H210P51.R.5.1	Corner spacing between H210P51 STD cell region, or Boundary Controlled H210P51 APR Block should be ≥ 1µm, except following condition 1. Anyone of corner belong to horizontal edge, that vertically abut with another H210P51 STD cell region, or Boundary Controlled H210P51 APR Block 2. Anyone of corner belong to vertical edge, that keep 0.051µm horizontal spacing with another H210P51 STD cell region, or Boundary Controlled H210P51 APR Block			

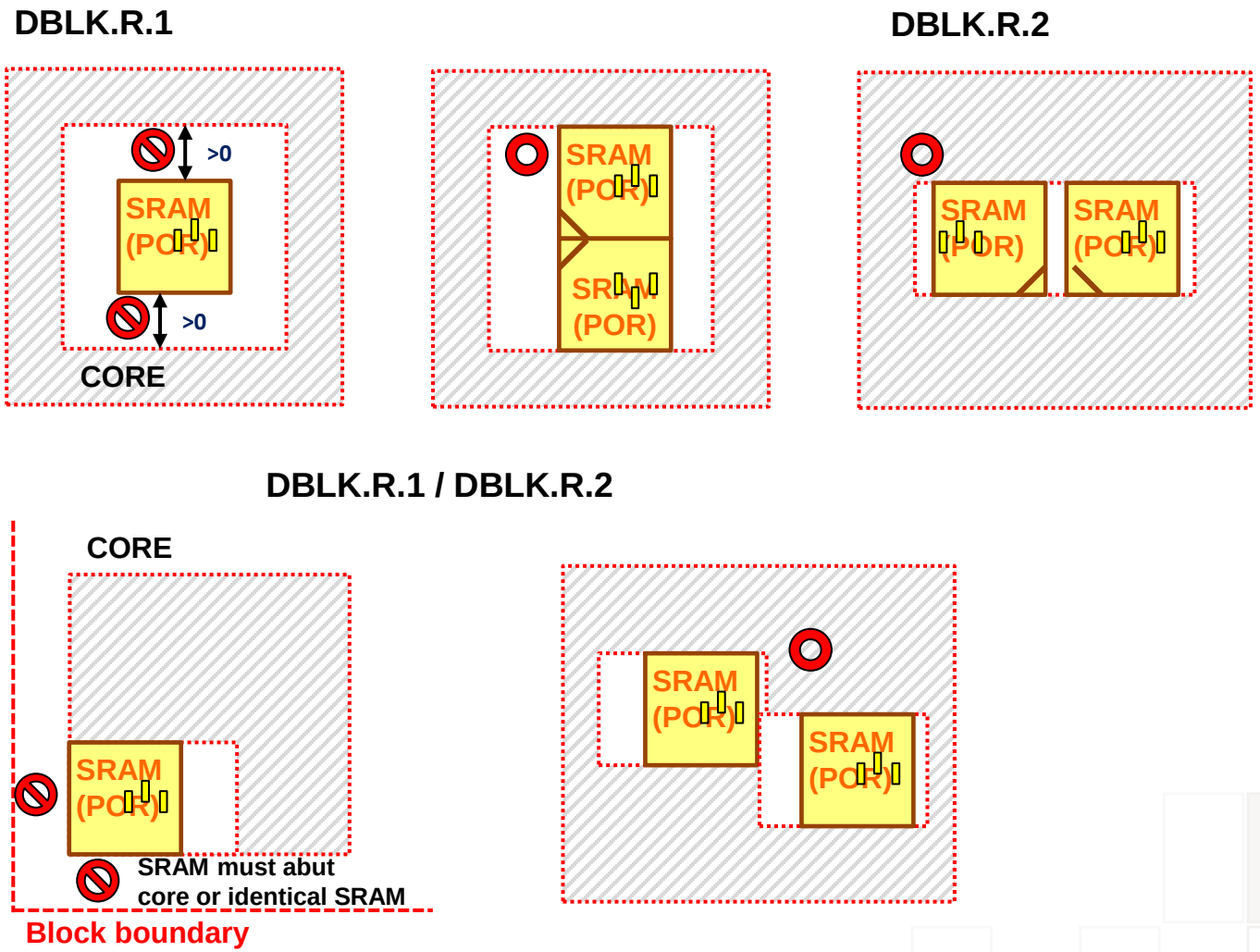
Unleash Innovation

TSMC POR SRAM Guidelines

Chip-integration Design Guideline for PnR
Specific Section for H210P51

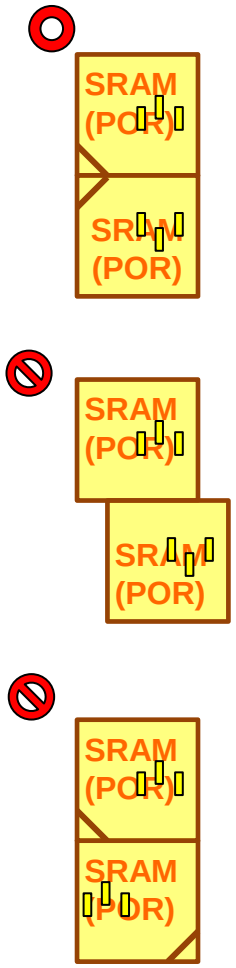
- **Placement**

Guidelines of TSMC POR SRAM

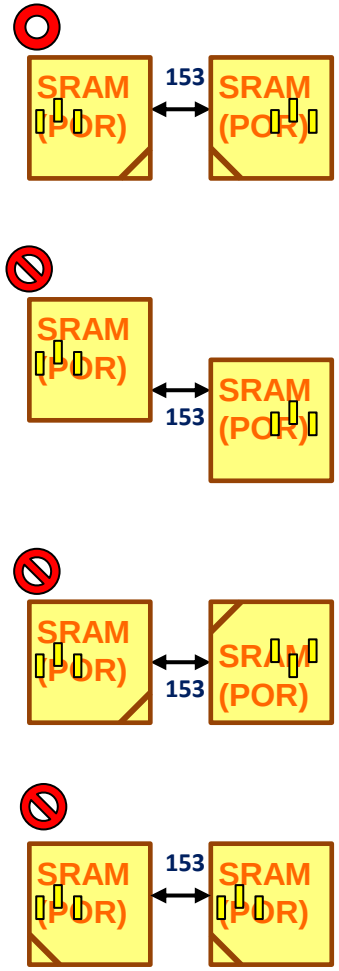


Guidelines of TSMC POR SRAM

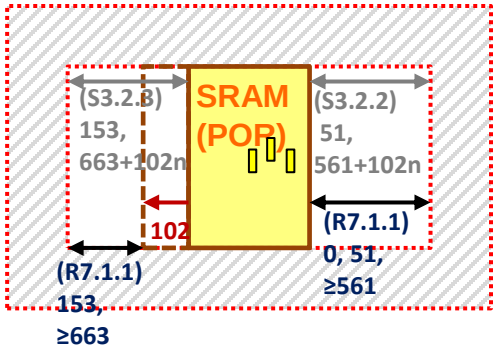
DBLK.R.1.1

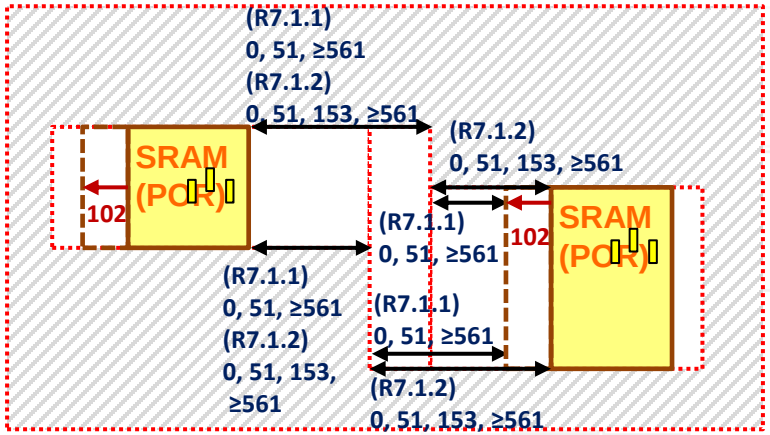


DBLK.R.2.1
DBLK.S.8.2.2

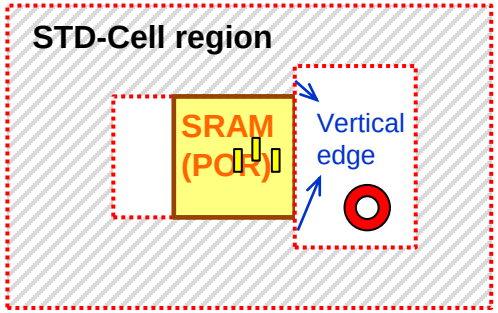


DBLK.R.7.1.1 / DBLK.R.7.1.2

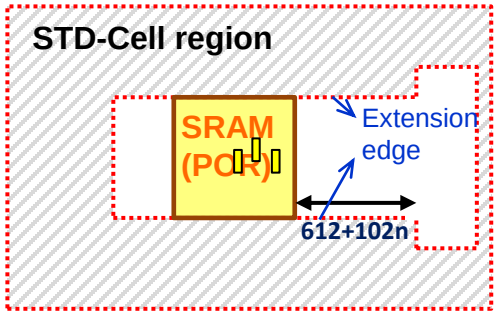




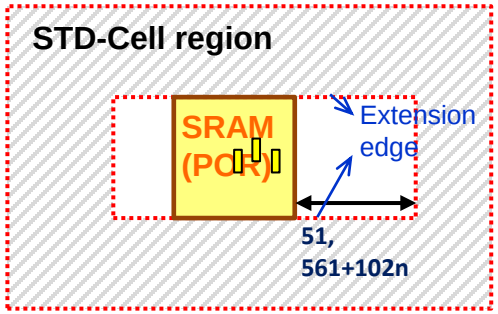
DBLK.R.7.1.1/DBLK.7.1.2 Detail (Pin side)



Vertical edge of STD cell region aligns macro edge of SRAM pin side is allowed

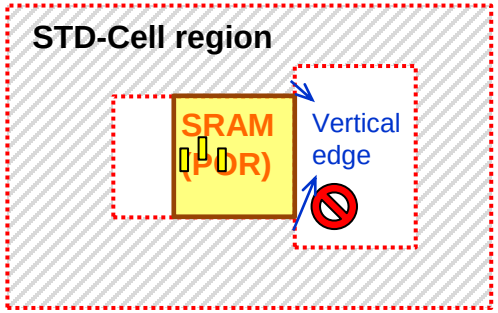


When extension edge of STD cell region from pin side is end in 90 degree corner, length of extension edge should be 0.612+0.102*n µm

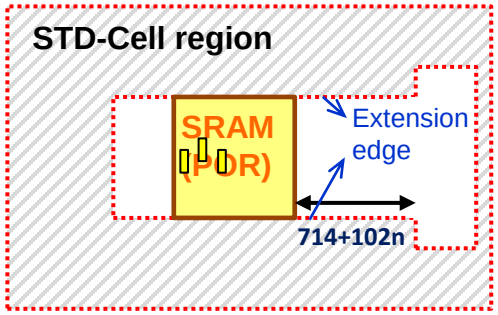


When extension edge of STD cell region from pin side is end in 270 degree corner, length of extension edge should be 0.051 or 0.561+0.102*n µm

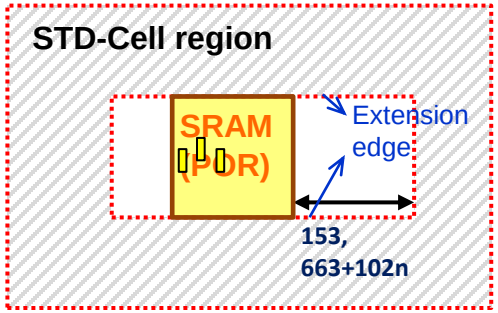
DBLK.R.7.1.1/DBLK.7.1.2 Detail (Array side)



Vertical edge of STD cell region aligns macro edge of SRAM array side is NOT allowed



When extension edge of STD cell region from array side is end in 90 degree corner, length of extension edge should be 0.714+0.102*n µm



When extension edge of STD cell region from array side is end in 270 degree corner, length of extension edge should be 0.153 or 0.663+0.102*n µm

Guideline of TSMC POR SRAM Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.R.1	Horizontal edge of TSMC POR SRAM must fully abut H210P51 STD cell region, or mirror abut same edge of identical SRAM			
DBLK.R.1.1	Abutting horizontal edges of two TSMC POR SRAM must be fully aligned			
DBLK.R.2	Vertical edge of TSMC POR SRAM must project to H210P51 STD cell region, or another TSMC POR SRAM			
DBLK.R.2.1	Vertical edges of two TSMC POR SRAM with spacing 0.153um must be fully aligned			
DBLK.R.7.1.1	Projected length difference from H210P51 STD cell region to { TSMC POR SRAM size 0.102μm on array side } and, with vertical spacing = 0μm (except TSMC SRAM Pin Type 2), (Edge on H210P51 STD cell region must be longer than TSMC POR SRAM)	**R7.1.1**		0, 0.051, ≥0.561 μm
DBLK.R.7.1.2	Projected length difference between TSMC POR SRAM and H210P51 STD cell region, with vertical spacing = 0μm (except TSMC SRAM Pin Type 2) (Edge on H210P51 STD cell region must be longer than TSMC POR SRAM)	**R7.1.2**		0, 0.051, 0.153, ≥0.561 μm
DBLK.R.7.1.2.1	Projected length difference between TSMC POR SRAM Pin Type 2 and H210P51 STD cell region, with vertical spacing = 0μm (Edge on H210P51 STD cell region must be longer than TSMC POR SRAM Pin Type 2)	**R7.1.2**		0.153, ≥0.663 μm

Unleash Innovation

Chip-integration Design Guideline for APR

Specific Section for H280P57

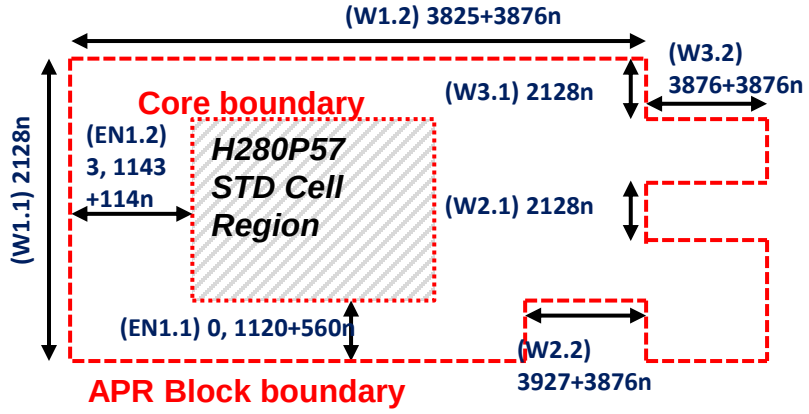
Unleash Innovation

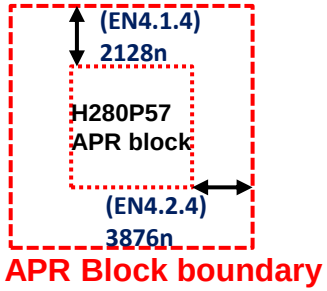
P76 Track Alignment

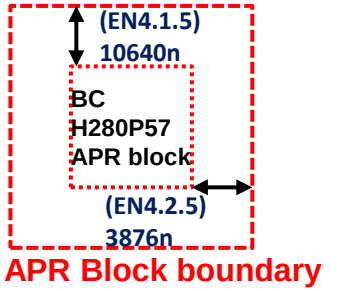
Chip-integration Design Guideline for APR
Specific Section for H280P57

- Track and Row

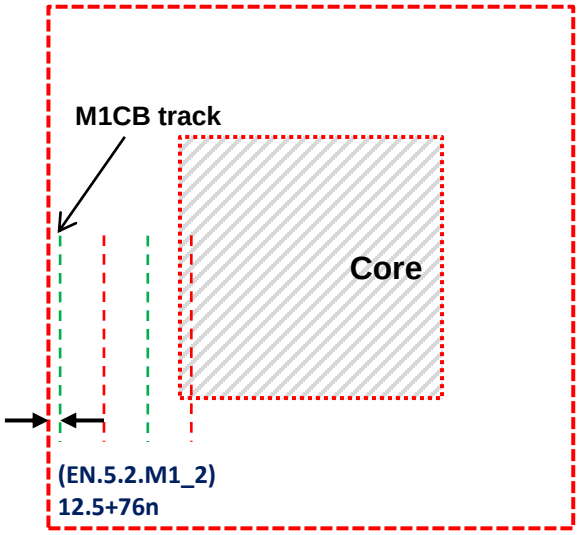
Guideline of Track Alignment (H280P57)

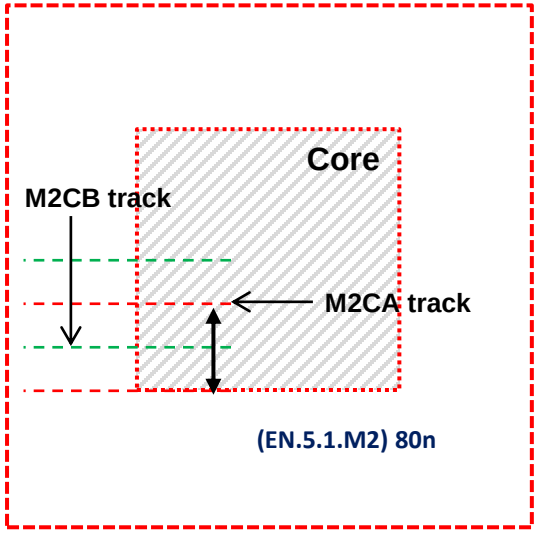


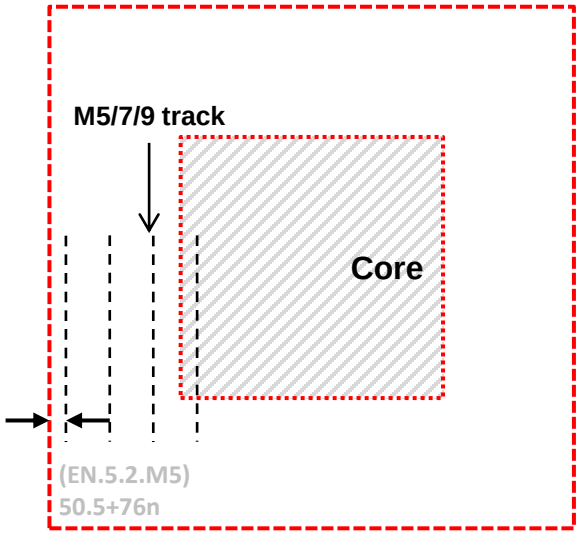


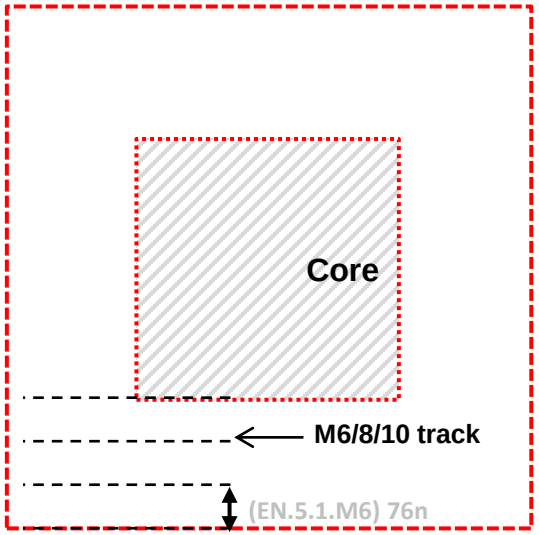


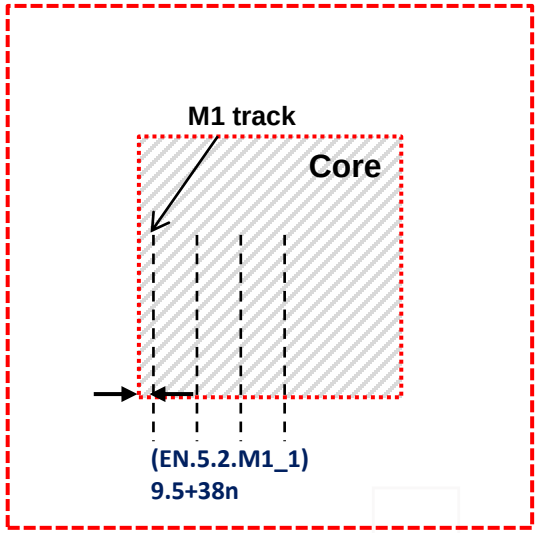
Guideline of Track Alignment (H280P57)











Guideline of Track Alignment (H280P57)

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.W.1.1:ALP76	Width of All H280P57 APR Block in vertical direction	**W1.1**	=	2.128*n µm
DBLK.H280P57.W.1.2:ALP76	Width of All H280P57 APR Block in horizontal direction	**W1.2**	=	3.825+3.876*n µm
DBLK.H280P57.W.2.1:ALP76	Vertical edge length of All H280P57 APR Block between two consecutive 270-270 degree corners	**W2.1**	=	2.128*n µm
DBLK.H280P57.W.2.2:ALP76	Horizontal edge length of All H280P57 APR Block between two consecutive 270-270 degree corners	**W2.2**	=	3.927+3.876*n µm
DBLK.H280P57.W.3.1:ALP76	Vertical edge length of All H280P57 APR Block between two consecutive 90-270 degree corners	**W3.1**	=	2.128*n µm
DBLK.H280P57.W.3.2:ALP76	Vertical edge length of All H280P57 APR Block between two consecutive 90-270 degree corners	**W3.2**	=	3.876+3.876*n µm
DBLK.H280P57.EN.1.1:ALP76	In All H280P57 APR block, Block edge enclosure H280P57 STD cell region (core) in vertical direction	**EN1.1**	=	0, 1.120+0.560*n µm
DBLK.H280P57.EN.1.2:ALP76	In All H280P57 APR block, Block edge enclosure H280P57 STD cell region (core) in horizontal direction	**EN1.2**	=	0.003, 1.143+0.114*n µm
DBLK.H280P57.EN.4.1.4:ALP76	In All H280P57 APR block, Block edge enclosure H280P57 APR block in vertical direction	**EN4.1.4**	=	2.128*n µm
DBLK.H280P57.EN.4.1.5:ALP76	In All H280P57 APR block, Block edge enclosure Boundary Controlled H280P57 APR block in vertical direction	**EN4.1.5**	=	10.64*n µm
DBLK.H280P57.EN.4.2.4:ALP76	In All H280P57 APR block, Block edge enclosure H280P57 APR block in horizontal direction	**EN4.2.4**	=	3.876*n µm
DBLK.H280P57.EN.4.2.5:ALP76	In All H280P57 APR block, Block edge enclosure Boundary Controlled H280P57 APR block in horizontal direction	**EN4.2.5**	=	3.876*n µm

Guideline of Track Alignment (H280P57)

***Guidelines in grey text are identical with H210P51 APR Block**

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.EN.5.1.M2_PROW	In All H280P57 APR block, Core enclosure horizontal M2CA track in vertical direction, if boundary cell is PROW	**EN.5.1.M2**	=	0.080*n µm
DBLK.H280P57.EN.5.1.M2_NROW	In All H280P57 APR block, Core enclosure horizontal M2CB track in vertical direction, if boundary cell is NROW		=	0.080*n µm
DBLK.EN.5.1.M6:ALP76	Block boundary enclosure horizontal M6 track in vertical direction	**EN.5.1.M6**	=	0.076*n µm
DBLK.EN.5.1.M8:ALP76	Block boundary enclosure horizontal M8 track in vertical direction	**EN.5.1.M6**	=	0.076*n µm
DBLK.EN.5.1.M10:ALP76	Block boundary enclosure horizontal M10 track in vertical direction	**EN.5.1.M6**	=	0.076*n µm
DBLK.H280P57.EN.5.2.M1	In All H280P57 APR block, Core boundary enclosure vertical M1 track in horizontal direction	**EN.5.2.M1_1**	=	0.0095+0.038*n µm
DBLK.H280P57.EN.5.2.M1:ALP76	In All H280P57 APR block, Block boundary enclosure vertical M1CB track in horizontal direction	**EN.5.2.M1_2**	=	0.0125+0.076*n µm
DBLK.EN.5.2.M5:ALP76	Block boundary enclosure vertical M5 track in horizontal direction	**EN.5.2.M5**	=	0.0505+0.076*n µm
DBLK.EN.5.2.M7:ALP76	Block boundary enclosure vertical M7 track in horizontal direction	**EN.5.2.M5**	=	0.0505+0.076*n µm
DBLK.EN.5.2.M9:ALP76	Block boundary enclosure vertical M9 track in horizontal direction	**EN.5.2.M5**	=	0.0505+0.076*n µm

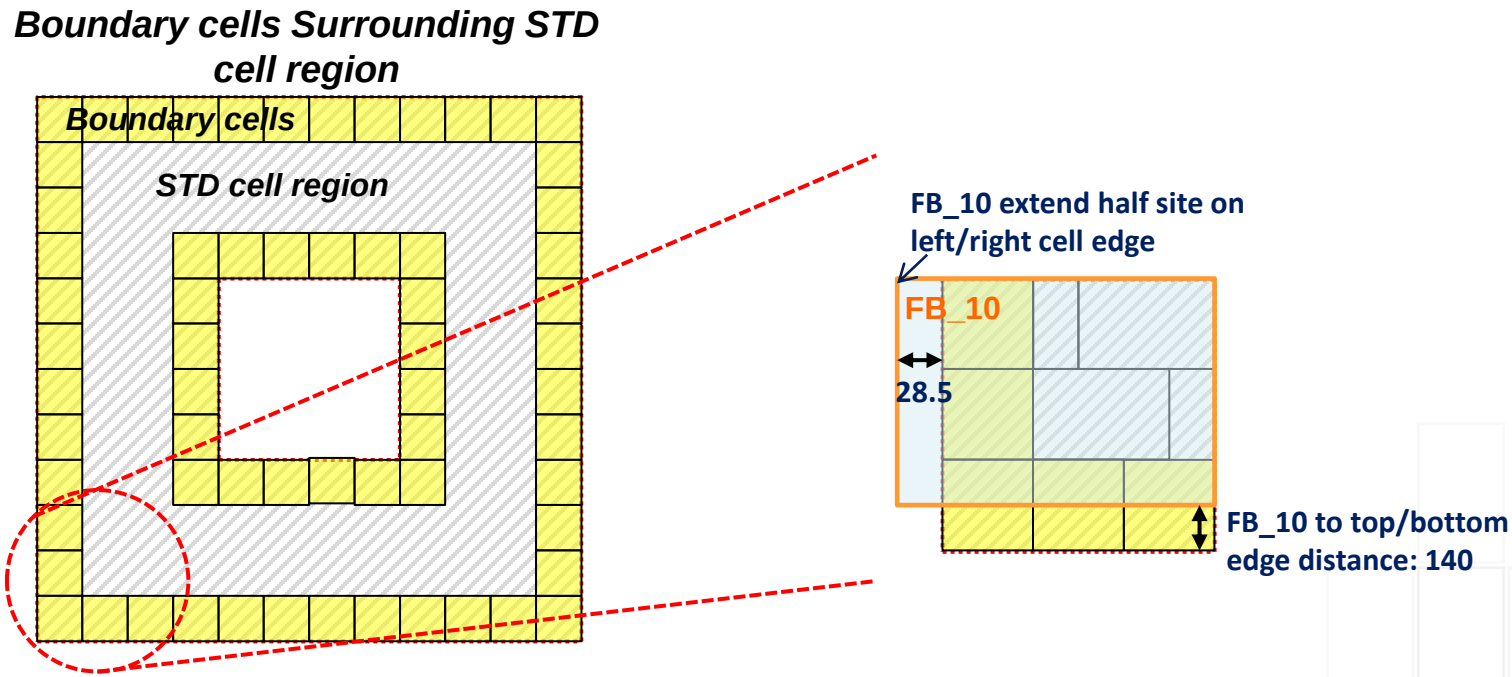
Unleash Innovation

H280P57 STD-Cell Region

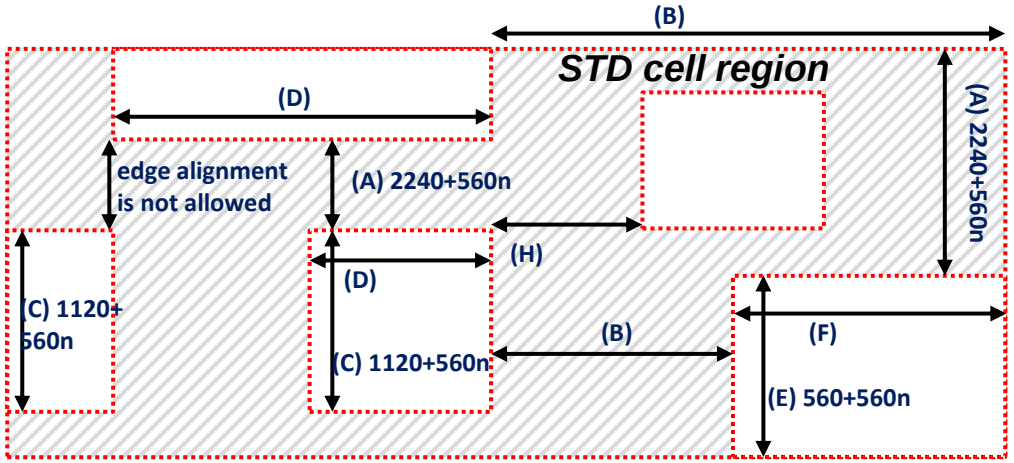
Chip-integration Design Guideline for APR
Specific Section for H280P57

- Dimension and Enclosure

H280P57 APR Block: FB_10 Region



H280P57 APR Block: STD Cell Region



Rule	Label	Boundary Cell Type	
		IW (Default)	CW
Width	(B)	4.047+0.114*n	3.477+0.114*n
Hole width	(D)	1.083+0.114*n	1.083+0.114*n
Jog length	(F)	1.140+0.114*n	0.798+0.114*n
Concave width	(H)	4.047+0.114*n	3.477+0.114*n

IW: Isolated NWELL boundary cell
CW: Common NWELL boundary cell

H280P57 APR Block: STD Cell Region

Default Guideline

Guideline No.	Guideline Description	Label	Op.	Rule
CORE.R.1	Boundary cell must surrounded on all edges of STD cell region	-		
CORE.H280P57.W.1.1	Width of H280P57 STD cell region in vertical direction	A	=	2.240+0.560*n µm
CORE.H280P57.W.1.2	Width of H280P57 STD cell region in horizontal direction	B	=	4.047+0.114*n µm
CORE.H280P57.W.2.1	Vertical edge length of H280P57 STD cell region between two consecutive 270-270 degree corners	C	=	1.120+0.560*n µm
CORE.H280P57.W.2.2	Horizontal edge length of H280P57 STD cell region between two consecutive 270-270 degree corners	D	=	1.083+0.114*n µm
CORE.H280P57.W.3.1	Vertical edge length of H280P57 STD cell region between two consecutive 90-270 degree corners	E	=	0.560+0.560*n µm
CORE.H280P57.W.3.2	Horizontal edge length of H280P57 STD cell region between two consecutive 90-270 degree corners	F	=	1.140+0.114*n µm
CORE.H280P57.W.4.2	Concave corner to concave corner width of H280P57 STD cell region in horizontal direction	H	=	4.047+0.114*n µm

Guideline Change when using CW (common well) type boundary Cells

Guideline No.	Guideline Description	Label	Op.	Rule
CORE.H280P57.W.1.2:BDRY CW	Width of H280P57 STD cell region in horizontal direction	B	=	3.477+0.114*n µm
CORE.H280P57.W.2.2:BDRY CW	Horizontal edge length of H280P57 STD cell region between two consecutive 270-270 degree corners	D	=	1.083+0.114*n µm
CORE.H280P57.W.3.2:BDRY CW	Horizontal edge length of H280P57 STD cell region between two consecutive 90-270 degree corners	F	=	0.798+0.114*n µm
CORE.H280P57.W.4.2:BDRY CW	Concave corner to concave corner width of H280P57 STD cell region in horizontal direction	H	=	3.477+0.114*n µm

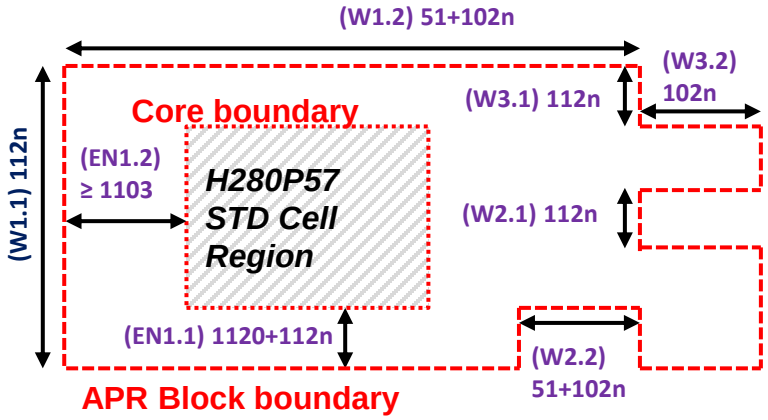
Unleash Innovation

H280P57 APR Block Design

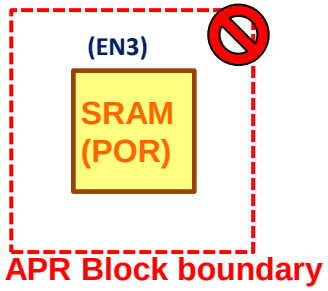
Chip-integration Design Guideline for APR Specific Section for H280P57

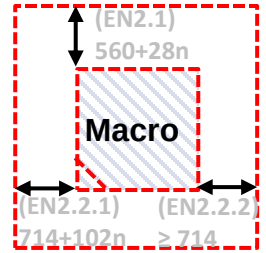
- H280P57 APR Block Design

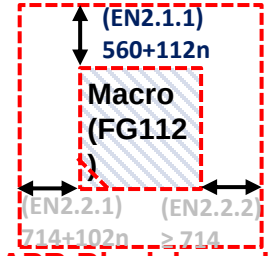
H280P57 APR Block Design Guidelines

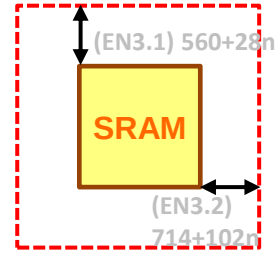


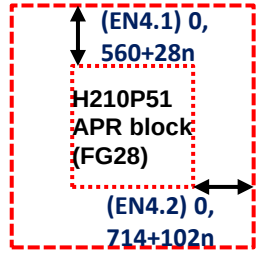
Notice:
Grey: Common guideline with other cell type
Blue labels: common guidelines for H280P57
Purple Labels: Non-BC guidelines
Green labels: BC guidelines

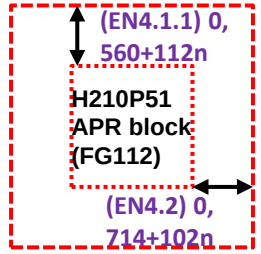


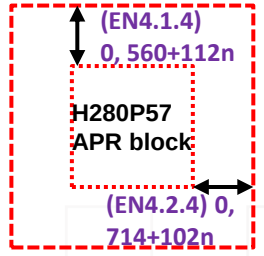


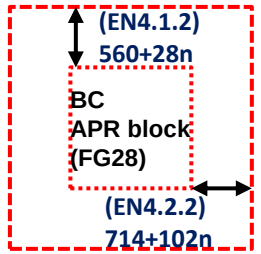


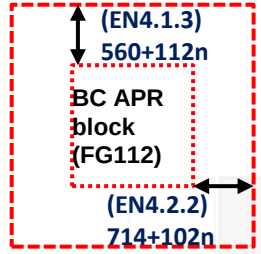


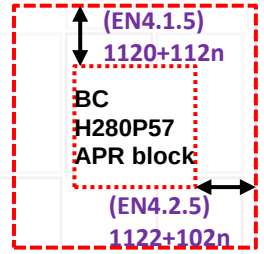




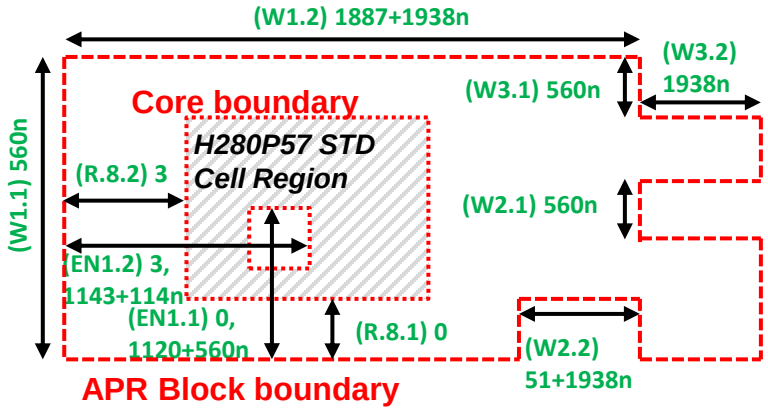


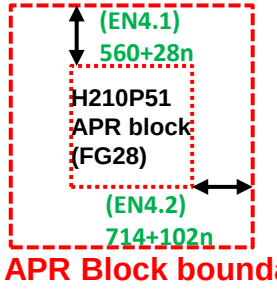


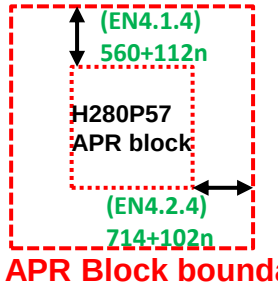


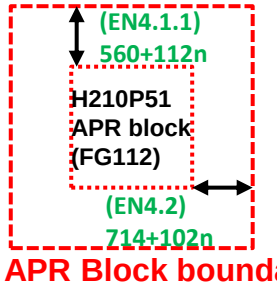


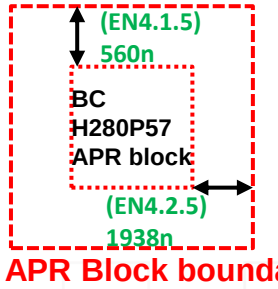
H280P57 APR Block Design Guidelines (Boundary Controlled)

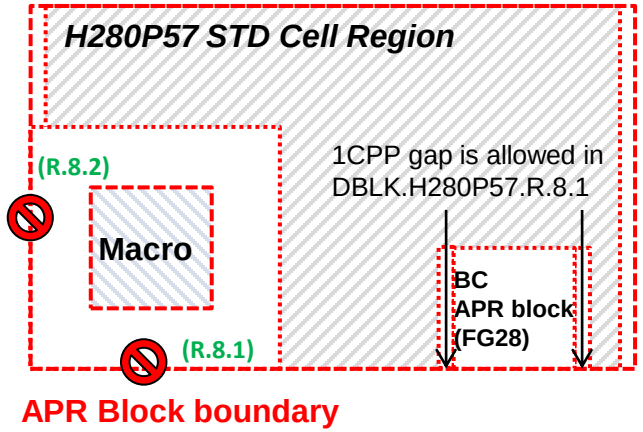


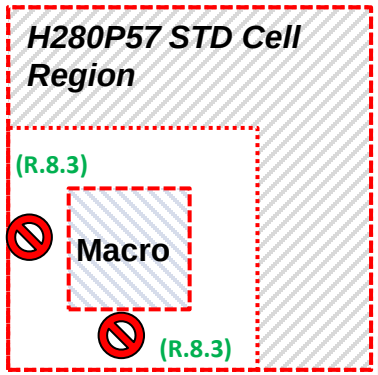


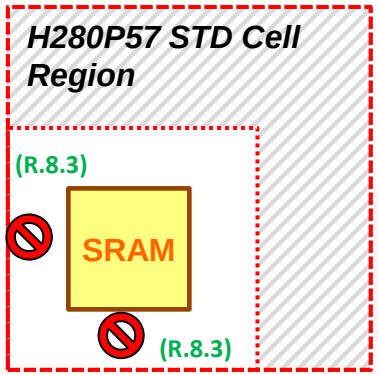


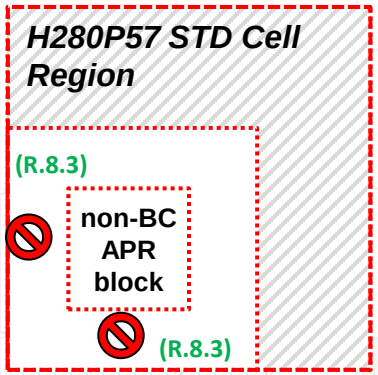












Notice:
Blue labels: common guidelines
Purple Labels: Non-BC guidelines
Green labels: BC guidelines

H280P57 APR Block Design

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.W.1.1:NOBC	Width of H280P57 APR Block in vertical direction	W1.1	=	0.112*n µm
DBLK.H280P57.W.1.1:BC	Width of H280P57 APR Block in vertical direction	W1.1	=	0.560*n µm
DBLK.H280P57.W.1.2:NOBC	Width of H280P57 APR Block in horizontal direction	W1.2	=	0.051+0.102*n µm
DBLK.H280P57.W.1.2:BC	Width of H280P57 APR Block in horizontal direction	W1.2	=	1.887+1.938*n µm
DBLK.H280P57.W.2.1:NOBC	Vertical edge length of H280P57 APR Block between two consecutive 270-270 degree corners	W2.1	=	0.112*n µm
DBLK.H280P57.W.2.1:BC	Vertical edge length of H280P57 APR Block between two consecutive 270-270 degree corners	W2.1	=	0.560*n µm
DBLK.H280P57.W.2.2:NOBC	Horizontal edge length of H280P57 APR Block between two consecutive 270-270 degree corners	W2.2	=	0.051+0.102*n µm
DBLK.H280P57.W.2.2:BC	Horizontal edge length of H280P57 APR Block between two consecutive 270-270 degree corners	W2.2	=	0.051+1.938*n µm
DBLK.H280P57.W.3.1:NOBC	Vertical edge length of H280P57 APR Block between two consecutive 90-270 degree corners	W3.1	=	0.112*n µm
DBLK.H280P57.W.3.1:BC	Vertical edge length of H280P57 APR Block between two consecutive 90-270 degree corners	W3.1	=	0.560*n µm
DBLK.H280P57.W.3.2:NOBC	Horizontal edge length of H280P57 APR Block between two consecutive 90-270 degree corners	W3.2	=	0.102*n µm
DBLK.H280P57.W.3.2:BC	Horizontal edge length of H280P57 APR Block between two consecutive 90-270 degree corners	W3.2	=	1.938*n µm
DBLK.H280P57.EN.1.1:NOBC	In H280P57 APR block, Block edge enclosure H280P57 STD cell region (core) in vertical direction	EN1.1	=	1.120+0.112*n µm
DBLK.H280P57.EN.1.1:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure H280P57 STD cell region (core) in vertical direction	EN1.1	=	0, 1.120+0.560*n µm

H280P57 APR Block Design

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.EN.1.2:NOBC	In H280P57 APR block, Block edge enclosure H280P57 STD cell region (core) in horizontal direction	EN1.2	≥	1.103 µm
DBLK.H280P57.EN.1.2:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure H280P57 STD cell region (core) in horizontal direction	EN1.2	=	0.003 1.143+0.114*n µm
DBLK.EN.2.1	Block edge enclosure Macro in vertical direction	EN2.1	=	0.560+0.028*n µm
DBLK.H280P57.EN.2.1.1	In All H280P57 APR block, Block edge enclosure Fin Grid 112nm Macro in vertical direction	EN2.1.1	=	0.560+0.112*n µm
DBLK.EN.2.2.1	Block edge enclosure Left edge of Macro in horizontal direction	EN2.2.1	=	0.714+0.102*n µm
DBLK.EN.2.2.2	Block edge enclosure Right edge of Macro in horizontal direction	EN2.2.2	≥	0.714 µm
DBLK.EN.3.1	Block edge enclosure TSMC SRAM in vertical direction	EN3.1	=	0.560+0.028*n µm
DBLK.EN.3.2	Block edge enclosure TSMC SRAM in horizontal direction	EN3.2	=	0.714+0.102*n µm
DBLK.H280P57.EN.3	TSMC POR SRAM is not allowed in All H280P57 APR block	EN3		
DBLK.H280P57.EN.4.1:NOBC	In H280P57 APR block, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1	=	0, 0.560+0.028*n µm
DBLK.H280P57.EN.4.1:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1	=	0.560+0.028*n µm
DBLK.H280P57.EN.4.1.1:NOBC	In H280P57 APR block, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.1	=	0, 0.560+0.112*n µm
DBLK.H280P57.EN.4.1.1:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure Non-BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.1	=	0.560+0.112*n µm
DBLK.H280P57.EN.4.1.2	In All H280P57 APR block, Block edge enclosure BC H210P51 APR block with Fin Grid 28nm in vertical direction	EN4.1.2	=	0.560+0.028*n µm
DBLK.H280P57.EN.4.1.3	In All H280P57 APR block, Block edge enclosure BC H210P51 APR block with Fin Grid 112nm in vertical direction	EN4.1.3	=	0.560+0.112*n µm
DBLK.H280P57.EN.4.1.4:NOBC	In H280P57 APR block, Block edge enclosure H280P57 APR block in vertical direction	EN4.1.4	=	0, 0.560+0.112*n µm
DBLK.H280P57.EN.4.1.4:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure H280P57 APR block in vertical direction	EN4.1.4	=	0.560+0.112*n µm

H280P57 APR Block Design

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.EN.4.1.5:NOBC	In H280P57 APR block, Block edge enclosure Boundary Controlled H280P57 APR block in vertical direction	EN4.1.5	=	1.120+0.112*n µm
DBLK.H280P57.EN.4.1.5:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure Boundary Controlled H280P57 APR block in vertical direction	EN4.1.5	=	0.560*n µm
DBLK.H280P57.EN.4.2:NOBC	In H280P57 APR block, Block edge enclosure H210P51 APR block w/o Boundary Controlled in horizontal direction	EN4.2	=	0, 0.714+0.102*n µm
DBLK.H280P57.EN.4.2:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure H210P51 APR block w/o Boundary Controlled in horizontal direction	EN4.2	=	0.714+0.102*n µm
DBLK.H280P57.EN.4.2.2	In All H280P57 APR block, Block edge enclosure Boundary Controlled H210P51 APR block in horizontal direction	EN4.2.2	=	0.714+0.102*n µm
DBLK.H280P57.EN.4.2.4:NOBC	In H280P57 APR block, Block edge enclosure H280P57 APR block in horizontal direction	EN4.2.4	=	0, 0.714+0.102*n µm
DBLK.H280P57.EN.4.2.4:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure H280P57 APR block in horizontal direction	EN4.2.4	=	0.714+0.102*n µm
DBLK.H280P57.EN.4.2.5:NOBC	In H280P57 APR block, Block edge enclosure Boundary Controlled H280P57 APR block in horizontal direction	EN4.2.5		1.122+0.102*n µm
DBLK.H280P57.EN.4.2.5:BC	In Boundary Controlled H280P57 APR block, Block edge enclosure Boundary Controlled H280P57 APR block in horizontal direction	EN4.2.5		1.938*n µm
DBLK.H280P57.R.8.1:BC	In Boundary Controlled H280P57 APR block, empty area cannot touch horizontal block edges (Rule checks block enclosure **Checked_Empty_Area_H280P57** in vertical direction >0) Definition of **Checked_Empty_Area_H280P57**: Checked_Empty_Area_H280P57 = Block NOT { { H280P57 STD cell region size 0.0285 in horizontal direction} OR {Boundary Controlled H280P57 APR Block size 0.0255 in horizontal direction} OR Macro }	R.8.1		
DBLK.H280P57.R.8.2:BC	In Boundary Controlled H280P57 APR block, empty area cannot touch vertical block edges (Rule checks block enclosure **Checked_Empty_Area_H280P57** in horizontal direction >0) Definition of Checked_Empty_Area_H280P57: Please refer to DBLK.H280P57.R.8.1:BC	R.8.2		
DBLK.H280P57.R.8.3:BC	In Boundary Controlled H280P57 APR block, macro, TSMC SRAM and APR block w/o Boundary Controlled must be surrounded by H280P57 STD cell region	R.8.3		

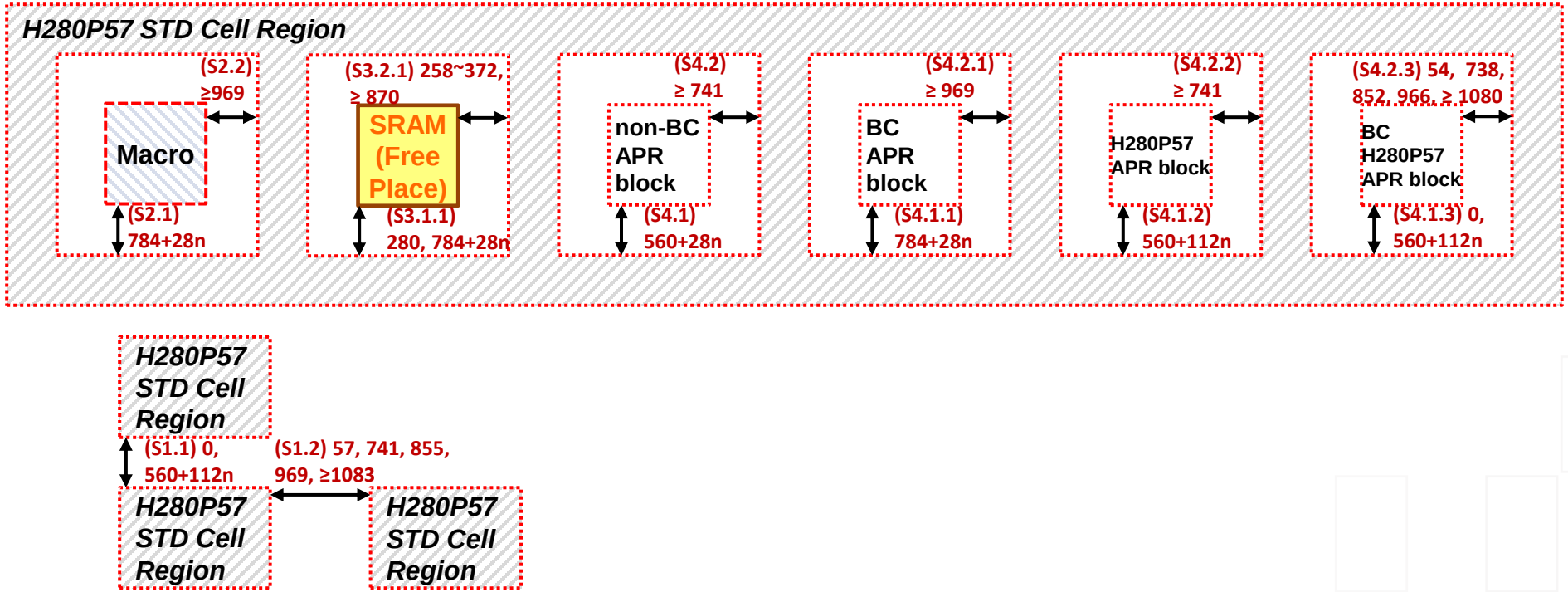
Unleash Innovation

H280P57 Spacing

Chip-integration Design Guideline for APR
Specific Section for H280P57

- **Placement**

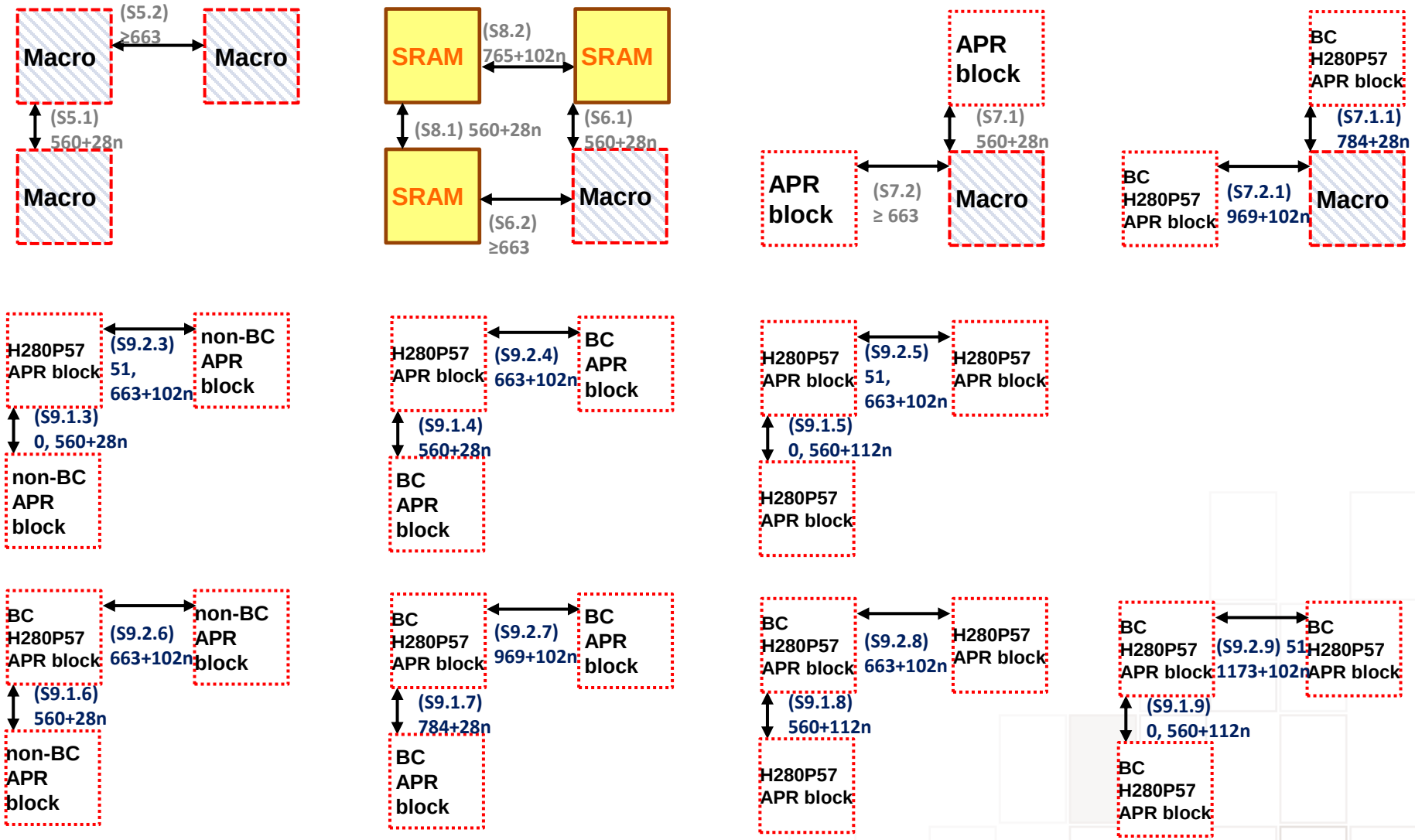
H280P57 APR Block: Spacing



H280P57 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.S.1.1	Spacing of H280P57 STD cell region in vertical direction (PRL≥-0.741μm)	S1.1	=	0, 0.560+0.112*n μm
DBLK.H280P57.S.1.2	Spacing of H280P57 STD cell region in horizontal direction (PRL≥-0.560μm)	S1.2	=	0.057, 0.741, 0.855, 0.969, ≥1.083 μm
DBLK.H280P57.S.2.1	Macro to H280P57 STD cell region spacing in vertical direction (PRL>-0.969μm)	S2.1	=	0.784+0.028*n μm
DBLK.H280P57.S.2.2	Macro to H280P57 STD cell region spacing in horizontal direction (PRL>-0.784μm)	S2.2	≥	0.969 μm
DBLK.H280P57.S.3.1.1	TSMC free placement SRAM to H280P57 STD cell region spacing in vertical direction (PRL>-0.969μm)	S3.1.1	=	0.280, 0.784+0.028*n μm
DBLK.H280P57.S.3.2.1	TSMC free placement SRAM to H280P57 STD cell region spacing in horizontal direction (PRL>-0.784μm)	S3.2.1	=	0.258~0.372, ≥0.870 μm
DBLK.H280P57.S.4.1	H210P51 APR block w/o Boundary Controlled to H280P57 STD cell region spacing in vertical direction (PRL > -0.741μm)	S4.1	=	0.560+0.028*n μm
DBLK.H280P57.S.4.1.1	Boundary Controlled H210P51 APR Block to H280P57 STD cell region spacing in vertical direction (PRL > -0.969μm)	S4.1.1	=	0.784+0.028*n μm
DBLK.H280P57.S.4.1.2	H280P57 APR block to H280P57 STD cell region spacing in vertical direction (PRL > -0.741μm)	S4.1.2	=	0.560+0.112*n μm
DBLK.H280P57.S.4.1.3	Boundary Controlled H280P57 APR block to H280P57 STD cell region spacing in vertical direction (PRL > -0.738μm)	S4.1.3	=	0, 0.560+0.112*n μm
DBLK.H280P57.S.4.2	H210P51 APR block w/o Boundary Controlled to H280P57 STD cell region spacing in horizontal direction (PRL > -0.560μm)	S4.2	≥	0.741 μm
DBLK.H280P57.S.4.2.1	Boundary Controlled H210P51 APR Block to H280P57 STD cell region spacing in horizontal direction (PRL > -0.784μm)	S4.2.1	≥	0.969 μm
DBLK.H280P57.S.4.2.2	H280P57 APR block to H280P57 STD cell region spacing in horizontal direction (PRL > -0.560μm)	S4.2.2	≥	0.741 μm
DBLK.H280P57.S.4.2.3	Boundary Controlled H280P57 APR block to H280P57 STD cell region spacing in horizontal direction (PRL > -1.077μm)	S4.2.3	≥	0.054, 0.738, 0.852, 0.966, ≥1.080 μm

H280P57 APR Block: Spacing



H280P57 APR Block: Spacing

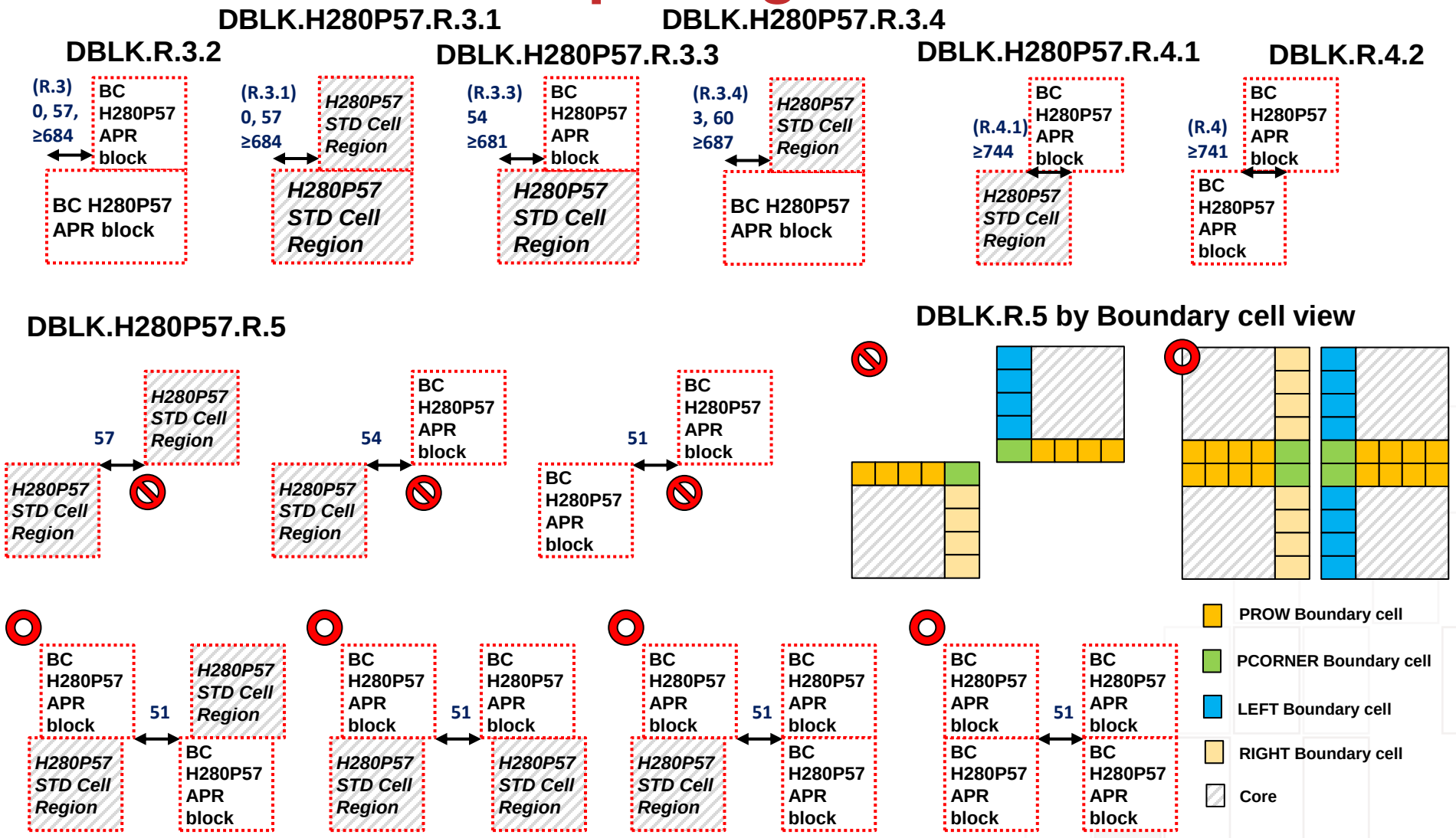
***Guidelines in grey text are identical with H210P51 APR Block**

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.S.5.1	Spacing from Macro to Macro in vertical direction (PRL>-0.663μm)	S5.1	=	0.560+0.028*n μm
DBLK.S.5.2	Spacing from Macro to Macro in horizontal direction (PRL>-0.560μm)	S5.2	≥	0.663 μm
DBLK.S.6.1	Spacing from TSMC SRAM to Macro in vertical direction (PRL>-0.663μm)	S6.1	=	0.560+0.028*n μm
DBLK.S.6.2	Spacing from TSMC SRAM to Macro in horizontal direction (PRL>-0.560μm)	S6.2	≥	0.663 μm
DBLK.S.7.1	Spacing from APR block to Macro in vertical direction (PRL>-0.663μm)	S7.1	=	0.560+0.028*n μm
DBLK.S.7.1.1	Spacing from Boundary Controlled H280P57 APR block to Macro in vertical direction (PRL>-0.969μm)	S7.1.1	=	0.784+0.028*n μm
DBLK.S.7.2	Spacing from APR block to Macro in horizontal direction (PRL>-0.560μm)	S7.2	≥	0.663 μm
DBLK.S.7.2.1	Spacing from Boundary Controlled H280P57 APR block to Macro in horizontal direction (PRL>-0.784μm)	S7.2.1	=	0.969+0.102*n μm
DBLK.S.8.1	Spacing of TSMC SRAM in vertical direction (PRL>-0.765μm), except: 1. Both TSMC SRAM are TSMC POR SRAM 2. Both TSMC SRAM are identical TSMC Free Placement SRAM, with mirrored orientation	S8.1	=	0.560+0.028*n μm
DBLK.S.8.1.3	Spacing of a pair of mirrored, identical TSMC Free Placement SRAM in vertical direction, except STD cell region in between (PRL >-0.765μm)	S8.1.3	=	0, 0.560+0.028*n μm
DBLK.S.8.2	Spacing of TSMC SRAM in horizontal direction (PRL >-0.560μm), except: 1. Both TSMC SRAM are TSMC POR SRAM 2. Both TSMC SRAM are identical TSMC Free Placement SRAM, with mirrored orientation	S8.2	=	0.765+0.102*n μm
DBLK.S.8.2.4	Array side spacing of a pair of mirrored, identical TSMC Free Placement SRAM in horizontal direction (PRL >-0.560μm)	S8.2.4	=	0.051, 0.765+0.102*n μm
DBLK.S.8.2.5	Pin side spacing of a pair of mirrored, identical TSMC Free Placement SRAM in horizontal direction (PRL >-0.560μm)	S8.2.5	=	0.765+0.102*n μm
DBLK.S.8.2.6	Array side spacing of TSMC ROM in horizontal direction (PRL >0μm)	S8.2.6	=	6.987+0.102*n μm

H280P57 APR Block: Spacing

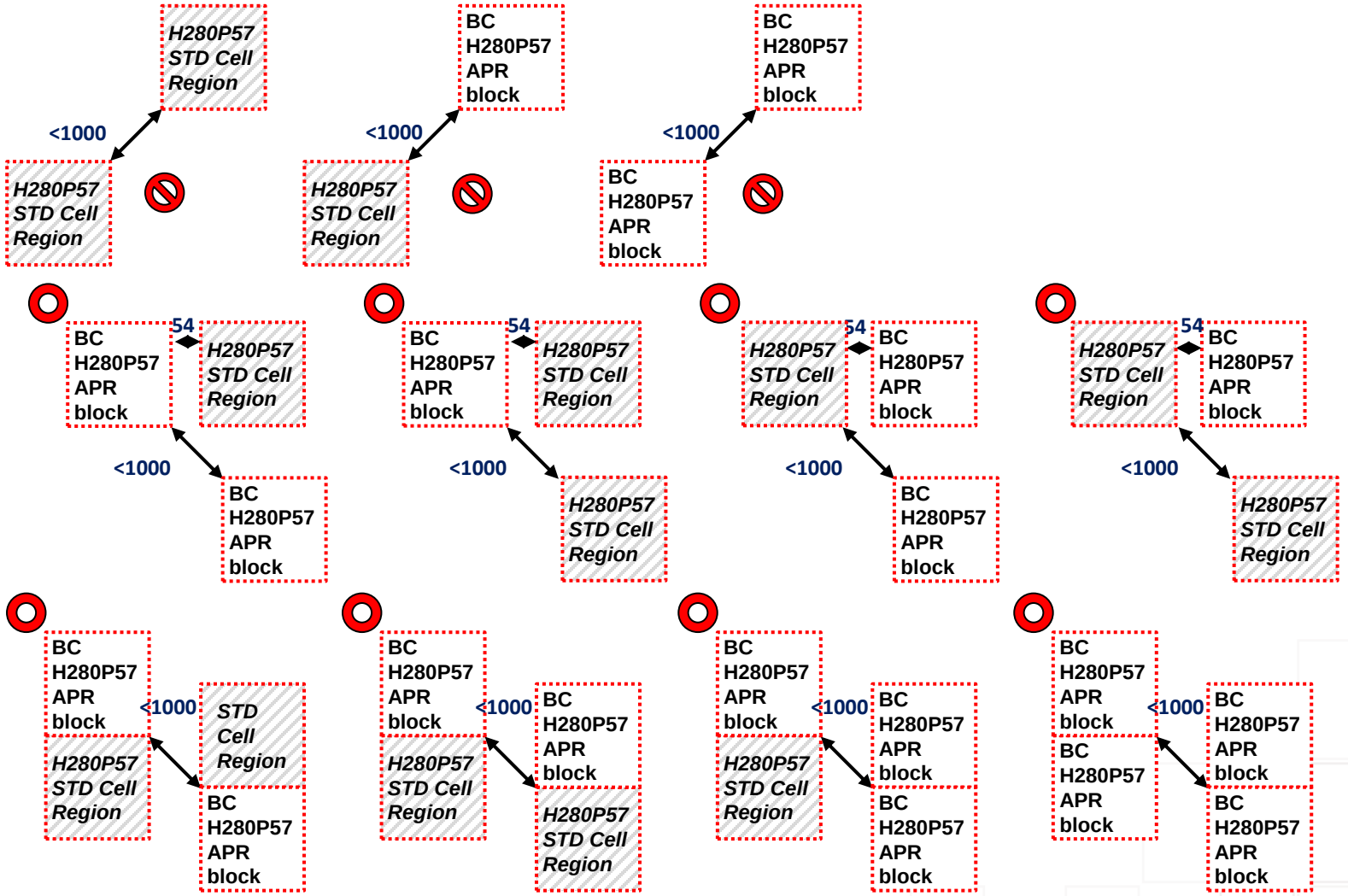
Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.S.9.1.3	Spacing from H210P51 APR block w/o Boundary Controlled to H280P57 APR block in vertical direction (PRL>-0.663μm)	**S9.1.3**	=	0, 0.560+0.028*n μm
DBLK.S.9.1.4	Spacing from Boundary Controlled H210P51 APR Block to H280P57 APR block in vertical direction (PRL>-0.663μm)	**S9.1.4**	=	0.560+0.028*n μm
DBLK.S.9.1.5	Spacing of H280P57 APR block in vertical direction (PRL>-0.663μm)	**S9.1.5**	=	0, 0.560+0.112*n μm
DBLK.S.9.1.6	Spacing from H210P51 APR block w/o Boundary Controlled to Boundary Controlled H280P57 APR block in vertical direction (PRL>-0.663μm)	**S9.1.6**	=	0.560+0.028*n μm
DBLK.S.9.1.7	Spacing from Boundary Controlled H210P51 APR Block to Boundary Controlled H280P57 APR block in vertical direction (PRL>-0.969μm)	**S9.1.7**	=	0.784+0.028*n μm
DBLK.S.9.1.8	Spacing from H280P57 APR block to Boundary Controlled H280P57 APR block in vertical direction (PRL>-0.663μm)	**S9.1.8**	=	0.560+0.112*n μm
DBLK.S.9.1.9	Spacing of Boundary Controlled H280P57 APR block in vertical direction (PRL>-0.051μm)	**S9.1.9**		0, 0.560+0.112*n μm
DBLK.S.9.2.3	Spacing from H210P51 APR block w/o Boundary Controlled to H280P57 APR block in horizontal direction (PRL>-0.560μm)	**S9.2.3**	=	0.051, 0.663+0.102*n μm
DBLK.S.9.2.4	Spacing from Boundary Controlled H210P51 APR Block to H280P57 APR block in horizontal direction (PRL>-0.560μm)	**S9.2.4**	=	0.663+0.102*n μm
DBLK.S.9.2.5	Spacing of H280P57 APR block in horizontal direction (PRL>-0.560μm)	**S9.2.5**	=	0.051, 0.663+0.102*n μm
DBLK.S.9.2.6	Spacing from H210P51 APR block w/o Boundary Controlled to Boundary Controlled H280P57 APR block in horizontal direction (PRL>-0.560μm)	**S9.2.6**	=	0.663+0.102*n μm
DBLK.S.9.2.7	Spacing from Boundary Controlled H210P51 APR Block to Boundary Controlled H280P57 APR block in horizontal direction (PRL>-0.784μm)	**S9.2.7**	=	0.969+0.102*n μm
DBLK.S.9.2.8	Spacing from H280P57 APR block to Boundary Controlled H280P57 APR block in horizontal direction (PRL>-0.560μm)	**S9.2.8**	=	0.663+0.102*n μm
DBLK.S.9.2.9	Spacing of Boundary Controlled H280P57 APR block in horizontal direction (PRL>-1.083μm)	**S9.2.9**	=	0.051, 1.173+0.102*n μm

H280P57 APR Block: Spacing



H280P57 APR Block: Spacing

DBLK.H280P57.R.5.1



H280P57 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.R.3.1	Project length difference between horizontal edges of H280P57 STD cell region when vertical abutting (This rule checks two H280P57 STD cell region in different power domain)	**R.3.1**	=	0, 0.057, ≥0.684 µm
DBLK.R.3.2	Project length difference between horizontal edges of Boundary Controlled H280P57 APR Block when vertical abutting	**R.3.2**	=	0, 0.057, ≥0.684 µm
DBLK.H280P57.R.3.3	Project length difference between horizontal edges of H280P57 STD cell region and vertically abutting Boundary Controlled H280P57 APR Block, when edge of H280P57 STD cell region is longer	**R.3.3**	=	0.054, ≥0.681 µm
DBLK.H280P57.R.3.4	Project length difference between horizontal edges of H280P57 STD cell region and vertically abutting Boundary Controlled H280P57 APR Block, when edge of Boundary Controlled H280P57 APR Block is equal or longer	**R.3.4**	=	0, 0.060, ≥0.687 µm
DBLK.H280P57.R.4.1	Overlap width of vertical abutting H280P57 STD cell region and Boundary Controlled H280P57 APR Block	**R.4.1**	≥	0.744 µm
DBLK.R.4.2	Overlap width of vertical abutting Boundary Controlled H280P57 APR Block	**R.4.2**	≥	0.741 µm

H280P57 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.H280P57.R.5	Forbid point touch (horizontal spacing 0.051, 0.054 or 0.057 μm, PRL =0) of 2 H280P57 STD cell region, or Boundary Controlled H280P57 APR Block, except 4 point touch (tCIC check spacing of **Checked_Empty_Area_H280P57** ≥ 0.001 μm, PRL ≥ -0.001 μm)			
DBLK.H280P57.R.5.1	Corner spacing between H280P57 STD cell region, or Boundary Controlled H280P57 APR Block should be ≥ 1μm, except following condition 1. Anyone of corner belong to horizontal edge, that vertically abut with another H280P57 STD cell region, or Boundary Controlled H280P57 APR Block 2. Anyone of corner belong to vertical edge of H280P57 STD cell region, that keep 0.057μm horizontal spacing with another H280P57 STD cell region 3. Anyone of corner belong to vertical edge of H280P57 STD cell region, that keep 0.054μm horizontal spacing with Boundary Controlled H280P57 APR Block 4. Anyone of corner belong to vertical edge of Boundary Controlled H280P57 APR Block, that keep 0.054μm horizontal spacing with H280P57 STD cell region 5. Anyone of corner belong to vertical edge of Boundary Controlled H280P57 APR Block, that keep 0.051μm horizontal spacing with another Boundary Controlled H280P57 APR Block			

H280P57 APR Block: Spacing

Guideline No.	Guideline Description	Label	Op.	Rule
DBLK.R.9	Project length Difference between two {Boundary Controlled H280P57 Block SIZE 0.0255µm in horizontal direction} with vertical spacing ≤ 1.077µm	R.9	=	0.114*n µm
DBLK.H280P57.R.9.1	Project length Difference between two {H280P57 STD cell region Block SIZE 0.0285µm in horizontal direction}with vertical spacing ≤ 1.077µm	R.9.1	=	0.114*n µm
DBLK.H280P57.R.9.2	Project length Difference from {H280P57 STD cell region SIZE 0.0285µm in horizontal direction} to {Boundary Controlled H280P57 Block SIZE 0.0255µm in horizontal direction} with vertical spacing ≤ 1.077µm	R.9.2	=	0.114*n µm

DBLK.H280P57.R.9 / DBLK.H280P57.R.9.1 / DBLK.H280P57.R.9.2