

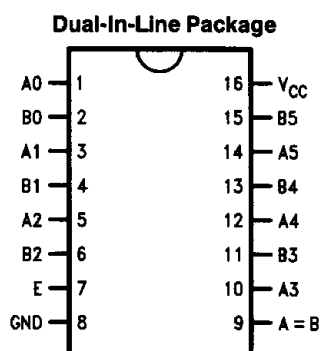
DM93S46

High-Speed 6-Bit Identity Comparator

General Description

The DM93S46 is a very high speed 6-bit identity comparator. The device compares two words of up to six bits and indicates identity in less than 12 ns. It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable input (E) is LOW, it forces the output LOW.

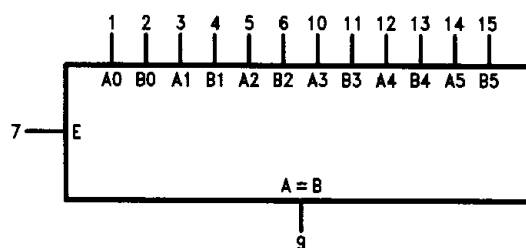
Connection Diagram



TL/F/9807-1

Order Number **DM93S46N**
See NS Package Number **N16E**

Logic Symbol



V_{CC} = Pin 16
GND = Pin 18

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Pin Name	Description
A0-A5	Word A Inputs
B0-B5	Word B Inputs
E	Enable Input (Active High)
A = B	A Equal to B Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 5.5V

Operating Free Air Temperature Range
DM93S 0°C to +70°C

Storage Temperature Range -65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM93S46			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			-1	mA
I _{OL}	Low Level Output Current			20	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.2	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.7	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min		0.35	0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			50	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.5V			-20	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	-40		-100	mA
I _{CC}	Supply Current	V _{CC} = Max			70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	Conditions	CL = 15 pF		Units
			Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n or B _n to A = B	E = 4.5V, Other Inputs = 4.5V, Test Each Input Individually	3.0 3.0	17 17	ns
t _{PLH} t _{PHL}	Propagation Delay A _n or B _n to A = B	E = 4.5V, Other Inputs = Gnd, Test Each Input Individually	3.0 3.0	14 15	ns
t _{PLH} t _{PHL}	Propagation Delay E to A = B	A _n = B _n	2.0 2.0	10 10	ns

Functional Description

The DM93S46 is a very high speed 6-bit identity comparator. The $A = B$ output is HIGH when the Enable (E) is HIGH and the two 6-bit words are equal. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. When any two of the equivalent bits from each word have different logic levels, the $A = B$ output is LOW.

$$(A = B) = (A_0 \oplus B_0) \cdot (A_1 \oplus B_1) \cdot (A_2 \oplus B_2) \cdot (A_3 \oplus B_3) \cdot (A_4 \oplus B_4) \cdot (A_5 \oplus B_5) \cdot E$$

An active HIGH Enable (E) provides a means of fast ripple expansion. By connecting the $A = B$ output of the first stage of the comparator to the enable of the next stage, the comparator can be expanded in 6-bit increments at an additional 4.5 ns per stage. An even faster expansion technique is achieved by connecting the $A = B$ outputs to a Schottky NAND gate. This method compares two words of up to 78 bits each in 15 ns (typical) using the '133 13-input Schottky NAND gate.

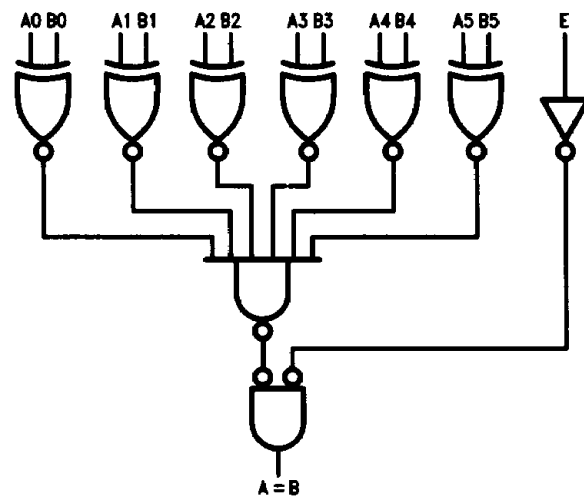
Truth Table

Inputs		Output
E	A_n, B_n	$A = B$
L	$A_n = B_n$	L
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	L
H	$A_n = B_n$	H

H = HIGH Voltage Level

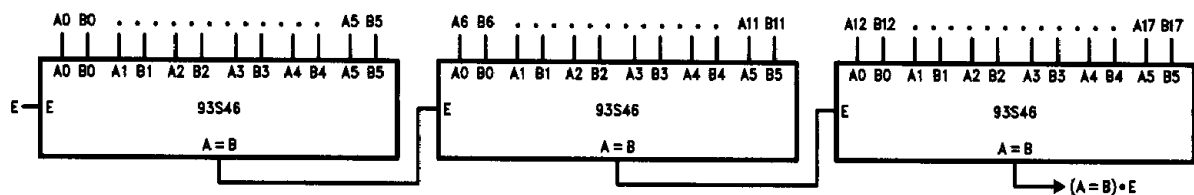
L = LOW Voltage Level

Logic Diagram



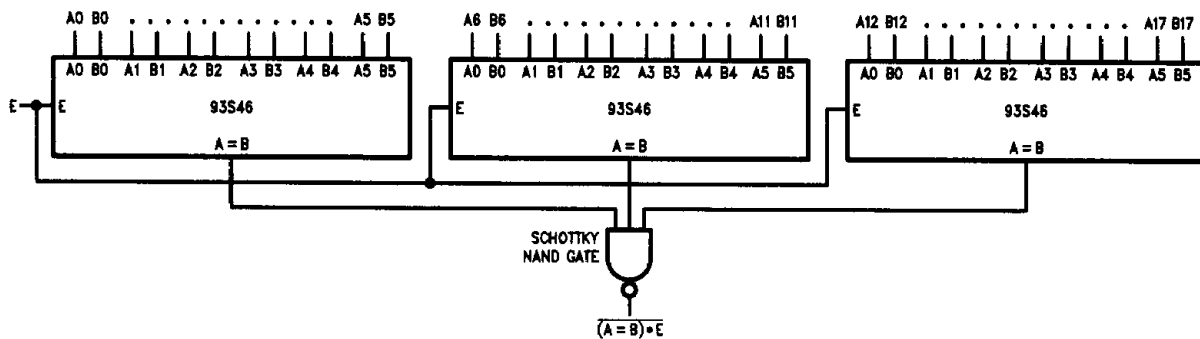
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Ripple Expansion



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Note: This simple method of expansion adds 4.5 ns for each additional '46 used.



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Note: This method of expansion adds one gate delay (≈ 3 ns) to the '46, independent of the word length that is compared.