Am93415/Am93425

1024 x 1 Bit TTL Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 1024-word x 1-bit RAMs
- Ultra-high speed (SA) version:
  Address Access time 20 ns
  High Speed (A) version:
  Address Access time 30 ns
  Standard version:
  Address Access time 45 ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am93425 series) or with open-collector outputs (Am93415 series)
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Plug in replacement for Fairchild 93415A/415 and 93425A/425, and Intel 2115/2125 series
- I_{CC} decreases as temperature increases

GENERAL DESCRIPTION

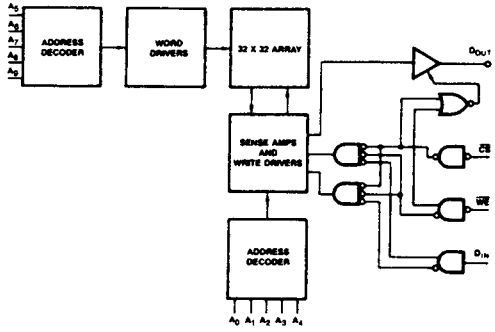
The Am93415 and Am93425 are fully decoded 1024 x 1 RAMs built with Schottky diode clamped transistors in conjunction with internal ECL circuitry. They are ideal for use in high-speed control and buffer memory applications. Easy memory expansion is provided by an active LOW chip select input ($\overline{CS}$) and either open-collector or three-state outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the data input (D_{IN}) is written into the addressed memory word and the output circuitry preconditioned so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or any time the chip select line is HIGH, the output of the memory goes to an inactive high-impedance state.

BLOCK DIAGRAM



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MODE SELECT TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	*Hi-Z	Not Selected
L	L	L	*Hi-Z	Write "0"
L	L	H	*Hi-Z	Write "1"
L	H	X	Selected Data	Read

H = HIGH L = LOW X = Don't Care

*Hi-Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the Am93425 series and as an output high level for the Am93415 series.

PRODUCT SELECTOR GUIDE

Access Time	20 ns	30 ns		40 ns	45 ns
Temperature Range	C	C	M	M	C
Open-Collector	Am93415SA	Am93415A	Am93415SA	Am93415A	Am93415A
Three-State	Am93425SA	Am93425A	Am93425SA	Am93425A	Am93425

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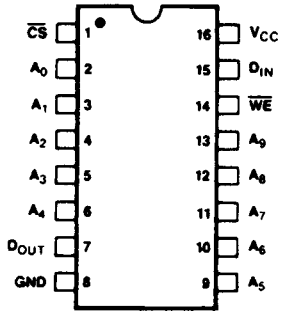
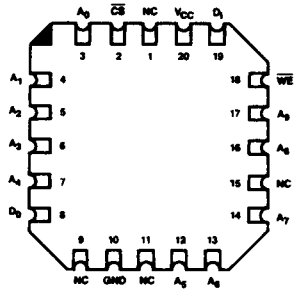
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD000900



CD000910

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM93425 SA D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
P = 16-Pin Plastic DIP (PD 016)
D = 16-Pin Ceramic DIP (CD 016)

B. SPEED OPTION
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
Am93415/Am93425
1024 x 1 Bit TTL Bipolar IMOX RAM
Am93415 = Open-Collector
Am93425 = Three-State

Valid Combinations	
AM93415SA	PC, PCB, DC, DCB
AM93425SA	
AM93415A	
AM93425A	
AM93415	
AM93425	

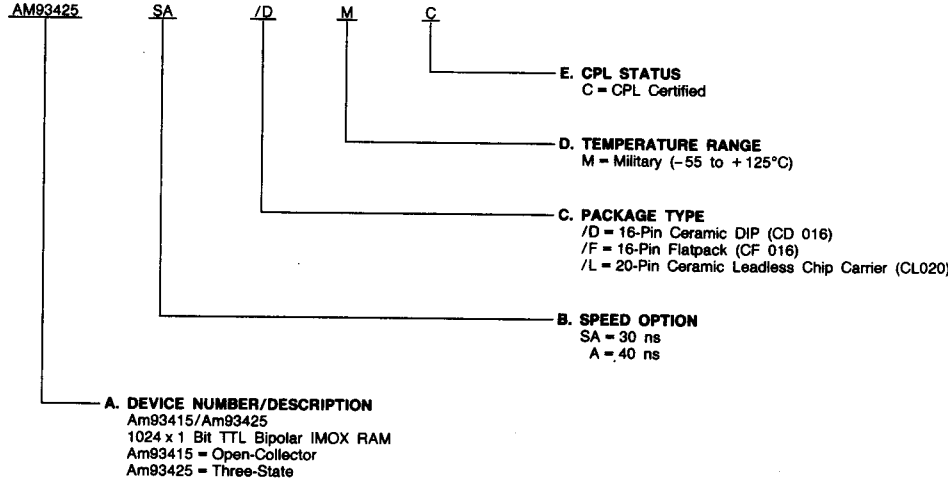
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status



Valid Combinations	
AM93425SA	/DMC, /FMC, /LMC
AM93415SA	
AM93425A	
AM93415A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 6)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

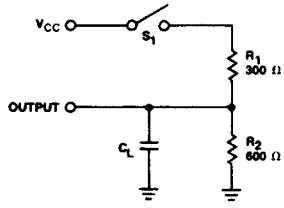
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −10.3 mA	COM'L	2.4	3.4		Volts
			I_{OH} = −5.2 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 16 mA		0.33	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.1			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V				−90	−400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V				1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 5)			−20	−50	−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.	SA Device				150	mA
			A and STD Devices				125	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −10 mA				−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 2.4 V		Am93415 Series Only		0	100	μA
				Am93425 Series Only		0	50	
		$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0.5 V, V_{CC} = Max.		Am93425 Series Only	−50	0		
C_{IN}	Input Pin Capacitance	See Note 4				8		pF
C_{OUT}	Output Pin Capacitance	See Note 4				10		pF

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies only to devices with three-state output. (Am93L425 series)
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Input and output capacitance measured on a sample basis using pulse technique.
5. Duration of the short circuit test should not be more than one second.
6. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
$\theta_{JA} \approx 60°C/W$ (with moving air) for CeramicDIP.
$\theta_{JC} \approx 10-17°C/W$ for Flatpack.

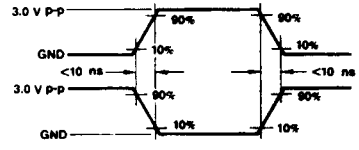
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



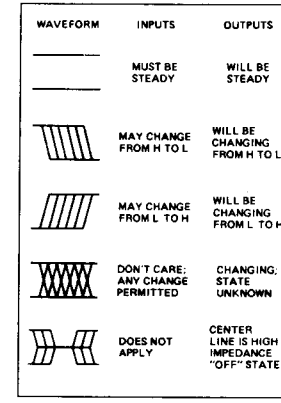
TC000171

SWITCHING TEST WAVEFORM



TW000031

KEY TO SWITCHING WAVEFORMS



KS000010

See notes 1, 2 and 3 of Switching Characteristics.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93415SA/25SA				Am93415A/25A				Units
			C devices		M devices		C devices		M devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PLH}(A)	Delay from Address to Output		20		30		30		40	ns
2	t_{PHL}(A)										
3	$t_{PZH}\overline{CS}$	Delay from Chip Select to Active Output and Correct Data		15		25		20		30	ns
4	$t_{PZL}\overline{CS}$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		15		25		25		35	ns
6	$t_{PZL}(\overline{WE})$										
7	t_s(A)	Setup Time Address (Prior to Initiation of Write)	5		5		5		5		ns
8	t_h(A)	Hold Time Address (After Termination of Write)	0		5		5		5		ns
9	t_s(DI)	Setup Time Data Input (Prior to Initiation of Write)	0		5		5		5		ns
10	t_h(DI)	Hold Time Data Input (After Termination of Write)	0		5		5		5		ns
11	$t_s(\overline{CS})$	Setup Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
12	$t_h(\overline{CS})$	Hold Time Chip Select (After Termination of Write)	0		5		5		5		ns
13	$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	15		25		20		30		ns
14	$t_{PHZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (Hi-Z)		20		30		20		30	ns
15	$t_{PLZ}(\overline{CS})$										
16	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		15		25		20		30	ns
17	$t_{PLZ}(\overline{WE})$										

*See the last page of this spec for Group A Subgroup Testing information.

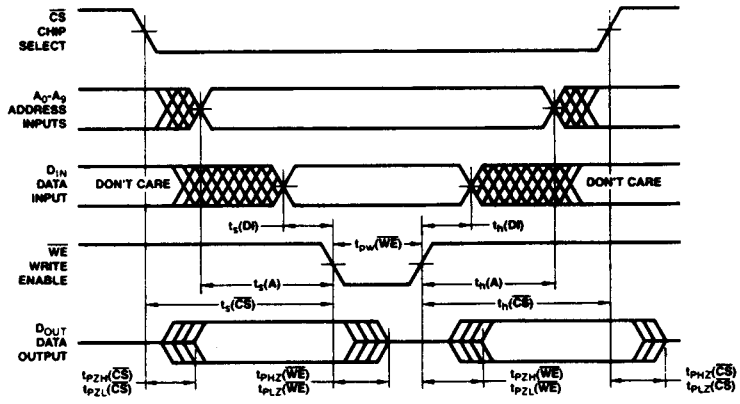
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93415/25 C devices Min.	Am93415/25 C devices Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output (Address Access Time)		45	ns
2	$t_{PHL}(A)$				
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data		35	ns
4	$t_{PZL}(\overline{CS})$				
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		40	ns
6	$t_{PZL}(\overline{WE})$				
7	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	10		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	5		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Initiation of Write)	5		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	5		ns
11	$t_s(\overline{CS})$	Setup Time Chip Select (Prior to Initiation of Write)	5		ns
12	$t_h(\overline{CS})$	Hold Time Chip Select (After Termination of Write)	5		ns
13	$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	30		ns
14	$t_{PHZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (Hi-Z)		35	ns
15	$t_{PLZ}(\overline{CS})$				
16	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		35	
17	$t_{PLZ}(\overline{WE})$				

Notes:
1. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
2. For open-collector devices (Am93415 series), all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CE}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.
3. For three-state output devices (Am93425 series), $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{HZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

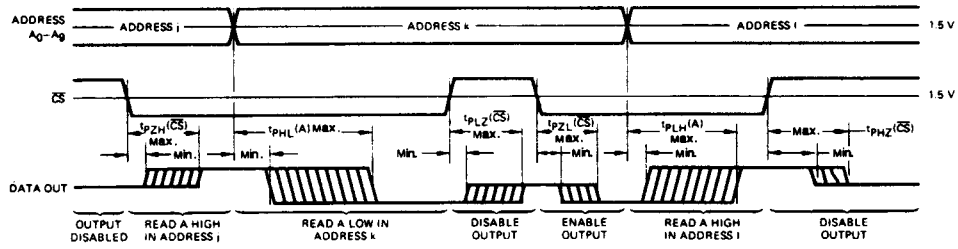
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF001150

Write Mode



WF001141

Switching delays from address and chip select inputs to the data output. For the Am93425SA/A/425, disabled output is OFF, represented by a single center line. For the Am93415SA/A/415, a disabled output is HIGH.

Read Mode

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	$t_{PLH}(A)$	9, 10, 11	10	$t_h(DI)$	9, 10, 11
2	$t_{PHL}(A)$	9, 10, 11	11	$t_s(\overline{CS})$	9, 10, 11
3	$t_{PZH}(\overline{CS})$	9, 10, 11	12	$t_h(\overline{CS})$	9, 10, 11
4	$t_{PZL}(\overline{CS})$	9, 10, 11	13	$t_{pw}(\overline{WE})$	9, 10, 11
5	$t_{PZH}(\overline{WE})$	9, 10, 11	14	$t_{PHZ}(\overline{CS})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$	9, 10, 11	15	$t_{PLZ}(\overline{CS})$	9, 10, 11
7	$t_s(A)$	9, 10, 11	16	$t_{PLZ}(\overline{WE})$	9, 10, 11
8	$t_h(A)$	9, 10, 11	17	$t_{PHZ}(\overline{WE})$	9, 10, 11
9	$t_s(DI)$	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.