- **Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)**
- **P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)**

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74LS374 . . . DW, N, OR NS PACKAGE
SN74LS374 . . . DB, DW, N, OR NS PACKAGE
SN74S373 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{OC}$	1		20	V_{CC}
1Q	2		19	8Q
1D	3		18	8D
2D	4		17	7D
2Q	5		16	7Q
3Q	6		15	6Q
3D	7		14	6D
4D	8		13	5D
4Q	9		12	5Q
GND	10		11	C†

† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . FK PACKAGE
(TOP VIEW)

† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
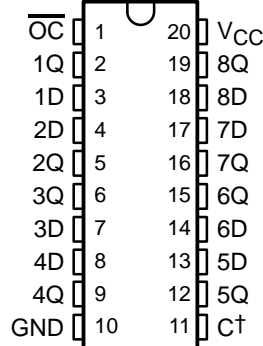
The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.
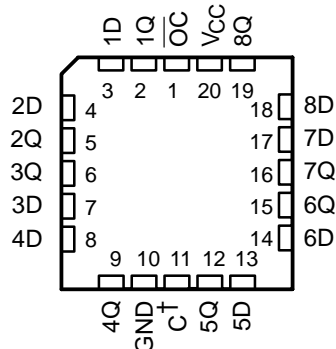
$\overline{OC}$ does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

ORDERING INFORMATION

T$_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS373N	SN74LS373N
		Tube	SN74LS374N	SN74LS374N
		Tube	SN74S373N	SN74S373N
		Tube	SN74S374N	SN74S374N
	SOIC – DW	Tube	SN74LS373DW	LS373
		Tape and reel	SN74LS373DWR	
		Tube	SN74LS374DW	LS374
		Tape and reel	SN74LS374DWR	
		Tube	SN74S373DW	S373
		Tape and reel	SN74S373DWR	
		Tube	SN74S374DW	S374
		Tape and reel	SN74S374DWR	
	SOP – NS	Tape and reel	SN74LS373NSR	74LS373
		Tape and reel	SN74LS374NSR	74LS374
		Tape and reel	SN74S374NSR	74S374
	SSOP – DB	Tape and reel	SN74LS374DBR	LS374A
−55°C to 125°C	CDIP – J	Tube	SN54LS373J	SN54LS373J
		Tube	SNJ54LS373J	SNJ54LS373J
		Tube	SN54LS374J	SN54LS374J
		Tube	SNJ54LS374J	SNJ54LS374J
		Tube	SN54S373J	SN54S373J
		Tube	SNJ54S373J	SNJ54S373J
		Tube	SN54S374J	SN54S374J
		Tube	SNJ54S374J	SNJ54S374J
	CFP – W	Tube	SNJ54LS373W	SNJ54LS373W
		Tube	SNJ54LS374W	SNJ54LS374W
		Tube	SNJ54S374W	SNJ54S374W
	LCCC – FK	Tube	SNJ54LS373FK	SNJ54LS373FK
		Tube	SNJ54LS374FK	SNJ54LS374FK
		Tube	SNJ54S373FK	SNJ54S373FK
		Tube	SNJ54S374FK	SNJ54S374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

'LS373, 'S373
(each latch)

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'LS374, 'S374
(each latch)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic diagrams (positive logic)

'LS373, 'S373
Transparent Latches

⎍ for 'S373 Only

'LS374, 'S374
Positive-Edge-Triggered Flip-Flops

⎍ for 'S374 Only

Pin numbers shown are for DB, DW, J, N, NS, and W packages.

schematic of inputs and outputs

'LS373

| EQUIVALENT OF DATA INPUTS | EQUIVALENT OF ENABLE- AND OUTPUT-CONTROL INPUTS | TYPICAL OF ALL OUTPUTS |

'LS374

| EQUIVALENT OF DATA INPUTS | EQUIVALENT OF CLOCK- AND OUTPUT-CONTROL INPUTS | TYPICAL OF ALL OUTPUTS |

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)† ('LS devices)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V

Input voltage, V_I . . . . 7 V

Off-state output voltage . . . . 5.5 V

Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 70°C/W

DW package . . . . 58°C/W

N package . . . . 69°C/W

NS package . . . . 60°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CLK high	15			15			ns
		CLK low	15			15			
t_{su}	Data setup time	'LS373	5↓			5↓			ns
		'LS374	20↑			20↑			
t_h	Data hold time	'LS373	20↓			20↓			ns
		'LS374‡	5↑			0↑			
T_A	Operating free-air temperature		−55		125	0		70	°C

‡ The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = –18 mA				–1.5			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				–20			–20	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				–0.4			–0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		–30		–130	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{max}			R_L = 667 Ω, C_L = 45 pF, See Note 3				35	50		MHz
t_{PLH}	Data	Any Q	R_L = 667 Ω, C_L = 45 pF, See Note 3		12	18				ns
t_{PHL}					12	18				
t_{PLH}	C or CLK	Any Q	R_L = 667 Ω, C_L = 45 pF, See Note 3		20	30		15	28	ns
t_{PHL}					18	30		19	28	
t_{PZH}	$\overline{OC}$	Any Q	R_L = 667 Ω, C_L = 45 pF, See Note 3		15	28		20	26	ns
t_{PZL}					25	36		21	28	
t_{PHZ}	$\overline{OC}$	Any Q	R_L = 667 Ω, C_L = 5 pF		15	25		15	28	ns
t_{PLZ}					12	20		12	20	

NOTE 3:   Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

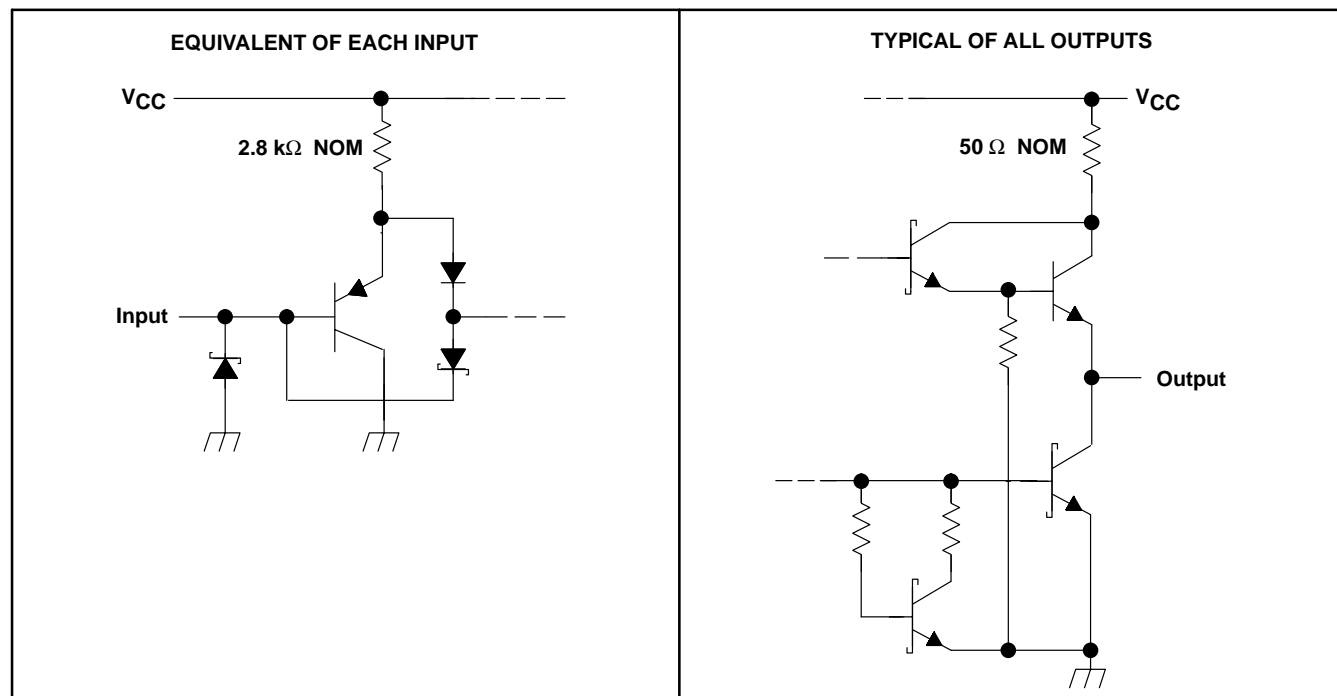## schematic of inputs and outputs

'S373 and 'S374   'S373 and 'S374

EQUIVALENT OF EACH INPUT

V$_{CC}$

2.8 kΩ NOM

Input

TYPICAL OF ALL OUTPUTS

V$_{CC}$

50 Ω NOM

Output

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†] ('S devices)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage, V_I .... 5.5 V
Off-state output voltage .... 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DW package .... 58°C/W
                                                    N package .... 69°C/W
                                                    NS package .... 60°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. Voltage values are with respect to network ground terminal.
         2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			SN54S'			**SN74S'**			**UNIT**
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−2			−6.5	mA
t_w	Pulse duration, clock/enable	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Data setup time	'S373	0↓			0↓			ns
		'S374	5↑			5↑			
t_h	Data hold time	'S373	10↓			10↓			ns
		'S374	2↑			2↑			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

PARAMETER		TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT
V_{IH}						2			V
V_{IL}								0.8	V
V_{IK}		V_{CC} = MIN,	I_I = –18 mA					–1.2	V
V_{OH}	SN54S'	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4	3.4		V
	SN74S'					2.4	3.1		
V_{OL}		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 20 mA			0.5	V
I_{OZH}		V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.4 V				50	µA
I_{OZL}		V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.5 V				–50	µA
I_I		V_{CC} = MAX,	V_I = 5.5 V					1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V					50	µA
I_{IL}		V_{CC} = MAX,	V_I = 0.5 V					–250	µA
I_{OS}§		V_{CC} = MAX				–40		–100	mA
I_{CC}		V_{CC} = MAX	'S373	Outputs high				160	mA
				Outputs low				160	
				Outputs disabled				190	
			'S374	Outputs high				110	
				Outputs low				140	
				Outputs disabled				160	
				CLK and $\overline{OC}$ at 4 V, D inputs at 0 V				180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			R_L = 280 Ω, C_L = 15 pF, See Note 3				75	100		MHz
t_{PLH}	Data	Any Q	R_L = 280 Ω, C_L = 15 pF, See Note 3		7	12				ns
t_{PHL}					7	12				
t_{PLH}	C or CLK	Any Q	R_L = 280 Ω, C_L = 15 pF, See Note 3		7	14		8	15	ns
t_{PHL}					12	18		11	17	
t_{PZH}	$\overline{OC}$	Any Q	R_L = 280 Ω, C_L = 15 pF, See Note 3		8	15		8	15	ns
t_{PZL}					11	18		11	18	
t_{PHZ}	$\overline{OC}$	Any Q	R_L = 280 Ω, C_L = 5 pF		6	9		5	9	ns
t_{PLZ}					8	12		7	12	

NOTE 3. Maximum clock frequency is tested with all outputs loaded.
f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
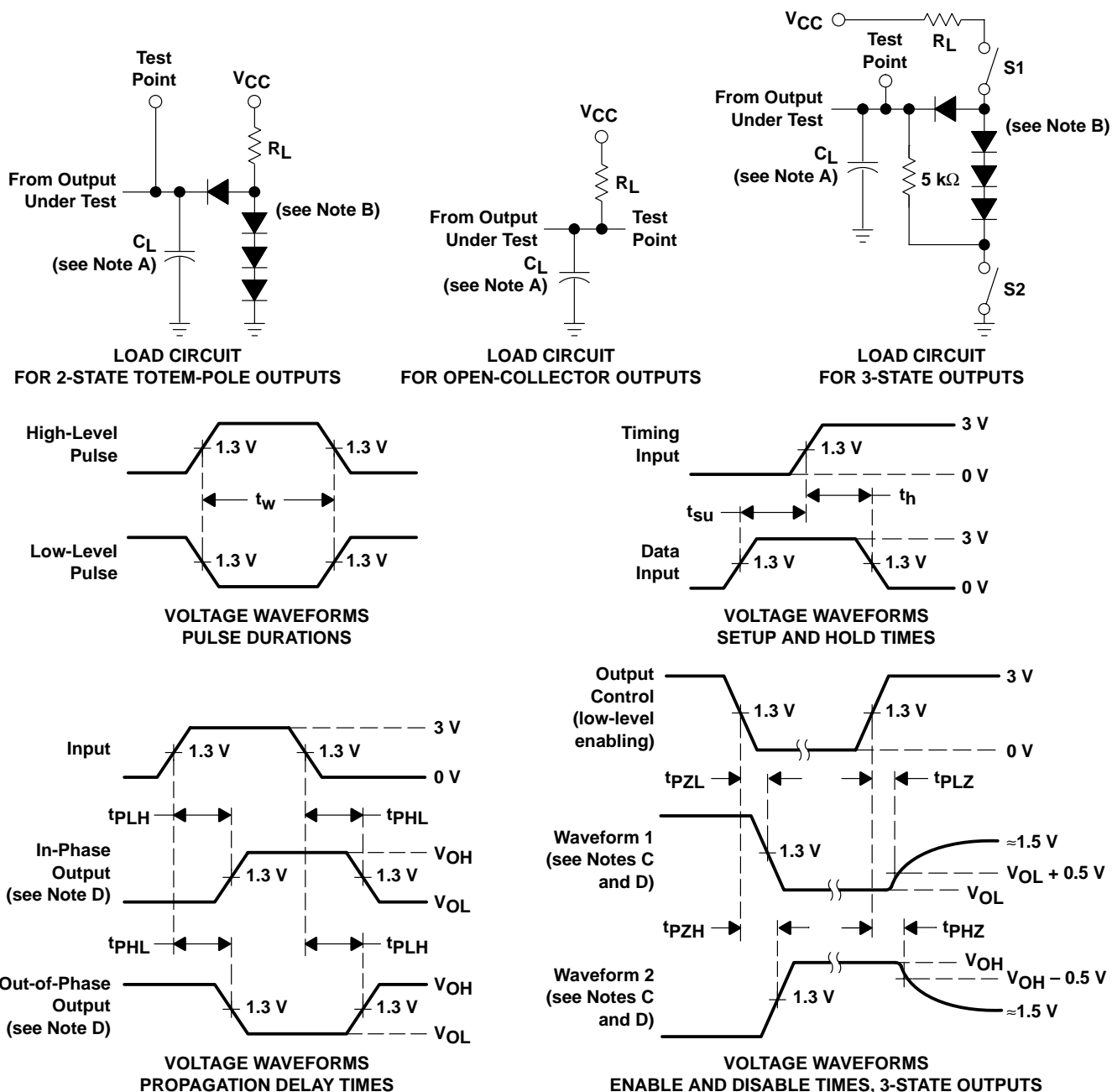t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES

LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
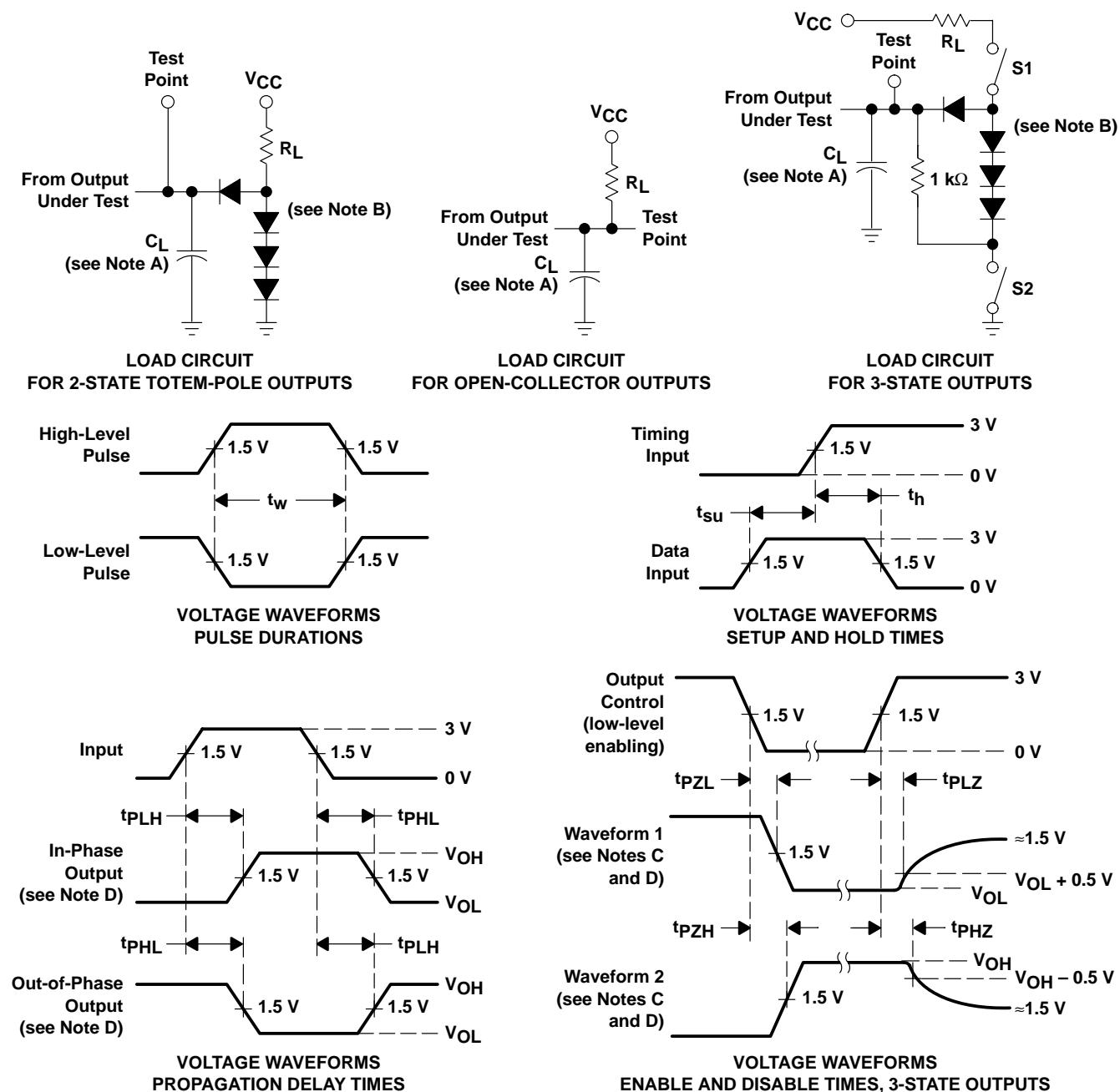**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 2.6 ns.
G. The outputs are measured one at a time with one input transition per measurement.
H. All parameters and waveforms are not applicable to all devices .

Figure 1. Load Circuits and Voltage Waveforms

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
SERIES 54S/74S DEVICES

LOAD CIRCUIT FOR 2-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATIONS

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

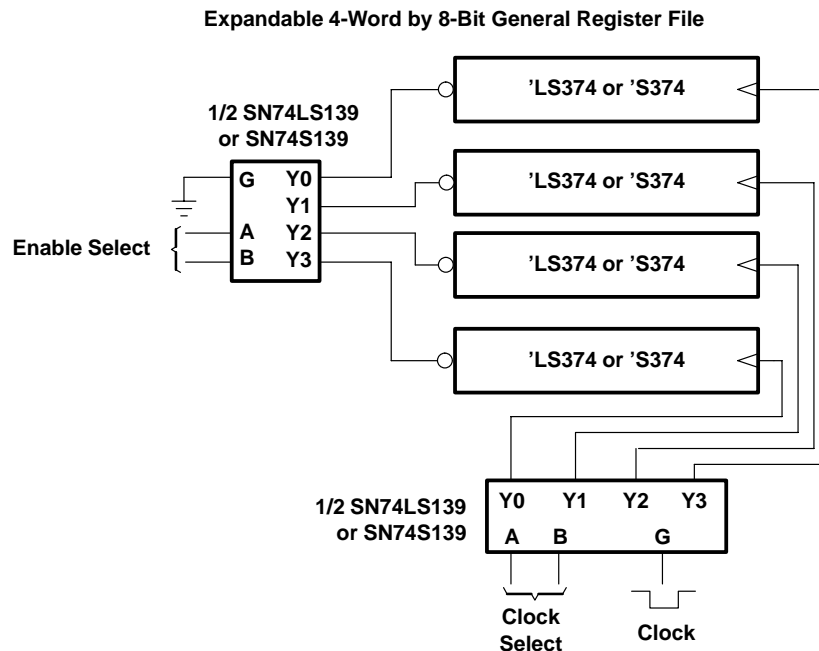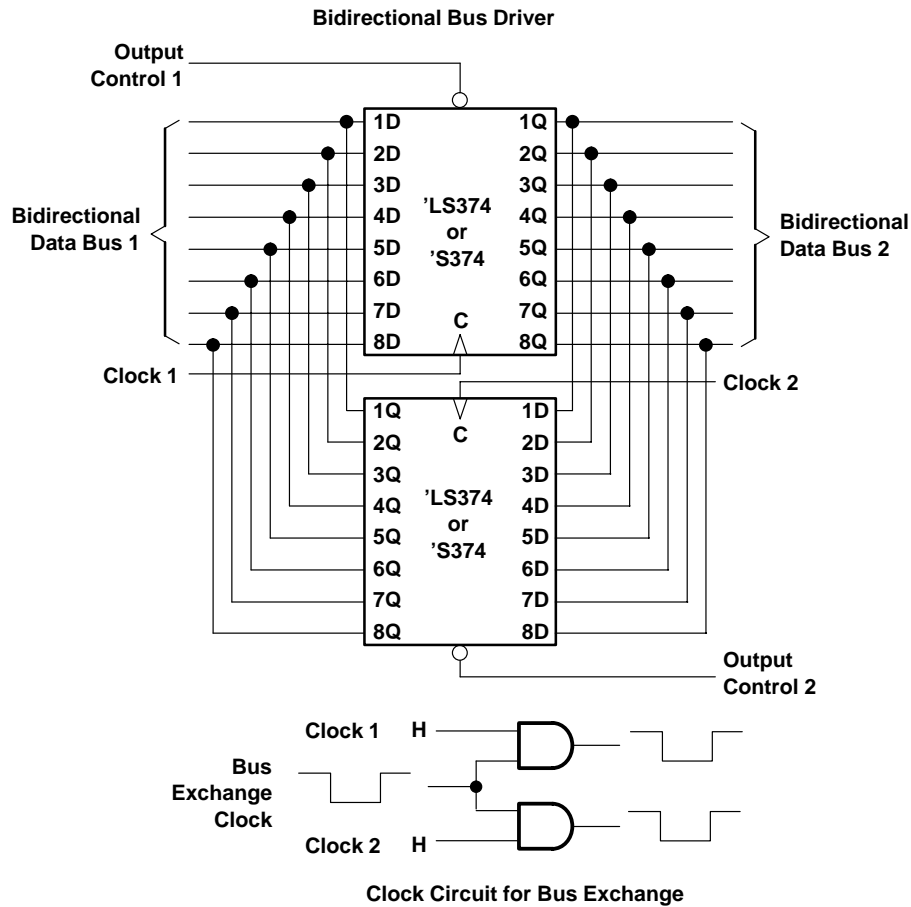**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω; t_r and t_f ≤ 7 ns for Series 54/74 devices and t_r and t_f ≤ 2.5 ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.
G. All parameters and waveforms are not applicable to all devices .

Figure 2. Load Circuits and Voltage Waveforms

TYPICAL APPLICATION DATA

Bidirectional Bus Driver

Clock Circuit for Bus Exchange

Expandable 4-Word by 8-Bit General Register File

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
78011022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78011022A SNJ54LS 374FK	Samples
7801102RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7801102RA SNJ54LS374J	Samples
7801102SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7801102SA SNJ54LS374W	Samples
JM38510/32502B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502B2A	Samples
JM38510/32502BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502BRA	Samples
JM38510/32502BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502BSA	Samples
JM38510/32502SRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502SRA	Samples
JM38510/32502SSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502SSA	Samples
JM38510/32503B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32503B2A	Samples
JM38510/32503BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32503BRA	Samples
JM38510/32503BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32503BSA	Samples
M38510/32502B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502B2A	Samples
M38510/32502BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502BRA	Samples
M38510/32502BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502BSA	Samples
M38510/32502SRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502SRA	Samples
M38510/32502SSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32502SSA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/32503B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32503B2A	Samples
M38510/32503BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32503BRA	Samples
M38510/32503BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 32503BSA	Samples
SN54LS373J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS373J	Samples
SN54LS374J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS374J	Samples
SN54S373J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S373J	Samples
SN54S374J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S374J	Samples
SN74LS373DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS373	Samples
SN74LS373N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS373N	Samples
SN74LS373NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS373N	Samples
SN74LS373NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS373	Samples
SN74LS374DB	LIFEBUY	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		LS374A	
SN74LS374DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374A	Samples
SN74LS374DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS374	Samples
SN74LS374N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS374N	Samples
SN74LS374NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS374N	Samples
SN74LS374NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS374	Samples
SN74S373N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S373N	Samples
SN74S374N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S374N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS373FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 373FK	Samples
SNJ54LS373J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS373J	Samples
SNJ54LS373W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS373W	Samples
SNJ54LS374FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78011022A SNJ54LS 374FK	Samples
SNJ54LS374J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7801102RA SNJ54LS374J	Samples
SNJ54LS374W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7801102SA SNJ54LS374W	Samples
SNJ54S373FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S 373FK	Samples
SNJ54S373J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S373J	Samples
SNJ54S374FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S 374FK	Samples
SNJ54S374J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S374J	Samples
SNJ54S374W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S374W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS373, SN54LS373-SP, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 :

- Catalog : SN74LS373, SN54LS373, SN74LS374, SN74S373, SN74S374

- Military : SN54LS373, SN54LS374, SN54S373, SN54S374

- Space : SN54LS373-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

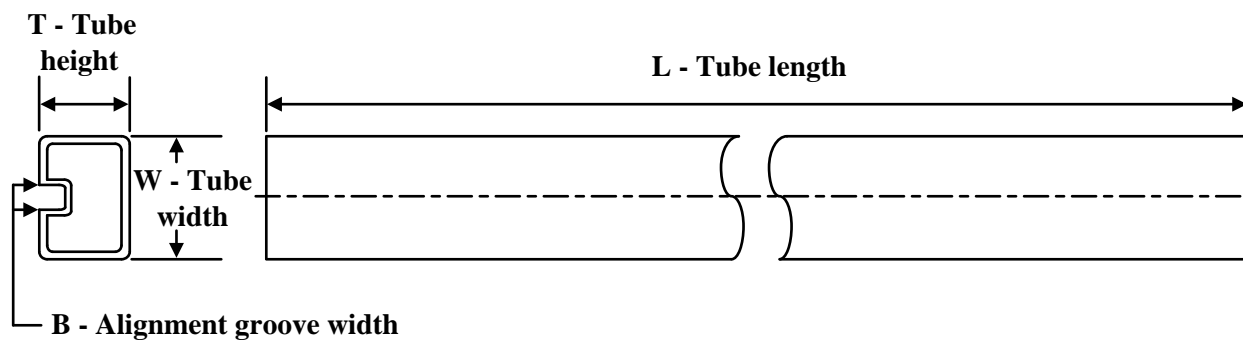| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS373NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS374NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS
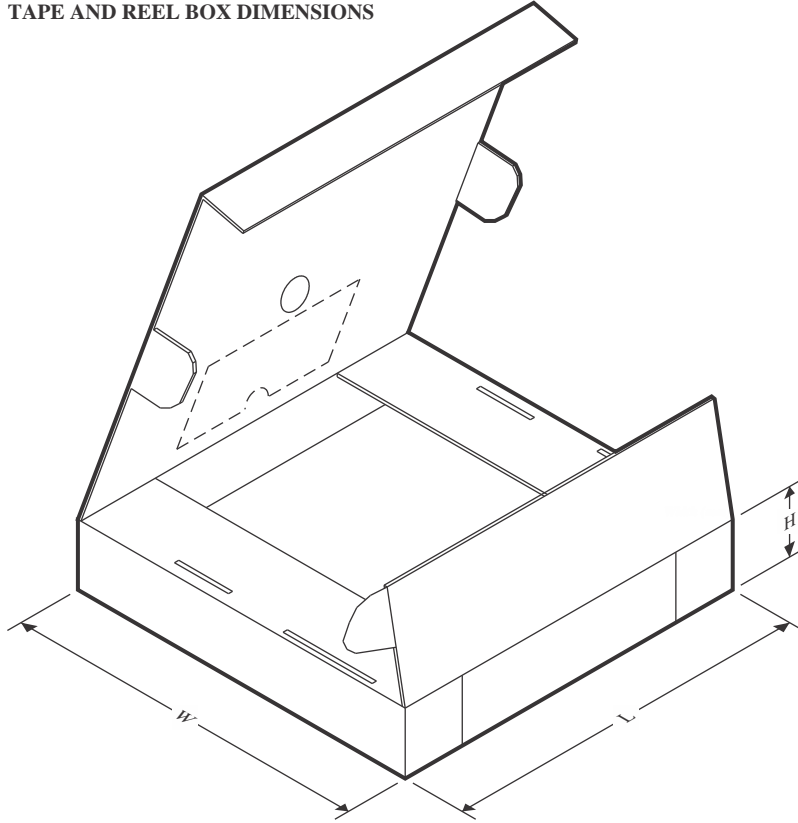
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS374DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LS374DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS374NSR	SO	NS	20	2000	356.0	356.0	41.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
78011022A	FK	LCCC	20	1	506.98	12.06	2030	NA
7801102SA	W	CFP	20	1	506.98	26.16	6220	NA
JM38510/32502B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/32502BSA	W	CFP	20	1	506.98	26.16	6220	NA
JM38510/32502SSA	W	CFP	20	1	506.98	26.16	6220	NA
JM38510/32503B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/32503BSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/32502B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/32502BSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/32502SSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/32503B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/32503BSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74LS373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS373NE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS374DB	DB	SSOP	20	70	530	10.5	4000	4.1
SN74LS374N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS374NE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74S373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74S374N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS373FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LS373W	W	CFP	20	1	506.98	26.16	6220	NA
SNJ54LS374FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LS374W	W	CFP	20	1	506.98	26.16	6220	NA
SNJ54S373FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54S374FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54S374W	W	CFP	20	1	506.98	26.16	6220	NA

8.2
7.4 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

7.5
6.9
NOTE 3

2X

5.85

10

11

20X 0.38
0.22

B

5.6
5.0
NOTE 4

$\oplus$ 0.1 Ⓜ C A B

C

0.1 C

SEATING
PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95
0.55

2 MAX

0.05 MIN

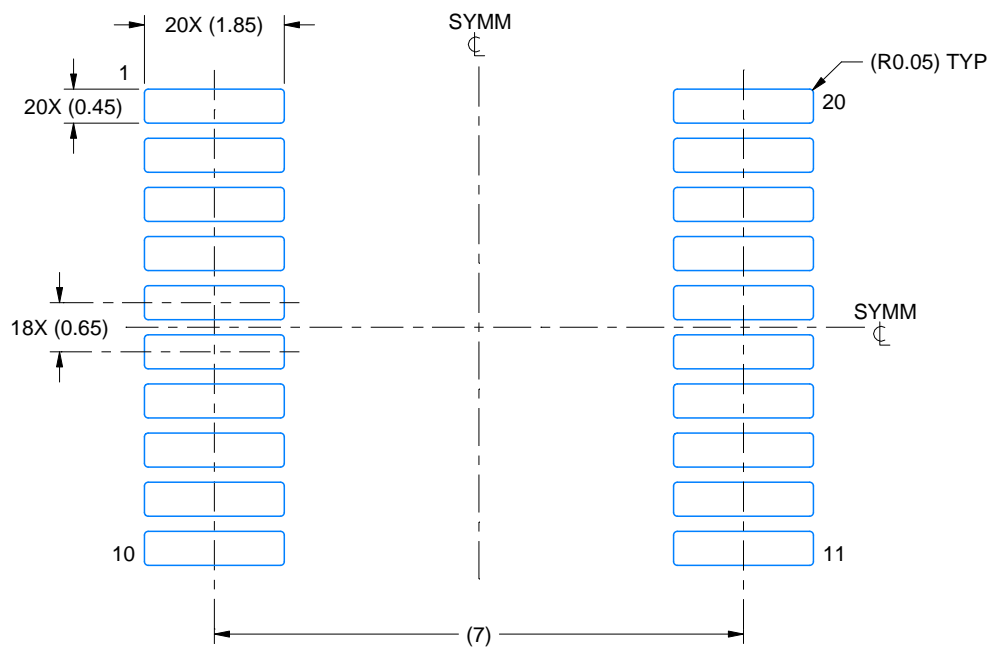DETAIL A
TYPICAL
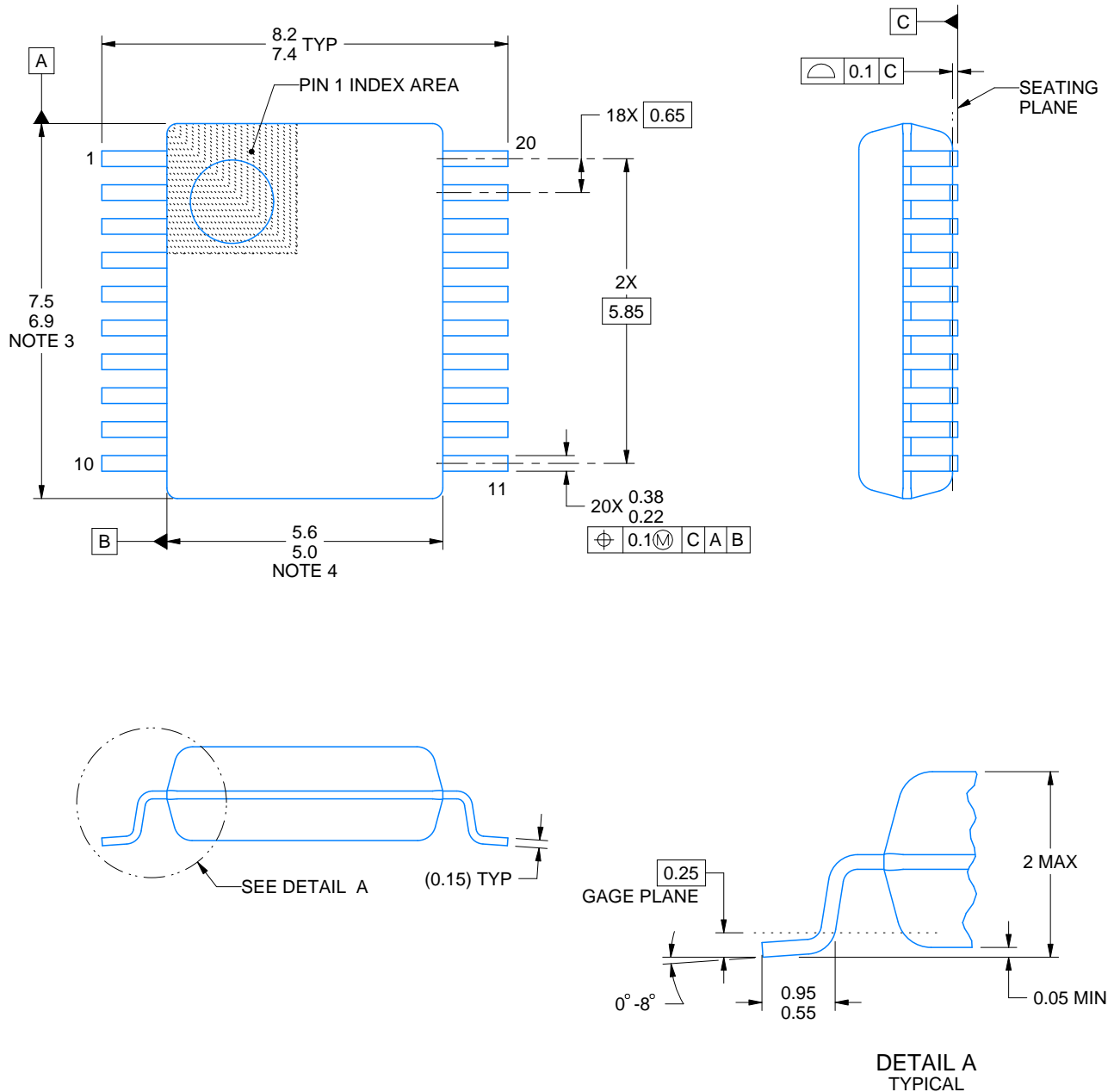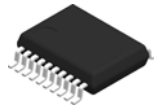
4214851/B   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

TEXAS
INSTRUMENTS
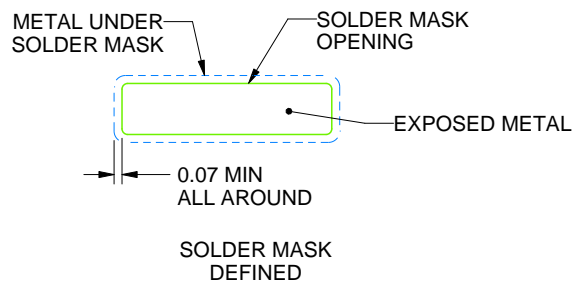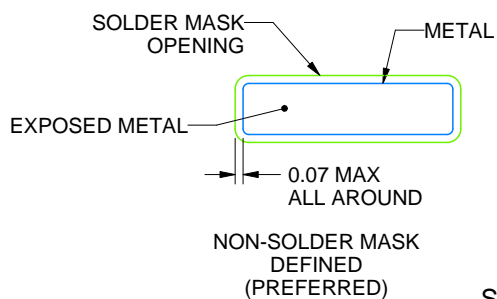www.ti.com

20X (1.85)

1

20X (0.45)

18X (0.65)

SYMM

(R0.05) TYP

20

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

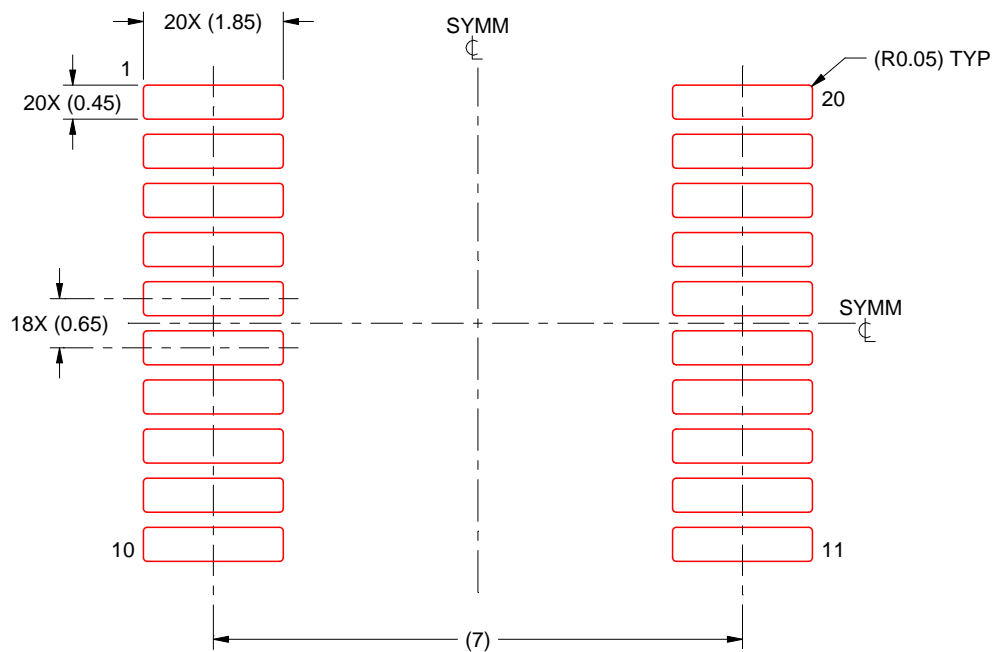**SOLDER MASK DETAILS**

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.85)

SYMM

(R0.05) TYP

1

20

20X (0.45)

18X (0.65)

SYMM

10

11

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

DIM PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R−GDIP−T∗∗)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS ∗∗	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
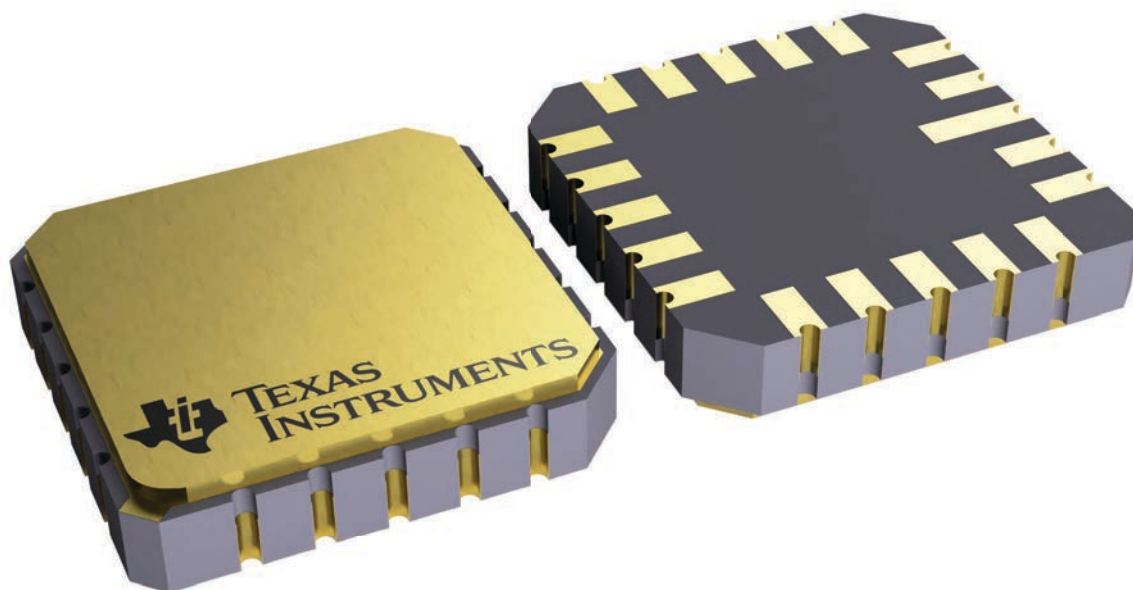   E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

FK 20

8.89 x 8.89, 1.27 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

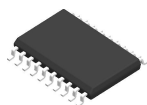4229370VA\

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION /C\	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
    /C\   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
    /D\   The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

18X [1.27]

20

13.0
12.6
NOTE 3

2X
[11.43]

10

11

B

7.6
7.4
NOTE 4

20X 0.51 / 0.31

⊕ | 0.25Ⓜ | C | A | B

C

SEATING PLANE

⌒ | 0.1 | C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25

GAGE PLANE

0° - 8°

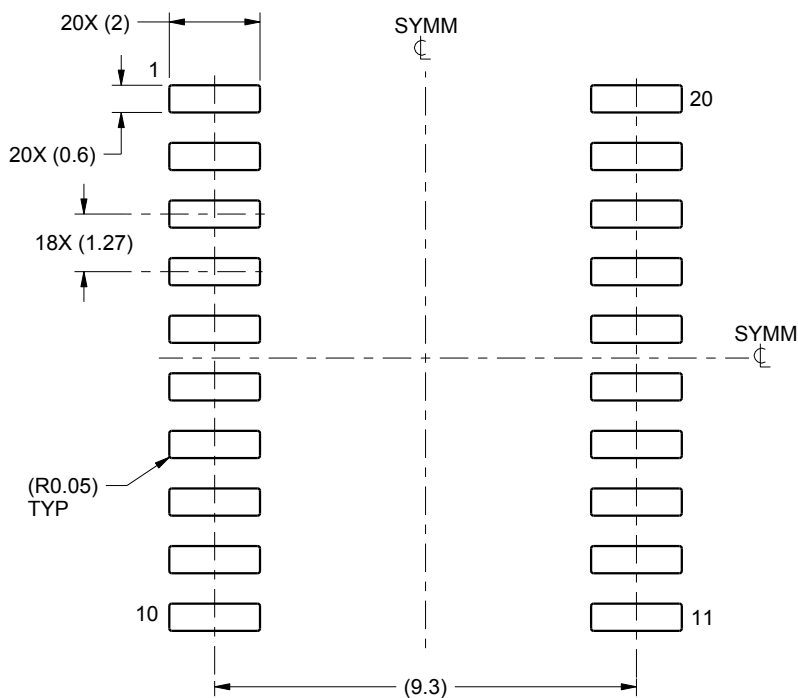1.27
0.40

0.3
0.1

DETAIL A
TYPICAL
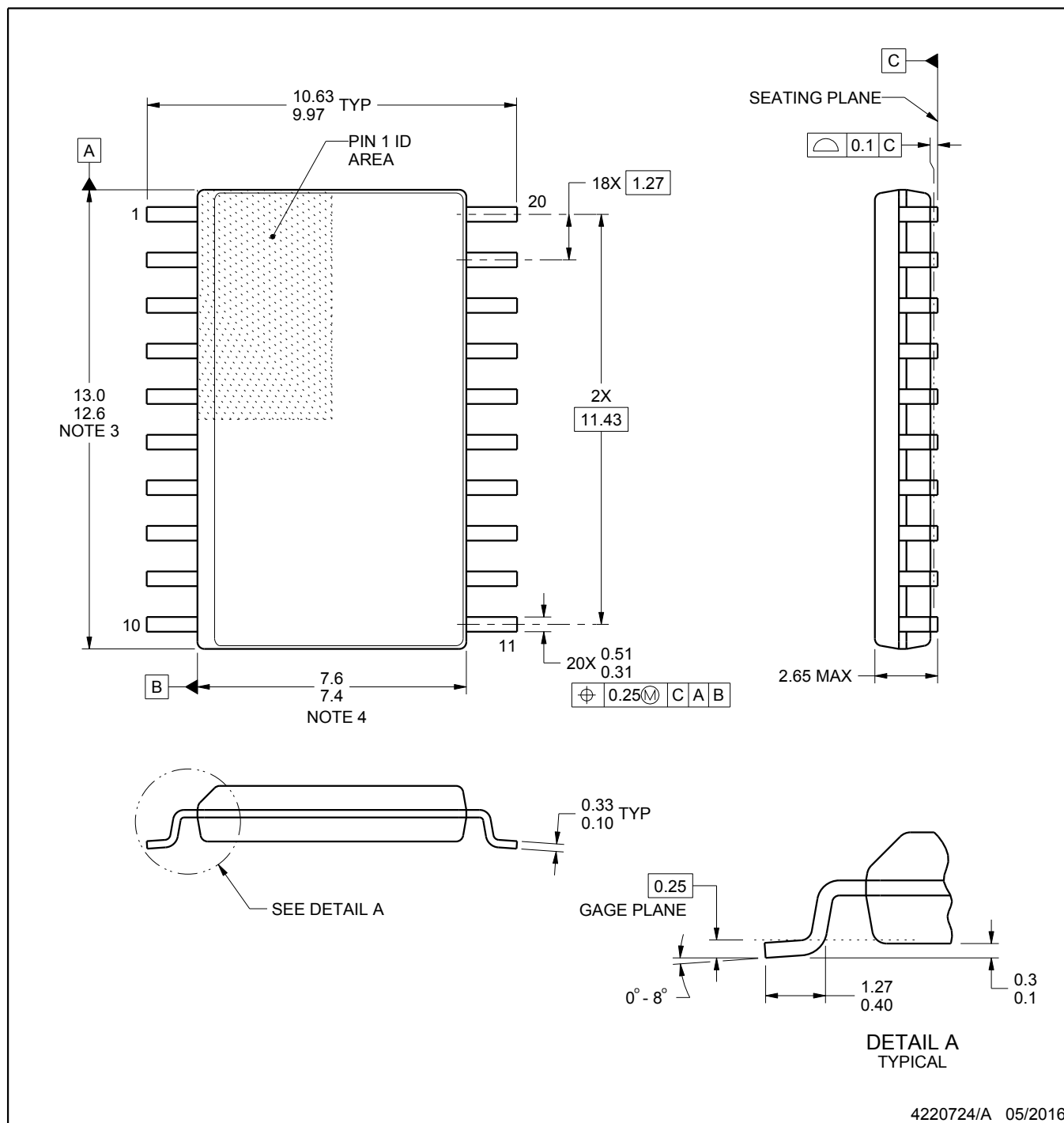
4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
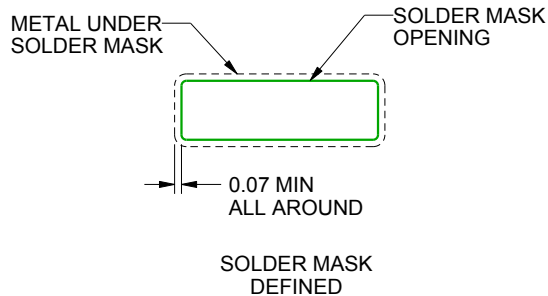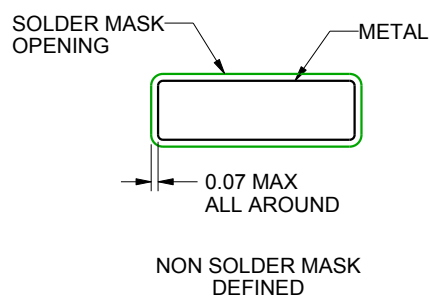5. Reference JEDEC registration MS-013.

20X (2)

1

20X (0.6)

18X (1.27)

(R0.05)
TYP

10

SYMM

20

SYMM

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM
₵

20

SYMM
₵

10

11

(9.3)

SOLDER PASTE EXAMPLE
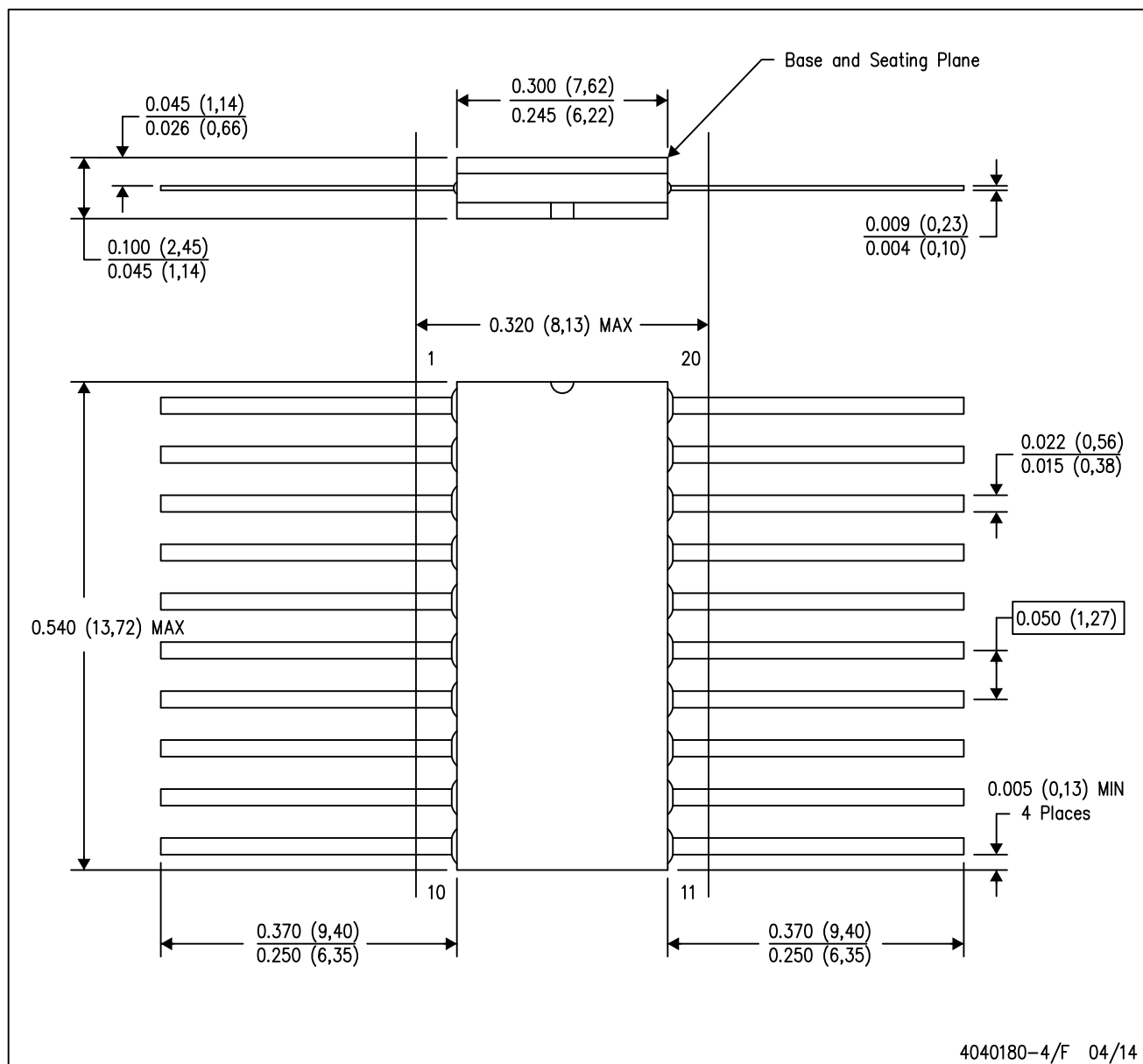BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.300 (7,62)
0.245 (6,22)

0.009 (0,23)
0.004 (0,10)

0.100 (2,45)
0.045 (1,14)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.050 (1,27)

0.540 (13,72) MAX

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil−Std 1835 GDFP2−F20

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