

# STM32 CubeMX

## 1. Description

### 1.1. Project

Project Name	MicroCAN_v3
Board Name	custom
Generated with:	STM32CubeMX 6.15.0
Date	07/28/2025

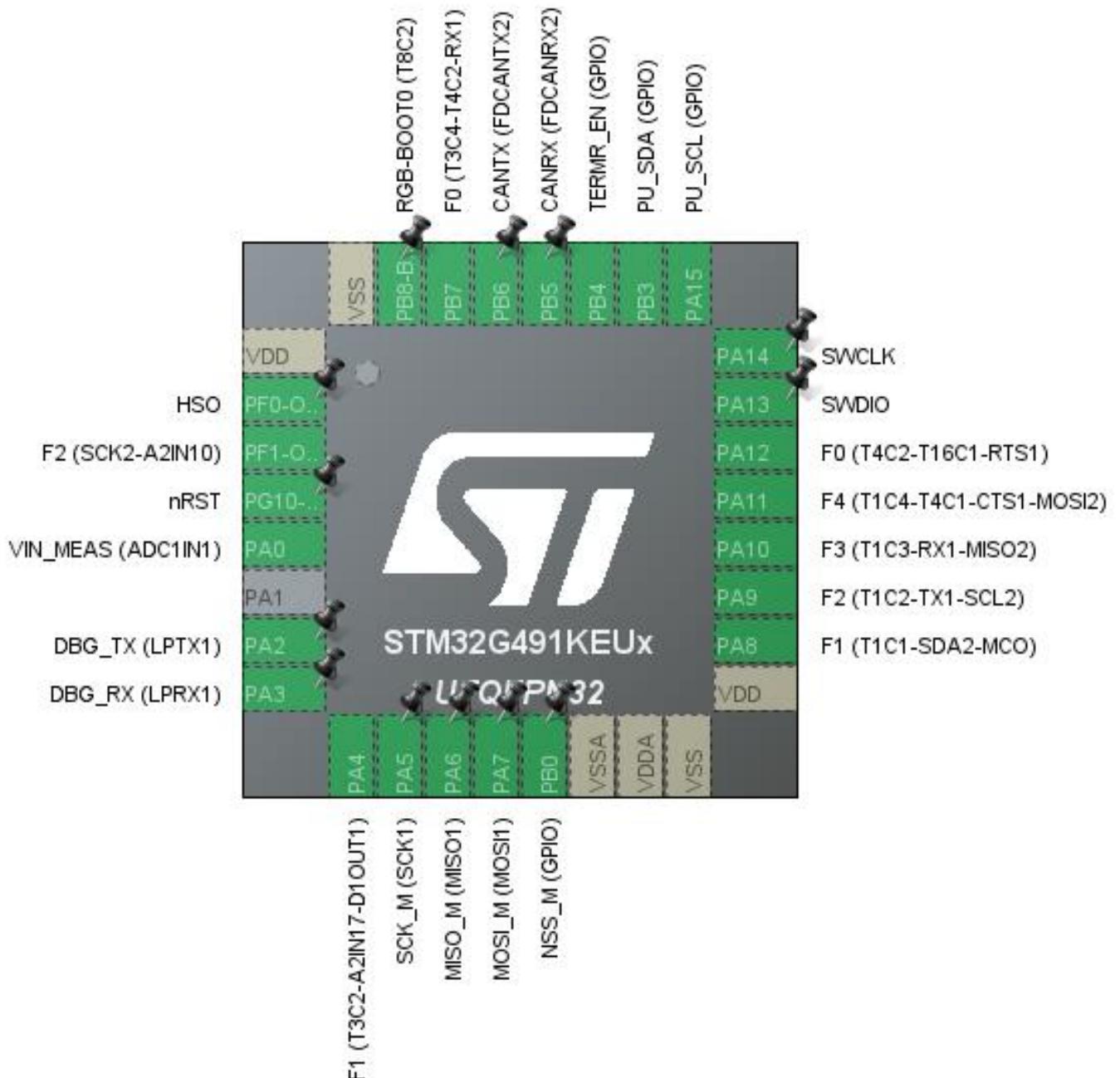
### 1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G491KEUx
MCU Package	UFQFPN32
MCU Pin number	32

### 1.3. Core(s) information

Core(s)	ARM Cortex-M4
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## **2. Pinout Configuration**

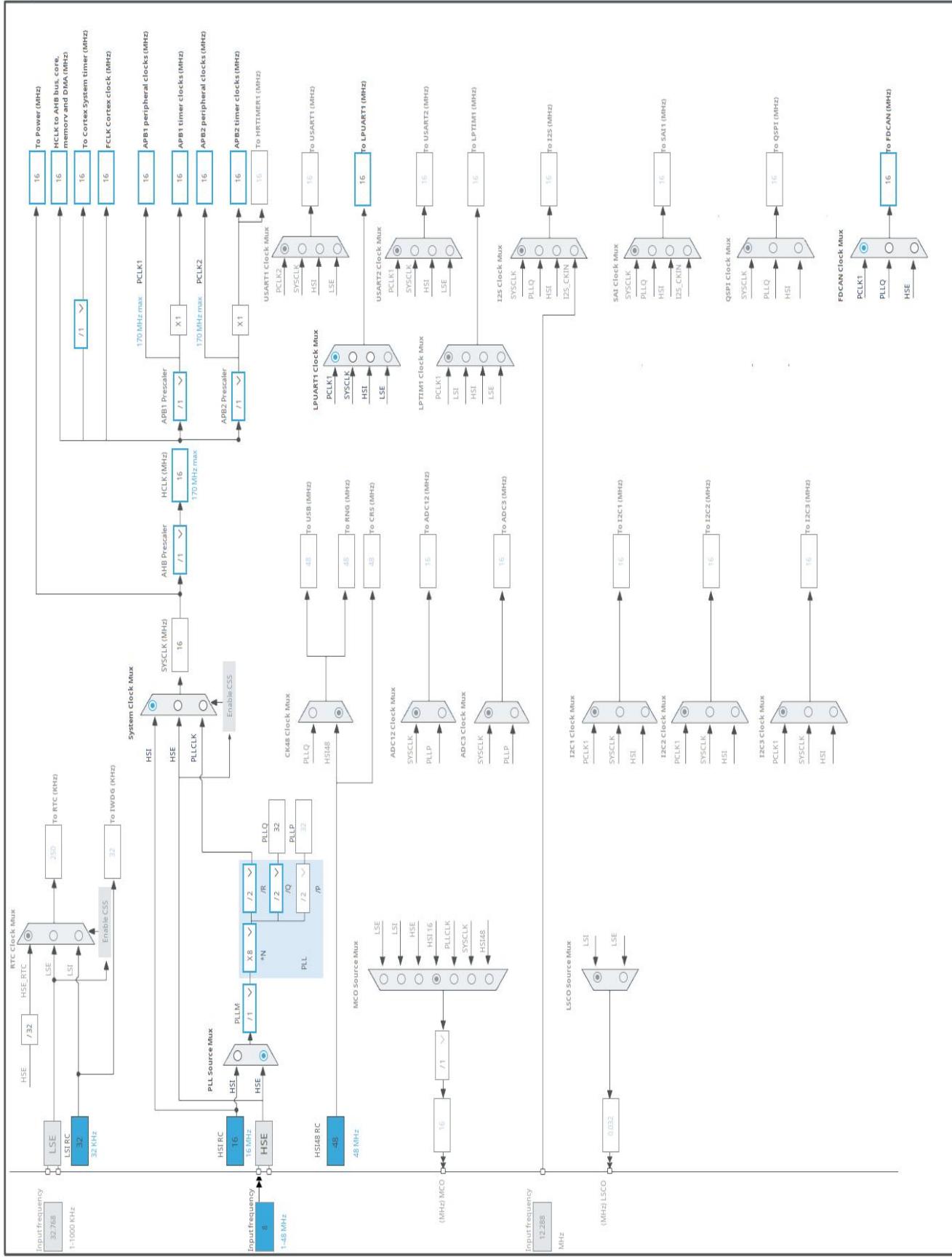


### 3. Pins Configuration

Pin Number UFQFPN32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0-OSC_IN	I/O	RCC_OSC_IN	HSO
3	PF1-OSC_OUT *	I/O	GPIO_Input	F2 (SCK2-A2IN10)
4	PG10-NRST *	I/O	GPIO_Input	nRST
5	PA0	I/O	ADC1_IN1	VIN_MEAS (ADC1IN1)
7	PA2	I/O	LPUART1_TX	DBG_TX (LPTX1)
8	PA3	I/O	LPUART1_RX	DBG_RX (LPRX1)
9	PA4 *	I/O	GPIO_Input	F1 (T3C2-A2IN17-D1OUT1)
10	PA5	I/O	SPI1_SCK	SCK_M (SCK1)
11	PA6	I/O	SPI1_MISO	MISO_M (MISO1)
12	PA7	I/O	SPI1_MOSI	MOSI_M (MOSI1)
13	PB0 *	I/O	GPIO_Output	NSS_M (GPIO)
14	VSSA	Power		
15	VDDA	Power		
16	VSS	Power		
17	VDD	Power		
18	PA8	I/O	TIM1_CH1	F1 (T1C1-SDA2-MCO)
19	PA9	I/O	TIM1_CH2	F2 (T1C2-TX1-SCL2)
20	PA10	I/O	TIM1_CH3	F3 (T1C3-RX1-MISO2)
21	PA11	I/O	TIM1_CH4	F4 (T1C4-T4C1-CTS1- MOSI2)
22	PA12 *	I/O	GPIO_Input	F0 (T4C2-T16C1-RTS1)
23	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
25	PA15 *	I/O	GPIO_Input	PU_SCL (GPIO)
26	PB3 *	I/O	GPIO_Input	PU_SDA (GPIO)
27	PB4 *	I/O	GPIO_Output	TERMR_EN (GPIO)
28	PB5	I/O	FDCAN2_RX	CANRX (FDCANRX2)
29	PB6	I/O	FDCAN2_TX	CANTX (FDCANTX2)
30	PB7 *	I/O	GPIO_Input	F0 (T3C4-T4C2-RX1)
31	PB8-BOOT0	I/O	TIM8_CH2	RGB-BOOT0 (T8C2)
32	VSS	Power		

\* The pin is affected with an I/O function

## **4. Clock Tree Configuration**



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
MCU	STM32G491KEUx
Datasheet	DS13122_Rev1

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

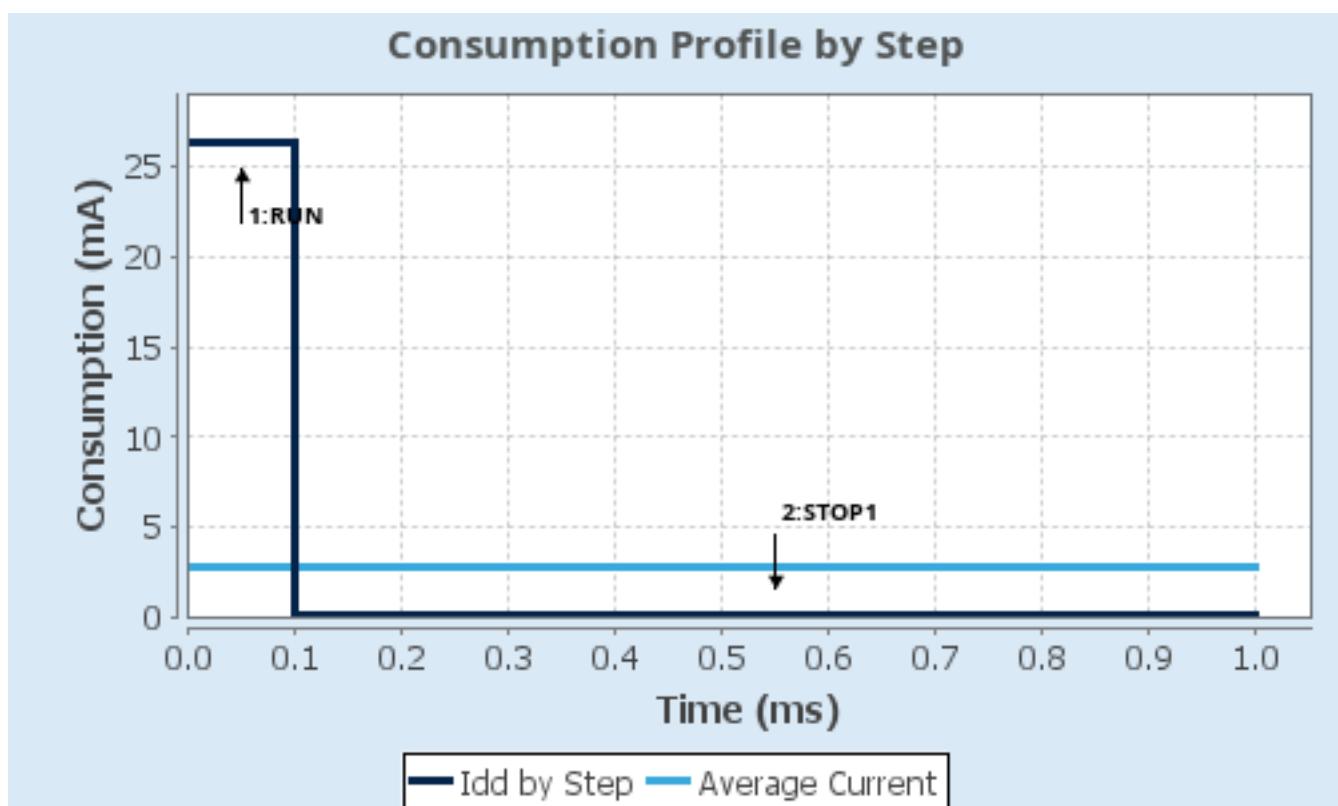
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP1
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Range1-Boost	NoRange
<b>Fetch Type</b>	FLASH/ART	NA
<b>CPU Frequency</b>	170 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	LSE LowDrive RTC
<b>Clock Source Frequency</b>	4 MHz	32.768 kHz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	26.4 mA	57.3 µA
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	213.0	0.0
<b>T<sub>a</sub> Max</b>	145.21	149.99
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	2.69 mA
Battery Life	1 month, 22 days, 3 hours	Average DMIPS	212.5 DMIPS

#### 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	MicroCAN_v3
Project Folder	/home/alex/DEV/STM32/CHIBIOS/C21DEV/MINICAN/MINICAN_V5_MICROCAN
Toolchain / IDE	EWARM V8.50
Firmware Package Name and Version	STM32Cube FW_G4 V1.6.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c./h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LPUART1_UART_Init	LPUART1
4	MX_TIM1_Init	TIM1
5	MX_FDCAN2_Init	FDCAN2
6	MX_SPI1_Init	SPI1
7	MX_ADC1_Init	ADC1
8	MX_TIM8_Init	TIM8

### 3. Peripherals and Middlewares Configuration

#### 3.1. ADC1

##### IN1: IN1 Single-ended

###### 3.1.1. Parameter Settings:

###### **ADCs\_Common\_Settings:**

Mode Independent mode

###### **ADC\_Settings:**

Clock Prescaler	Synchronous clock mode divided by 2
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
Overrun behaviour	Overrun data preserved

###### **ADC-Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	2.5 Cycles
Offset Number	No offset

###### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions Disable

###### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode false

###### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode false

###### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode false

### 3.2. FDCAN2

**mode: Activated**

#### 3.2.1. Parameter Settings:

##### **Basic Parameters:**

Clock Divider	Divide kernel clock by 1
Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Sync Jump Width	1
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Std Filters Nbr	0
Ext Filters Nbr	0
Tx Fifo Queue Mode	FIFO mode

##### **Bit Timings Parameters:**

Nominal Prescaler	16
Nominal Time Quantum	<b>1000.0 *</b>
Nominal Time Seg1	1
Nominal Time Seg2	1
Nominal Time for one Bit	<b>3000 *</b>
Nominal Baud Rate	<b>333333 *</b>

### 3.3. LPUART1

**Mode: Asynchronous**

#### 3.3.1. Parameter Settings:

##### **Basic Parameters:**

Baud Rate	209700
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### **Advanced Parameters:**

Data Direction	Receive and Transmit
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

**Advanced Features:**

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 3.4. RCC

#### High Speed Clock (HSE): BYPASS Clock Source

##### 3.4.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	64
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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**Peripherals Clock Configuration:**

Generate the peripherals clock configuration	TRUE
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### 3.5. SPI1

#### Mode: Full-Duplex Master

##### 3.5.1. Parameter Settings:

**Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>8.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

### 3.6. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

**mode: save power of non-active UCPD - deactivate Dead Battery pull-up**

### 3.7. TIM1

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

3.7.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2                          Reset (UG bit from TIMx\_EGR)

**Break And Dead Time management - BRK Configuration:**

BRK State                          Disable

BRK Polarity                          High

BRK Filter (4 bits value)                          0

BRK Sources Configuration

- Digital Input                          Disable

- COMP1                          Disable

- COMP2                          Disable

- COMP3                          Disable

- COMP4                          Disable

**Break And Dead Time management - BRK2 Configuration:**

BRK2 State                          Disable

BRK2 Polarity                          High

BRK2 Filter (4 bits value)                          0

BRK2 Sources Configuration

- Digital Input                          Disable

- COMP1                          Disable

- COMP2                          Disable

- COMP3                          Disable

- COMP4                          Disable

**Break And Dead Time management - Output Configuration:**

Automatic Output State                          Disable

Off State Selection for Run Mode (OSSR)                          Disable

Off State Selection for Idle Mode (OSSI)                          Disable

Lock Configuration                          Off

**Clear Input:**

Clear Input Source                          Disable

**PWM Generation Channel 1:**

Mode                          PWM mode 1

Pulse (16 bits value)                          0

Output compare preload                          Enable

Fast Mode                          Disable

CH Polarity                          High

CH Idle State                          Reset

**PWM Generation Channel 2:**

Mode                          PWM mode 1

Pulse (16 bits value)                          0

Output compare preload                          Enable

Fast Mode                          Disable

CH Polarity                          High

CH Idle State                          Reset

### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

### PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## 3.8. TIM8

### Channel2: PWM Generation CH2

#### 3.8.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

##### Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- COMP3	Disable

- COMP4 Disable

**Break And Dead Time management - BRK2 Configuration:**

BRK2 State Disable

BRK2 Polarity High

BRK2 Filter (4 bits value) 0

BRK2 Sources Configuration

- Digital Input Disable

- COMP1 Disable

- COMP2 Disable

- COMP3 Disable

- COMP4 Disable

**Break And Dead Time management - Output Configuration:**

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

**Clear Input:**

Clear Input Source Disable

**PWM Generation Channel 2:**

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	VIN_MEAS (ADC1IN1)
FDCAN2	PB5	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	CANRX (FDCANRX2)
	PB6	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	CANTX (FDCANTX2)
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	DBG_TX (LPTX1)
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	DBG_RX (LPRX1)
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	HSO
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SCK_M (SCK1)
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	MISO_M (MISO1)
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	MOSI_M (MOSI1)
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	F1 (T1C1-SDA2-MCO)
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	F2 (T1C2-TX1-SCL2)
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	F3 (T1C3-RX1-MISO2)
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	F4 (T1C4-T4C1-CTS1-MOSI2)
TIM8	PB8-BOOT0	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	RGB-BOOT0 (T8C2)
GPIO	PF1-OSC_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	F2 (SCK2-A2IN10)
	PG10-NRST	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	nRST
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	F1 (T3C2-A2IN17-D1OUT1)
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NSS_M (GPIO)
	PA12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	F0 (T4C2-T16C1-RTS1)
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PU_SCL (GPIO)
	PB3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PU_SDA (GPIO)
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TERMR_EN (GPIO)
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	F0 (T3C4-T4C2-RX1)

### 4.2. DMA configuration

nothing configured in DMA service

## 4.3. NVIC configuration

### 4.3.1. NVIC

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
ADC1 and ADC2 global interrupt		unused	
TIM1 break interrupt and TIM15 global interrupt		unused	
TIM1 update interrupt and TIM16 global interrupt		unused	
TIM1 trigger and commutation interrupts and TIM17 global interrupt		unused	
TIM1 capture compare interrupt		unused	
SPI1 global interrupt		unused	
TIM8 break interrupt		unused	
TIM8 update interrupt		unused	
TIM8 trigger and commutation interrupts		unused	
TIM8 capture compare interrupt		unused	
FPU global interrupt		unused	
FDCAN2 interrupt 0		unused	
FDCAN2 interrupt 1		unused	
LPUART1 global interrupt		unused	

### 4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

MicroCAN\_v3 Project  
Configuration Report

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

##### Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Utilities
DMA	ADC1 ✓	TIM1 ✓	FDCAN2 ✓				
GPIO ✓		TIM8 ✓	LPUART1 ✓				
NVIC ✓			SPI1 ✓				
RCC ✓							
SYS ✓							

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32g4_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32g4_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip</a>
System View	<a href="https://www.st.com/resource/en/svd/stm32g4_svd.zip">https://www.st.com/resource/en/svd/stm32g4_svd.zip</a>
Description	
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-usb-c-pd-solutions-presentation.pdf">https://www.st.com/resource/en/product_presentation/stm32-usb-c-pd-solutions-presentation.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32g4-series-product-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32g4-series-product-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32g4.pdf">https://www.st.com/resource/en/flyer/flstm32g4.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/fldpstfc11120.pdf">https://www.st.com/resource/en/flyer/fldpstfc11120.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>

- Application Notes [https://www.st.com/resource/en/application\\_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf)
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