1. Description

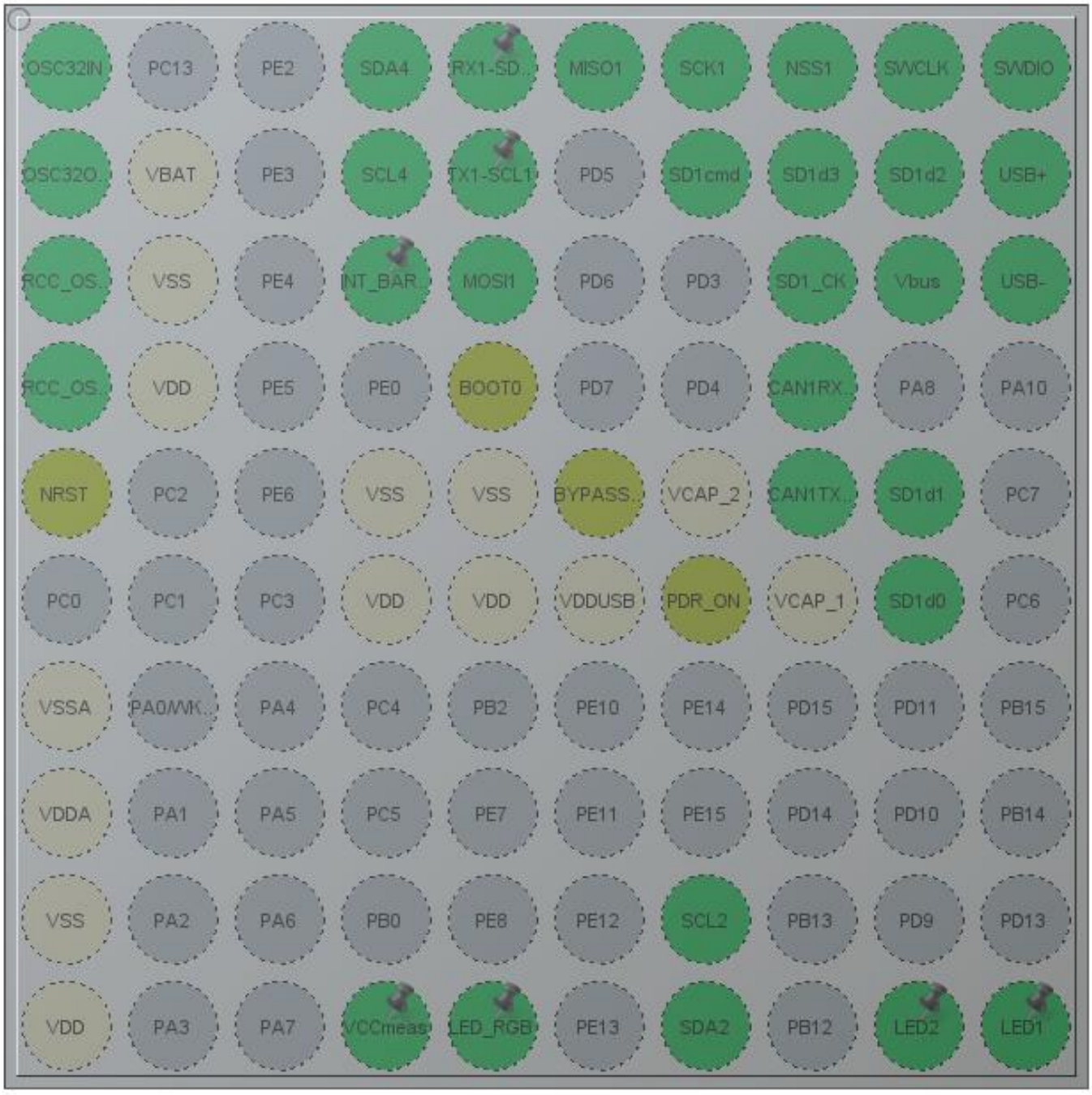
1.1. Project

Project Name	SmartProbe_v003
Board Name	custom
Generated with:	STM32CubeMX 5.6.0
Date	03/17/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F777VIHx
MCU Package	TFBGA100
MCU Pin number	100

2. Pinout Configuration



TFBGA100 (Top view)

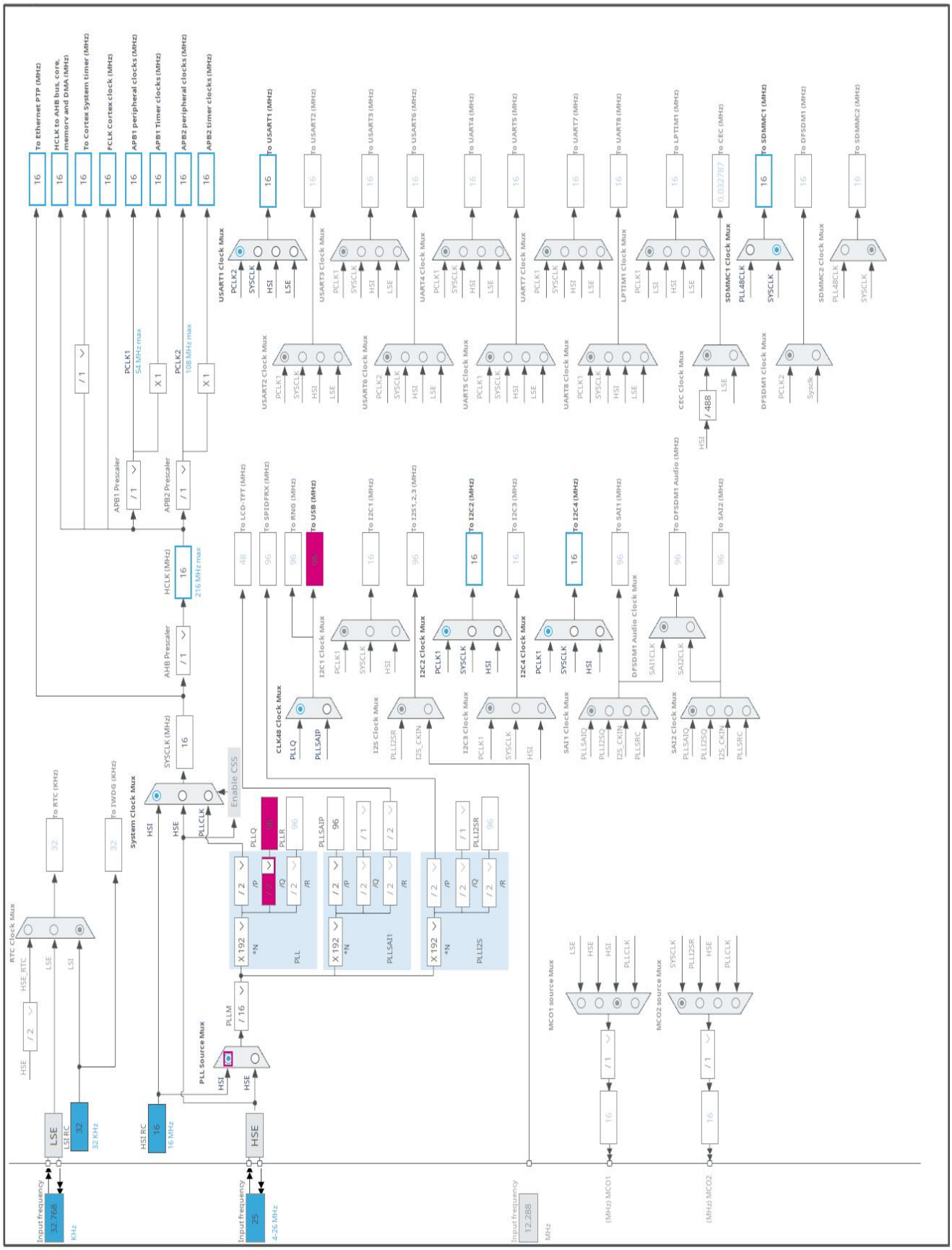
3. Pins Configuration

Pin Number TFBGA100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PC14/OSC32_IN	I/O	RCC_OSC32_IN	OSC32IN
A4	PB9	I/O	I2C4_SDA	SDA4
A5	PB7	I/O	USART1_RX	RX1-SDA1
A6	PB4	I/O	SPI1_MISO	MISO1
A7	PB3	I/O	SPI1_SCK	SCK1
A8	PA15	I/O	SPI1_NSS	NSS1
A9	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
A10	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
B1	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	OSC32OUT
B2	VBAT	Power		
B4	PB8	I/O	I2C4_SCL	SCL4
B5	PB6	I/O	USART1_TX	TX1-SCL1
B7	PD2	I/O	SDMMC1_CMD	SD1cmd
B8	PC11	I/O	SDMMC1_D3	SD1d3
B9	PC10	I/O	SDMMC1_D2	SD1d2
B10	PA12	I/O	USB_OTG_FS_DP	USB+
C1	PH0/OSC_IN	I/O	RCC_OSC_IN	
C2	VSS	Power		
C4	PE1 *	I/O	GPIO_Input	INT_BARO
C5	PB5	I/O	SPI1_MOSI	MOSI1
C8	PC12	I/O	SDMMC1_CK	SD1_CK
C9	PA9	I/O	USB_OTG_FS_VBUS	Vbus
C10	PA11	I/O	USB_OTG_FS_DM	USB-
D1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
D2	VDD	Power		
D5	BOOT0	Boot		
D8	PD0	I/O	CAN1_RX	CAN1RX-RX4
E1	NRST	Reset		
E4	VSS	Power		
E5	VSS	Power		
E6	BYPASS_REG	Reset		
E7	VCAP_2	Power		
E8	PD1	I/O	CAN1_TX	CAN1TX-TX4
E9	PC9	I/O	SDMMC1_D1	SD1d1
F4	VDD	Power		
F5	VDD	Power		

Pin Number TFBGA100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F6	VDDUSB	Power		
F7	PDR_ON	Reset		
F8	VCAP_1	Power		
F9	PC8	I/O	SDMMC1_D0	SD1d0
G1	VSSA	Power		
H1	VDDA	Power		
J1	VSS	Power		
J7	PB10	I/O	I2C2_SCL	SCL2
K1	VDD	Power		
K4	PB1	I/O	ADC1_IN9	VCCmeas
K5	PE9	I/O	TIM1_CH1	LED_RGB
K7	PB11	I/O	I2C2_SDA	SDA2
K9	PD8 *	I/O	GPIO_Output	LED2
K10	PD12 *	I/O	GPIO_Output	LED1

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	SmartProbe_v003
Project Folder	/home/alex/DEV/STM32/CHIBIOS/C19DEV/SMARTPROBE_M777/smart_probe
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F777VIHx
Datasheet	028294_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

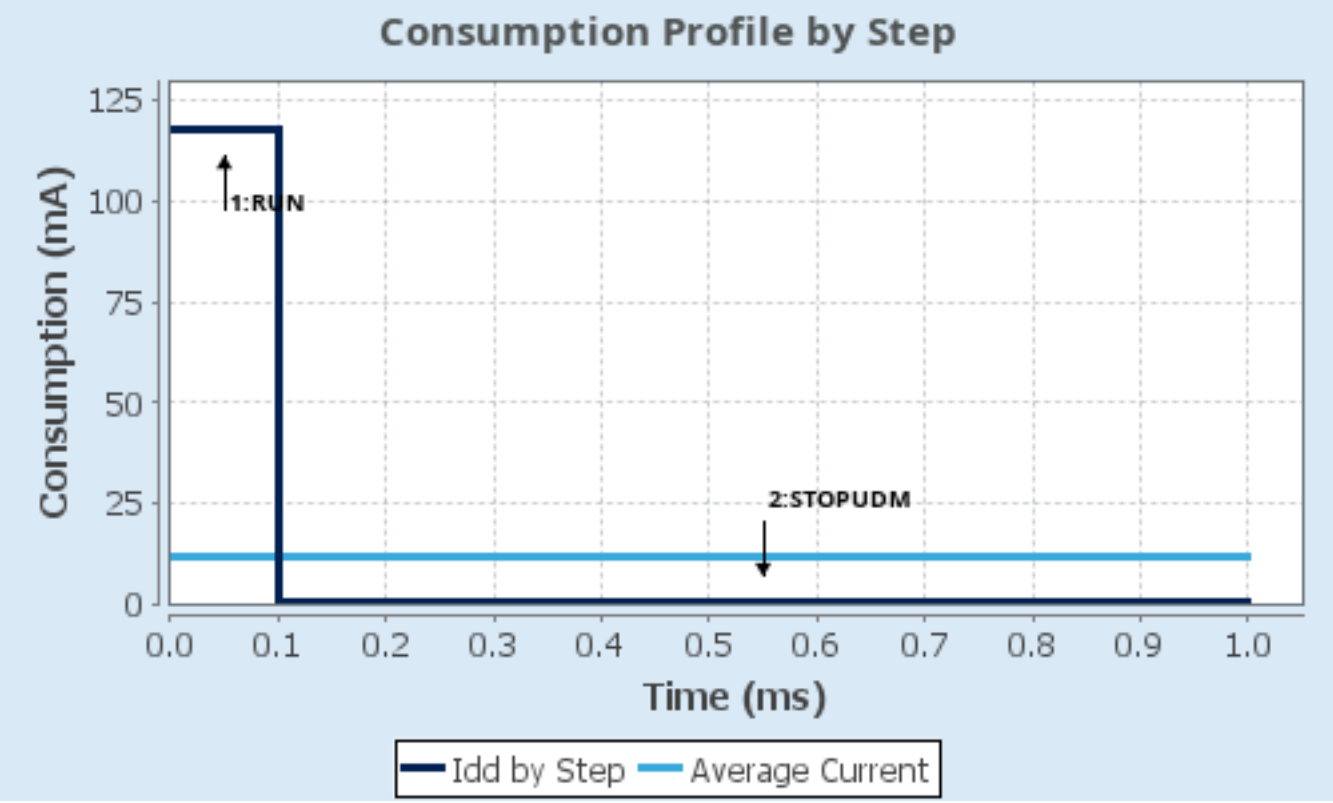
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	88.26	104.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 9
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CAN1

mode: Mode

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**1000.0 ***
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time

ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.3. GPIO

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00303D5B

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. I2C4

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00303D5B

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Disabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

7.7. SDMMC1

Mode: SD 4 bits Wide bus

7.7.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition

SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.8. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

7.9. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.10. TIM1

Channel1: PWM Generation CH1

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. USB_OTG_FS

Mode: Device_Only

mode: Activate_VBUS

7.12.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	VCCmeas
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN1RX-RX4
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN1TX-TX4
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	SCL2
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	SDA2
I2C4	PB9	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	SDA4
	PB8	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	SCL4
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	OSC32IN
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	OSC32OUT
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SD1cmd
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SD1d3
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SD1d2
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SD1_CK
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SD1d1
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SD1d0
SPI1	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MISO1
	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SCK1
	PA15	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	NSS1
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOSI1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LED_RGB
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	RX1-SDA1
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TX1-SCL1
USB_OTG_FS	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB+
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	Vbus
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB-
GPIO	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_BARO
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM1_CH1	DMA2_Stream1	Memory To Peripheral	Low

TIM1_CH1: DMA2_Stream1 DMA request Settings:

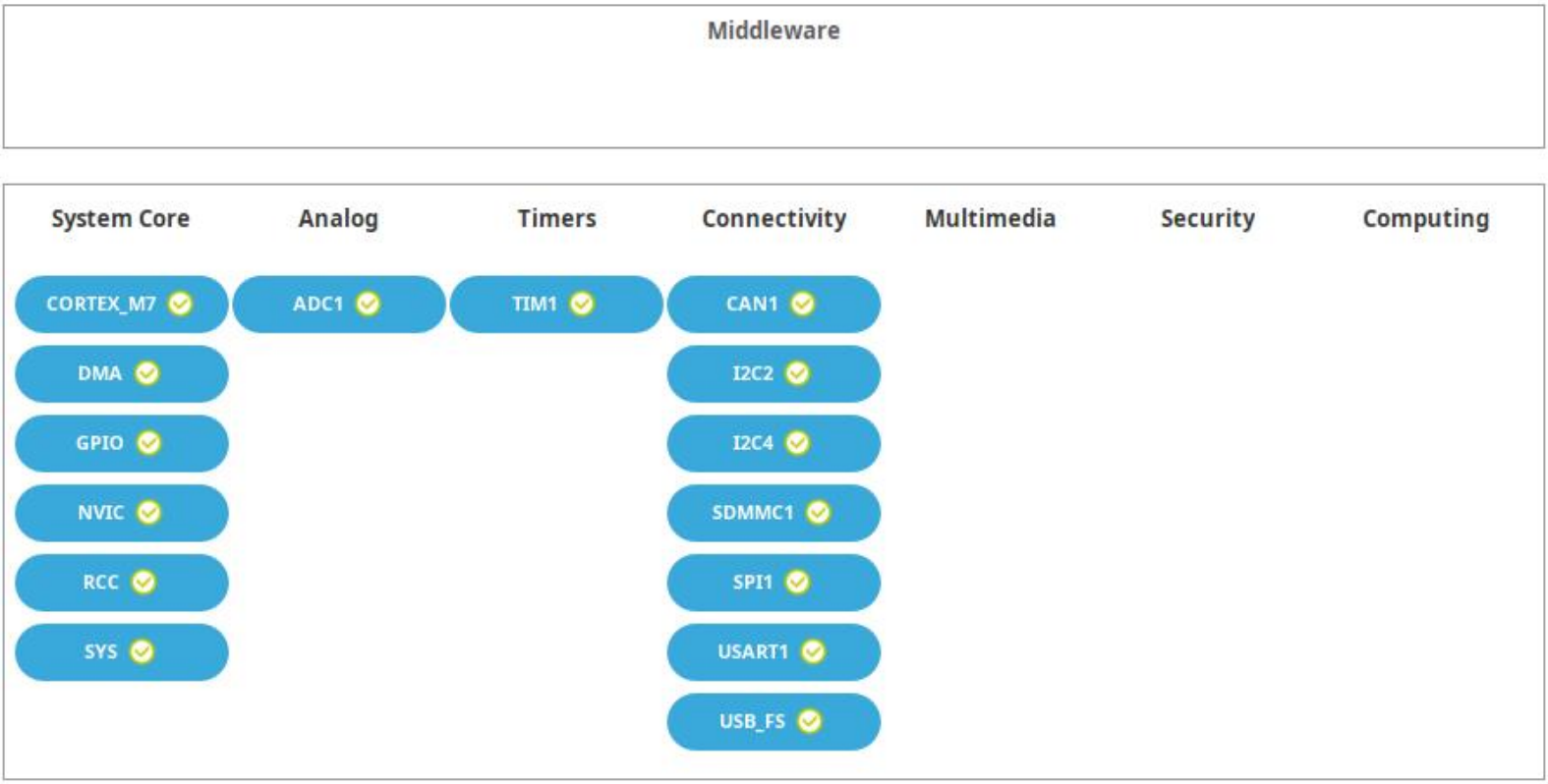
Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 stream1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX0 interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
SDMMC1 global interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report