

Core

L1 cache

L2 cache

Core

L1 cache

L2 cache

Core

L1 cache

L2 cache

Core

L1 cache

L2 cache

L3 cache

Core

L1 cache

L2 cache

Core

L1 cache

L2 cache

Core

L1 cache

L2 cache

Core

L1 cache

L2 cache