EECE571D 2025W1 Assignment 3 (100 points)

Due: December 5, 2025

A three-phase MMC is connected to a constant DC voltage source on its DC-side, and its AC-side is connected to an infinite bus through an LR filter. The MMC system has the following specifications (please pay attention to the units):

- Grid voltage: 4.16 kV (line-to-line, RMS)
- Grid frequency: 50 Hz
- DC-link voltage: 8 kV
- Rated power: 1 MVA
- Number of submodules (SMs) per arm: 4
- Arm inductance: 3 mH
- No arm resistance
- SM capacitance: 5 mF
- Modulation scheme: Level-shifted PWM
    - Carrier frequency: 1650 Hz
    - Hint: When constructing level-shifted carrier signals, the Repeating Sequence block from Simulink is useful
- Control mode: GFL PQ control

General guidelines:

- You can simulate the MMC system in either MATLAB/Simulink, PSCAD, or PLECS
- You can re-use your work from previous assignments
- Converter latency and higher-order harmonics can be neglected
- Use PI controller for all MMC controls, but you don't need to show the design process
- You do not need to design the outer PQ controller loop: Instead, divide your power set-points by grid voltage to obtain inner current controller references
- You can specify the initial voltages of all SM capacitors to their rated voltage in the EMT software (i.e., assume they are all pre-charged)

1. [**10 points**] Design the LR filter values for the MMC, using the procedure developed in class. Then use these values in all subsequent questions.

2. [**60 points**] Implement GFL PQ control, circulating current control, and SM capacitor voltage balancing control for your MMC. Simulate the converter system: In the beginning, set both P^{ref} and Q^{ref} to 0, and subsequently, step up P^{ref} to 1 MW. Plot the following and briefly comment on the results:
    i. i_d and i_d^{ref} on the same plot
    ii. i_q and i_q^{ref} on the same plot
    iii. Measured real and reactive powers at the PCC on the same plot
    iv. 3-phase circulating currents on the same plot

v. Upper and lower arm currents of phase a on the same plot
vi. All four submodule capacitor voltages for the upper arm of phase a on the same plot

3. [**15 points**] Repeat question (2) but disable the circulating current control only. Briefly comment on the results (e.g., compare your waveforms to the ones obtained from question (2)).

4. [**15 points**] Repeat question (2) but disable the SM capacitor voltage balancing control only (i.e., you do not need to sort the SM voltages to determine which SMs to insert). Briefly comment on the results (e.g., compare your waveforms to the ones obtained from question (2)).