EECE571D 2025W1 Assignment 1 (100 points)

Due: October 24, 2025

A three-phase two-level VSC is connected to a constant DC voltage source on its DC-side, and its AC-side is connected to an infinite bus through an LR filter. The VSC system has the following specifications:

- Grid voltage: 580 V (line-to-line, RMS)
- Grid frequency: 60 Hz
- DC-link voltage: 1000 V
- Rated power: 100 kVA
- Modulation strategy: Sinusoidal PWM
- Control mode: GFL PQ control
- Switching frequency: 3.06 kHz

For all subsequent questions, you may use any design procedure to obtain your controller parameters. Bode plots, root locus, MATLAB SISOTOOL, Nyquist plot, state-space designs are all accepted, but trial-and-error methods are not acceptable.

You do not need to design the outer PQ controller loop: instead, divide your power set-points by grid voltage to obtain inner current controller references.

You can simulate the VSC system in either MATLAB/Simulink, PSCAD, or PLECS. Converter latency and higher-order harmonics can be neglected.

1. [**10 points**] Design the LR filter values for the VSC, using the procedure developed in class. Then use these values in all subsequent questions.

2. [**40 points**] Design PI current controller and PLL controller for the VSC, using the net control block diagram models developed in class.
    a. Show your detailed design procedure for current controller (e.g., provide bode plot/root locus plot of your system, any calculations you have done, and/or any code, and explain why you have chosen the final controller parameters) and provide the final PI controller design in the format of $C(s) = k_p + \frac{k_i}{s}$
    b. Show your detailed design procedure for PLL controller (e.g., provide bode plot/root locus plot of your system, any calculations you have done, and/or any code, and explain why you have chosen the final controller parameters) and provide the final PI controller design in the format of $H(s) = k_{pPLL} + \frac{k_{iPLL}}{s}$
    c. Simulate the GFL VSC with your controllers: In the beginning, set both P^{ref} and Q^{ref} to 0, and subsequently, step up P^{ref} to 100 kW. Plot the following and briefly comment on the results (make sure you plot the waveforms for a total of 6 cycles, i.e., 2 cycles before step change and 4 cycles after step change)

i. i_d and i_d^{ref} on the same plot
ii. i_q and i_q^{ref} on the same plot
iii. 3-phase AC currents on the same plot
iv. Measured real and reactive powers at the PCC on the same plot

d. Repeat part (c) with a step change of 100 kVAr in reactive power exchange

3. [**40 points**] Repeat question (2) by placing second order low-pass filters on the i_{dq} measurements. The filter has a unity gain, $\omega_n = 5000\, rad/s$, $\zeta = 0.8$, with an expression of

$$L(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Keep in mind that there is no need to (i) re-design LR filter and (ii) re-design PLL controller again for this question.

4. [**10 points**] For the 3-phase system shown in class (gnd—V_t—L—R—V_s—gnd), we showed that $\left[V_{s\alpha\beta0}\right] = R\left[i_{\alpha\beta0}\right] + L\frac{d}{dt}\left[i_{\alpha\beta0}\right] + \left[V_{t\alpha\beta0}\right]$, where R and L are scalars. How, if at all, does this formulation change if V_s is unbalanced?

General advice: Don't over-think and over-complicate yourself. Follow the standard procedures you've learned, and everything should be fine. Ask me whenever you run into difficulties.