Assignment 1

Wednesday, October 8, 2025 2:05 PM

A three-phase two-level VSC is connected to a constant DC voltage source on its DC-side, and its AC-side is connected to an infinite bus through an LR filter. The VSC system has the following

- Grid voltage: 580 V (line-to-line, RMS) = √u, rem\$
- Grid frequency: 60 Hz
- DC-link voltage: 1000 V
- Rated power: 100 kVA = Spare
- Modulation strategy: Sinusoidal PWM
- Control mode: GFL PQ control
- Switching frequency: 3.06 kHz

For all subsequent questions, you may use any design procedure to obtain your controller parameters. Bode plots, root locus, MATLAB SISOTOOL, Nyquist plot, state-space designs are all accepted, but trial-and-error methods are not acceptable.

You do not need to design the outer PQ controller loop: instead, divide your power set-points by grid voltage to obtain inner current controller references.

You can simulate the VSC system in either MATLAB/Simulink, PSCAD, or PLECS. Converter latency and higher-order harmonics can be neglected.

1. [10 points] Design the LR filter values for the VSC, using the procedure developed in class. Then use these values in all subsequent questions.

VIL, RM = 580 V

$$\frac{V_{L}^{2}}{S_{base}} = \frac{V_{L}^{2}}{S_{base}} = R_{base} = X_{base} = \frac{580^{2}}{100 \cdot 10^{2}} = 3.364 \text{ s.}$$

$$L_{base} = \frac{X_{base}}{w_{0}} = \frac{3.364}{w_{0}} = 9.9 \text{ mH}$$

• Quality forcer:
$$Q = \frac{w_0 L}{R} = \frac{\chi_c}{R} \implies idealy Q > 75%$$

- 2. [40 points] Design PI current controller and PLL controller for the VSC, using the net control block diagram models developed in class.
 - a. Show your detailed design procedure for current controller (e.g., provide bode plot/root locus plot of your system, any calculations you have done, and/or any code, and explain why you have chosen the final controller parameters) and provide the final By an example of the form of a (a) b , a

loop gain:
$$L(U) = \left(\frac{K_r}{L_r}\right)^{\frac{r+k_i}{r+k_i}} \Rightarrow L(I) = \frac{K_r}{L_s}$$
 reservation gain Integral gain [losed-loop transfer function: $\frac{id(I)}{i\int_{I}^{ref}(U)} = G_i(S) = \frac{1}{L_iS+1}$, Choose $k_p = \frac{1}{L_i} \rightarrow k_i = \frac{1}{L_i}$

• Choose T_i so its small far fast current controller reviewer, but large enough s.t. $\frac{1}{T_i}$ (b.w) is about 10× smaller than switching drequery (fsw= 3.06 kH2) $\Rightarrow T_i = 3 \text{ ms} \quad \forall \quad \frac{1}{T_i} \sim 0.3 \text{ kH2}$

$$K_{p} = \frac{L}{T_{1}} = \frac{1.3 \text{ mH}}{3 \text{ m/s}} = 0.43 \text{ CV/A}$$

$$K_1 = \frac{R}{C_1} = \frac{1.3 \, \Omega}{3 \, \text{mg}} = 0.475$$
 CV/A)

$$C(3) = 0.43 + \frac{0.43}{5}$$

- b. Show your detailed design procedure for PLL controller (e.g., provide bode plot/root locus plot of your system, any calculations you have done, and/or any code, and explain why you have chosen the final controller parameters) and provide the final PI controller design in the format of $H(s) = k_{pPLL} + \frac{k_{IPLL}}{s}$
 - · Goal: requare Vsq at sco

- " Stree Romearting dround strendy state wo, w(0)=000 ? Wmin & w & winds
- · [Wm in , wmmx] ~ [55, 65 HZ] → close to we but not too clase
- Crosey-book thanker fruction: $\frac{1}{6} = \frac{1+\alpha n_2}{2\alpha n_2}$ where $\alpha n_2 = \frac{2}{6} \left(\frac{2}{7} \right) \left(\frac{2}{7} \right)$

$$\frac{\mathbf{1}^{LSE}}{\mathbf{1}} = \frac{(1 + \sqrt{2} (k^{L} + \frac{2}{k^{L}})(\frac{2}{l})}{\sqrt{2} (k^{L} + \frac{2}{k^{L}})(\frac{2}{l})} = \frac{2 + \sqrt{2} k^{L} + \sqrt{2} k^{L}}{\sqrt{2} k^{L} + \sqrt{2} k^{L}}$$

Denominator: S2+V, KeS+VsKi

damping totio:
$$S_1 = \frac{V_s \, K_P}{2 \, \sqrt{\hat{V}_s \, K_1}}$$