Vypracovanie PC_1

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Link to depository: https://github.com/alexander-bekec/Digital-electronics-1

1. Boolean Postulates:

In EDA Playground, verify basic Boolean postulates:

$$x \cdot \overline{x} = 0$$
$$x + \overline{x} = 1$$
$$x + x + x = x$$
$$x \cdot x \cdot x = x$$

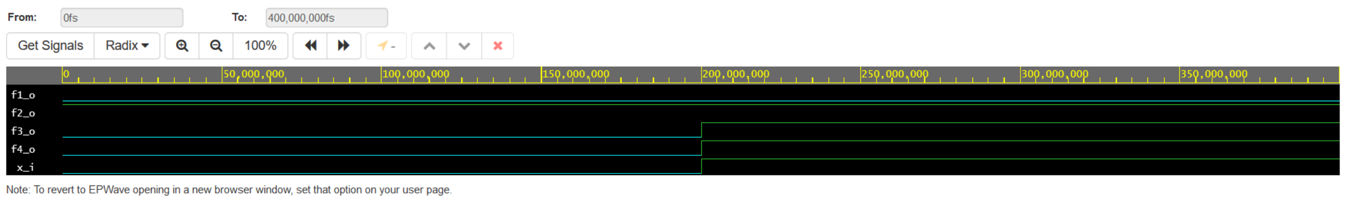
https://www.edaplayground.com/x/bG6s

```vhdl
--Boolean Postulates
library IEEE;
use IEEE.std_logic_1164.all;

entity gates is
    port(
        x_i : in std_logic;
        f1_o : out std_logic;
        f2_o : out std_logic;
        f3_o : out std_logic;
        f4_o : out std_logic
    );
end entity gates;

architecture dataflow of gates is
begin
    f1_o <= x_i and (not x_i);
    f2_o <= x_i or (not x_i);
    f3_o <= x_i or x_i or x_i;
    f4_o <= x_i and x_i and x_i;

end architecture dataflow;
```



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

2. Distributive Laws:

In EDA Playground, verify Distributive laws:

$$x \cdot y + x \cdot z = x \cdot (y + z)$$
$$(x + y) \cdot (x + z) = x + (y \cdot z)$$

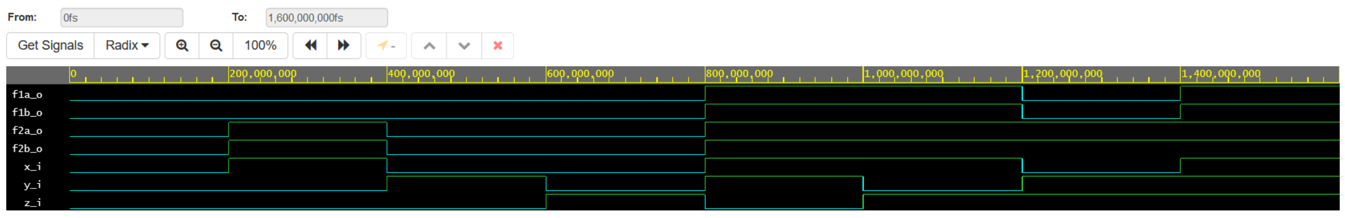
https://www.edaplayground.com/x/RY5v

```
--Distributive Laws
library IEEE;
use IEEE.std_logic_1164.all;

entity gates is
    port(
        x_i : in std_logic;
        y_i : in std_logic;
        z_i : in std_logic;
        f1a_o : out std_logic;
        f1b_o : out std_logic;
        f2a_o : out std_logic;
        f2b_o : out std_logic
    );
end entity gates;

architecture dataflow of gates is
begin
    f1a_o <= (x_i and y_i) or (x_i and z_i);
    f1b_o <= x_i and (y_i or z_i);
    f2a_o <= (x_i or y_i) and (x_i or z_i);
    f2b_o <= x_i or (y_i and z_i);

end architecture dataflow;
```



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3. DeMorgan's Laws

Use De Morgan's laws and modify the following logic function to the form with NAND and NOR gates only. Verify all three functions in EDA Playground tool.

$$f(c,b,a) = \overline{b}\,a + \overline{c}\,\overline{b}$$
$$f(c,b,a)_{\mathrm{NAND}} =$$
$$f(c,b,a)_{\mathrm{NOR}} =$$

https://www.edaplayground.com/x/MDrq

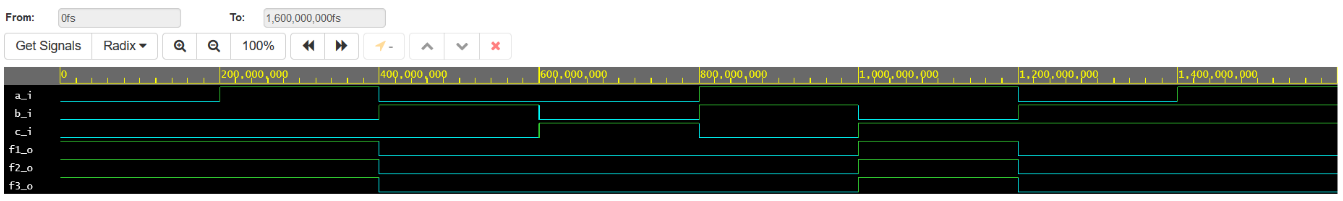
```
--DeMorgan's Laws
library IEEE;
```

```
use IEEE.std_logic_1164.all;

entity gates is
    port(
        a_i : in std_logic;
        b_i : in std_logic;
        c_i : in std_logic;
        f1_o : out std_logic;
        f2_o : out std_logic;
        f3_o : out std_logic
    );
end entity gates;

architecture dataflow of gates is
begin
    f1_o <= ((not b_i) and a_i) or ((not c_i) and (not b_i));
    f2_o <= not ((not ((not b_i) and a_i)) and (not ((not c_i) and (not b_i))));
    f3_o <= (not (b_i or (not a_i))) or (not (c_i or b_i));

end architecture dataflow;
```



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c	b	a	f(c,b,a)
0	0	0	1
0	0	1	1
0	1	0	0
1	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0
1	1	1	0