Vypracovanie PC_3

Alexander Bekeč, 221096

Link to depository: https://github.com/alexander-bekec/Digital-electronics-1

1. Preparation task

Switch	Pin connection	LED	Pin connection
SW0	J15	LED0	H17
SW1	L16	LED1	K15
SW2	M13	LED2	J13
SW3	R15	LED3	N14
SW4	R17	LED4	R18
SW5	T18	LED5	V17
SW6	U18	LED6	U17
SW7	R13	LED7	U16
SW8	T8	LED8	V16
SW9	U8	LED9	T15
SW10	R16	LED10	U14
SW11	T13	LED11	T16
SW12	H6	LED12	V15
SW13	U12	LED13	V14
SW14	U11	LED14	V12
SW15	V10	LED15	V11

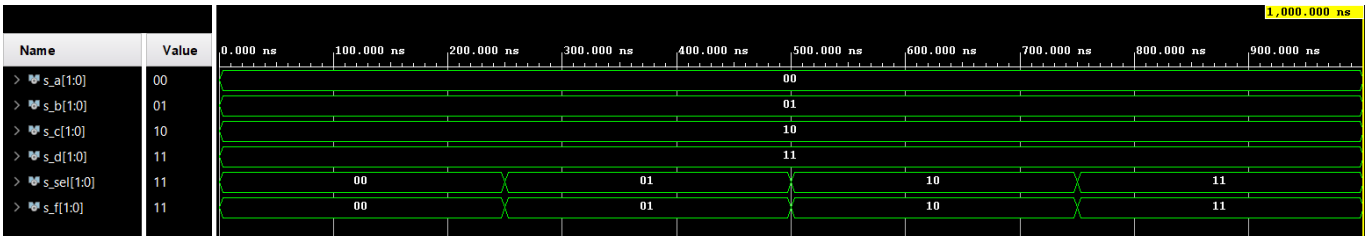
2. 2-bit 4-to-1 multiplexer

```
-- Architecture (Source file)
library IEEE;
use IEEE.std_logic_1164.all;

entity mux_2bit_4to1 is
    port(
        a_i           : in  std_logic_vector(2 - 1 downto 0);
        b_i           : in  std_logic_vector(2 - 1 downto 0);
        c_i           : in  std_logic_vector(2 - 1 downto 0);
        d_i           : in  std_logic_vector(2 - 1 downto 0);
```

```
        sel_i         : in  std_logic_vector(2 - 1 downto 0);
        f_o           : out std_logic_vector(2 - 1 downto 0)
    );
end entity mux_2bit_4to1;

architecture Behavioral of mux_2bit_4to1 is
begin
    f_o    <= a_i when (sel_i = "00") else
              b_i when (sel_i = "01") else
              c_i when (sel_i = "10") else
              d_i;
end architecture Behavioral;
```

```
-- Stimulus process (Testbench file)
library IEEE;
use IEEE.std_logic_1164.all;

entity tb_mux_2bit_4to1 is

end entity tb_mux_2bit_4to1;

architecture testbench of tb_mux_2bit_4to1 is

    signal s_a       : std_logic_vector(2 - 1 downto 0);
    signal s_b       : std_logic_vector(2 - 1 downto 0);
    signal s_c       : std_logic_vector(2 - 1 downto 0);
    signal s_d       : std_logic_vector(2 - 1 downto 0);
    signal s_sel     : std_logic_vector(2 - 1 downto 0);
    signal s_f       : std_logic_vector(2 - 1 downto 0);

begin
    uut_mux_2bit_4to1 : entity work.mux_2bit_4to1
        port map(
            a_i     => s_a,
            b_i     => s_b,
            c_i     => s_c,
            d_i     => s_d,
            sel_i   => s_sel,
            f_o     => s_f
        );

    p_stimulus : process
    begin
        report "Stimulus process started" severity note;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "00"; wait for 250 ns;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "01"; wait for 250 ns;
```

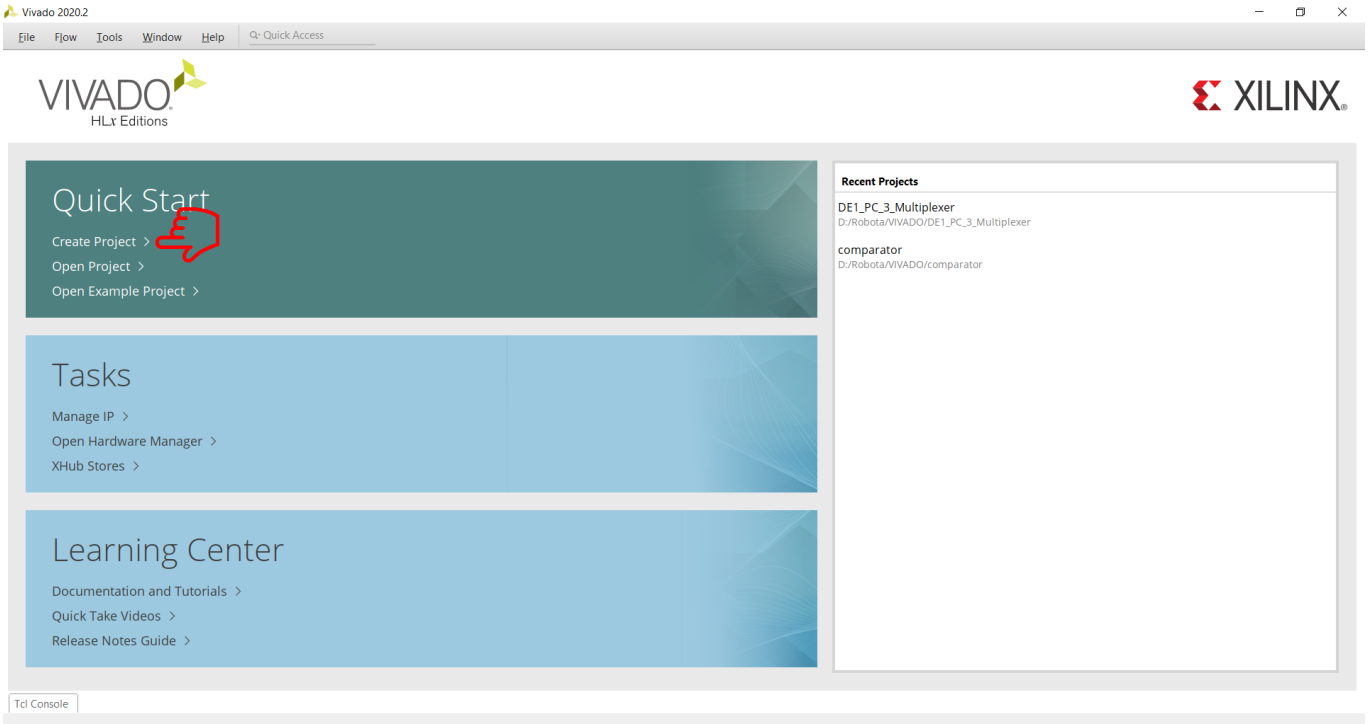
```
        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "10"; wait for 250 ns;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "11"; wait for 250 ns;

        report "Stimulus process finished" severity note;
        wait;
    end process p_stimulus;

end architecture testbench;
```



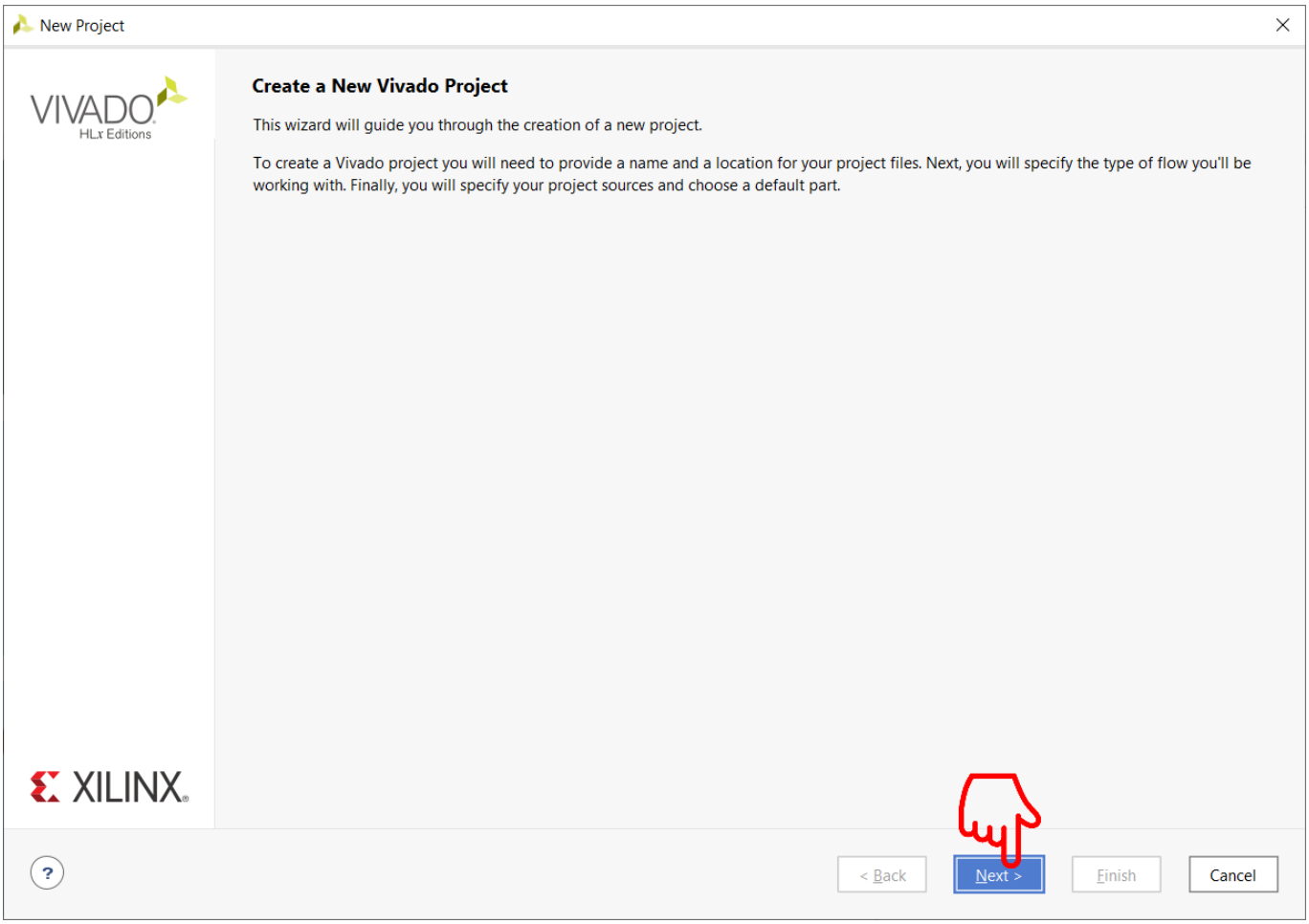
3. Vivado Tutoriál

Vytvorenie projektu

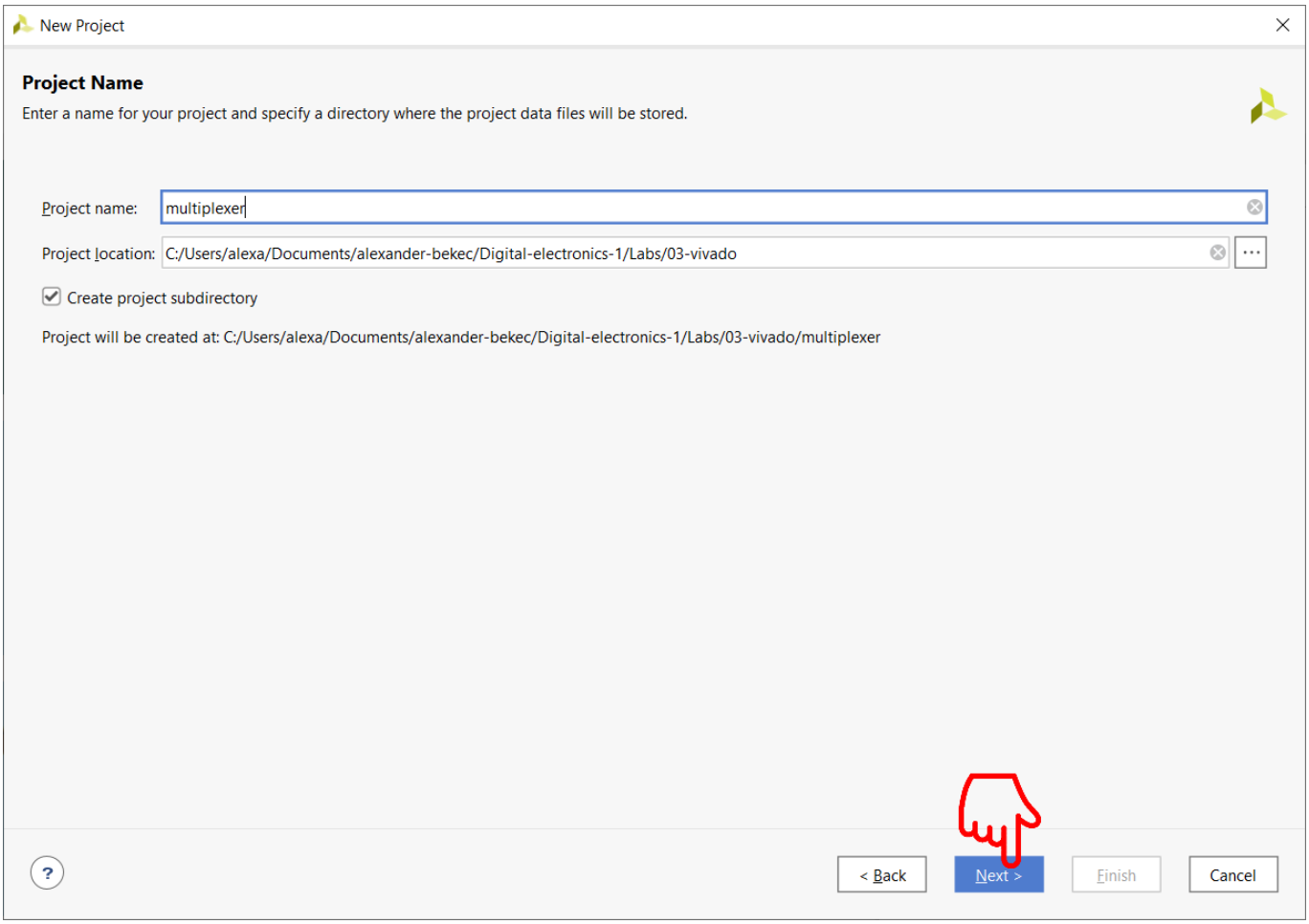
V hlavnom menu programu klikneme v sekcii Quick Start na Create Project:



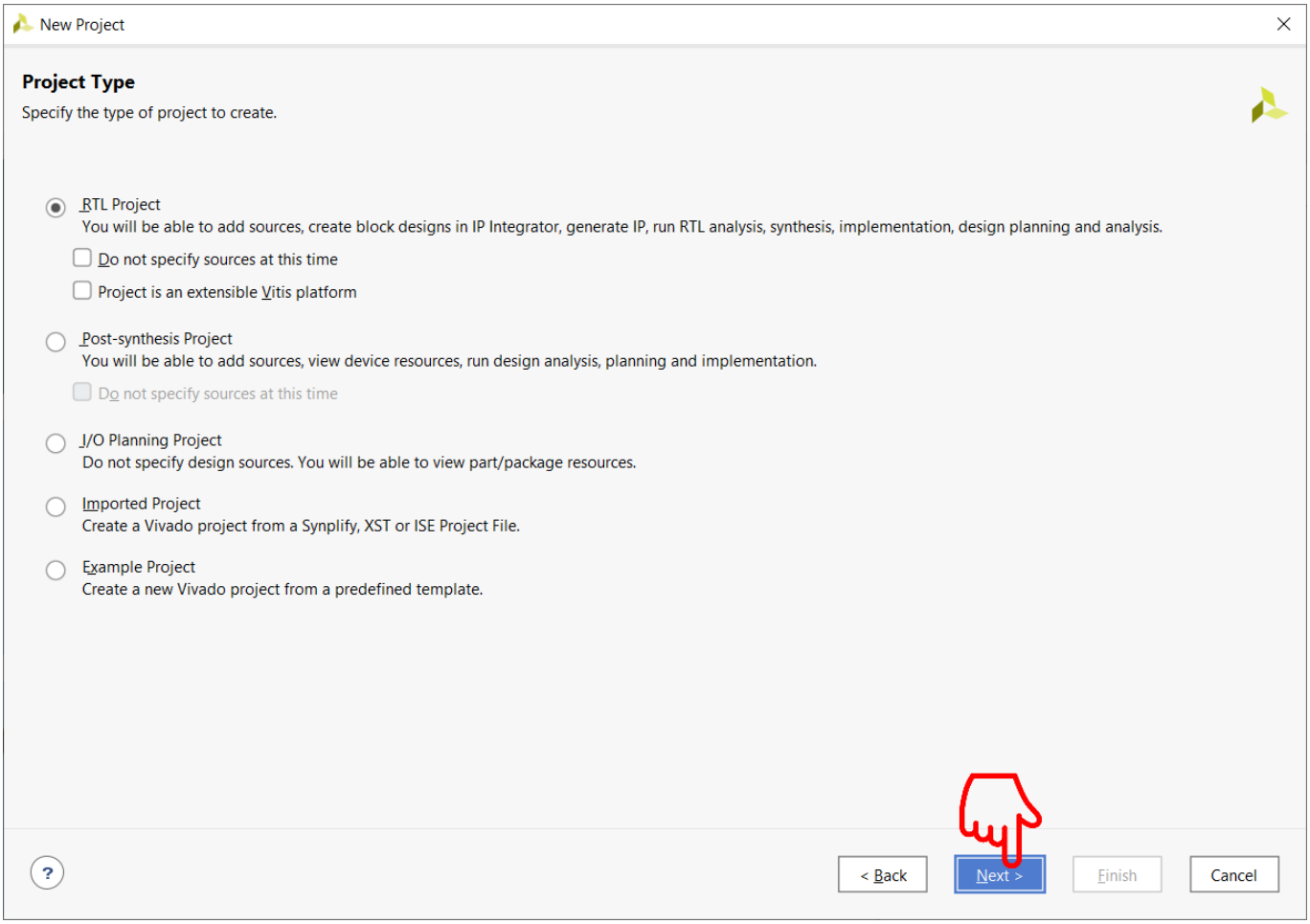
V nasledujúcom okne "Create a New Vivado Project" klikneme na Next >



Otvorí sa okno "Project Name", v ktorom definujeme názov projektu a adresu k miestu jeho uloženia. Po zadaní klikneme na Next >

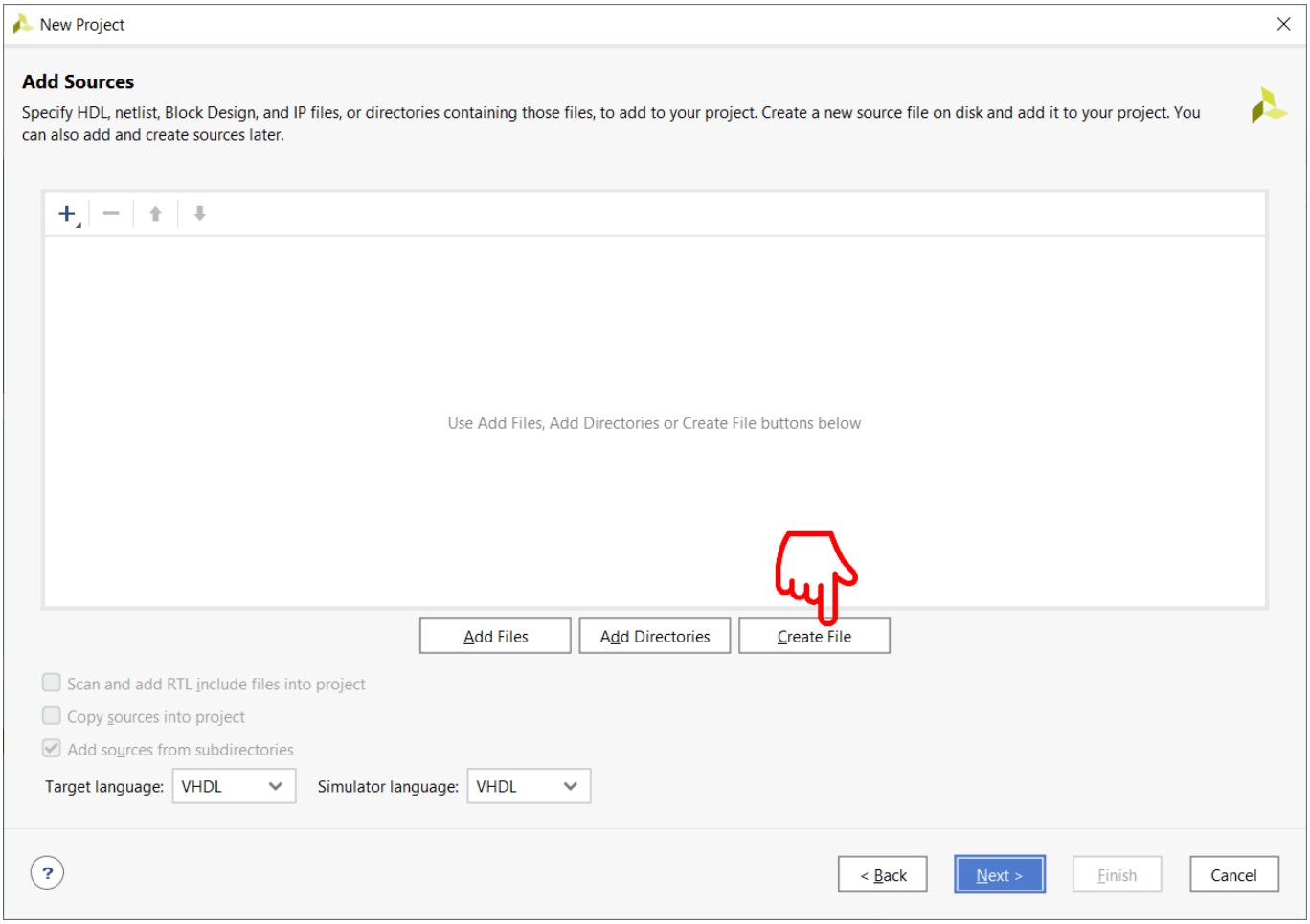


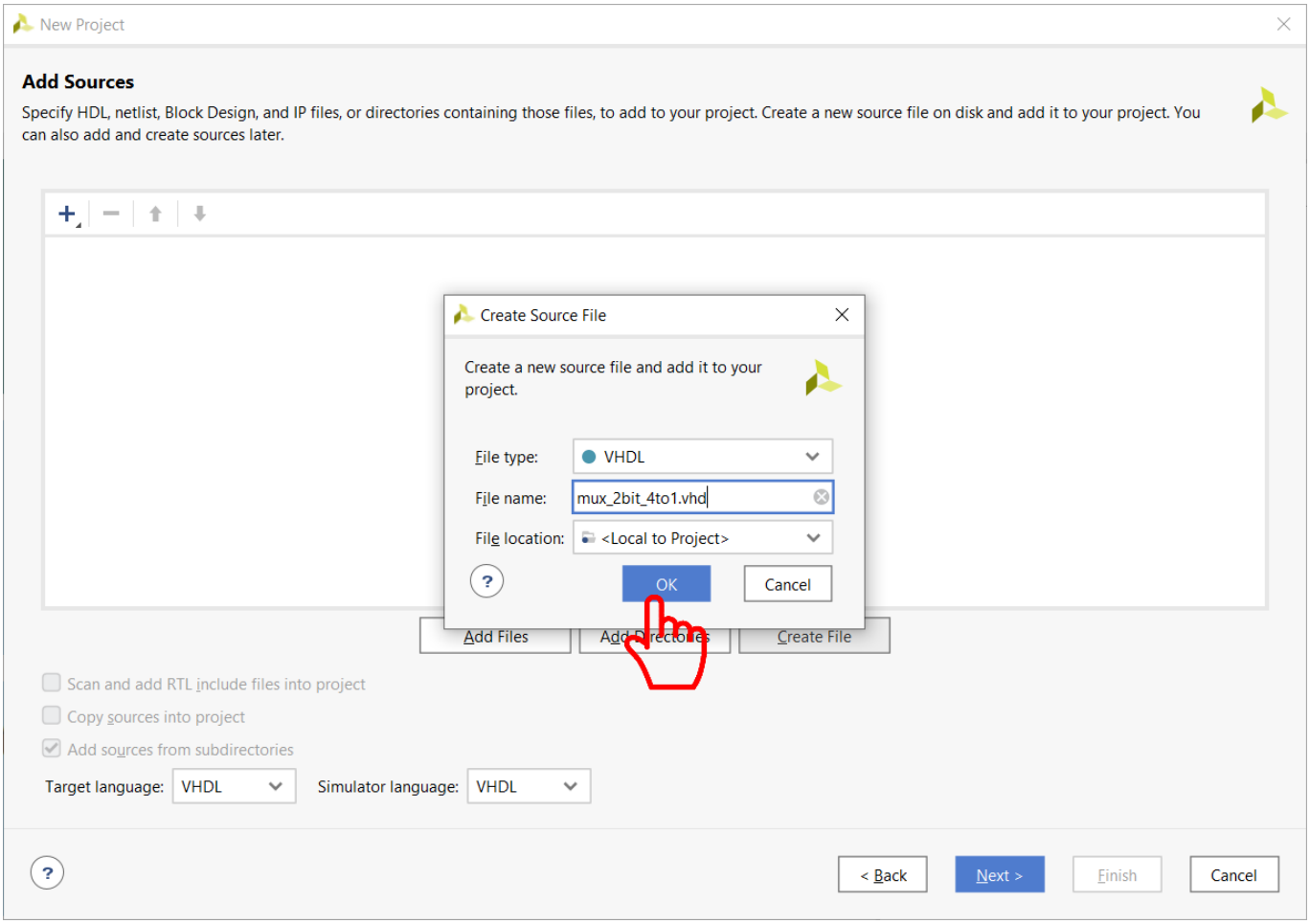
V nasledujúcom okne "Project Type" klikneme na Next > (bez zmeny zaškrtávacích políčok)



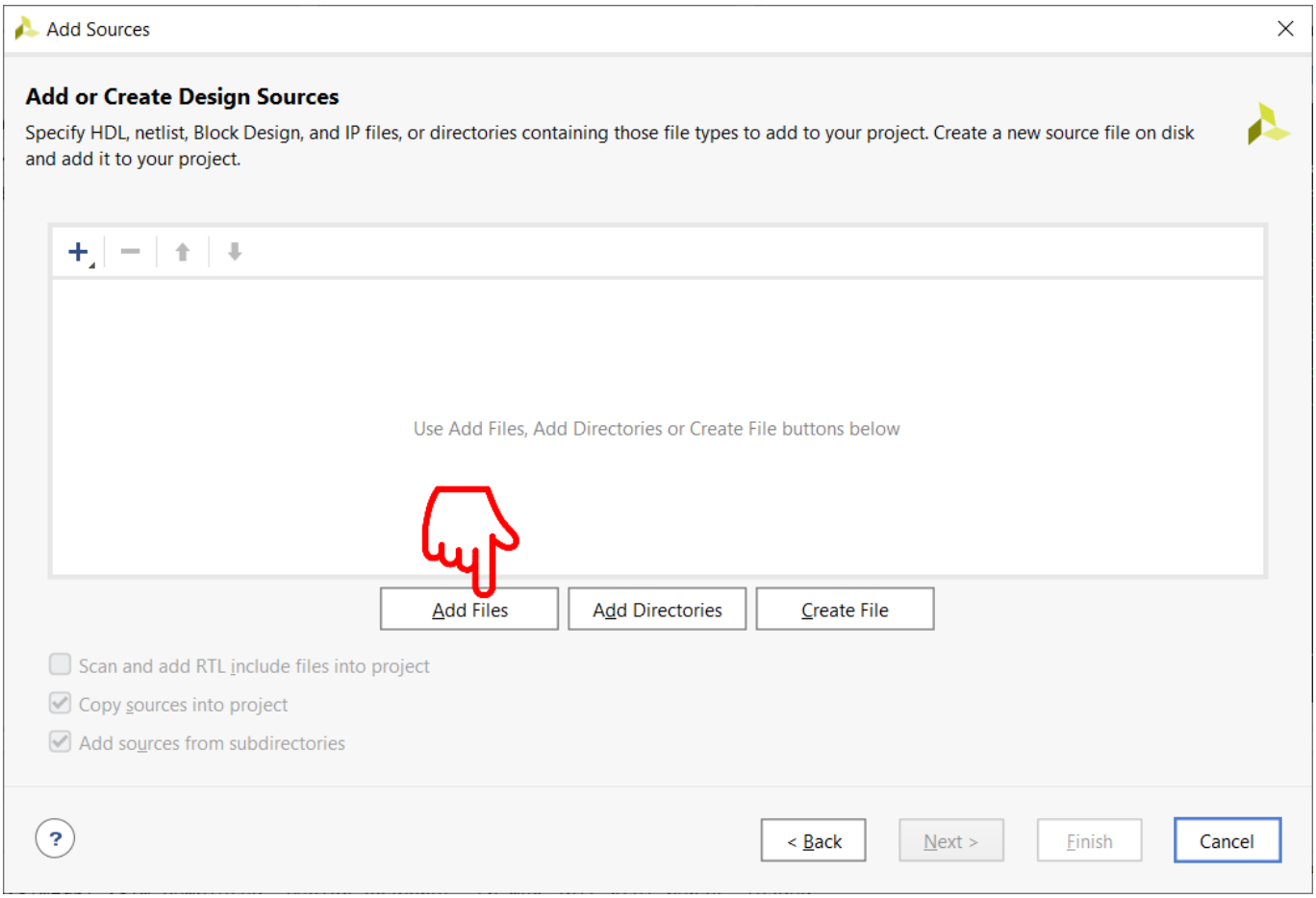
V ďalšom okne "Add Sources" pridávame alebo vytvárame nový zdrojový súbor

Vytvorenie zdrojového súboru (Create File):



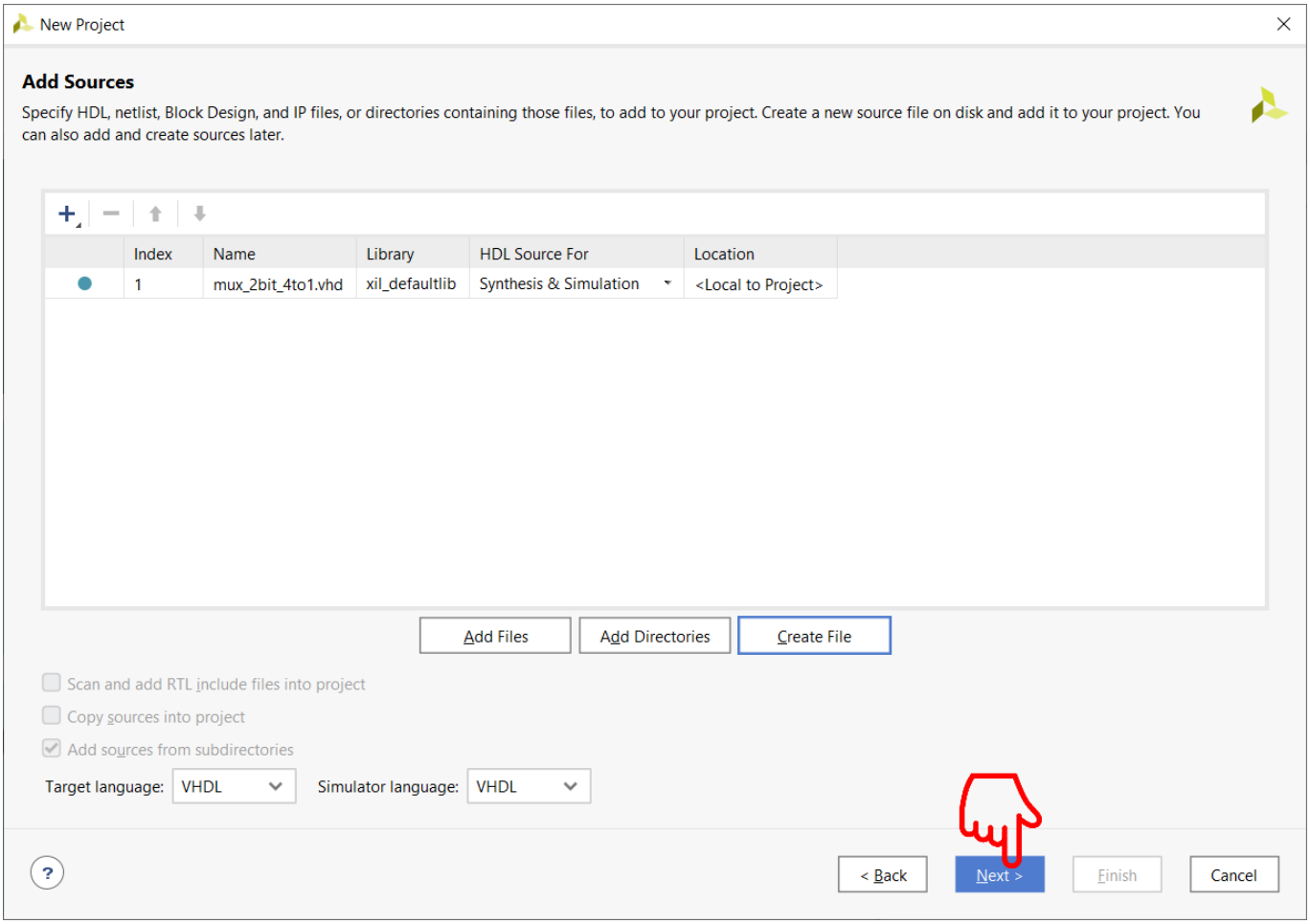


Pridanie existujúceho zdrojového súboru (Add Files):


Add Sources
Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel

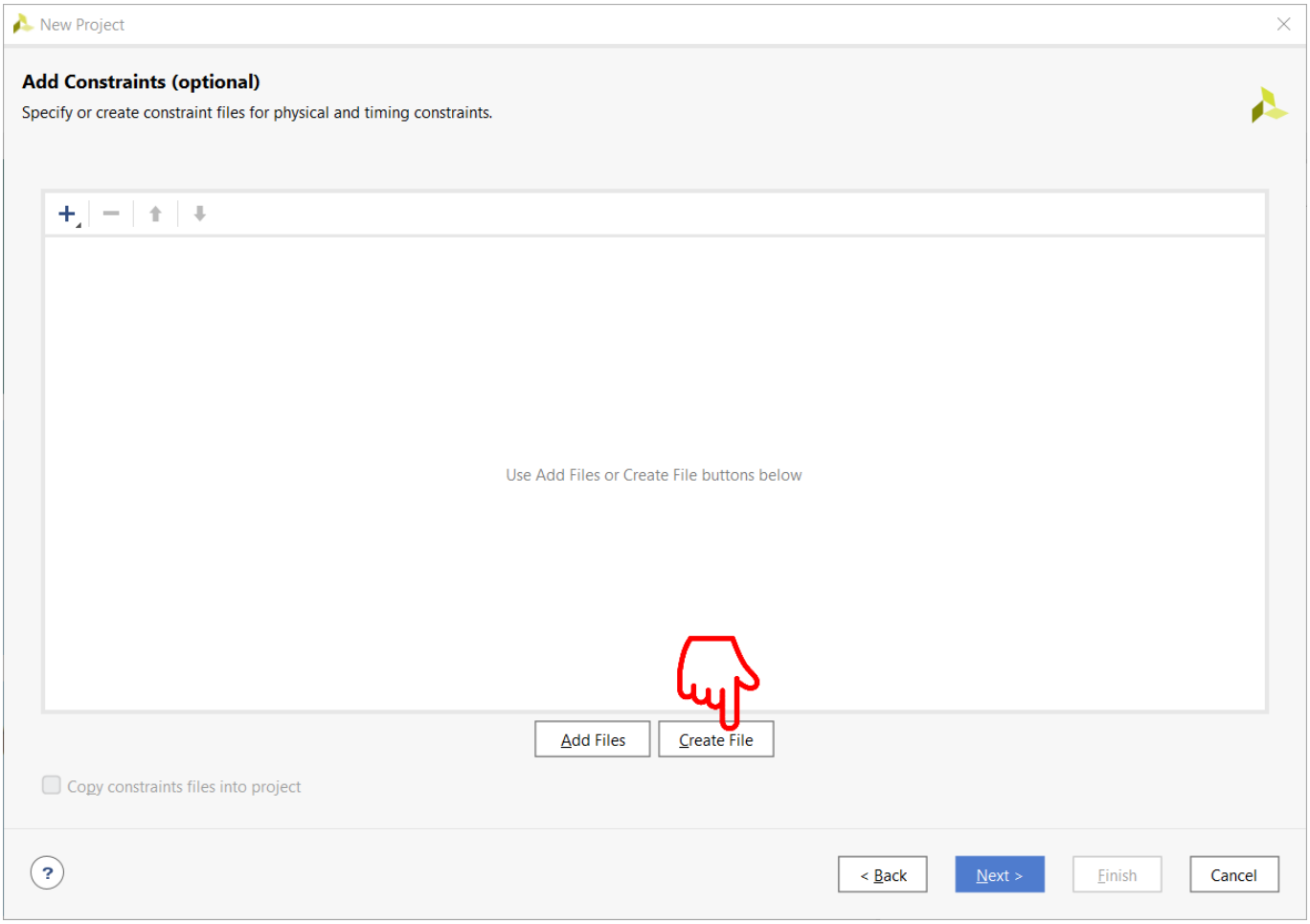

Add Source Files
Look in: new
mux_2bit_4to1.vhd
Recent Directories
C:/Users/alexa/Documents/alexander-bekec/Digi...
File Preview
library IEEE;
use IEEE.std_logic_1164.all;
entity mux_2bit_4to1 is
port(
a_i : in std_logic_vect
b_i : in std_logic_vect
c_i : in std_logic_vect
d_i : in std_logic_vect
sel_i : in std_logic_vect
f_o : out std_logic_vect
);
File name: mux_2bit_4to1.vhd
Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verilog, vr, vg, vb, tf, vlog, vp, vm, veo, svo, vh, h, svh, vhp, svhp, edn, edf, edif, ngc, sv, svp, bmm, mif, mem, elf, dnp, bd, bxml, xco, xci, xc...
OK
Cancel

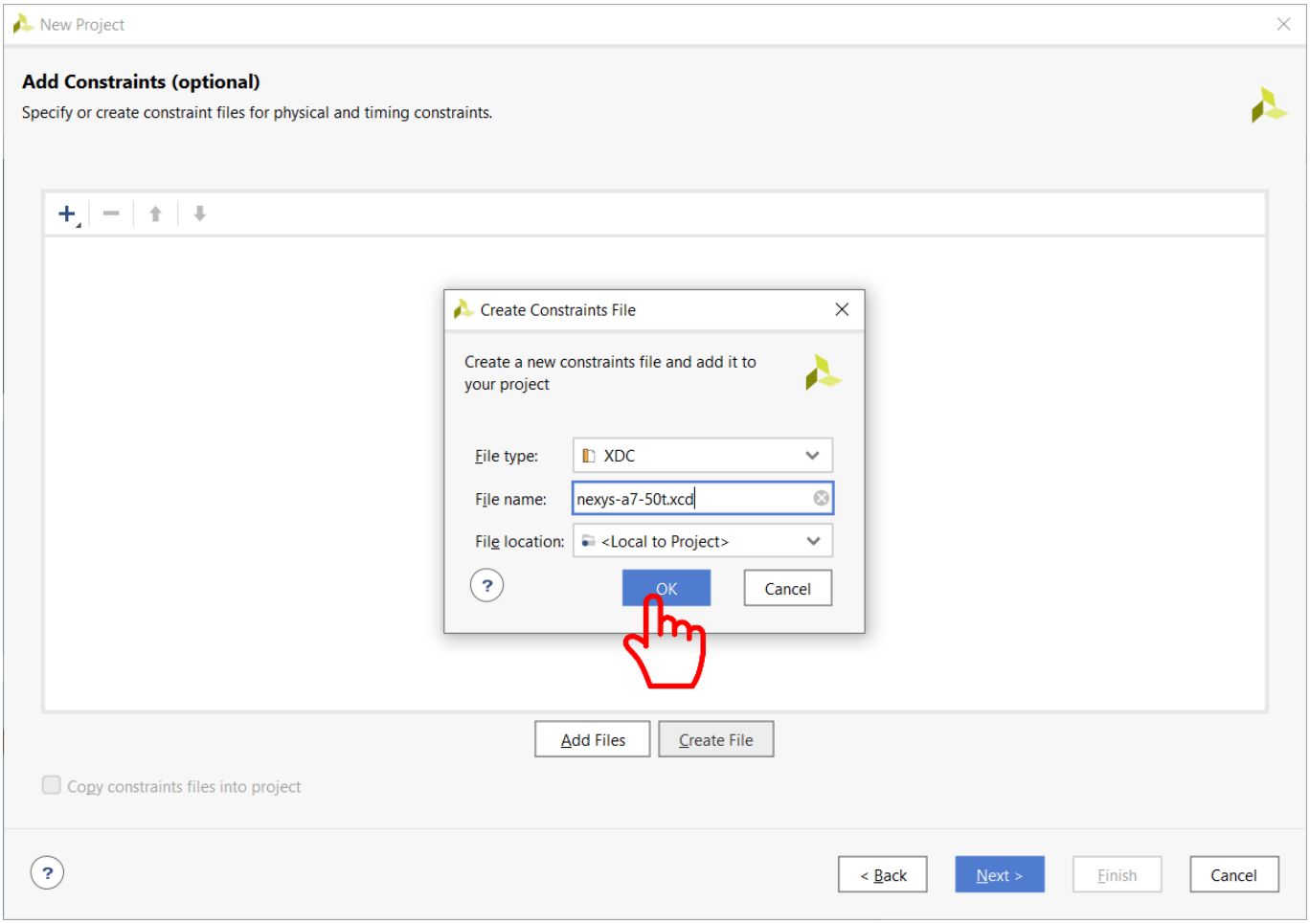
Po vytvorení alebo pridaní súboru klikneme na Next >

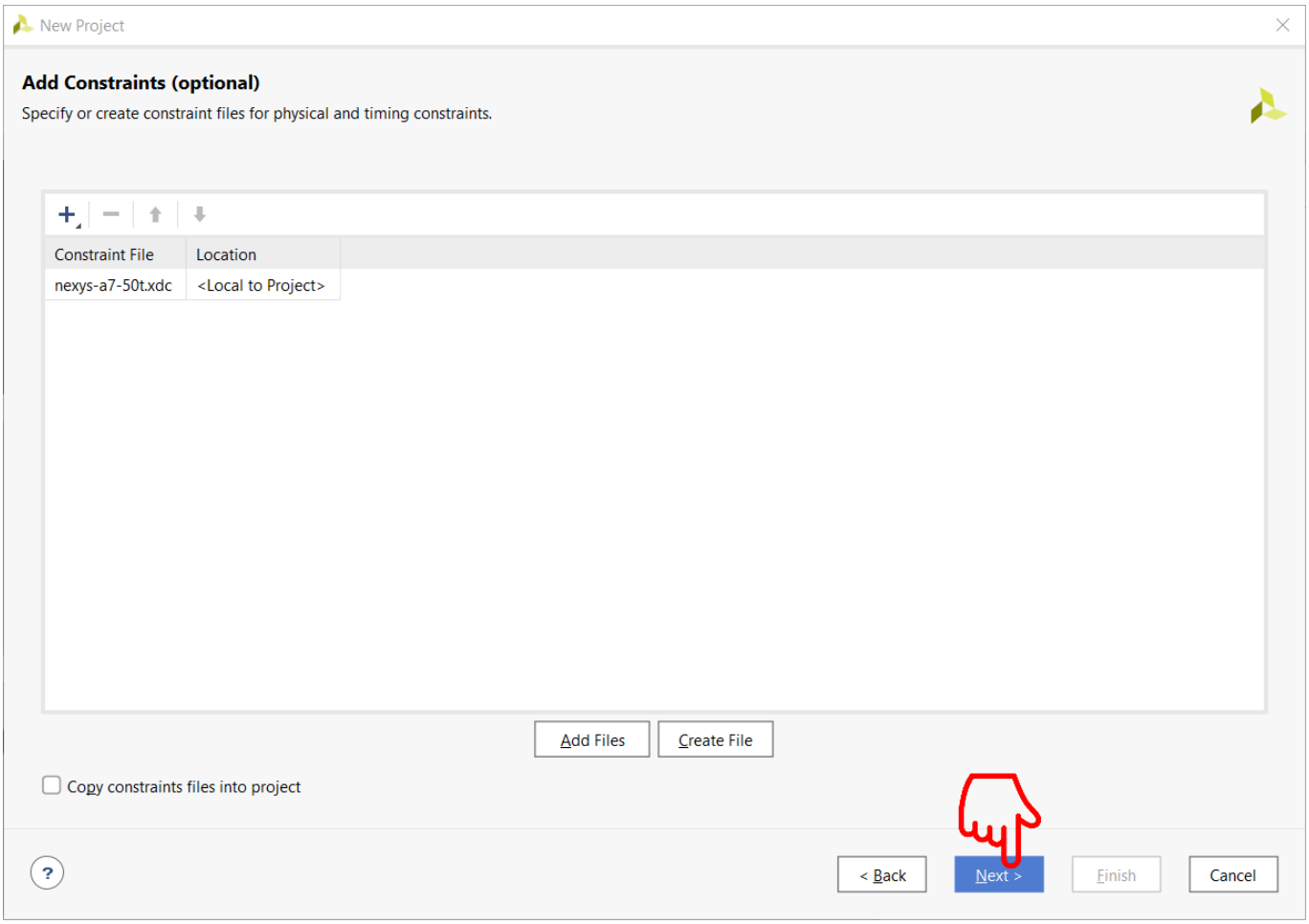


To nás presunulo do okna "Add Constraints"

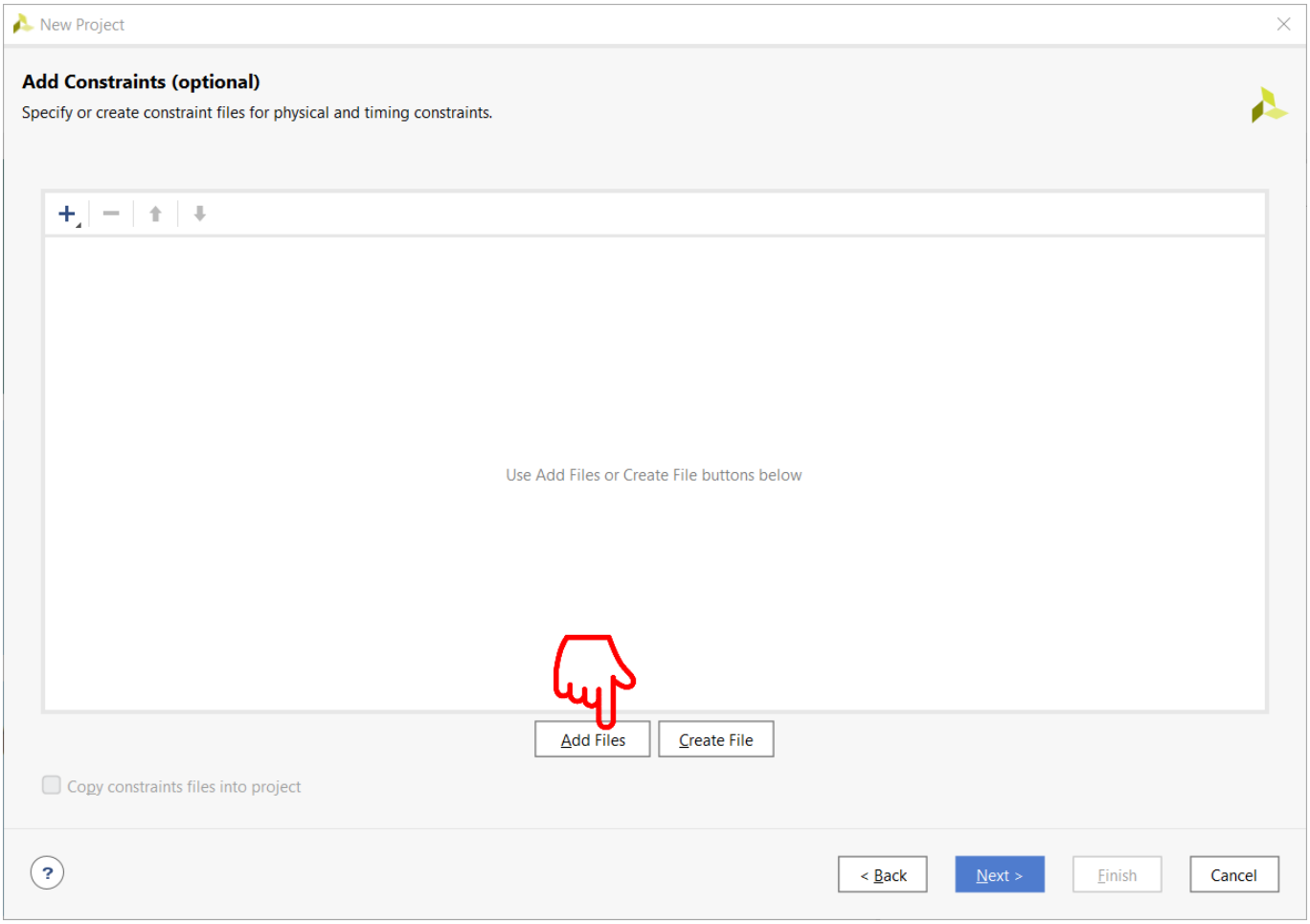
Vytvorenie súboru (Create File):

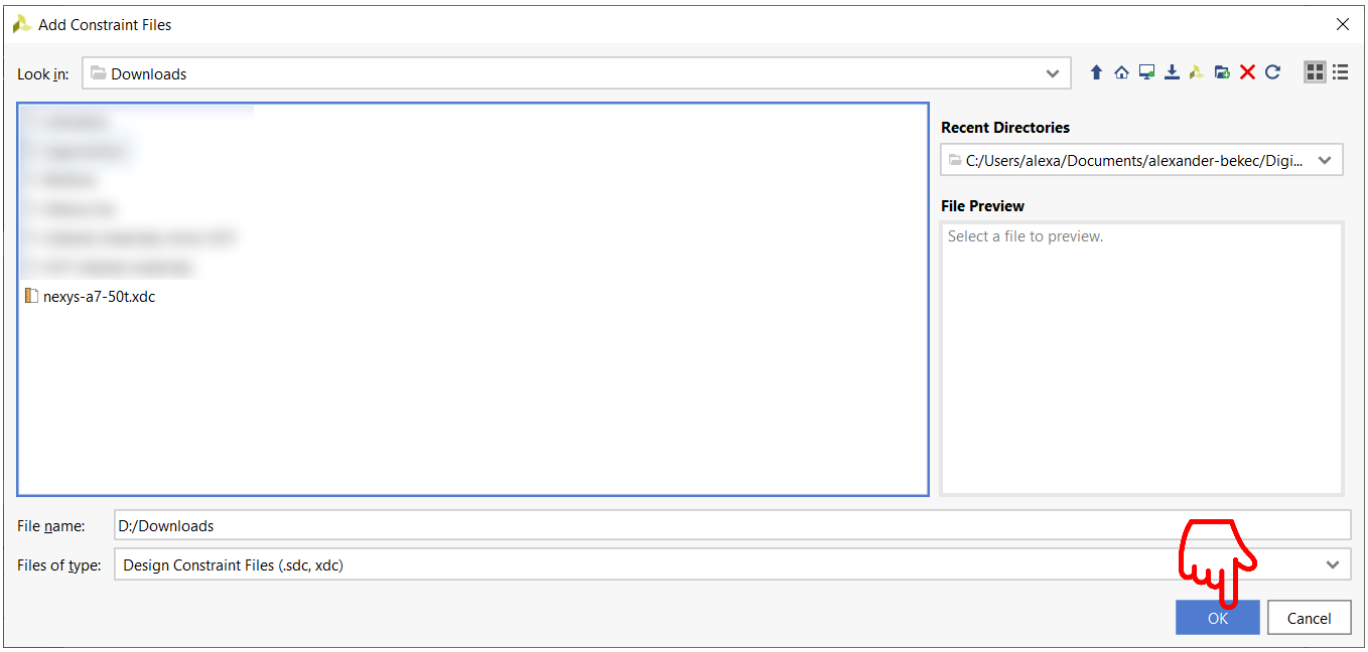


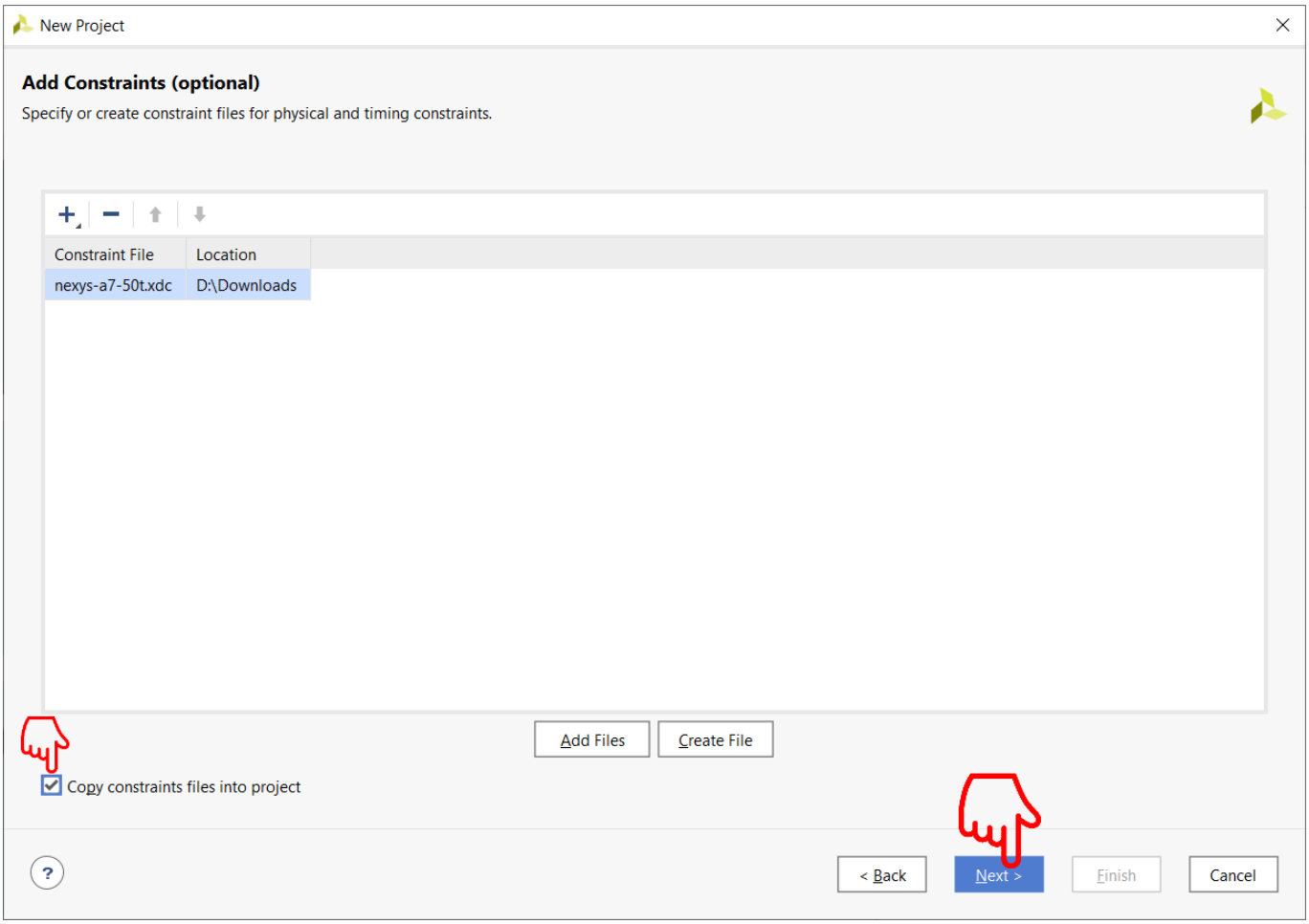




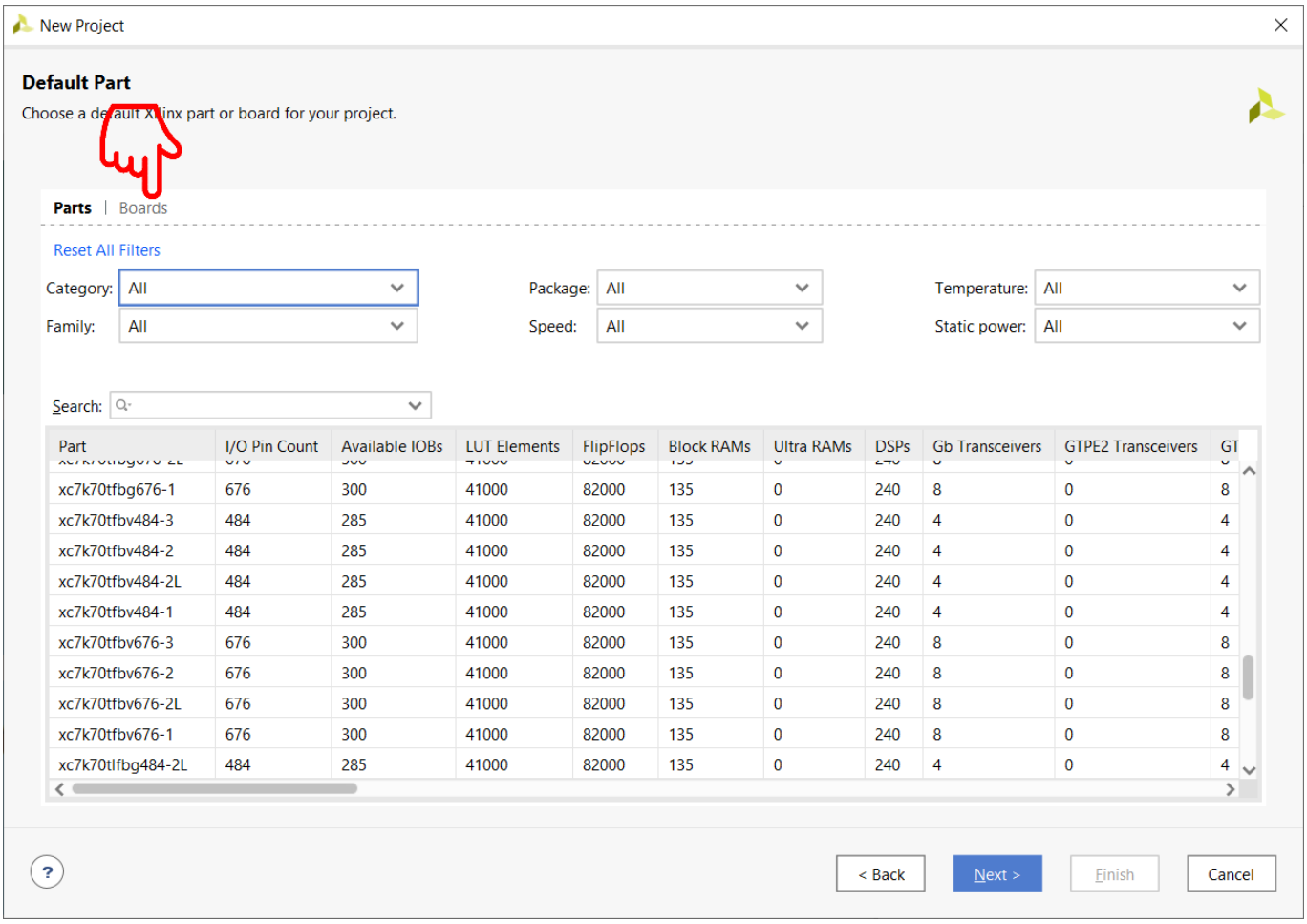
Pridanie existujúceho súboru (Add Files):

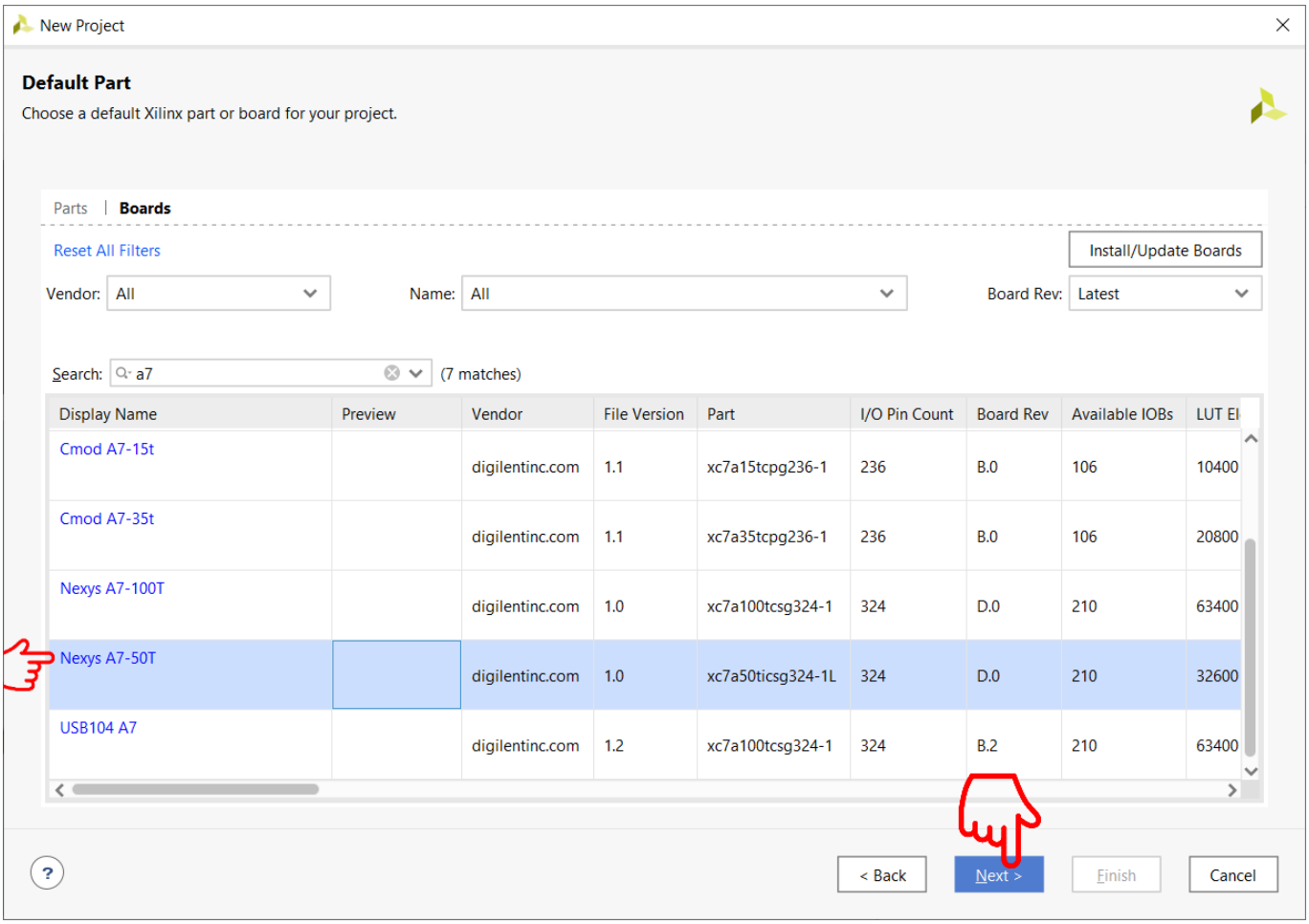




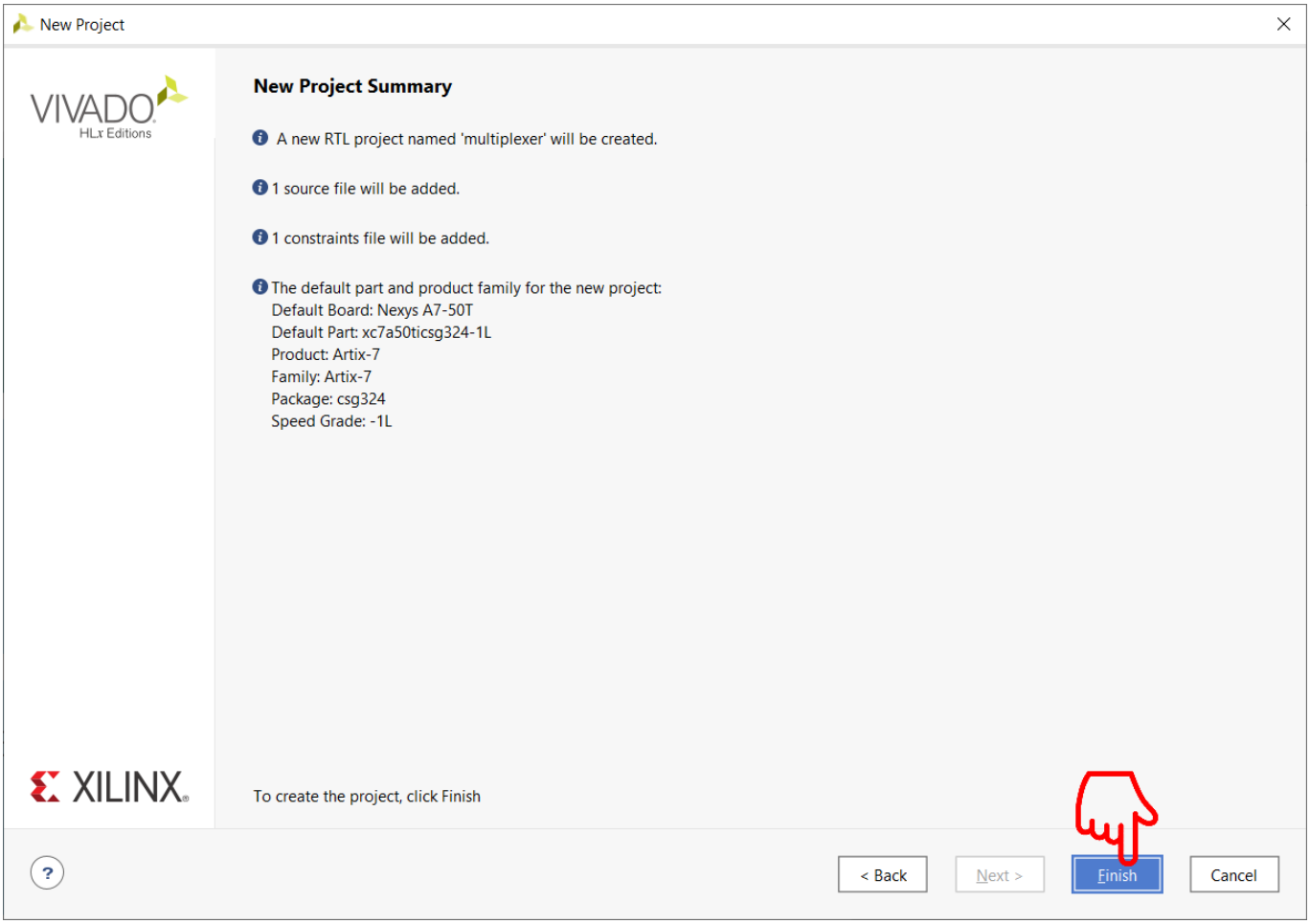


Kliknutie na Next > nás v oboch prípadoch presunie do okna s výberom súčiastky (Default Part)


New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: All
Package: All
Temperature: All
Family: All
Speed: All
Static power: All
Search:
Part | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra RAMs | DSPs | Gb Transceivers | GTPE2 Transceivers | GT
xc7k70tfbg676-1 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0 | 8
xc7k70tfbv484-3 | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0 | 4
xc7k70tfbv484-2 | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0 | 4
xc7k70tfbv484-2L | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0 | 4
xc7k70tfbv484-1 | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0 | 4
xc7k70tfbv676-3 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0 | 8
xc7k70tfbv676-2 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0 | 8
xc7k70tfbv676-2L | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0 | 8
xc7k70tfbv676-1 | 676 | 300 | 41000 | 82000 | 135 | 0 | 240 | 8 | 0 | 8
xc7k70tlfbg484-2L | 484 | 285 | 41000 | 82000 | 135 | 0 | 240 | 4 | 0 | 4
< Back
Next >
Finish
Cancel

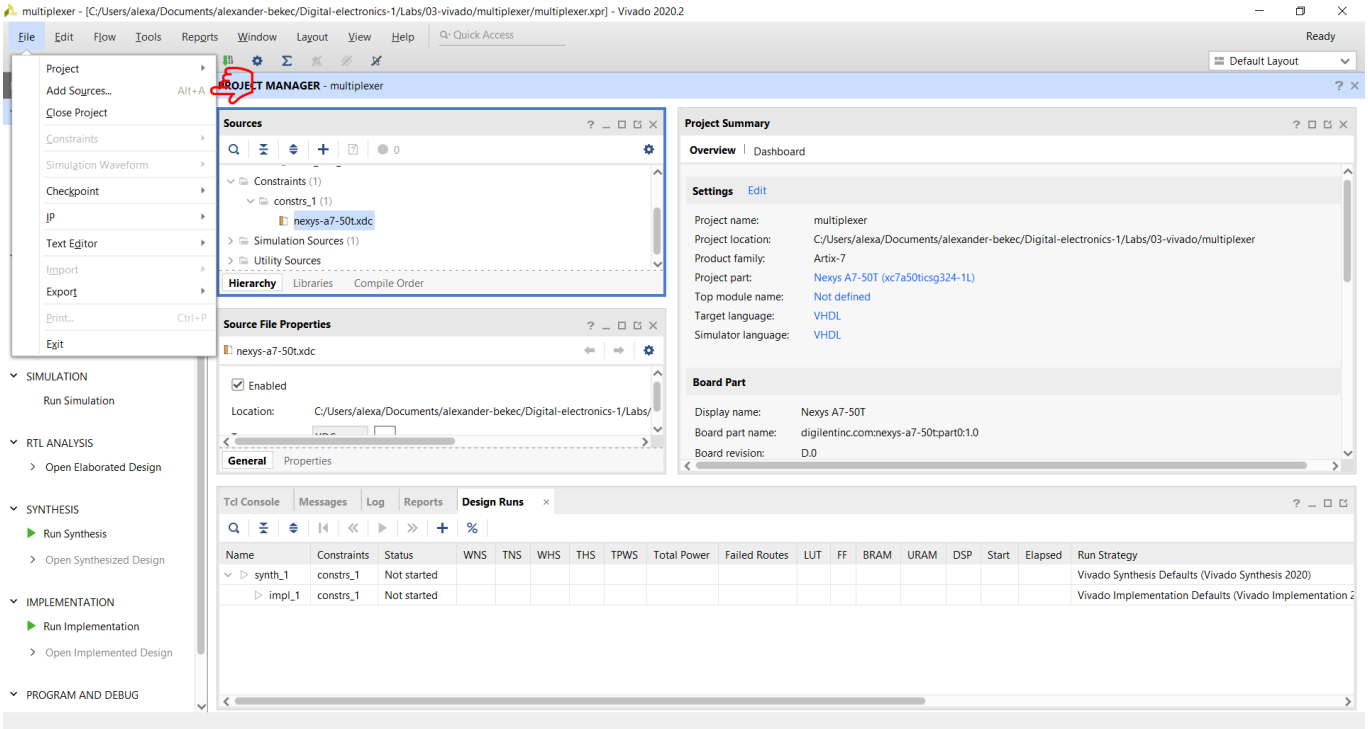

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Install/Update Boards
Vendor: All
Name: All
Board Rev: Latest
Search: a7
(7 matches)
Display Name | Preview | Vendor | File Version | Part | I/O Pin Count | Board Rev | Available IOBs | LUT El
Cmod A7-15t | digilentinc.com | 1.1 | xc7a15tcpg236-1 | 236 | B.0 | 106 | 10400
Cmod A7-35t | digilentinc.com | 1.1 | xc7a35tcpg236-1 | 236 | B.0 | 106 | 20800
Nexys A7-100T | digilentinc.com | 1.0 | xc7a100tcsg324-1 | 324 | D.0 | 210 | 63400
Nexys A7-50T | digilentinc.com | 1.0 | xc7a50ticsg324-1L | 324 | D.0 | 210 | 32600
USB104 A7 | digilentinc.com | 1.2 | xc7a100tcsg324-1 | 324 | B.2 | 210 | 63400
< Back
Next >
Finish
Cancel

Potvrdenie výberu stlačením Next > nás presunie do okna so zhrnutím nastavení projektu

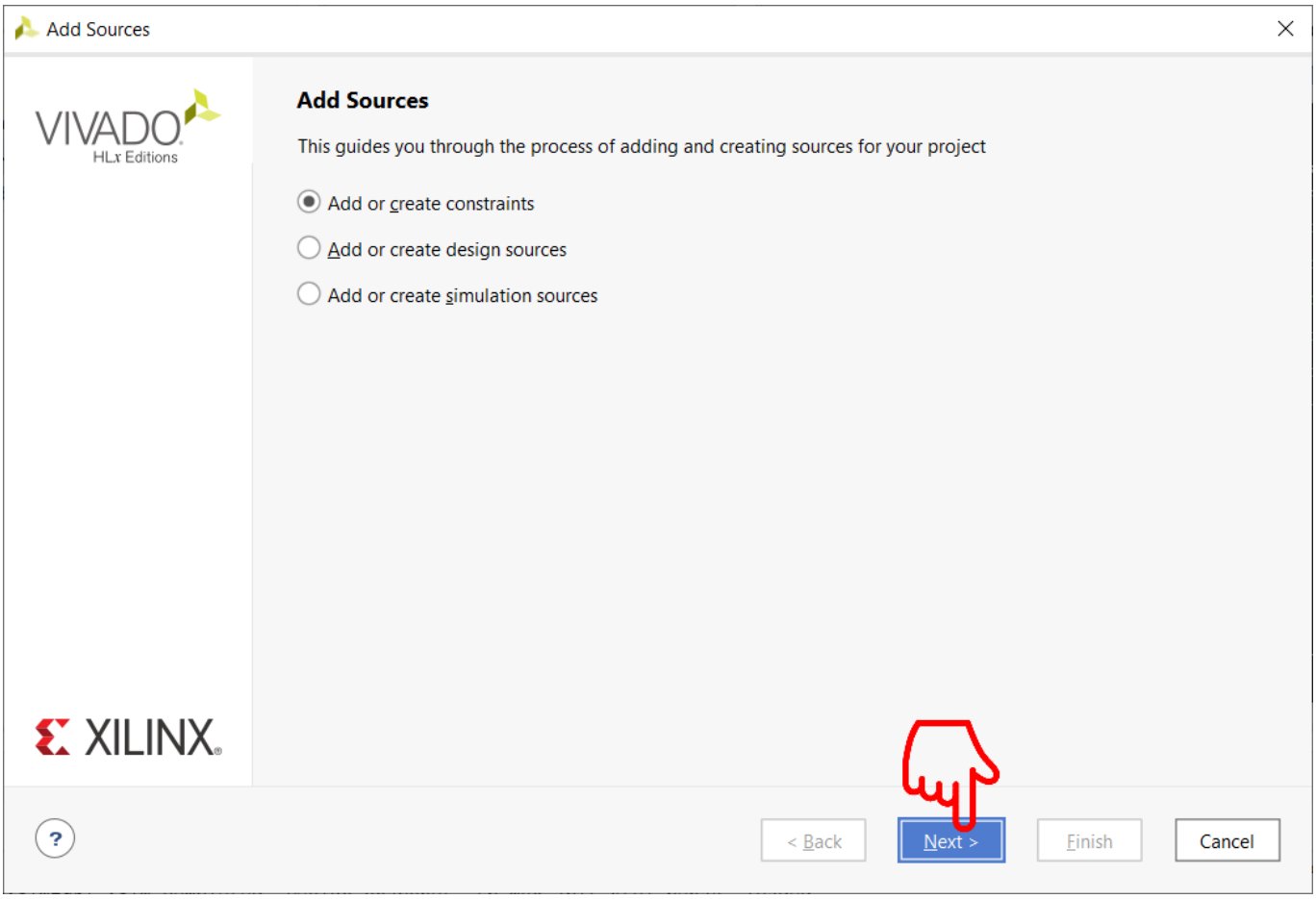


Pridanie súboru v rámci programu

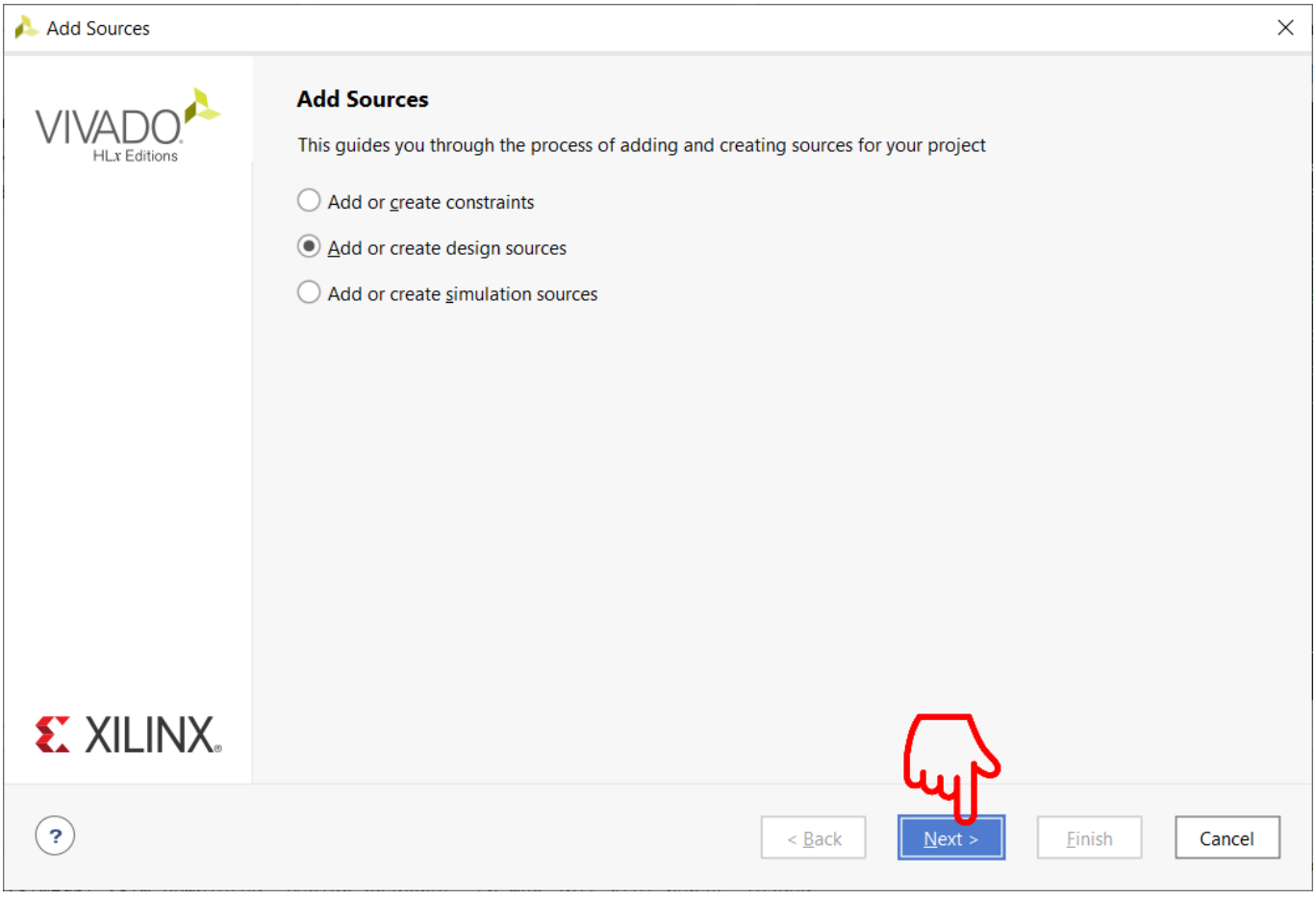
Súbor v rámci projektu pridáme cez File > Add Sources... (Alt + A)



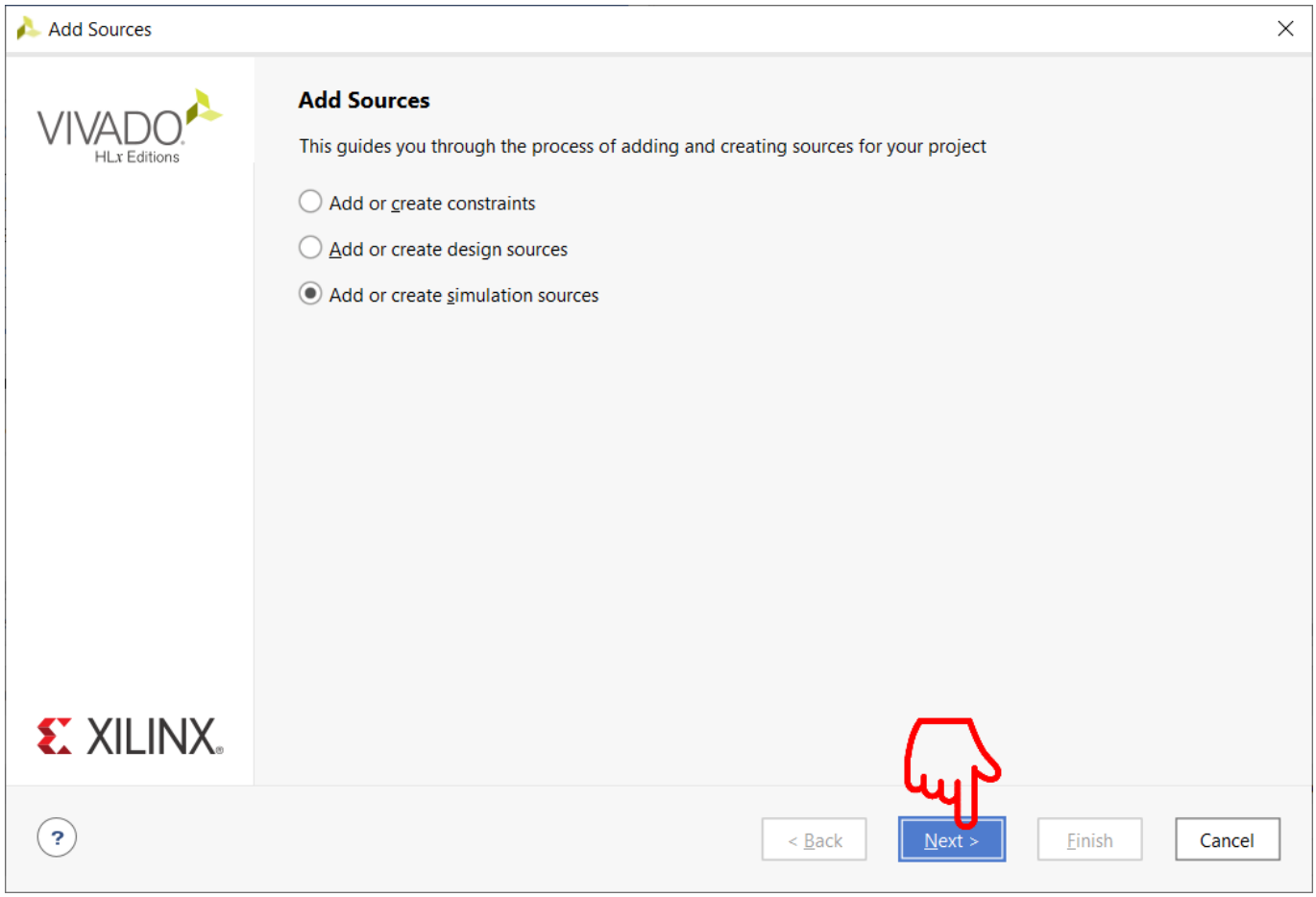
Add or Create Constrains (v ďalších oknách vedie rovnako ako pri vytváraní projektu):

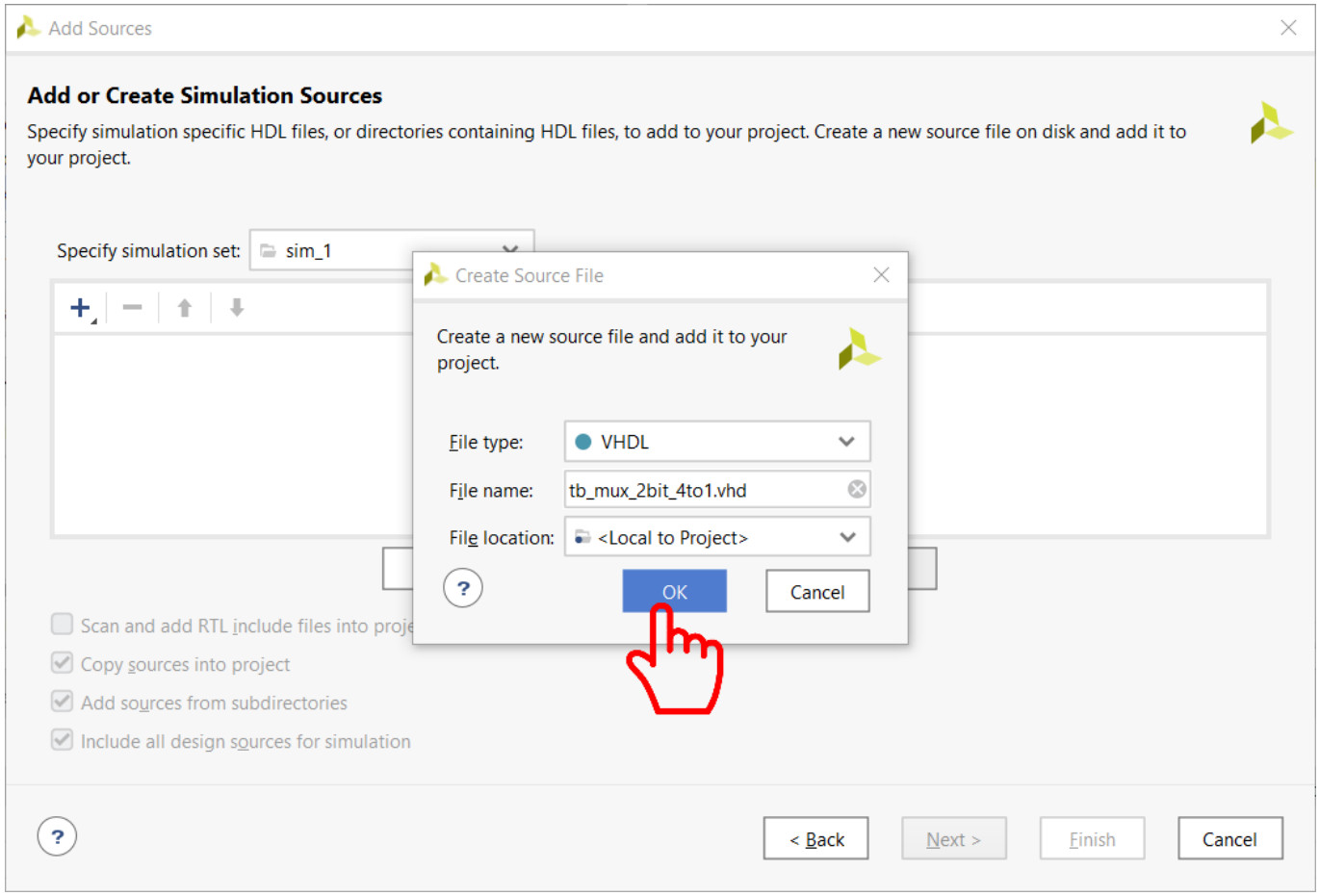


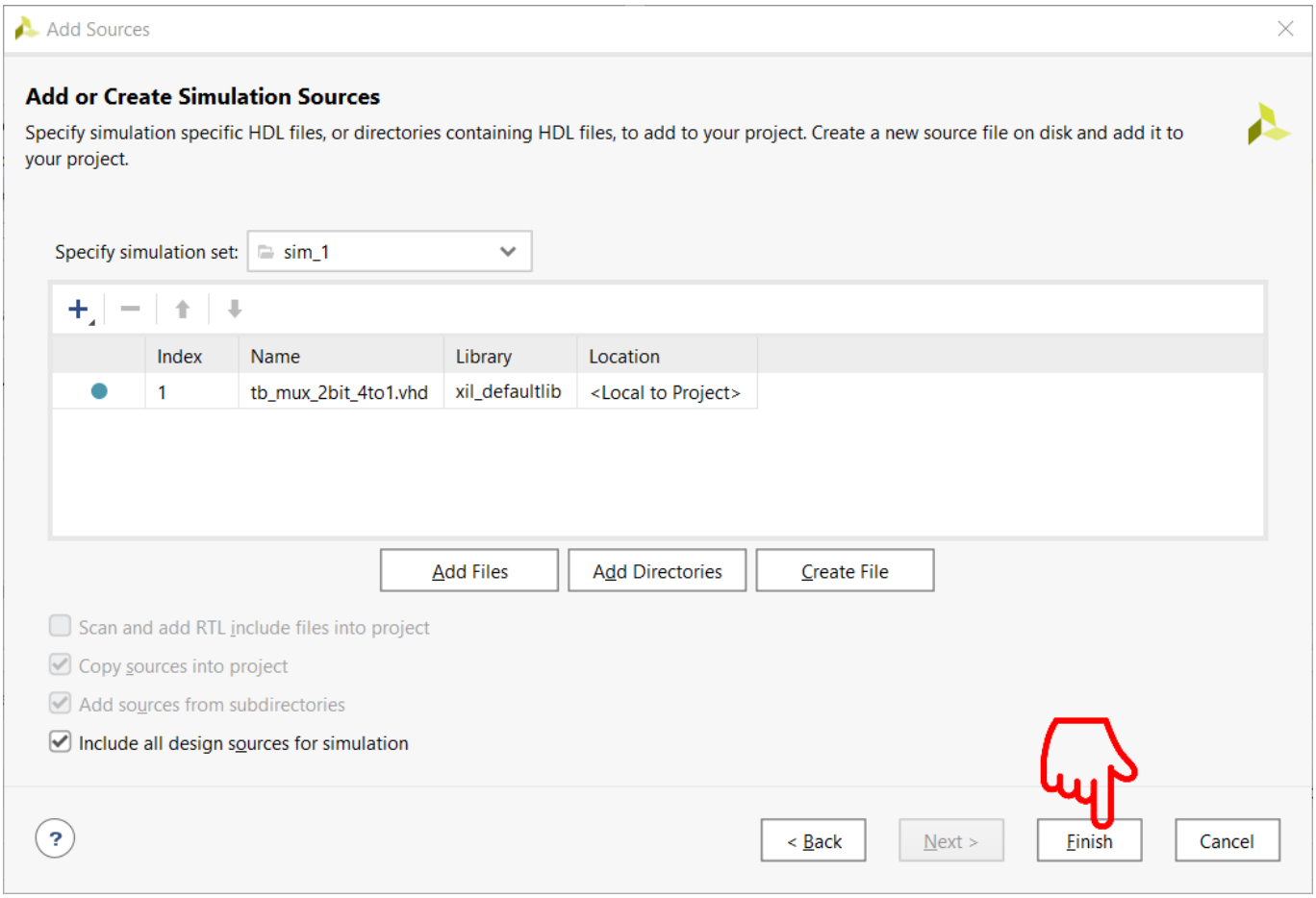
Add or Create Design Sources (v ďalších oknách vedie rovnako ako pri vytváraní projektu):



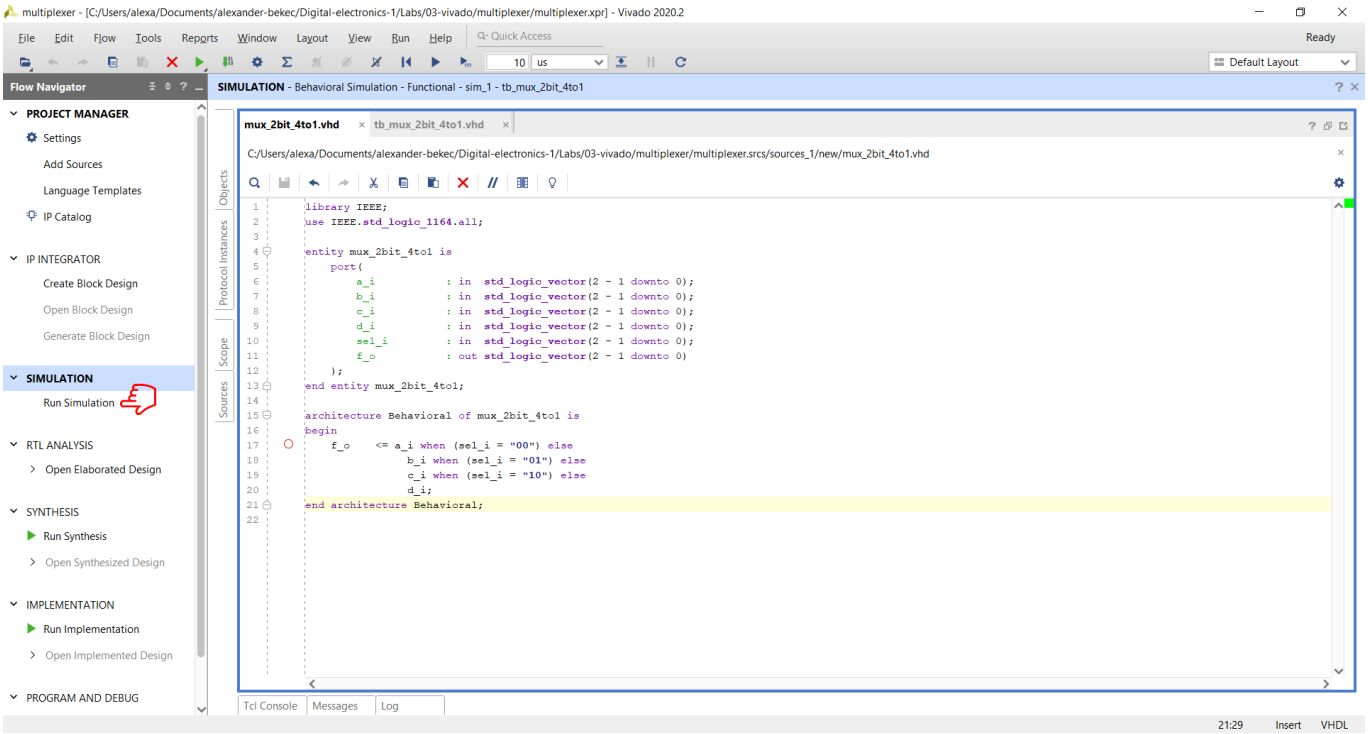
Add or Create Simulation Sources (Testbench)

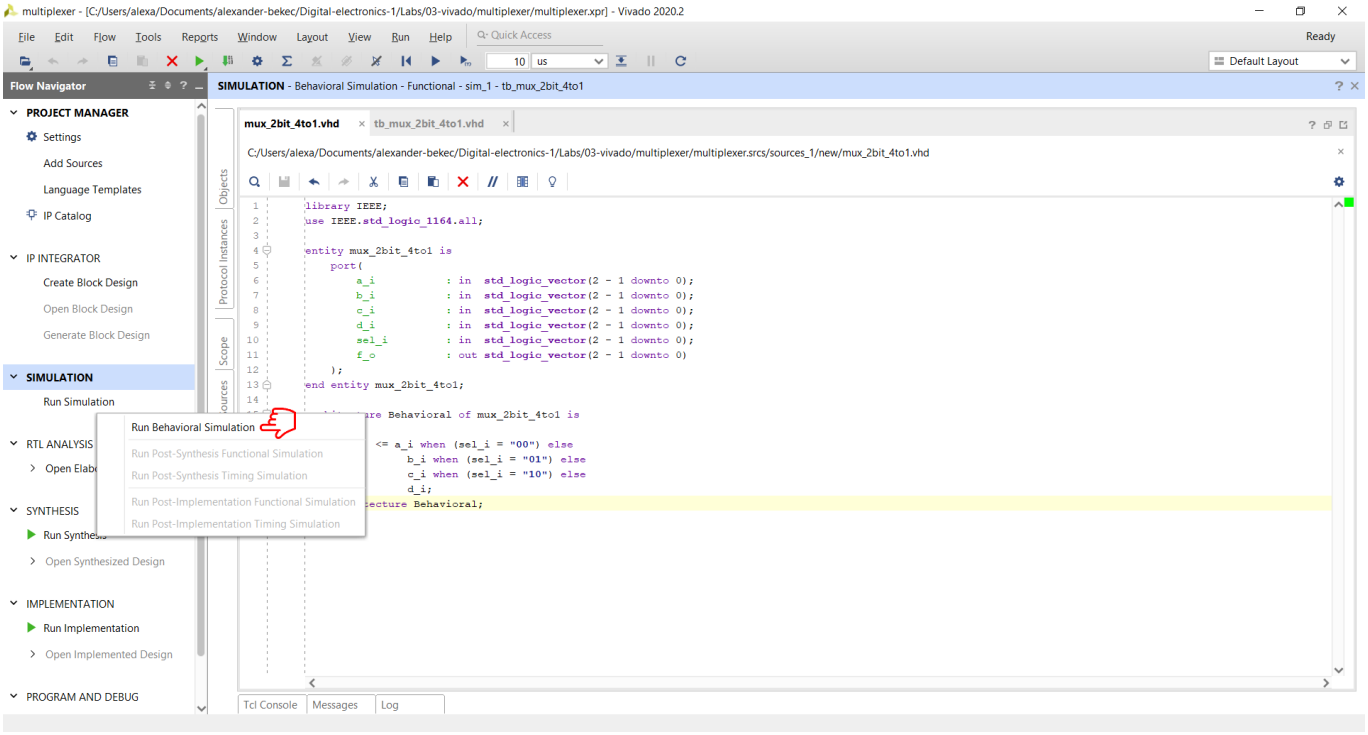

Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
tb_mux_2bit_4to1.vhd
File location:
<Local to Project>
OK
Cancel
Scan and add RTL include files into proje
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel



Run Simulation


multiplexer - [C:/Users/alexa/Documents/alexander-bekec/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_mux_2bit_4to1
mux_2bit_4to1.vhd
tb_mux_2bit_4to1.vhd
C:/Users/alexa/Documents/alexander-bekec/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.srcs/sources_1/new/mux_2bit_4to1.vhd
library IEEE;
use IEEE.std_logic_1164.all;
entity mux_2bit_4to1 is
port(
a_i : in std_logic_vector(2 - 1 downto 0);
b_i : in std_logic_vector(2 - 1 downto 0);
c_i : in std_logic_vector(2 - 1 downto 0);
d_i : in std_logic_vector(2 - 1 downto 0);
sel_i : in std_logic_vector(2 - 1 downto 0);
f_o : out std_logic_vector(2 - 1 downto 0)
);
end entity mux_2bit_4to1;
architecture Behavioral of mux_2bit_4to1 is
begin
f_o <= a_i when (sel_i = "00") else
b_i when (sel_i = "01") else
c_i when (sel_i = "10") else
d_i;
end architecture Behavioral;
Tcl Console
Messages
Log
21:29
Insert
VHDL


multiplexer - [C:/Users/alexa/Documents/alexander-bekec/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
SYNTHESIS
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_mux_2bit_4to1
mux_2bit_4to1.vhd
tb_mux_2bit_4to1.vhd
C:/Users/alexa/Documents/alexander-bekec/Digital-electronics-1/Labs/03-vivado/multiplexer/multiplexer.srcs/sources_1/new/mux_2bit_4to1.vhd
library IEEE;
use IEEE.std_logic_1164.all;
entity mux_2bit_4to1 is
port(
a_i : in std_logic_vector(2 - 1 downto 0);
b_i : in std_logic_vector(2 - 1 downto 0);
c_i : in std_logic_vector(2 - 1 downto 0);
d_i : in std_logic_vector(2 - 1 downto 0);
sel_i : in std_logic_vector(2 - 1 downto 0);
f_o : out std_logic_vector(2 - 1 downto 0)
);
end entity mux_2bit_4to1;
Tcl Console
Messages
Log