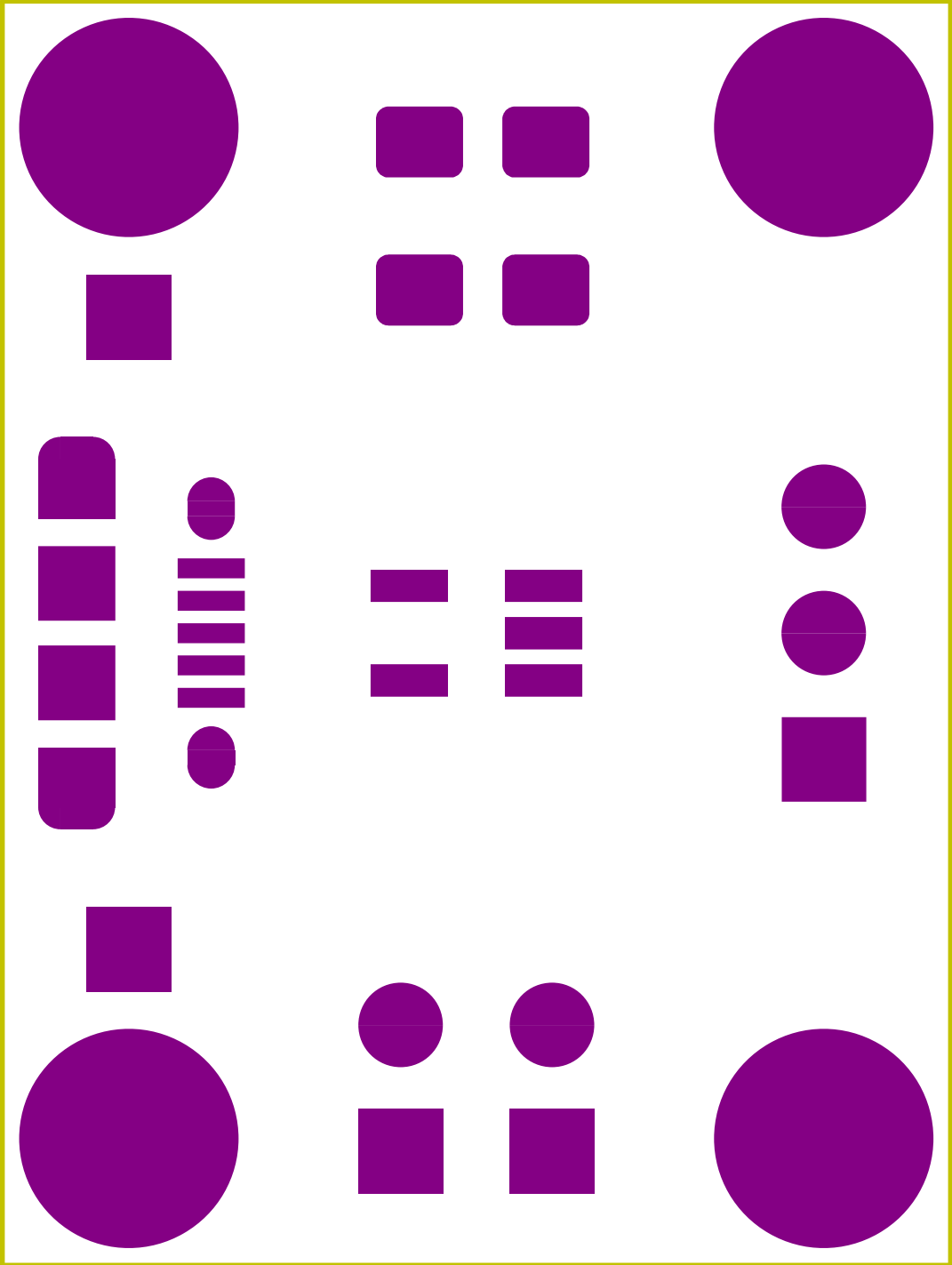
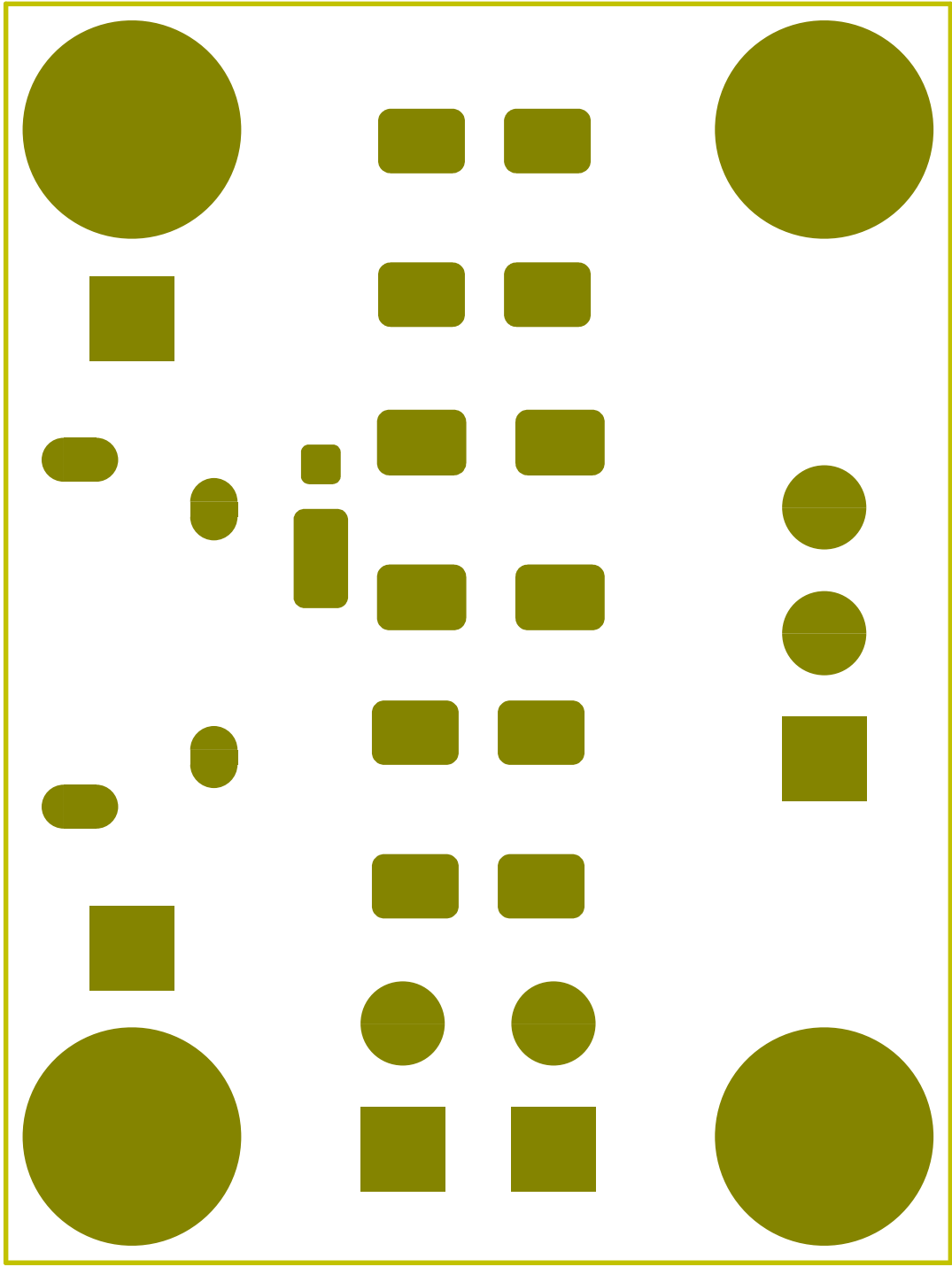


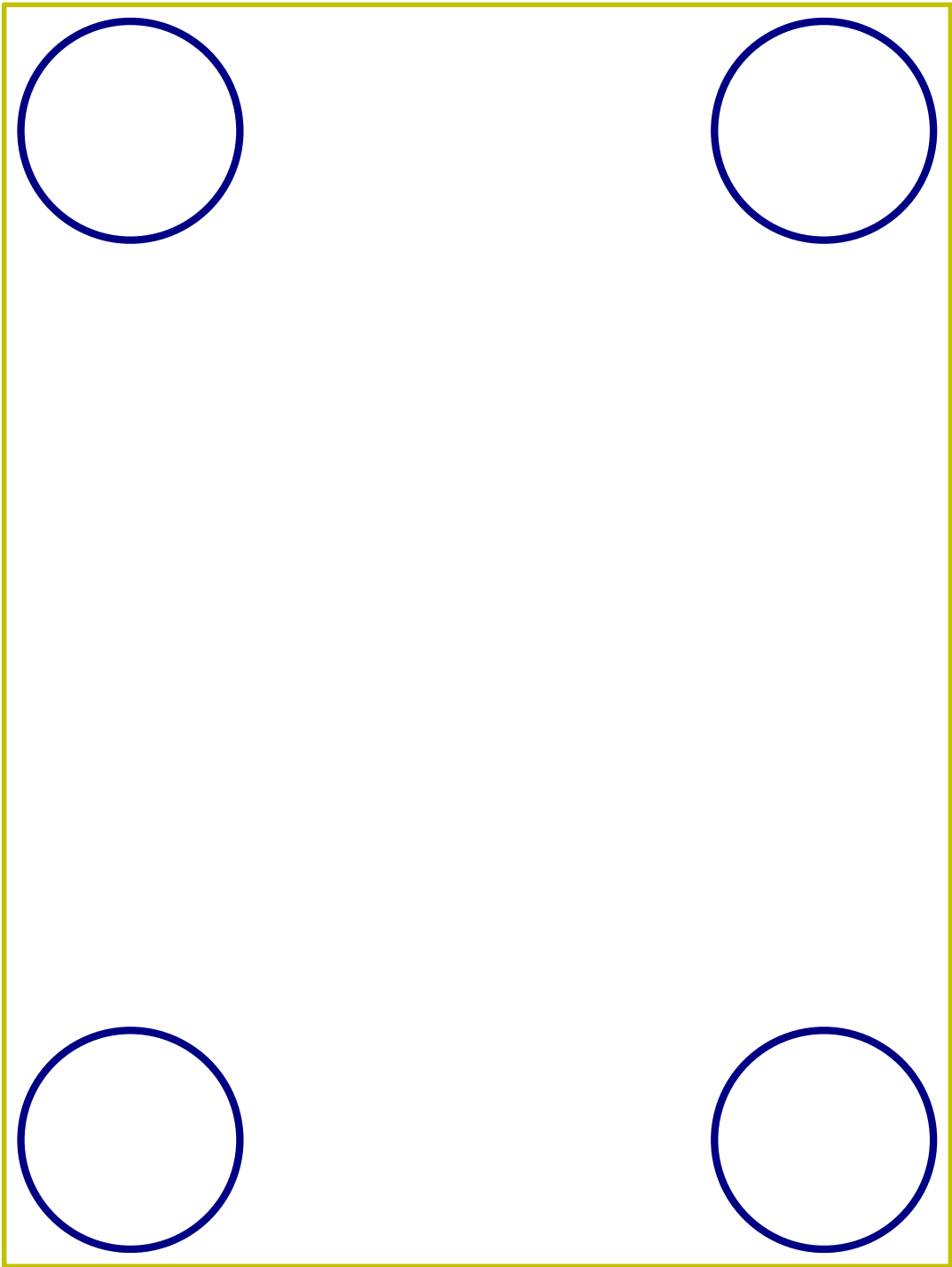
$$\begin{array}{ccccc}
 & + & + & - & \\
 \overline{B_4} & = & \overline{C_2} & = & \overline{B_1} \\
 & = & & = & \\
 \overline{B_3} & = & \overline{C_1} \boxed{\overline{\phantom{000}}} & = & \overline{B_5} \\
 & + & & & -
 \end{array}$$

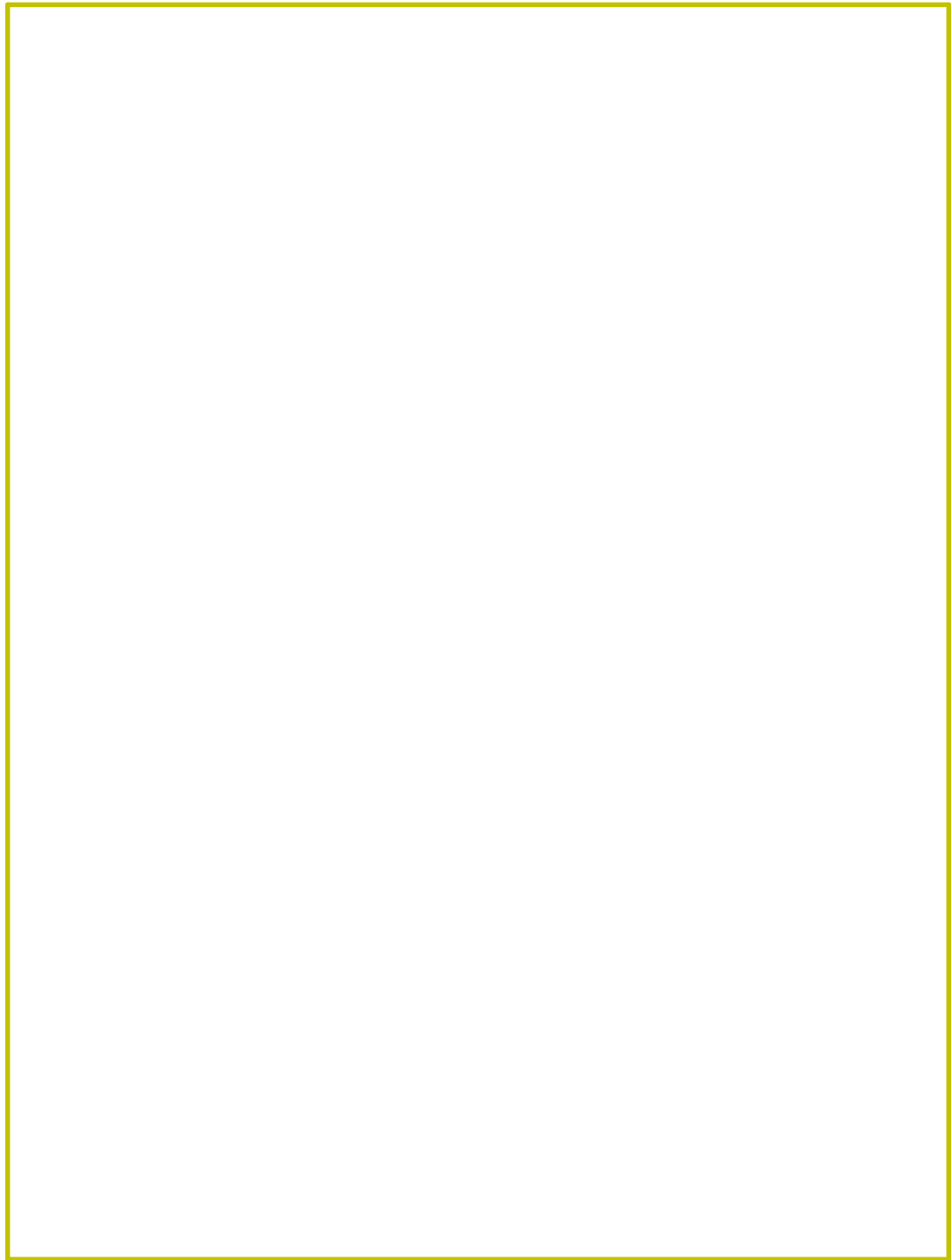


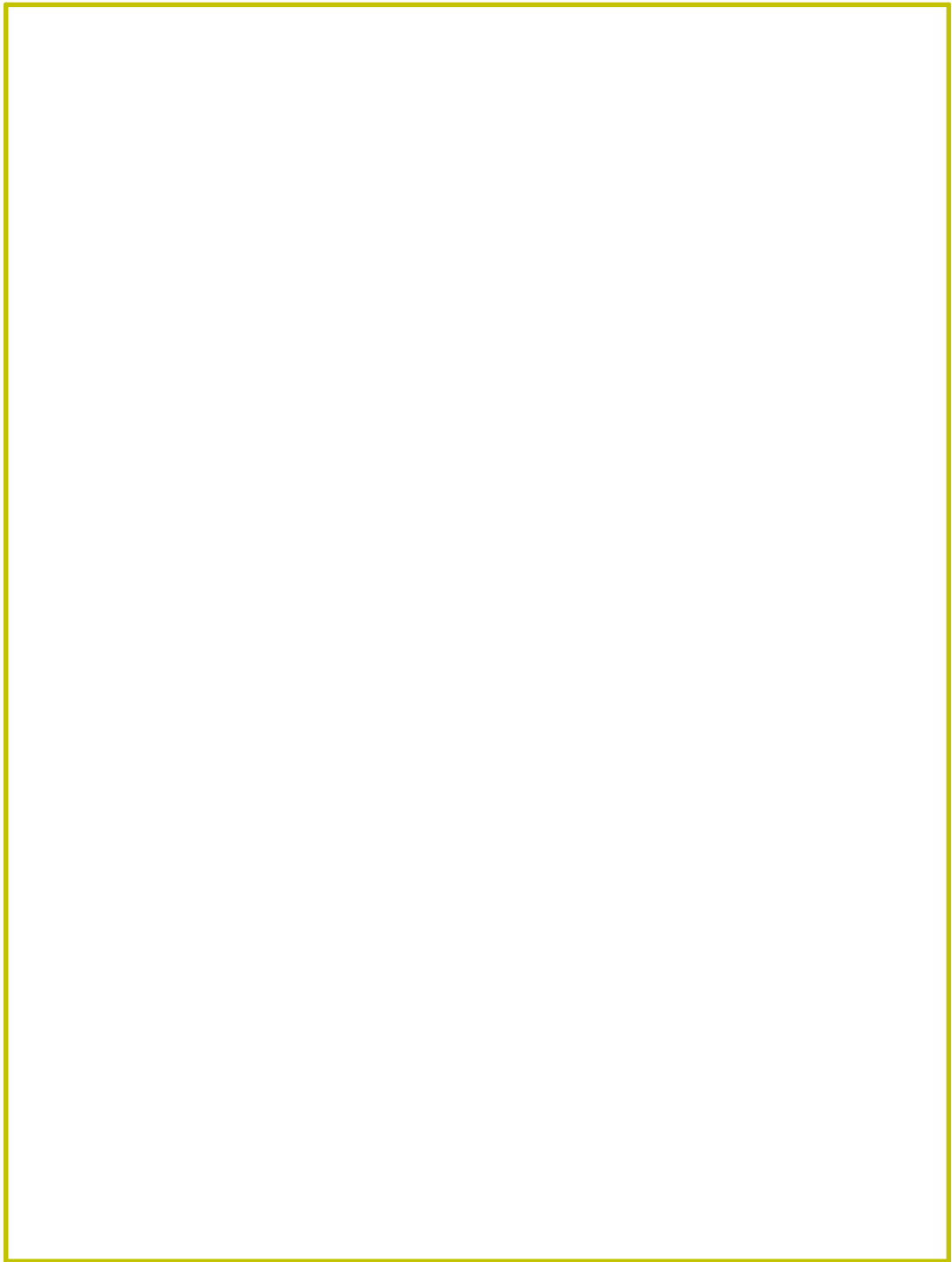


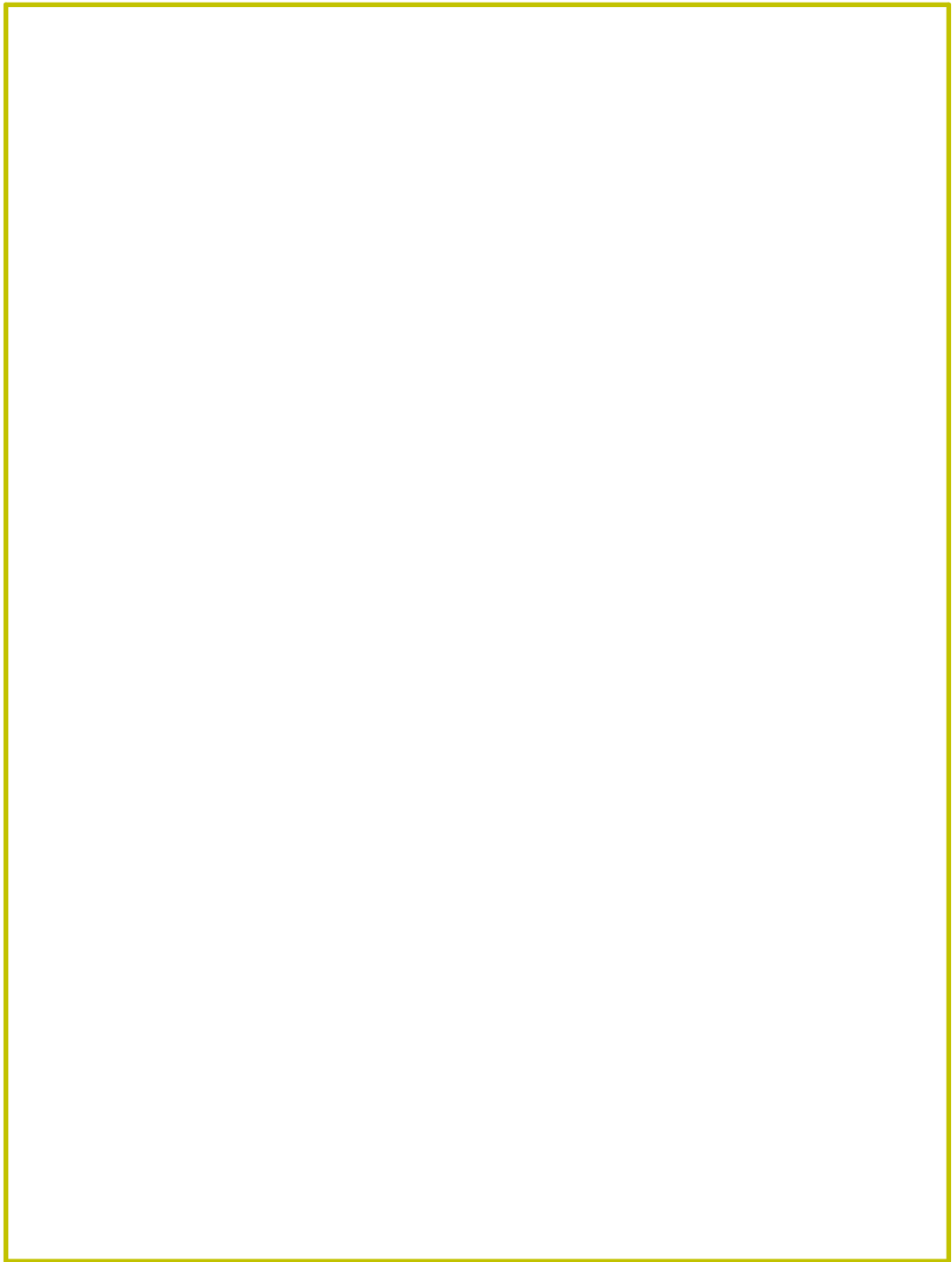


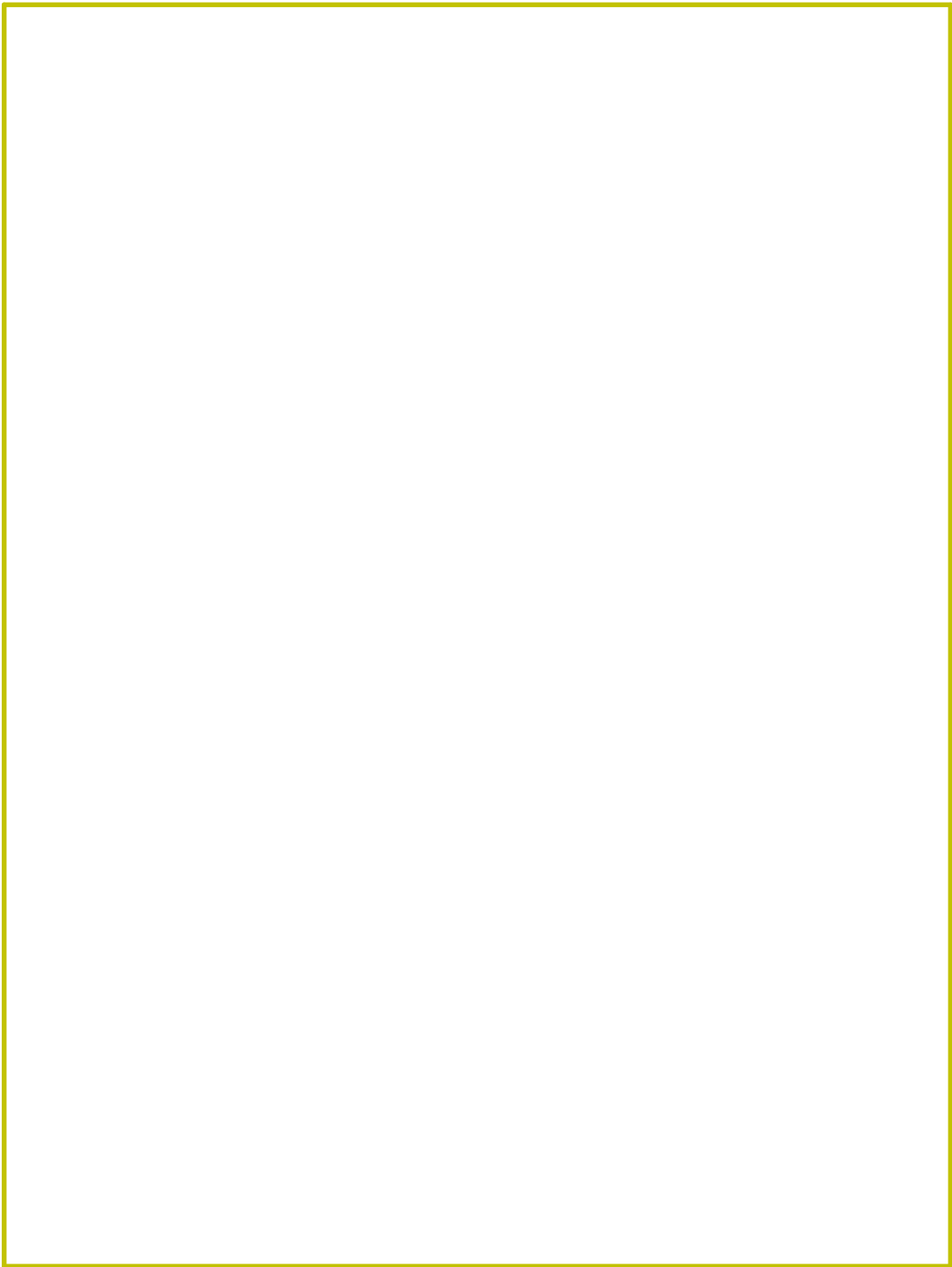
PCB Edge



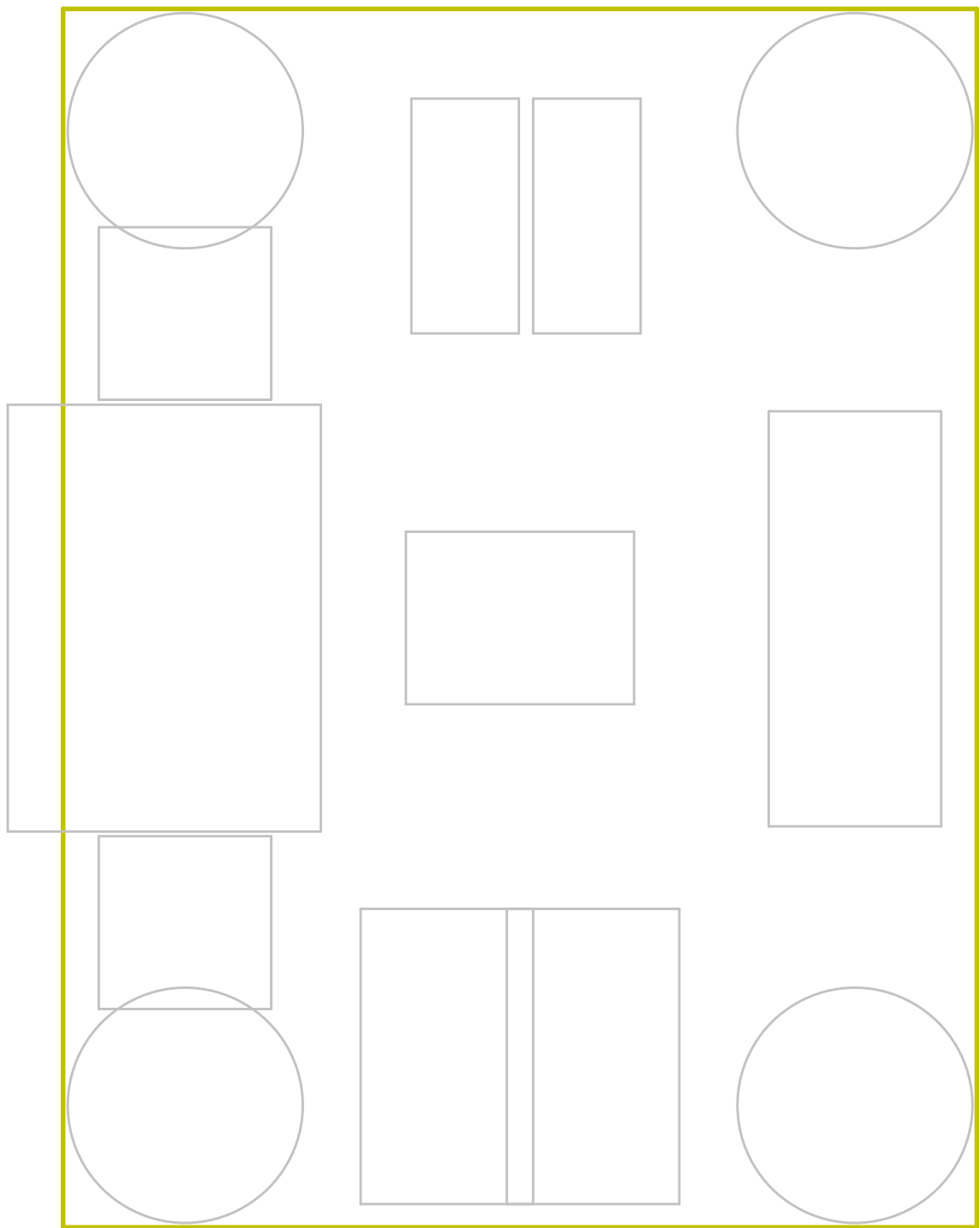


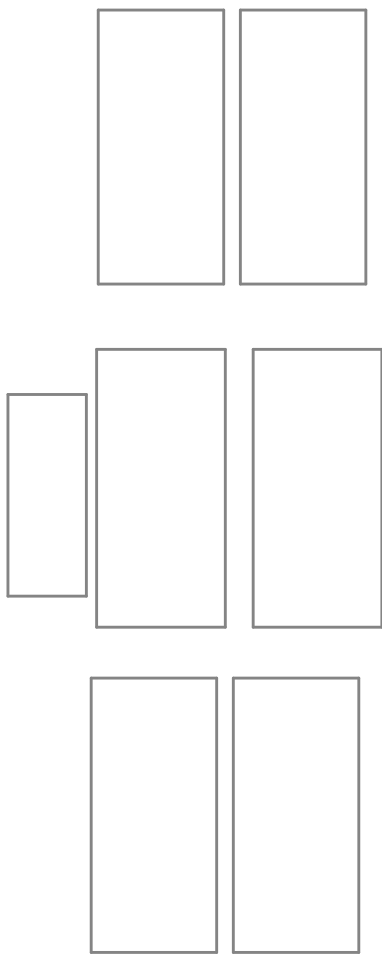


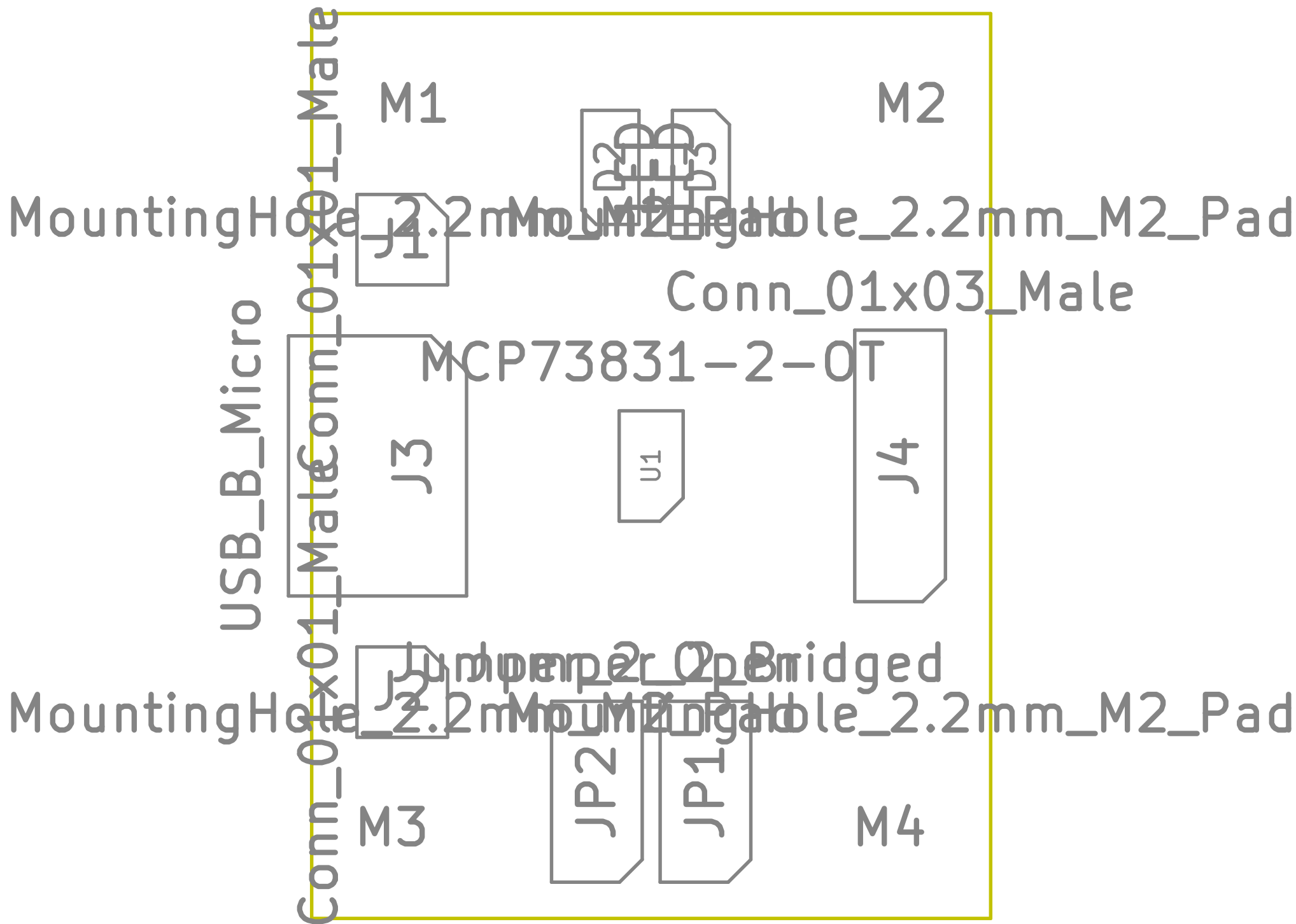












$t_{\text{LOR}}$

$R_4$

$R_3$

$t_{\text{LOR}}$

$t_{\text{LOR}}$

$t_{\text{LOR}}$

$t_{\text{LOR}}$

$t_{\text{LOR}}$

SK

$t_{\text{LOR}}$

$R_5$