# RL78/G13

## Low-power Consumption Operation

R01AN0465EJ0100
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## Introduction

This application note describes general methods of reducing power consumption and methods of setting the low-power consumption functions of the RL78/G13. It also describes how to set the CPU/peripheral hardware clock and how to reduce power consumption by using the HALT and STOP modes.

## Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

## Contents

## 1. Specifications

The sample program covered in this application note switches operation modes by a switch input. The operation modes to be set are normal operation mode, HALT mode, and STOP mode in which the RL78/G13 operates with the high-speed on-chip oscillator clock, and normal operation mode and HALT mode (referred to as sub-HALT mode) in which the RL78/G13 operates with the subsystem clock.

Table 1.1 lists a peripheral function to be used and it uses. Figure 1.1 shows an overview of sample code operation. Table 1.2 lists the operations of the sample code in each operation mode.

**Table 1.1 Peripheral Function to be Used and its Use**

| Peripheral Function | Use |
|---|---|
| INTP0 | Switch input |

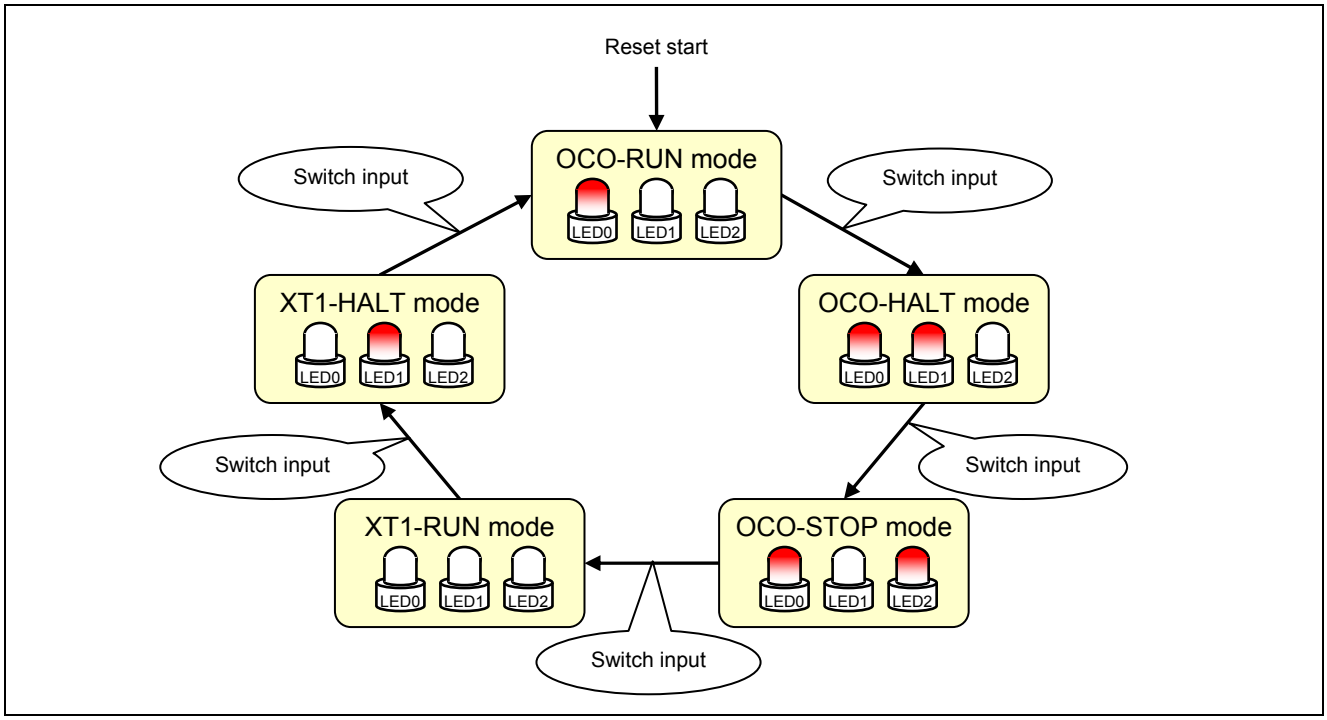


**Figure 1.1 Overview of Sample Code Operation**

**Table 1.2 Operation of Sample Code in Each Operation Mode**

| Operation Mode | CPU/Peripheral Hardware Clock ($f_{CLK}$) | Operation | LED Indication | | |
|---|---|---|---|---|---|
| | | | LED0 | LED1 | LED2 |
| OCO-RUN | High-speed on-chip oscillator clock ($f_{IH}$) Note 1 | Normal operation | On | Off | Off |
| OCO-HALT | High-speed on-chip oscillator clock ($f_{IH}$) Note 1 | HALT mode | On | On | Off |
| OCO-STOP | High-speed on-chip oscillator clock ($f_{IH}$) Note 1 | STOP mode | On | Off | On |
| XT1-RUN | Subsystem clock ($f_{SUB}$) Note 2 | Normal operation | Off | Off | Off |
| XT1-HALT | Subsystem clock ($f_{SUB}$) Note 2 | Sub-HALT mode | Off | On | Off |

Notes: 1. The frequency of the high-speed on-chip oscillator is set to 1 MHz. The flash operation mode is set to LS (low-speed main).
2. The oscillation mode of the XT1 oscillator is set to ultra-low power consumption oscillation (oscillation margin: small).

## 1.1 General Methods for Reducing Power Consumption

The following are general methods for reducing power that microcontrollers consume:

(1) Use of standby mode

(2) Selection of standby mode suitable for processing

(3) Use of an appropriate oscillator and its oscillation frequency

(4) Processing of unused ports

**(1) Use of standby mode**

The operation modes of a microcontroller is classified roughly into two groups: normal operation mode, in which the microcontroller executes programs, and standby mode, to which the microcontroller can transition when it does not need to execute programs.

In many applications, the microcontrollers do not always have to execute programs. They wait for signal to be input externally and for time to elapse with a timer. The consumption power is reduced by switching from normal operation mode to standby mode.

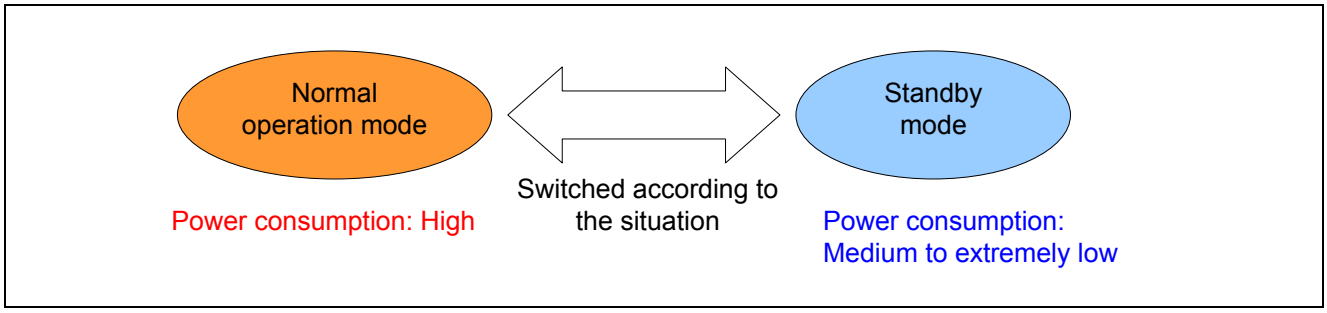


**Figure 1.2 Basic Operation Mode of Microcontrollers**

The RL78/G13 microcontroller has the following four standby modes:

- (1) HALT mode: The CPU operation clock is stopped. The main system clock is supplied to the peripheral hardware. (Power consumption is medium)
- (2) Sub-HALT mode: The CPU operation clock is stopped. The subsystem clock is supplied to the peripheral hardware. (Power consumption is low to extremely low)
- (3) STOP mode: The main system clock is stopped. The subsystem clock retains the status before STOP mode was set. (Power consumption is extremely low)
- (4) SNOOZE mode Note: Specific peripheral hardware can operate. (Power consumption is medium to extremely low)

Note: It depends on the peripheral hardware that operates.

Remarks: The SNOOZE mode is available only when the high-speed on-chip oscillator clock is used. After the STOP mode is exited due to the occurrence of a specified trigger, it is possible to perform A/D conversion, slave reception via the CSI00, and data reception via the UART0, without operating the CPU. This mode reduces power consumption because the CPU is in STOP mode when it is idling.
A similar function is the wakeup function of the IICA. This function can set the STOP mode until the IICA is specified as a slave device by the master and thus reduces power consumption of the system. For details, refer to the following application note: Serial Interface IICA (for Slave Transmission/Reception) (document No. R01AN0463E).

Figure 1.3 shows the status of the normal operation mode and standby mode.

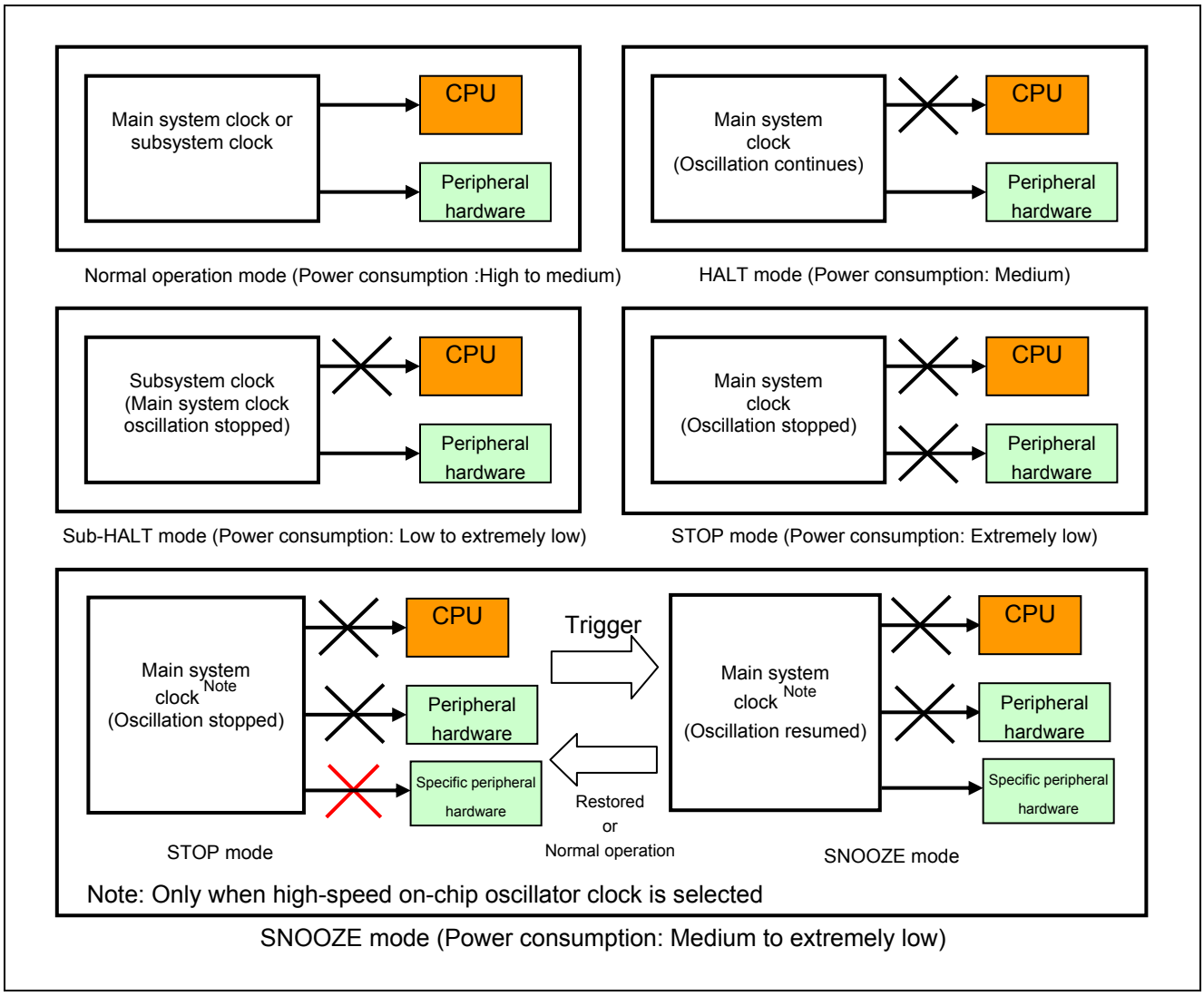


**Figure 1.3 Operation Mode Status**

Each operation mode is overviewed as follows.

1) HALT mode

In the HALT mode, the clock is not supplied to the CPU, but supplied to the peripheral hardware. Therefore, power consumption is not significantly reduced. However, this mode has advantages that the peripheral functions can continue to operate and that the CPU can operate immediately after this mode is exited.

2) Sub-HALT mode

The transition to the sub-HALT mode is possible if the main system clock is stopped and a HALT instruction is executed during execution of program in the subsystem clock. Power consumption in this mode is reduced more than in the HALT mode, in which the main system clock is supplied. The real-time counter and timers can continue to operate because the subsystem clock is supplied to the peripheral hardware. The processing speed of the peripheral hardware in the sub-HALT mode, which uses the subsystem clock, is slower than in HALT mode, which uses the main system clock.

3) STOP mode

Because the main system clock is stopped in this mode, power consumption can be reduced more than in the HALT mode. Because the clock to the peripheral hardware is also stopped, the peripheral hardware that can operate in this mode is limited. It is necessary to keep the oscillation stabilization time of the main system clock after the STOP mode is exited. The subsystem clock, which retains the status before the STOP mode was set, can operate the real-time counter and other timers. In addition, the data stored in the on-chip RAM is retained in this mode.

4) SNOOZE mode

In the SNOOZE mode, specific peripheral hardware can operate in addition to the peripheral hardware that can operate in the STOP mode. It is possible to perform A/D conversion, slave reception via the CSI00, and data reception via the UART0, without operating the CPU. This mode contributes to power consumption reduction because the CPU is in STOP mode when it is idling.

This mode can be specified only when the high-speed on-chip oscillator is selected as the CPU/peripheral hardware clock ($f_{CLK}$).

For a detailed description of the SNOOZE mode, refer to the following application note:

- RL78/G13 Low-power Consumption (SNOOZE Mode UART) (R01AN0742E) Application Note

Table 1.3 summarizes the features of the standby modes.

**Table 1.3 Features of Standby Modes**

| Standby Mode | Peripheral Hardware | Power Consumption | Restoration from Standby Mode |
|---|---|---|---|
| HALT mode | Enabled | Medium | High speed |
| Sub-HALT mode | Enabled Note | Low to extremely low | Low speed |
| STOP mode | Mostly stopped | Extremely low | Medium speed (dependent on clock selected) |
| SNOOZE mode | Mostly stopped | Medium to extremely low | Medium speed |

Note. The peripheral hardware that cannot operate with the subsystem clock cannot be used in the sub-HALT mode.

**(2) Selection of standby mode suitable for processing**

The standby modes that the RL78/G13 supports are the HALT, sub-HALT, STOP, and SNOOZE modes. It is essential that the most suitable standby mode be selected according to the operating environment of the system.

1) To restore from standby mode quickly

Use the HALT mode in which the CPU can quickly restore from the standby mode. Depending on the clock used, the STOP mode may be able to be used. Select a standby mode according to the system (time required to restore from STOP mode: ceramic resonator = tens of μs to hundreds of μs, high-speed on-chip oscillator = 30 μs).

2) To operate the peripheral hardware in a standby mode

Carefully operate the peripheral hardware during the standby period. The STOP mode can be used in addition to the HALT and sub-HALT mode in the following cases:

- Using only the peripheral hardware, such as RTC and timers, that can operate with the subsystem clock alone
- Using as an IICA0 slave device (using the wakeup function)
- Using CSI00 slave reception or UART0 data reception (9600 bps max.) (using the SNOOZE mode)
- Monitoring the analog signals for A/D (using the SNOOZE mode)

3) To switch between the standby mode and the normal operation mode

It is necessary to consider the average power consumption of the system. Determine the operation mode while considering the period during which the CPU is in the standby status and its power consumption and the period during which the CPU is in the normal operation status and its power consumption. Generally, the STOP mode which consumes the least power is effective when the CPU stays in the standby status for a long period of time, the HALT mode which requires the shortest time to restore from the standby status is effective when the CPU exits the standby status frequently, and the sub-HALT mode which does not use the main system clock is effective when the system load is minimum.

Table 1.4 summarizes the above description.

**Table 1.4 Applications and Suitable Standby Modes**

| Application | Suitable Standby Mode |
|---|---|
| Applications that switch between normal and standby modes periodically<br>(applications that stay longer in the standby status) | STOP mode |
| Applications that switch between normal and standby modes frequently<br>(applications that require quick restoration from the standby status) | HALT mode |
| Applications that impose less load on the system | Sub-HALT mode |
| Applications that perform communication during the standby period | HALT or SNOOZE mode |

Note: It is assumed that there is no problem with the peripheral hardware to be used in any mode.

**(3) Use of an appropriate oscillator and its oscillation frequency**

The crystal resonator has characteristics of excellent frequency accuracy and long oscillation stabilization time. Because it consumes power even during the oscillation stabilization period, it consumes more power as its oscillation stabilization time gets longer, which is the major demerit of the crystal resonator. For applications in which the frequency accuracy is not significant, the oscillation stabilization time of the oscillator can be reduced by using the ceramic resonator or high-speed on-chip oscillator. As a result, the power consumption of the system can also be reduced.

The ceramic resonator is inferior to the crystal resonator in the frequency accuracy and has a shorter oscillation stabilization time, which leads to power consumption reduction.

The high-speed on-chip oscillator is inferior to the ceramic resonator in the frequency accuracy. However, the high-speed on-chip oscillator can reduce power consumption more than the ceramic resonator. In addition, the high-speed on-chip oscillator dispenses with an external resonator, leading to reduction of system production cost. Table 1.5 summarizes the features of the above-mentioned clocks.

Power consumption is proportional to the operating frequency of the CPU. For applications in which the CPU's processing speed is not important, the power consumption of the system can be reduced by lowering the operating frequency of the CPU.

**Table 1.5 Features of the Clocks**

| | Oscillation Frequency Accuracy | Oscillation Stabilization Time |
|---|---|---|
| Crystal resonator | Very high (about 0.001%) | Long (several ms to tens of ms) |
| Ceramic resonator | Lower than the crystal resonator (about 0.5%) | Short (tens of µs to hundreds of µs) |
| High-speed on-chip oscillator | Lower than the ceramic resonator (about 1%) | Short (30 µs max.) |

## 1.2 Power Consumption Reduction Functions Specific to the RL78/G13

The RL78/G13 has a function of reducing its power consumption. This section describes that function and the procedure for setting it.

**(1) Stopping the supply of the clock to unused peripheral hardware**

Specify whether to supply the clock to peripheral hardware by setting the peripheral enable register 0 (PER0). Power consumption and noise can be reduced by stopping the supply of the clock signal to unused hardware.
Figure 1.4 shows the format of the peripheral enable register. Figure 1.5 shows a function overview of this register.

Address: F00F0H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PER0 | RTCEN | IICA1EN | ADCEN | IICA0EN | SAU1EN | SAU0EN | TAU1EN | TAU0EN |

| TAUnEN | Control of timer array unit n input clock supply |
|---|---|
| 0 | Stops input clock supply.<br>• SFR used by the timer array unit n cannot be written.<br>• The timer array unit n is in the reset status. |
| 1 | Enables input clock supply.<br>• SFR used by the timer array unit n cannot be read and written. |

| SAUnEN | Control of serial array unit n input clock supply |
|---|---|
| 0 | Stops input clock supply.<br>• SFR used by the serial array unit n cannot be written.<br>• The serial array unit n is in the reset status. |
| 1 | Enables input clock supply.<br>• SFR used by the serial array unit n cannot be read and written. |

| IICAnEN | Control of serial interface IICAn input clock supply |
|---|---|
| 0 | Stops input clock supply.<br>• SFR used by the serial interface IICAn cannot be written.<br>• The serial interface IICAn is in the reset status. |
| 1 | Enables input clock supply.<br>• SFR used by the serial interface IICAn cannot be read and written. |

| ADCEN | Control of A/D converter input clock supply |
|---|---|
| 0 | Stops input clock supply.<br>• SFR used by the A/D converter cannot be written.<br>• The A/D converter is in the reset status. |
| 1 | Enables input clock supply.<br>• SFR used by the A/D converter cannot be read and written. |

| RTCEN | Control of real-time clock (RTC) and 12-bit interval timer input clock supply Note |
|---|---|
| 0 | Stops input clock supply.<br>• SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written.<br>• The real-time clock (RTC) and 12-bit interval timer are in the reset status. |
| 1 | Enables input clock supply.<br>• SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be read and written. |

Note: The input clock that can be controlled through RTCEN is used by the CPU to access the real-time counter (RTC). RTCEN cannot be used to control the supply the clock ($f_{SUB}$) to drive the real-time counter.

**Figure 1.4 Format of Peripheral Enable Register 0 (PER0)**

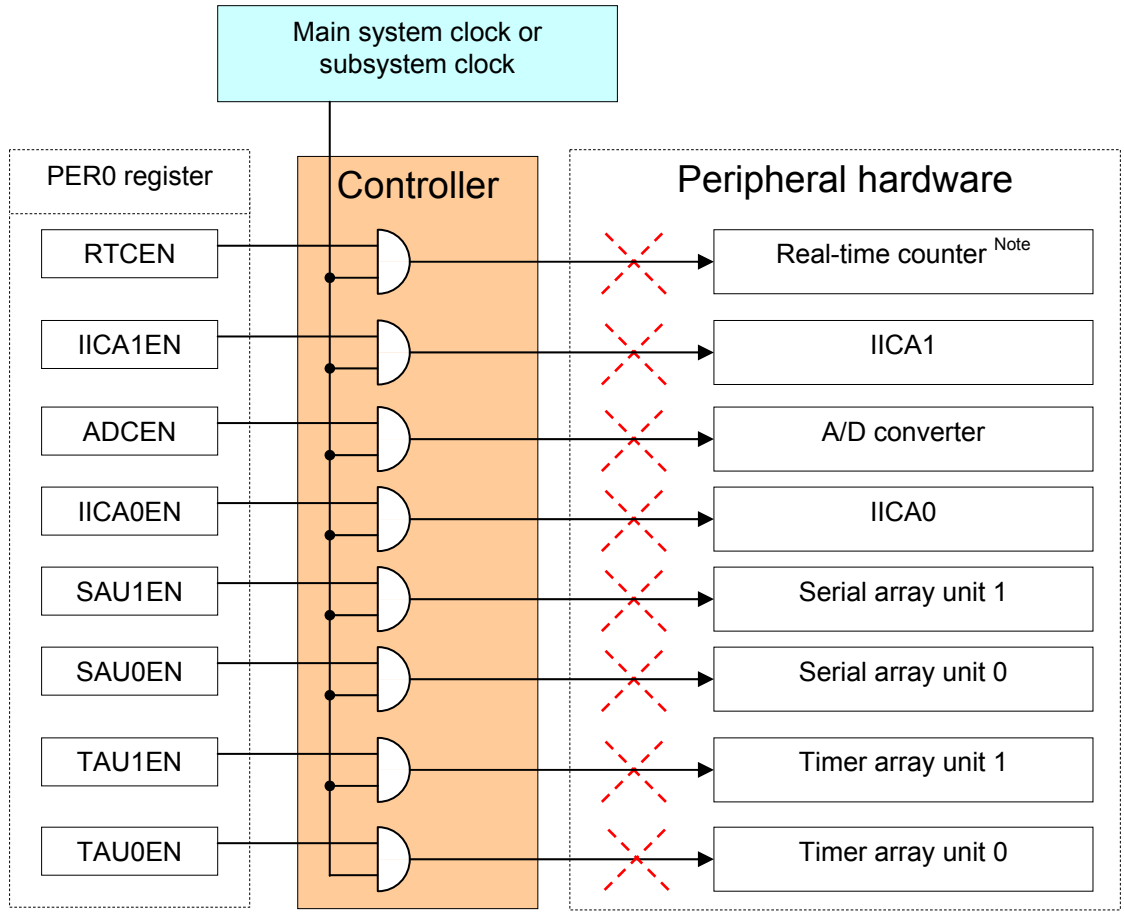


**Figure 1.5 Function Overview of the Peripheral Enable Register**

**(2) Setting in STOP and HALT modes while subsystem clock is selected as CPU clock**

This register is used to reduce power consumption by stopping as many unnecessary clock functions as possible.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions, except the real-time clock and interval timer, is stopped in the STOP and HALT modes while the subsystem clock is selected as CPU clock. Set the RTCLPC bit to 1 to operate only the real-time clock and 12-bit interval timer on the subsystem clock (ultra-low power operation) in the STOP and sub-HALT modes. Set bit 7 (RTCEN) of the peripheral enable registers 0 (PER0) and 1 before this setting.

Figure 1.6 shows the format of the operation speed mode control register.

Address: F00F3H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| OSMC | RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |

| WUTMMCK0 | Selection of operation clock for real-time clock and 12-bit interval timer |
|---|---|
| 0 | Subsystem clock |
| 1 | Low-speed on-chip oscillator clock |

| RTCLPC | Setting in STOP and HALT modes while subsystem clock is selected as CPU clock |
|---|---|
| 0 | Enables supply of subsystem clock to peripheral functions. |
| 1 | Stops supply of subsystem clock to peripheral functions other than real-time clock and 12-bit interval timer. |

**Figure 1.6 Format of Operation Speed Mode Control Register (OSMC)**

**(3) Controlling the regulator output voltage**

The RL78/G13 includes a circuit for operating the device at a constant voltage. The regulator output voltage is 2.1 V (typ.) in normal operation mode and 1.8 V (typ.) in low power consumption mode.

Table 1.6 lists the output voltage conditions of the regulator.

**Table 1.6 Regulator Output Voltage Conditions**

| Mode | Output Voltage | Condition |
|---|---|---|
| Low voltage main mode | 1.8 V | — |
| Low-speed main mode | | |
| High-speed main mode | 1.8 V | In STOP mode |
| | | When both the high-speed system clock ($f_{MX}$) and high-speed on-chip oscillator clock ($f_{IH}$) are stopped during CPU operation with the subsystem clock ($f_{XT}$). |
| | | When both the high-speed system clock ($f_{MX}$) and high-speed on-chip oscillator clock ($f_{IH}$) are stopped during the HALT mode when the CPU operation with the subsystem clock ($f_{XT}$) has been set. |
| | 2.1 V | Other than above (include during on-chip debugging mode) Note |

Note: In transition to the subsystem clock operation or the STOP mode during the on-chip debugging, the regulator output voltage is kept at 2.1 V (not decline to 1.8 V).

**(4) Setting of flash operation mode**

The RL78/G13 allows the flash operation mode to be selected. Power consumption can be reduced by selecting the appropriate flash operation mode according to the power voltage ($V_{DD}$) and CPU operating frequency using bits 7 and 6 of the option byte (000C2H).

Figure 1.7 shows the format of the option byte (000C2H).

Address: 000C2H/010C2H Note

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CMODE1 | CMODE0 | 1 | 0 | FRQSEL3 | FRQSEL2 | FRQSEL1 | FRQSEL0 |

| FRQSEL3 | FRQSEL2 | FRQSEL1 | FRQSEL0 | Frequency of the high-speed on-chip oscillator |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 32 MHz |
| 0 | 0 | 0 | 0 | 24 MHz |
| 1 | 0 | 0 | 1 | 16 MHz |
| 0 | 0 | 0 | 1 | 12 MHz |
| 1 | 0 | 1 | 0 | 8 MHz |
| 1 | 0 | 1 | 1 | 4 MHz |
| 1 | 1 | 0 | 1 | 1 MHz |
| Other than above | | | | Setting prohibited |

| CMODE1 | CMODE0 | Setting of flash operation mode | | |
|---|---|---|---|---|
| | | | Operating Frequency Range | Operating Voltage Range |
| 0 | 0 | LV (low-voltage main) mode | 1 MHz to 4 MHz | 1.6 V to 5.5 V |
| 1 | 0 | LS (low-speed main) mode | 1 MHz to 8 MHz | 1.8 V to 5.5 V |
| 1 | 1 | HS (high-speed main) mode | 1 MHz to 16 MHz | 2.4 V to 5.5 V |
| | | | 1 MHz to 32 MHz | 2.7 V to 5.5 V |
| Other than above | | Setting prohibited | | |

Note: Set the same value in 000C2H and 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

**Figure 1.7 Format of Option Byte (000C2H/010C2H)**

**(5) Subsystem clock ultra-low power consumption oscillation mode**

The RL78/G13 incorporates a subsystem clock oscillator circuit that consumes less power than the conventional products. Power consumption of the device can further be reduced by setting the XT1 oscillator to ultra-low power consumption oscillation mode through the clock operation mode control register (CMC).

Figure 1.8 shows the format of the clock operation mode control register.

Address: FFFA0H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CMC | EXCLK | OSCSEL | EXCLKS | OSC SELS | 0 | AMPHS1 | AMPHS0 | AMPH |

| AMPHS1 | AMPHS0 | XT1 oscillator oscillation mode selection Note | |
|---|---|---|---|
| 0 | 0 | Low power consumption oscillation mode (default) | Oscillation margin: Medium |
| 0 | 1 | Normal oscillation | Oscillation margin: Large |
| 1 | 0 | Ultra-low power consumption oscillation | Oscillation margin: Small |
| 1 | 1 | Setting prohibited | |

Note: As the XT oscillator becomes oscillation mode with lower power consumption, its oscillation margin becomes smaller.

Cautions:
1. The CMC register can be written only once after reset release, by an eight-bit memory manipulation instruction.
2. After reset release, set the CMC register before X1 or XT1 oscillation is started as set by the clock operation status control register (CSC).
3. Set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.
4. When the CMC register is used at the default (00H), set 00H in this register after reset release to prevent malfunctioning during a program loop.

**Figure 1.8 Format of Clock Operation Mode Control Register (CMC)**

Table 1.7 shows a list of the power consumption reduction functions specific to the RL78/G13.

**Table 1.7 List of Power Consumption Reduction Functions Specific to the RL78/G13**

| Power Consumption Reduction Method | Register to be Set |
|---|---|
| Stopping the supply of the clock to unused peripheral hardware | Peripheral enable register 0 (PER0) |
| Setting in using the STOP mode, or the HALT mode when the CPU is operating with the subsystem clock | Operation speed mode control register (OSMC) |
| Reduction of the regulator output voltage | — |
| Setting of flash operation mode | Option byte (000C2H/010C2H) |
| Subsystem clock ultra-low power consumption oscillation mode | Clock operation mode control register (CMC) |

## 2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

**Table 2.1 Operation Check Conditions**

| Item | Description |
|---|---|
| Microcontroller used | RL78/G13 (R5F100LEA) |
| Operating frequency | • High-speed on-chip oscillator (HOCO) clock: 1 MHz<br>• Subsystem clock: 32.768 kHz<br>• CPU/peripheral hardware clock: 1 MHz/32.768 kHz Note |
| Operating voltage | 5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.)<br>LVD operation ($V_{LVI}$): Reset mode which uses 2.81 V (2.76 V to 2.87 V) |
| Integrated development environment | CubeSuite+ V1.00.01 from Renesas Electronics Corp. |
| C compiler | CA78K0R V1.20 from Renesas Electronics Corp. |

Note: The CPU/peripheral hardware clock setting is switched according to the operation mode of the application.

## 3. Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G13 Initialization (R01AN0451E) Application Note

# 4. Description of the Hardware

## 4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

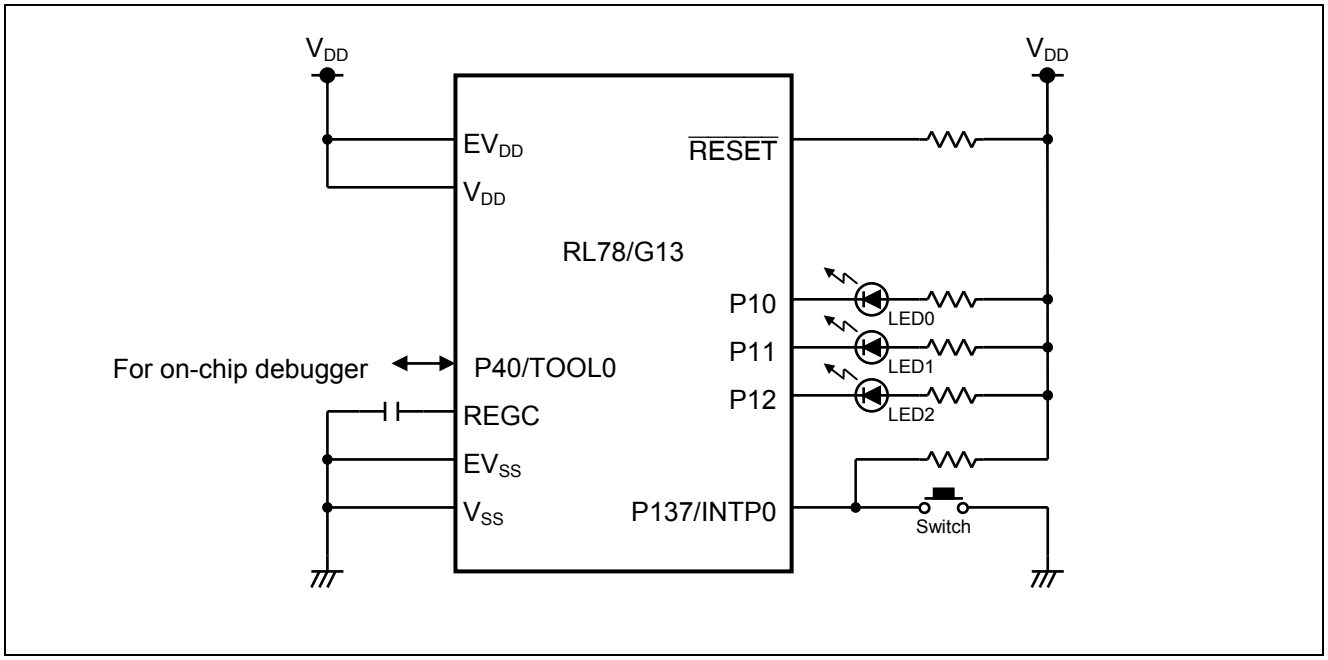


**Figure 4.1 Hardware Configuration**

Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to $V_{DD}$ or $V_{SS}$ via a resistor).
2. Connect any pins whose name begins with $EV_{SS}$ to $V_{SS}$ and any pins whose name begins with $EV_{DD}$ to $V_{DD}$, respectively.
3. $V_{DD}$ must be held at not lower than the reset release voltage ($V_{LVI}$) that is specified as LVD.

## 4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

**Table 4.1 Pins to be Used and Their Functions**

| Pin Name | I/O | Description |
|---|---|---|
| P10 | Output | LED0 lighting control port |
| P11 | Output | LED1 lighting control port |
| P12 | Output | LED2 lighting control port |
| P137/INTP0 | Input | Switch input port |

# 5. Description of the Software

## 5.1 Operation Outline

The sample program covered in this application note has five operation modes which are selected by a switch input. The operation modes are switched in the following order by each switch input: (1), (2), (3), (4), (5), and (1) ….

(1) OCO-RUN mode : High-speed on-chip oscillator operation, normal operation mode
(2) OCO-HALT mode : High-speed on-chip oscillator operation, HALT mode
(3) OCO-STOP mode : High-speed on-chip oscillator operation, STOP mode
(4) XT1-RUN mode : Subsystem clock operation, normal operation mode
(5) XT1-HALT mode : Subsystem clock operation, HALT mode (sub-HALT mode)

(1) Initialize the clock generator.

<Conditions for setting>

- Set the flash operation mode to LS (low-speed main). Note
- Set the oscillation frequency of the high-speed on-chip oscillator to 1 MHz. Note
- Select the high-speed on-chip oscillator clock ($f_{IH}$) as the main system clock ($f_{MAIN}$).
- Set the operation mode of the subsystem clock pin to XT1 oscillation and connect a crystal resonator to the XT1/P123 and XT2/EXCLKS/P124 pins.
- Set the oscillation mode of the XT1 oscillator to ultra-low power consumption oscillation.
- Select the main system clock ($f_{MAIN}$) as the CPU/peripheral hardware clock ($f_{CLK}$).

Note: The flash operation mode and high-speed on-chip oscillator frequency are set in the user option byte (000C2H/010C2H).

(2) Set the I/O ports.

- LED lighting control ports (LED0 to LED2): Set ports P10 to P12 for output.
- Switch input: Set the P137/INTP0 pin for INTP0 falling edge detection interrupt mode (using an external pull-up resistor).

(3) Display the operation mode on the LED.

(4) Set each operation mode and wait for a switch input.

- In the OCO-RUN mode, the main system clock ($f_{MAIN}$) is selected as the CPU/peripheral hardware clock ($f_{CLK}$) and the XT1 oscillator is stopped. Subsequently, the CPU waits for a switch input.
- In the OCO-HALT mode, the CPU transitions to the HALT mode and waits for a switch input.
- In the OCO-STOP mode, the CPU transitions to the STOP mode and waits for a switch input.
- In the XT1-RUN mode, the subsystem clock ($f_{SUB}$) is selected as the CPU/peripheral hardware clock ($f_{CLK}$) and the high-speed on-chip oscillator clock is stopped. Subsequently, the CPU waits for a switch input.
- In the XT1-HALT mode, the CPU transitions to the HALT mode and waits for a switch input.

(5) Recognize a switch input and switch the operation mode.

- The operation mode is switched upon detection of the falling edge of a signal at the P137/INTP0 pin. A loop count of about 10 ms is set according to the frequency of the CPU/peripheral hardware clock ($f_{CLK}$).
- The application cycles through the loop the specified number of times and checks for about 10 ms equivalent of chatters. When the application subsequently recognizes the presence of a switch input, it switches the operation mode.

Caution: For detailed usage notes on the product, refer to RL78/G13 User's Manual: Hardware.

## 5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

**Table 5.1 Option Byte Settings**

| Address | Value | Description |
|---|---|---|
| 000C0H/010C0H | 11101111B | Disables the watchdog timer.<br>(Stops counting after the release from the reset status.) |
| 000C1H/010C1H | 01111111B | LVD reset mode which uses 2.81 V (2.76 V to 2.87 V) |
| 000C2H/010C2H | 10101101B | LS mode, HOCO: 1 MHz |
| 000C3H/010C3H | 10000100B | Enables the on-chip debugger. |

## 5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

**Table 5.2 Constants for the Sample Program**

| Constant | Setting | Description |
|---|---|---|
| MODE_OCO_RUN | 0 | Operation mode (OCO-RUN mode) |
| MODE_OCO_HALT | 1 | Operation mode (OCO-HALT mode) |
| MODE_OCO_STOP | 2 | Operation mode (OCO-STOP mode) |
| MODE_SUB_RUN | 3 | Operation mode (XT1-RUN mode) |
| MODE_SUB_HALT | 4 | Operation mode (XT1-HALT mode) |
| MODE_MAX | 5 | Maximum value of operation mode |
| HIOCLK | 0 | High-speed on-chip oscillator clock |
| SUBXT1CLK | 3 | XT1 oscillator clock |
| MD_OK | 0x00U | Normal termination |
| MD_ARGERROR | 0x81U | Error termination (invalid argument) |
| P_LED | P1 | LED lighting control port |
| led_pattern[0] | 0b00000110 | Display pattern by LED0 to LED2 in OCO-RUN mode |
| led_pattern[1] | 0b00000100 | Display pattern by LED0 to LED2 in OCO-HALT mode |
| led_pattern[2] | 0b00000010 | Display pattern by LED0 to LED2 in OCO-STOP mode |
| led_pattern[3] | 0b00000111 | Display pattern by LED0 to LED2 in XT1-RUN mode |
| led_pattern[4] | 0b00000101 | Display pattern by LED0 to LED2 in XT1-HALT mode |

## 5.4 List of Variable

Table 5.3 lists the global variable that is used by this sample program.

**Table 5.3 Global Variable**

| Type | Variable Name | Contents | Function Used |
|---|---|---|---|
| static enum mode | operate_mode | Operation mode | main() |

## 5.5 List of Functions

Table 5.4 lists the global functions that are used by this sample program.

**Table 5.4 Functions**

| Function Name | Outline |
|---|---|
| R_INTC0_Start | INTP0 interrupt enable processing |
| R_CGC_Set_fCLK | CPU/peripheral hardware clock switch processing |

## 5.6 Function Specifications

Shown below are the functions that are used in this sample program.

[Function Name] R_INTC0_Start

| | |
|---|---|
| Synopsis | INTP0 interrupt enable processing |
| Header | r_cg_intc.h |
| Declaration | void R_INTC0_Start(void) |
| Explanation | This function enables INTP0 interrupts and starts sampling switch input. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function Name] R_CGC_Set_fCLK

| | |
|---|---|
| Synopsis | CPU/peripheral hardware clock switch processing |
| Header | r_cg_cgc.h |
| Declaration | MD_STATUS R_CGC_Set_fCLK(enum ClockMode mode) |
| Explanation | This function switches the CPU/peripheral hardware clock ($f_{CLK}$) to the clock that is specified in the argument. The clock to be switched can be specified as the high-speed on-chip oscillator clock or XT1 clock. If any other clock is specified, this function does not switch the clock and returns an argument error . The clock that is specified in the argument is set for oscillation before the clock is switched. After the clock is switched, the unused clock is stopped. |
| Arguments | enum ClockMode mode : [Specification of clock to be specified as the CPU/peripheral hardware clock ($f_{CLK}$)] |
| Return value | [MD_OK]: Normal termination<br>[MD_ARGERROR]: Error termination (invalid argument) |
| Remarks | None |

## 5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

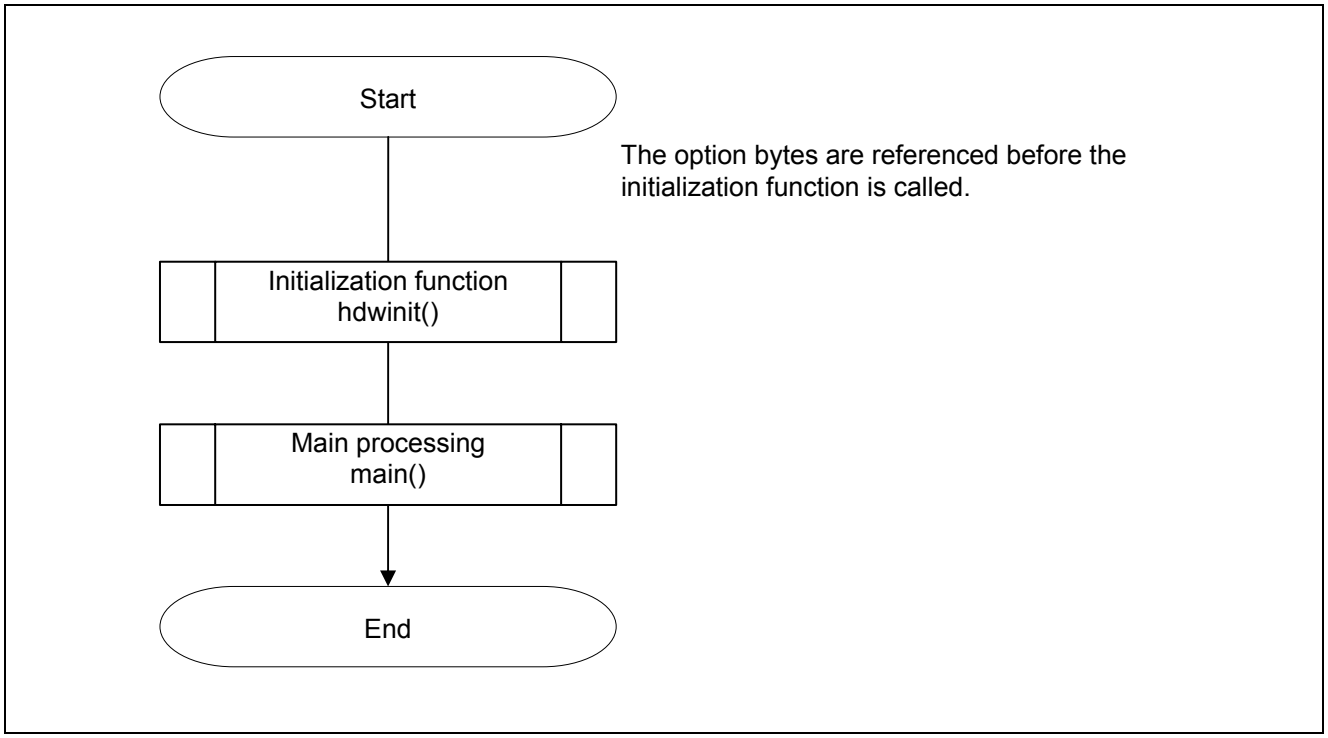


**Figure 5.1 Overall Flow**

Caution: For the settings of the option bytes other than 000C2H/010C2H, refer to the section entitled "Flowcharts" in RL78/G13 Initialization (R01AN0451E) Application Note.

Setting the high-speed on-chip oscillator and flash operation mode

- Option byte (000C2H/010C2H)
  Set the flash operation mode.
  Set the high-speed on-chip oscillator frequency.

Address: 000C2H / 010C2H [Note]

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CMODE1 | CMODE0 | 1 | 0 | FRQSEL3 | FRQSEL2 | FRQSEL1 | FRQSEL0 |
| **1** | **0** | **1** | 0 | **1** | **1** | **0** | **1** |

Bits 7 and 6

| CMODE1 | CMODE0 | Setting of flash operation mode | | |
|---|---|---|---|---|
| | | | Operating frequency range | Operating voltage range |
| 0 | 0 | LV (low voltage main) mode | 1 MHz to 4 MHz | 1.6 V to 5. 5V |
| **1** | **0** | **LS (low-speed main) mode** | **1 MHz to 8 MHz** | **1.8 V to 5.5 V** |
| 1 | 1 | HS (high-speed main) mode | 1 MHz to 16 MHz | 2.4 V to 5.5 V |
| | | | 1 MHz to 32 MHz | 2.7 V to 5.5 V |
| Other than above | | Setting prohibited | | |

Bits 3 to 0

| FRQSEL3 | FRQSEL2 | FRQSEL1 | FRQSEL0 | Frequency of the high-speed on-chip oscillator |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 32 MHz |
| 0 | 0 | 0 | 0 | 24 MHz |
| 1 | 0 | 0 | 1 | 16 MHz |
| 0 | 0 | 0 | 1 | 12 MHz |
| 1 | 0 | 1 | 0 | 8 MHz |
| 1 | 0 | 1 | 1 | 4 MHz |
| **1** | **1** | **0** | **1** | **1 MHz** |
| Other than above | | | | Setting prohibited |

Note: Set the same value in 000C2H and 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

### 5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

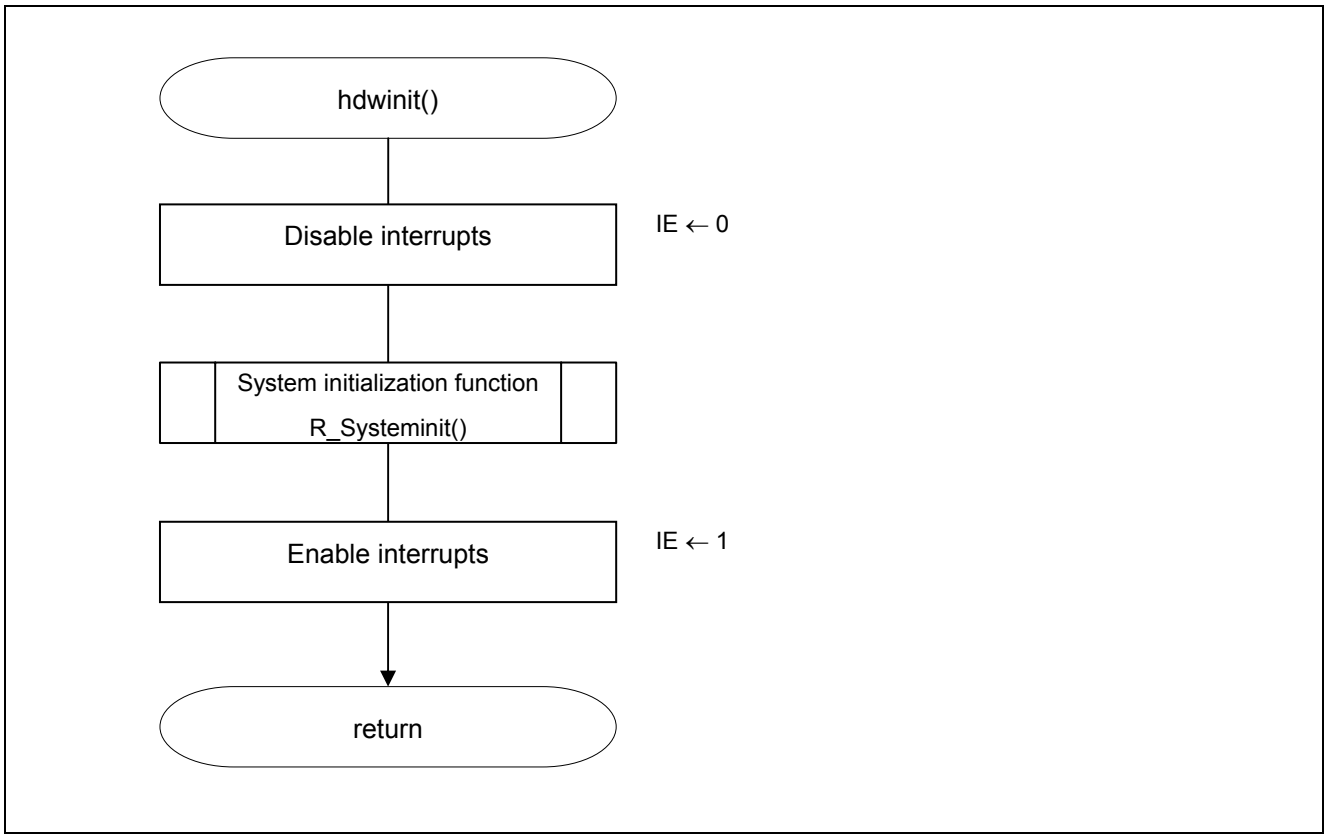


**Figure 5.2 Initialization Function**

### 5.7.2 System Initialization Function

Figure 5.3 shows the flowchart for the system initialization function.

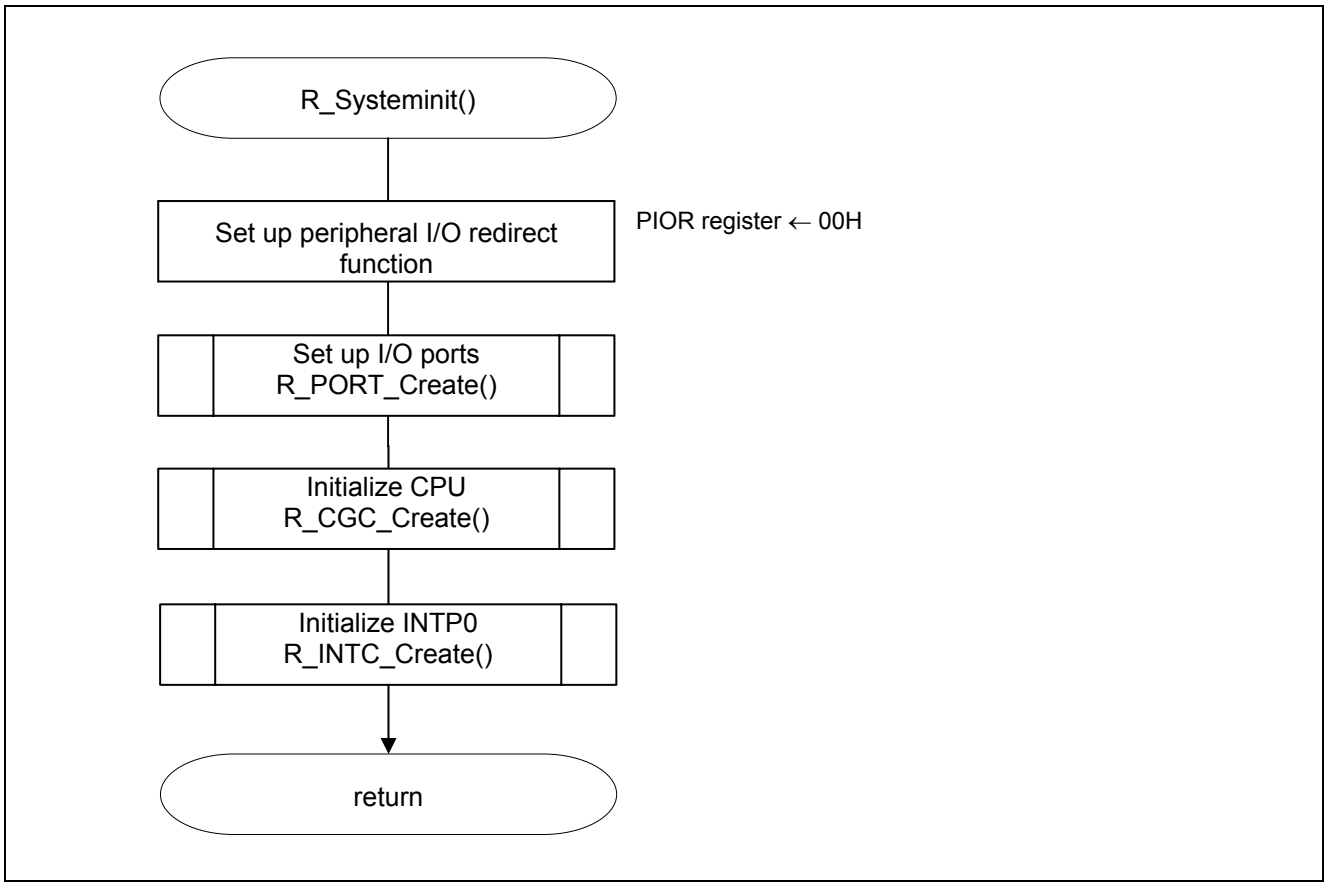


**Figure 5.3 System Initialization Function**

### 5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

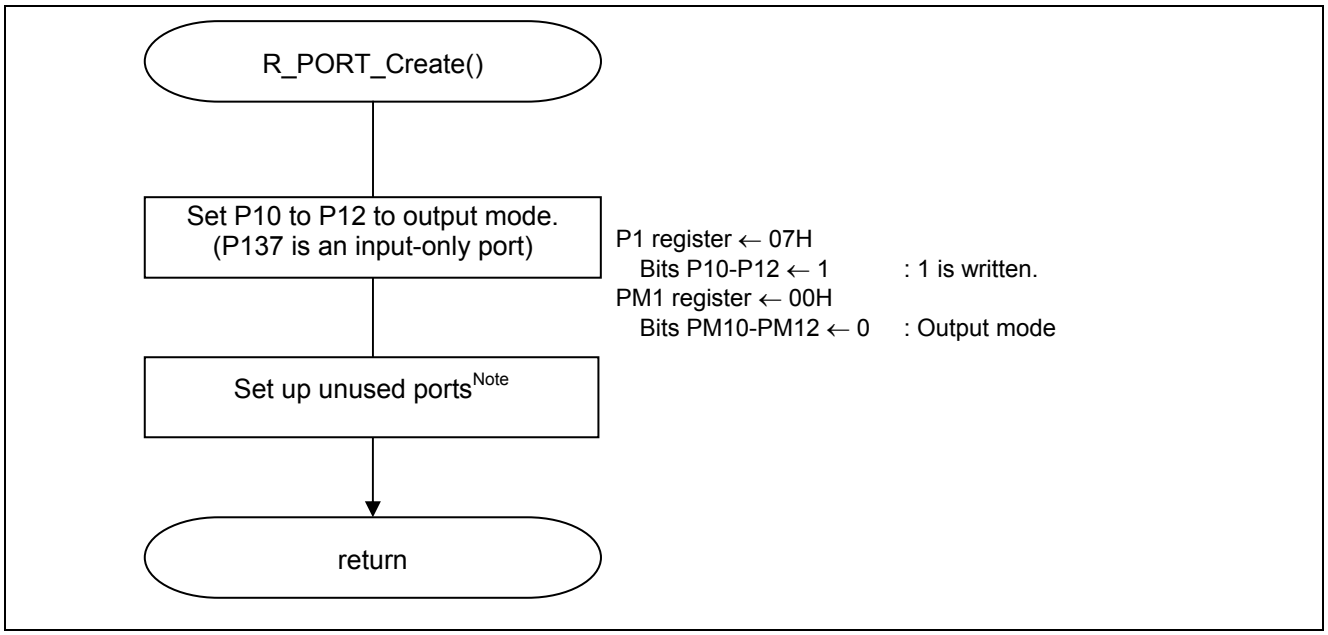


**Figure 5.4 I/O Port Setup**

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to $V_{DD}$ or $V_{SS}$ via a separate resistor.

Setting up the LED0 to LED2 Pins

- Port register 1 (P1)
- Port mode register 1 (PM1)
  Select the I/O mode and output level of the ports for LED0 to LED2.

Symbol: P1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
| x | x | x | x | x | **1** | **1** | **1** |

Bit 2

| P12 | P12 pin output data control (in output mode) |
|---|---|
| 0 | Output 0 |
| **1** | **Output 1** |

Bit 1

| P11 | P11 pin output data control (in output mode) |
|---|---|
| 0 | Output 0 |
| **1** | **Output 1** |

Bit 0

| P10 | P10 pin output data control (in output mode) |
|---|---|
| 0 | Output 0 |
| **1** | **Output 1** |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: PM1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |
| x | x | x | x | x | **0** | **0** | **0** |

Bit 2

| PM12 | P12 pin I/O mode selection |
|---|---|
| **0** | **Output mode (output buffer on)** |
| 1 | Input mode (output buffer off) |

Bit 1

| PM11 | P11 pin I/O mode selection |
|---|---|
| **0** | **Output mode (output buffer on)** |
| 1 | Input mode (output buffer off) |

Bit 0

| PM10 | P10 pin I/O mode selection |
|---|---|
| **0** | **Output mode (output buffer on)** |
| 1 | Input mode (output buffer off) |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

### 5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

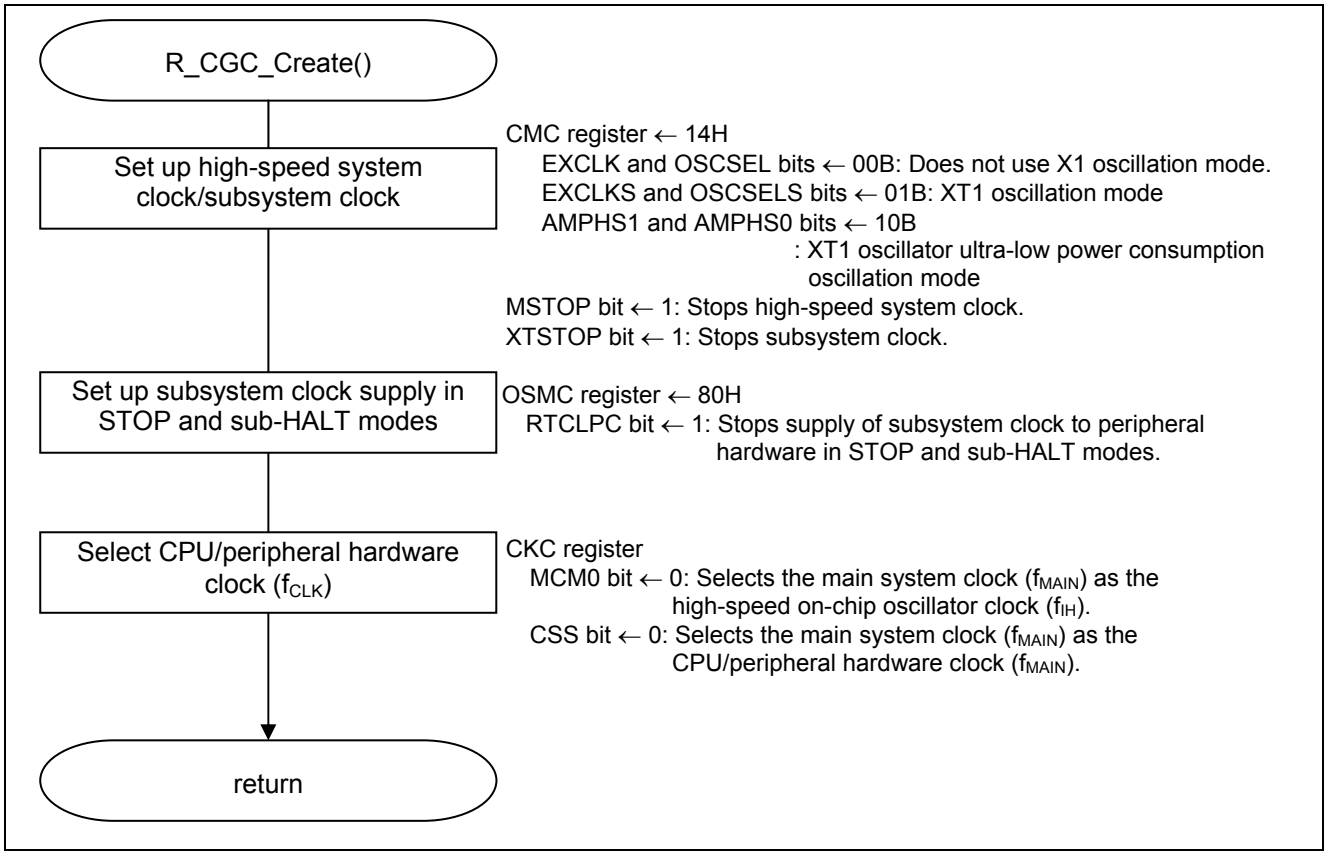


**Figure 5.5 CPU Clock Setup**

Setting up the clock operation mode

- Clock operation mode control register (CMC)
  High-speed system clock pin operation mode: Input port mode
  Subsystem clock pin operation mode: XT1 oscillation mode
  XT1 oscillator oscillation mode: Ultra-low power consumption oscillation

Symbol: CMC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EXCLK | OSCSEL | EXCLKS | OSCSELS | 0 | AMPHS1 | AMPHS0 | AMPH |
| **0** | **0** | **0** | **1** | 0 | **1** | **0** | 0 |

Bits 7 and 6

| EXCLK | OSCSEL | High-speed system clock pin operation mode | X1/P121 pin | X2/EXCLK/P122 pin |
|---|---|---|---|---|
| **0** | **0** | **Input port mode** | **Input port** | |
| 0 | 1 | X1 oscillation mode | Crystal/ceramic resonator connection | |
| 1 | 0 | Input port mode | Input port | |
| 1 | 1 | External clock input mode | Input port | External clock input |

Bits 5 and 4

| EXCLKS | OSCSELS | Subsystem clock pin operation mode | XT1/P123 pin | XT2/EXCLKS/P124 pin |
|---|---|---|---|---|
| 0 | 0 | Input port mode | Input port | |
| **0** | **1** | **XT1 oscillation mode** | **Crystal resonator connection** | |
| 1 | 0 | Input port mode | Input port | |
| 1 | 1 | External clock input mode | Input port | External clock input |

Bits 2 and 1

| AMPHS1 | AMPHS0 | XT1 oscillator oscillation mode select Note | |
|---|---|---|---|
| 0 | 0 | Low power consumption oscillation (default) | Oscillation margin: Medium |
| 0 | 1 | Normal oscillation | Oscillation margin: Large |
| **1** | **0** | **Ultra-low power consumption oscillation** | **Oscillation margin: Small** |
| 1 | 1 | Setting prohibited | |

Note: As the XT oscillator becomes oscillation mode with lower power consumption, its oscillation margin becomes smaller.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Controlling the operation of the clocks

- Clock operation status control register (CSC)
  High-speed system clock operation control: Stopped
  Subsystem clock operation control: Stopped
  High-speed on-chip oscillator clock operation control: Operating

Symbol: CSC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MSTOP | XTSTOP | 0 | 0 | 0 | 0 | 0 | HIOSTOP |
| **1** | **1** | 0 | 0 | 0 | 0 | 0 | **0** |

Bit 7

| MSTOP | High-speed system clock operation control | | |
|---|---|---|---|
| | X1 oscillation mode | External clock input mode | Input port mode |
| 0 | X1 oscillator operating | External clock from EXCLK pin is valid | **Input port** |
| **1** | X1 oscillator stopped | External clock from EXCLK pin is invalid | |

Bit 6

| XTSTOP | Subsystem clock operation control | | |
|---|---|---|---|
| | X1 oscillation mode | External clock input mode | Input port mode |
| 0 | X1 oscillator operating | External clock from EXCLKS pin is valid | Input port |
| **1** | **XT1 oscillator stopped** | External clock from EXCLKS pin is invalid | |

Bit 0

| HIOSTOP | High-speed on-chip oscillator clock operation control |
|---|---|
| **0** | **High-speed on-chip oscillator operating** |
| 1 | High-speed on-chip oscillator stopped |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Controlling the operation speed mode

- Operation speed mode control register (OSMC)
  Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock
  : Disables the supply of the subsystem clock to the peripheral hardware.
  Operating clock for the real-time clock and 12-bit interval timer
  : Subsystem clock

  Symbol: OSMC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |
| **1** | 0 | 0 | **0** | 0 | 0 | 0 | 0 |

  Bit 7

| RTCLPC | Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock |
|---|---|
| 0 | Enables supply of subsystem clock to peripheral functions |
| **1** | **Stops supply of subsystem clock to peripheral functions other than real-time clock and 12-bit interval timer** |

  Bit 4

| WUTMMCK0 | Selection of operation clock for real-time clock and 12-bit interval timer |
|---|---|
| **0** | **Subsystem clock** |
| 1 | Low-speed on-chip oscillator clock |

  Caution: The OSMC register is intended to be used to reduce power consumption by reducing the operating current of the device in the STOP and HALT modes while the subsystem clock is selected as CPU clock. For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the CPU/peripheral hardware clock ($f_{CLK}$)

- System clock control register (CKC)
  $f_{CLK}$ initial value: High-speed on-chip oscillator clock ($f_{IH}$)

Symbol: CKC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLS | CSS | MCS | MCM0 | 0 | 0 | 0 | 0 |
| 0 | **0** | 0 | **0** | 0 | 0 | 0 | 0 |

Bit 6

| CSS | Selection of CPU/peripheral hardware clock ($f_{CLK}$) |
|---|---|
| **0** | **Main system clock ($f_{MAIN}$)** |
| 1 | Subsystem clock ($f_{SUB}$) |

Bit 4

| MCM0 | Main system clock ($f_{MAIN}$) operation control |
|---|---|
| **0** | **Selects the high-speed on-chip oscillator clock ($f_{IH}$) as the main system clock ($f_{MAIN}$)** |
| 1 | Selects the high-speed system clock ($f_{MX}$) as the main system clock ($f_{MAIN}$). |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

### 5.7.5 INTP0 Initialization

Figure 5.6 shows the flowchart for initializing INTP0.

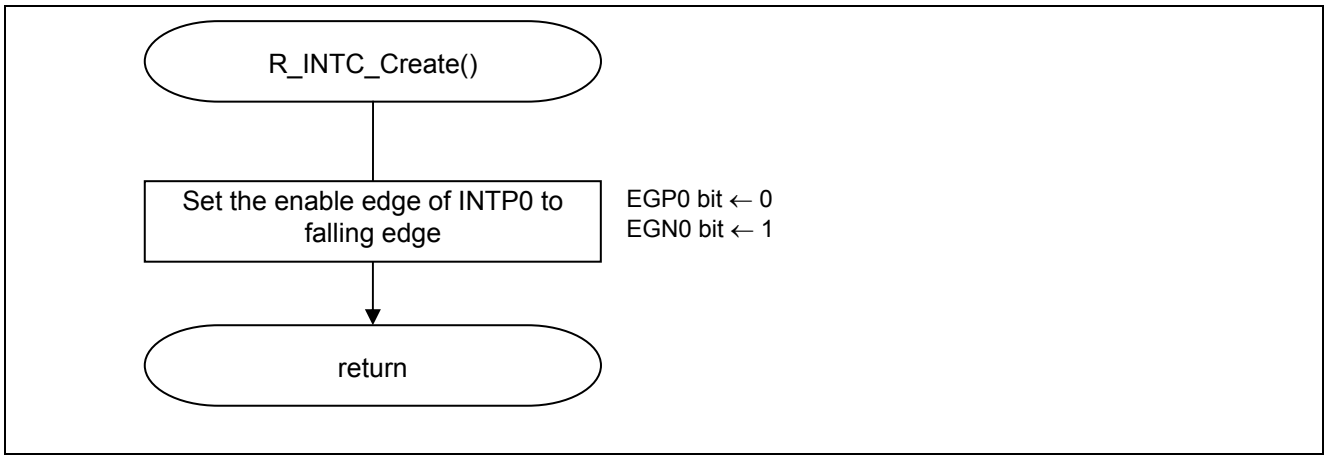


**Figure 5.6 INTP0 Initialization**

Setting up the INTP0 pin edge detection

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  Enable edge of INTP0: Falling edge

Symbol: EGP0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EGP7 | EGP6 | EGP5 | EGP4 | EGP3 | EGP2 | EGP1 | EGP0 |
| x | x | x | x | x | x | x | **0** |

Symbol: EGN0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EGN7 | EGN6 | EGN5 | EGN4 | EGN3 | EGN2 | EGN1 | EGN0 |
| x | x | x | x | x | x | x | **1** |

Bit 0

| EGP0 | EGN0 | INTP0 pin enable edge selection |
|---|---|---|
| 0 | 0 | Edge detection disabled |
| **0** | **1** | **Falling edge** |
| 1 | 0 | Rising edge |
| 1 | 1 | Both rising and falling edges |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

### 5.7.6 Main Processing

Figures 5.7 to 5.9 show the flowcharts for main processing.

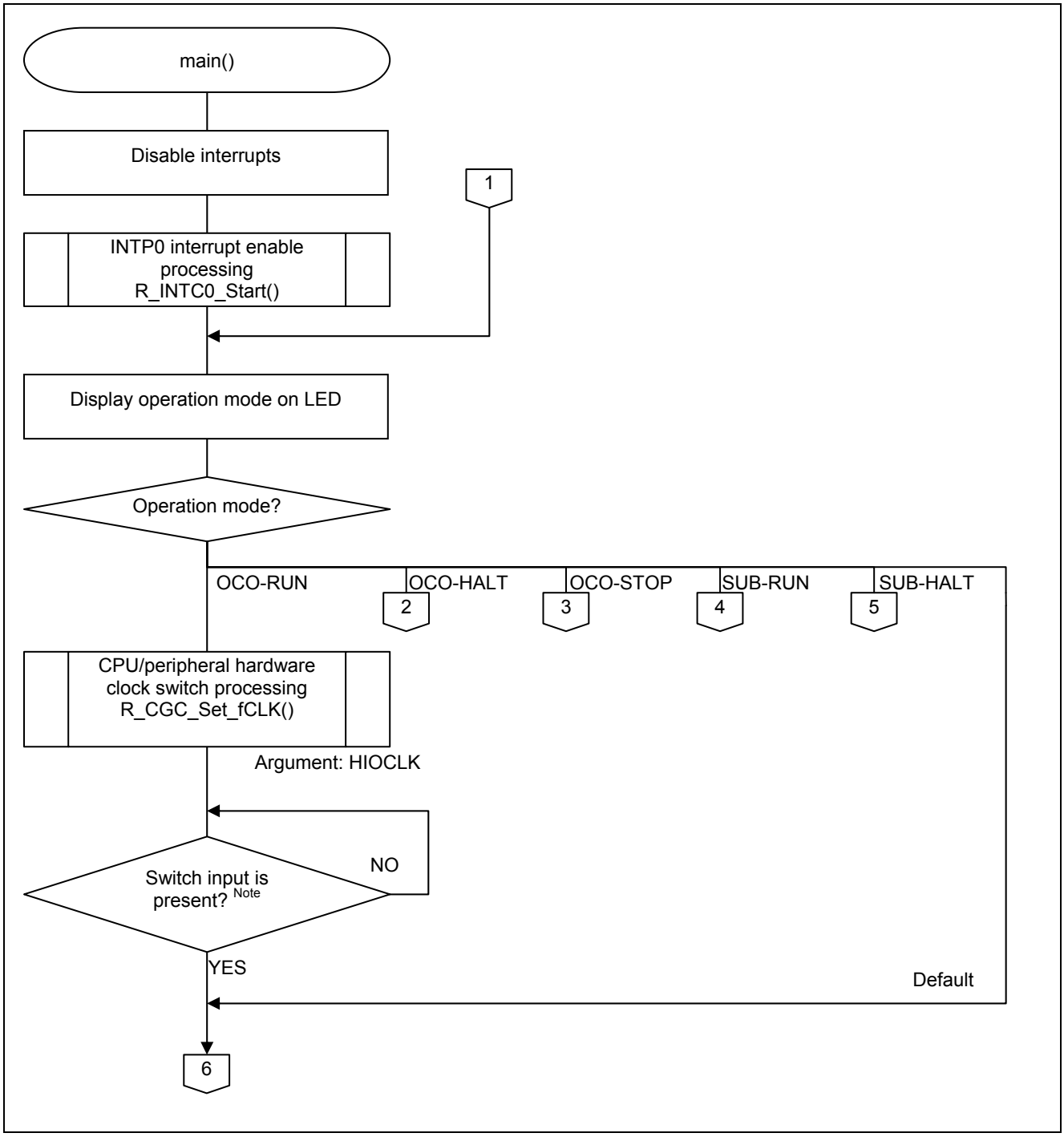


**Figure 5.7 Main Processing (1/3)**

Note: The switch input is checked by examining the INTP0 interrupt request flag (PIF0).

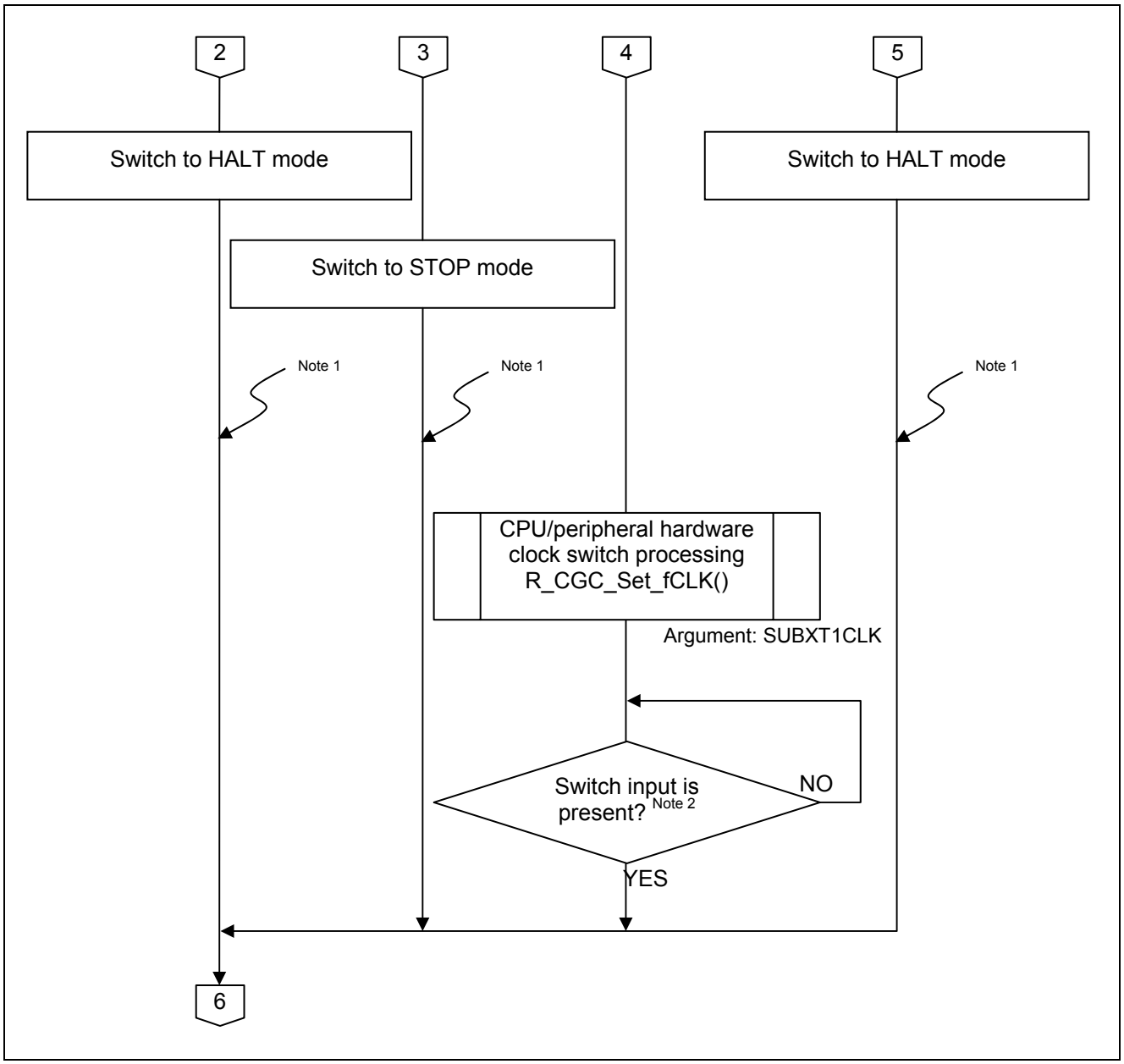


**Figure 5.7 Main Processing (2/3)**

Notes: 1. The HALT and STOP modes are exited by a switch input (occurrence of an INTP0 interrupt).
2. The switch input is checked by examining the INTP0 interrupt request flag (PIF0).

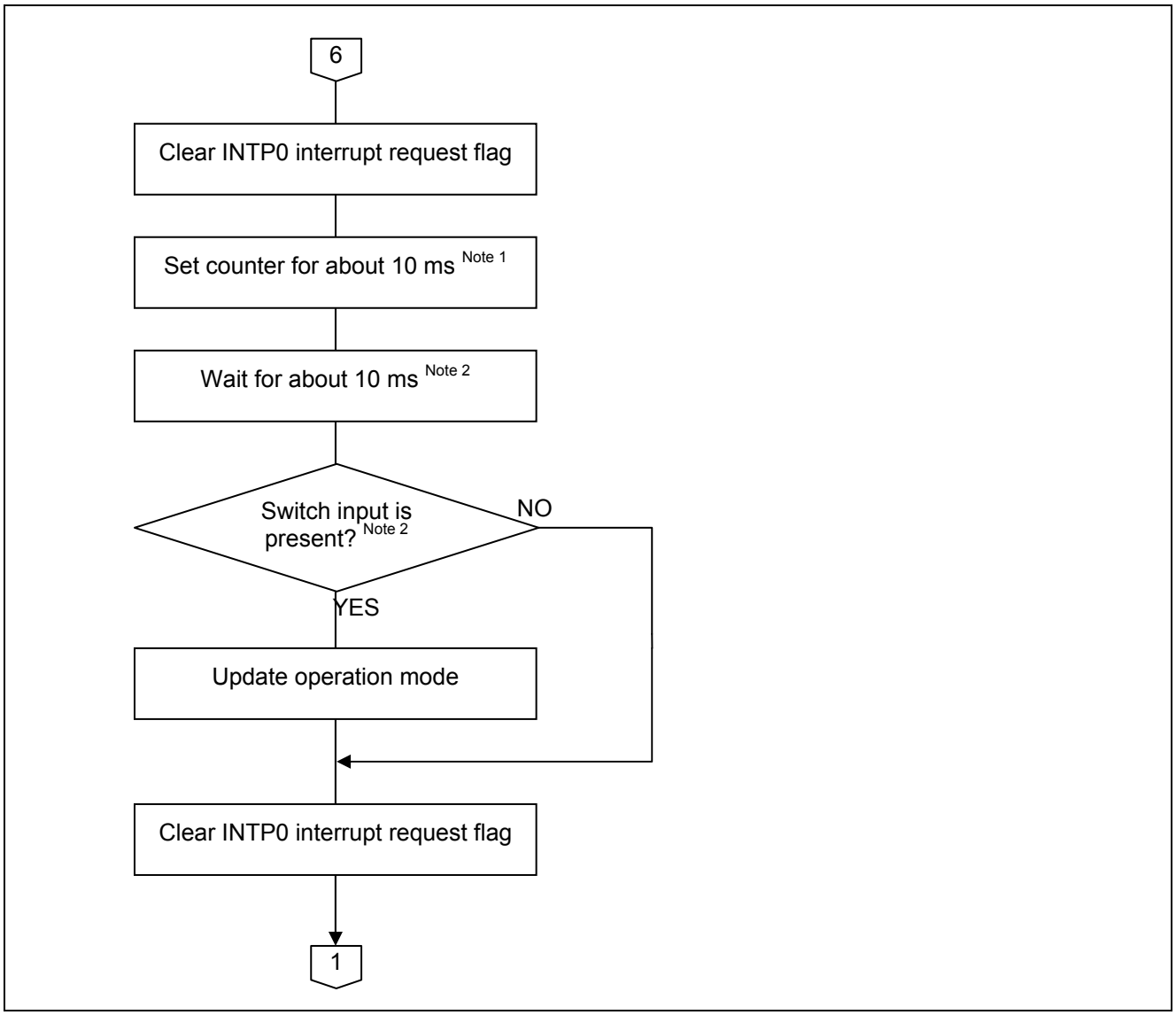


**Figure 5.7 Main Processing (3/3)**

Notes: 1. The main processing checks the $f_{CLK}$ setting and sets up a wait loop of about 10 ms.
2. The main processing checks a switch input again in about 10 ms after the occurrence of an INTP0 interrupt to avoid chattering. The switch input in this case is checked by examining the level of the input signal at the P137 pin.

### 5.7.7 INTP0 Interrupt Enable Processing

Figure 5.10 shows the flowchart for the INTP0 interrupt enable processing.

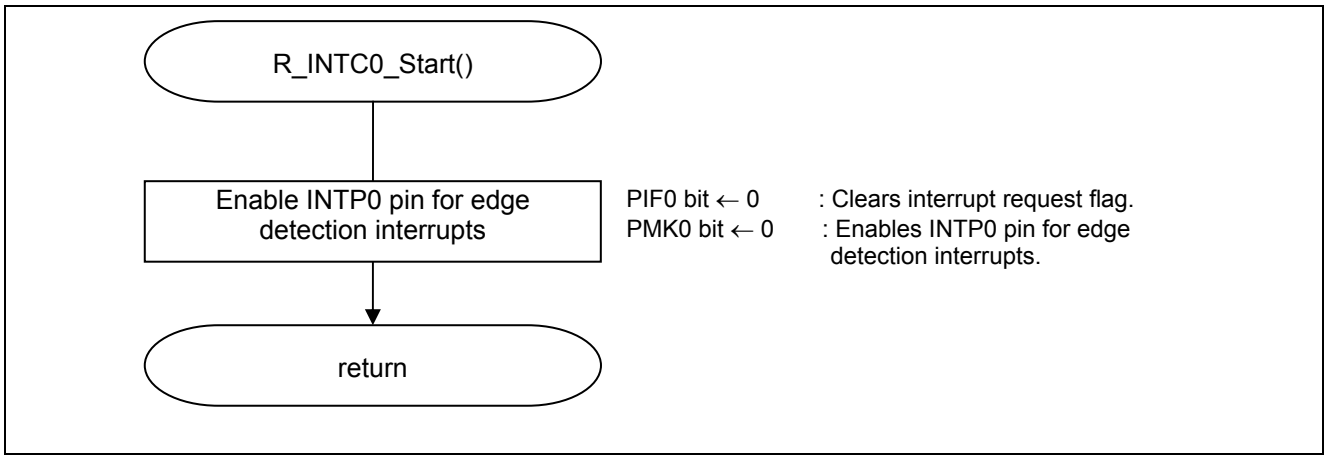


**Figure 5.10 INTP0 Interrupt Enable Processing**

Setting INTP0 interrupt

- Interrupt request flag register (IF0L)
  Clears interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clears interrupt mask.

Symbol: IF0L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PIF5 | PIF4 | PIF3 | PIF2 | PIF1 | PIF0 | LVIIF | WDTIIF |
| x | x | x | x | x | **0** | x | x |

Bit 2

| PIF0 | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated** |
| **1** | Interrupt request signal is generated, interrupt request status |

Symbol: MK0L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PMK5 | PMK4 | PMK3 | PMK2 | PMK1 | PMK0 | LVIMK | WDTIMK |
| x | x | x | x | x | **0** | x | x |

Bit 2

| PMK0 | Interrupt processing control |
|---|---|
| **0** | **Interrupt processing enabled** |
| **1** | Interrupt processing disabled |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

### 5.7.8 CPU/Peripheral Hardware Clock Switch Processing

Figures 5.11 and 5.12 show the flowcharts for the CPU/peripheral hardware clock processing.

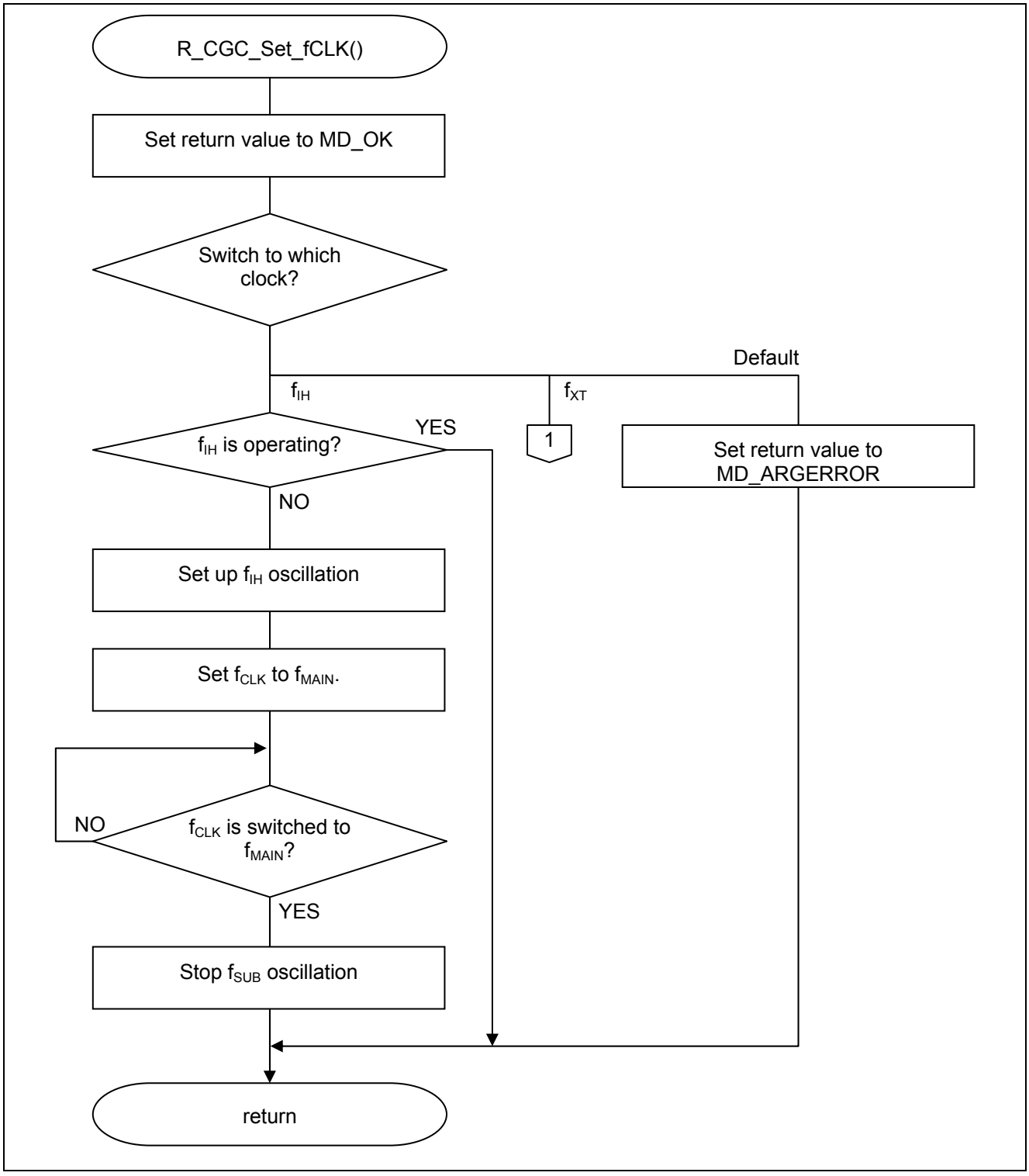


**Figure 5.11 CPU/Peripheral Hardware Clock Switch Processing (1/2)**

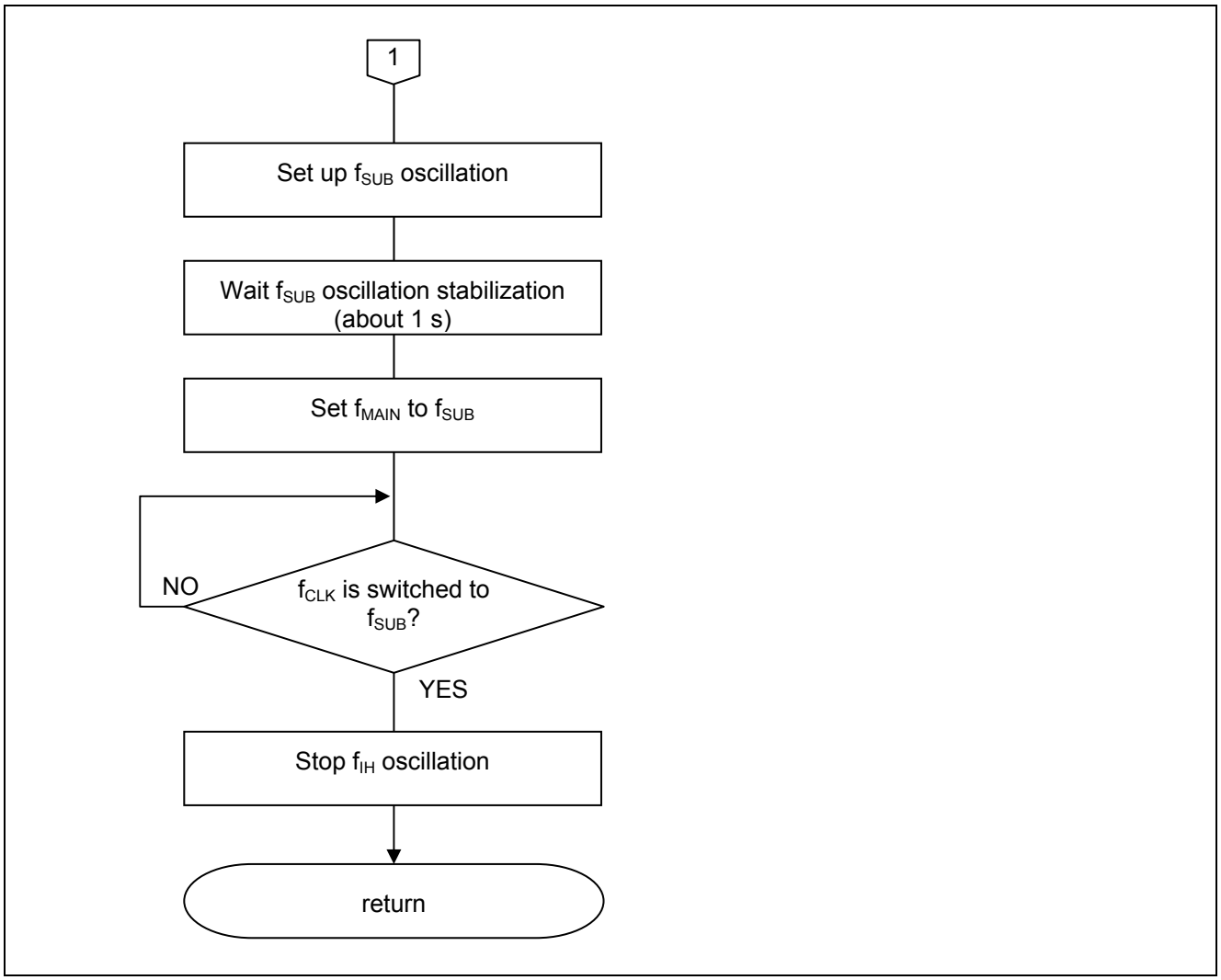


**Figure 5.12 CPU/Peripheral Hardware Clock Switch Processing (2/2)**

Setting the CPU/peripheral hardware clock ($f_{CLK}$) and checking its status

- System clock control register (CKC)
  Selects $f_{CLK}$ and checks its status.

Symbol: CKC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLS Note | CSS | MCS Note | MCM0 | 0 | 0 | 0 | 0 |
| **0/1** | **0/1** | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7

| CLS Note | Status of CPU/peripheral hardware clock ($f_{CLK}$) |
|---|---|
| **0** | **Main system clock ($f_{MAIN}$)** |
| **1** | **Subsystem clock ($f_{SUB}$)** |

Bit 6

| CSS | Selection of CPU/peripheral hardware clock ($f_{CLK}$) |
|---|---|
| **0** | **Main system clock ($f_{MAIN}$)** |
| **1** | **Subsystem clock ($f_{SUB}$)** |

Note: Bits 7 and 5 are read-only.
Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Checking the clocks and setting up their operation modes

- Clock operation status control register (CSC)
  Checks operating status of the clock designated as the CPU/peripheral hardware clock ($f_{CLK}$) and sets its operating mode.

Symbol: CSC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MSTOP | XTSTOP | 0 | 0 | 0 | 0 | 0 | HIOSTOP |
| 1 | **0/1** | 0 | 0 | 0 | 0 | 0 | **0/1** |

Bit 6

| XTSTOP | Subsystem clock operation control | | |
|---|---|---|---|
| | XT1 oscillation mode | External clock input mode | Input port mode |
| 0 | **XT1 oscillator operating** | External clock from EXCLKS pin is valid | Input port |
| 1 | **XT1 oscillator stopped** | External clock from EXCLKS pin is invalid | |

Bit 0

| HIOSTOP | High-speed on-chip oscillator clock operation control |
|---|---|
| **0** | **High-speed on-chip oscillator operating** |
| **1** | **High-speed on-chip oscillator stopped** |

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

## 6. Sample Code

The sample code is available on the Renesas Electronics Website.

## 7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

## Website and Support

Renesas Electronics Website

- http://www.renesas.com/index.jsp

Inquiries

- http://www.renesas.com/contact/

| Revision Record | RL78/G13 Low-power Consumption Operation |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jan. 18, 2012 | — | First edition issued |
| | | | |

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
  - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
  - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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