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David N. Mashburn, Stephen J. Hinkson, Marcella C. Woods, Jonathan M. Gilligan, Mark R. Holcomb, and John P. Wikswo

A high-voltage cardiac stimulator for field shocks of a whole heart in a bath

David N. Mashburn
Department of Physics and Astronomy, Vanderbilt University, Nashville, Tennessee 37235, USA

Stephen J. Hinkson[a]
Labcyte Inc., Sunnyvale, California 94089, USA

Marcella C. Woods
Department of Biomedical Engineering, Vanderbilt University, Nashville, Tennessee 37235, USA

Jonathan M. Gilligan
Department of Earth and Environmental Sciences, Vanderbilt University, Nashville, Tennessee 37235, USA

Mark R. Holcomb
Department of Physics and Astronomy, Vanderbilt University, Nashville, Tennessee 37235, USA

John P. Wikswo
Department of Physics and Astronomy, Vanderbilt University, Nashville, Tennessee 37235, USA, Department of Biomedical Engineering, Vanderbilt University, Nashville, Tennessee 37235, USA, Department of Molecular Physiology and Biophysics, Vanderbilt University, Nashville, Tennessee 37235, USA, and Vanderbilt Institute for Integrative Biosystems Research and Education, Vanderbilt University, Nashville, Tennessee 37235, USA

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Defibrillators are a critical tool for treating heart disease; however, the mechanisms by which they halt fibrillation are still not fully understood and are the subject of ongoing research. Clinical defibrillators do not provide the precise control of shock timing, duration, and voltage or other features needed for detailed scientific inquiry, and there are few, if any, commercially available units designed for research applications. For this reason, we have developed a high-voltage, programmable, capacitive-discharge stimulator optimized to deliver defibrillation shocks with precise timing and voltage control to an isolated animal heart, either in air or in a bath. This stimulator is capable of delivering voltages of up to 500 V and energies of nearly 100 J with timing accuracy of a few microseconds and with rise and fall times of 5 μs or less and is controlled only by two external timing pulses and a control computer that sets the stimulation parameters via a LABVIEW interface. Most importantly, the stimulator has circuits to protect the high-voltage circuitry and the operator from programming and input-output errors. This device has been tested and used successfully in field shock experiments on rabbit hearts as well as other protocols requiring high voltage. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2796832]

INTRODUCTION

Cardiac electrodynamics is the study of the normal and pathological electrophysiological functioning of the heart. Of particular interest is fibrillation, when the electrical activity of the heart is reentrant, preventing the heart from normal, rhythmic contraction. The standard treatment for fibrillation is to deliver a strong electrical shock to the heart. If successful, this shock will reset the electrical activity and return the heart to a normal sinus rhythm.[1,2] Laboratory studies of defibrillation benefit from a stimulator that is adequately flexible to perform a variety of experimental procedures as well as simulate many different clinical defibrillators. Our research requires that the stimulator satisfies the following specifications. The stimulus pulse must have clean leading and falling edges for studying the passive (electrotonic) response of cardiac tissue that occurs in the first few milliseconds after stimulation, prior to the onset of propagating electrophysiological activation. In the resting state of the device current should not be allowed to flow between the electrodes on the heart, i.e., the circuit must be open when the device is not stimulating, to avoid half-cell effects that might otherwise occur at the electrode-tissue interface.[3] The initial voltage on the capacitors must be programmable and consistent, and the applied voltage should decay slowly enough to facilitate both short (<50 μs) and long ($\geqslant 10$ ms) stimuli. The device should not be current limited for loads above 10 Ω and hence must be able to deliver currents of up to 50 A. Also, the device must have precise control of pulse duration and timing that can be monitored, so that instruments such as cameras, transient optical sources, and other electrical stimuli can be synchronized with the stimulation. As with any device capable of such large shocks, proper safety mea-

[a]Formerly of Ventritex, Inc. and St. Jude Medical, Inc.

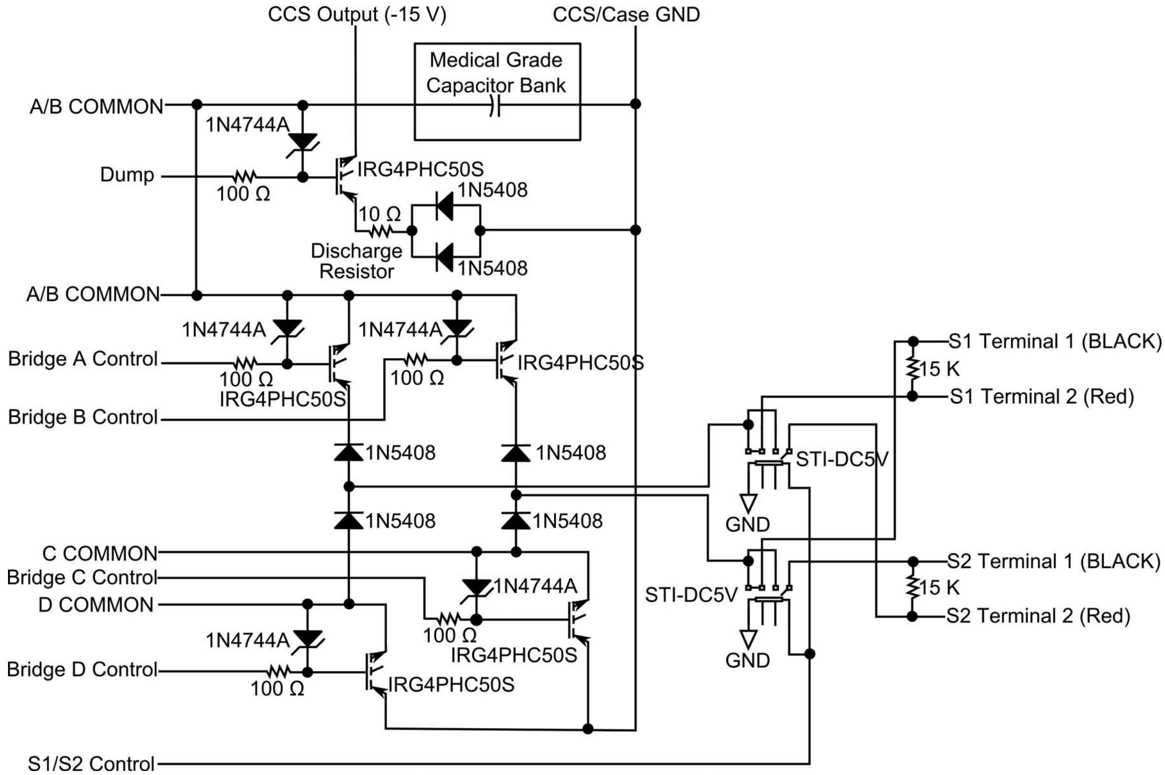

FIG. 1. Schematic of the diode bridge and the other high-voltage components of the stimulator. The discharge signal comes from the NI 6503 card. Bridge controls A–D are connected to the bridge. The terminals at the right are the two sets of high-voltage outputs.

sures must also be taken to prevent potentially fatal injuries. The stimulator described in this paper conforms to all of these requirements.

DEVICE DESIGN

The core of our defibrillator is formed by a set of medical-grade capacitors, which receive power from a commercial voltage-programmable capacitor-charging supply (CCS-400, Converter Power, Inc.). To protect the user from the high voltage, the circuit board, capacitors, and the CCS are surrounded by a rack-mounted, insulating Plexiglas™ box. The computer interface uses a National Instruments 6503 digital input-output (I/O) card to control a 12 bit digital-to-analog converter (DAC) in the stimulator, which provides the reference voltage to the CCS. The CCS uses this voltage with a multiplication factor of 100 as the output voltage. This card also controls digital lines for changing the polarity of the output, activating or deactivating capacitor charging, controlling the internal discharging of the capacitors through a 10 Ω resistive load, and directing the output to one of two pairs of banana plugs (termed S1 and S2). The stimulator uses optical isolation to separate the computer inputs and low-voltage circuitry from the high-voltage portion of the box. A full diode bridge enables the polarity switching and a pair of relays enables the output switching. This diode bridge and the entire high-voltage schematic are pictured in Fig. 1.

An important feature of our design is that the output of the defibrillator is left in an open-circuit state at the end of the shock, thereby eliminating potential problems that can occur with current sources that present a low impedance when in the off state and thereby connect the defibrillation electrodes with a short circuit.[3]

Into this basic defibrillator, we have incorporated features specifically designed to address several issues in safety, reliability, and functionality. While it would be expedient to allow the computer interface to connect directly to each of the four transistors controlling the diode bridge, such an approach would allow the bridge to be incorrectly configured through programming or I/O errors to create direct shorts that would immediately lead to the destruction of bridge components, as well as pose some risk to the capacitors. To address this potential problem, we use two logic chips at the inputs to the diode bridge to limit the possible configurations to an acceptable set. This logic circuit is pictured in Fig. 2.

To reduce the risk to the operator of injury during an inadvertent single-sided contact with the defibrillator or the

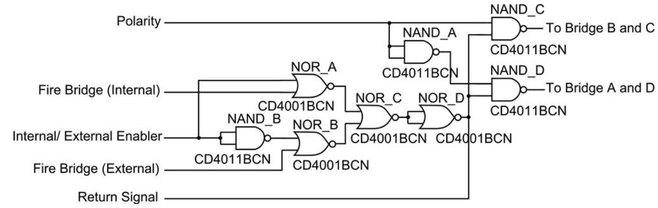

FIG. 2. Intermediate logic stage between the digital computer outputs and the diode bridge. This circuit is meant to protect the bridge from programming and I/O errors. Fire bridge (external) is the external TTL pulse from the timing and data acquisition computer. Fire bridge (internal) comes from the stimulator control computer and can be used for testing. Return signal is a TTL output on the front panel that can be used to monitor the firing of the device for testing.

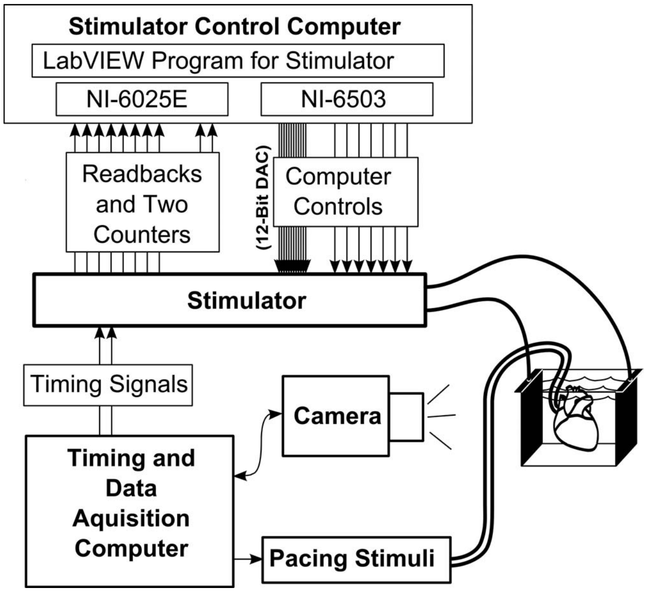

FIG. 3. Overview of experimental setup illustrating the data flow.

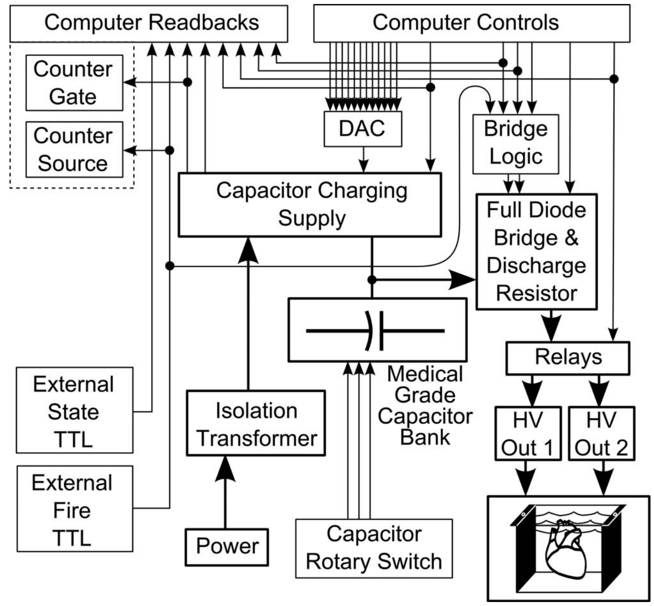

FIG. 4. A block diagram of the stimulator. Arrows indicate the direction of data flow. Dark black connections are for the high voltage. Optical isolation is not pictured.

heart during defibrillation, an isolation transformer (Triad Magnetics, N-53MG) at the power input to the system ensures that both terminals of the defibrillator are floating with respect to any external ground.

While a single computer might control shock timing, defibrillator configuration, and data acquisition, potential timing difficulties can arise when using a non-real-time operating system such as WINDOWS XP™ to acquire images of the cardiac response. To avoid such problems, we used a dedicated stimulator control computer to operate the major defibrillator functions through the NI 6503 card and a totally separate timing and data acquisition computer unburdened to deliver to the defibrillator simply two transistor-transistor logic (TTL) pulses, one to control the firing of the bridge and another flexible "state change" signal to the device. This configuration was achieved by using a second National Instruments card (NI 6025E) in the stimulator control computer for readbacks and pulse counting, allowing the stimulator control computer to monitor the activity of the device and send signals appropriately. An overview of the experimental setup is given in Fig. 3 and a block diagram of the stimulator is given in Fig. 4. A detailed description of the functioning of the stimulator control computer and the interface to the device will be given below.

Clinical defibrillators typically use a single value of capacitance and control the charge delivered by adjusting the charging voltage or possibly the pulse duration. Given that some of our measurements are made on an isolated heart in a saline bath with large plate electrodes on opposite sides of the bath while others are done with intracavity catheter electrodes and the heart in air, the resistance presented to the defibrillator output can vary by orders of magnitude. Similarly, we had need of extremely short ($\leqslant 50$ μs) pulses at high voltage with minimal *RC* decay. To provide the requisite control of the discharge characteristics, we provided for the selection of a range of capacitances by creating a bank of capacitors totaling 750 μF. As pictured in Fig. 5, we use a rotary switch and three relays to switch between any of five combinations of capacitors with capacitance ranging from 150 μF up to the full 750 μF. For example, two 300 μF, 300 V rated capacitors in series create a 150 μF capacitor capable of handling 600 V. The maximum capacitance allows for much longer duration pulses and energy delivery of almost 100 J. Because commercial access to medical-grade capacitors is restricted, it may be necessary to substitute industrial capacitors.

DEVICE LIMITATIONS

As stated, this device is capable of delivering up to 500 V from 750 μF of capacitance. The charging time, however, is not insignificant. In fact, the current drain on the CCS-400 is so great when operating with the highest values of capacitance that it was necessary to reduce the user-specified charging duty cycle to one-third of that used in low-capacitance mode to prevent the CCS from indicating a fault condition. With this adjustment, the CCS requires almost a full second to fully charge the 750 μF capacitance to 500 V. However, with only 150 μF, this duty cycle reduction is not necessary, and the device can charge to 500 V in a few dozen milliseconds. The design of our control hardware and software readily accommodates these adjustments.

SOFTWARE AND STIMULATOR OPERATION

To provide the capabilities required in our research environment, the operation of the stimulator, the control computer, and the timing computer must be rather complex and needs detailed explanation. The system can be in three different states, each regulated by the control computer: safe, charging, and armed. In the safe state, the stimulator is discharged, not charging, disarmed, and set to zero input voltage. In the charging state, the voltage is set and the device is charging but disarmed. In the armed state, the device is not charging but is charged and armed. Figure 6 is a cartoon

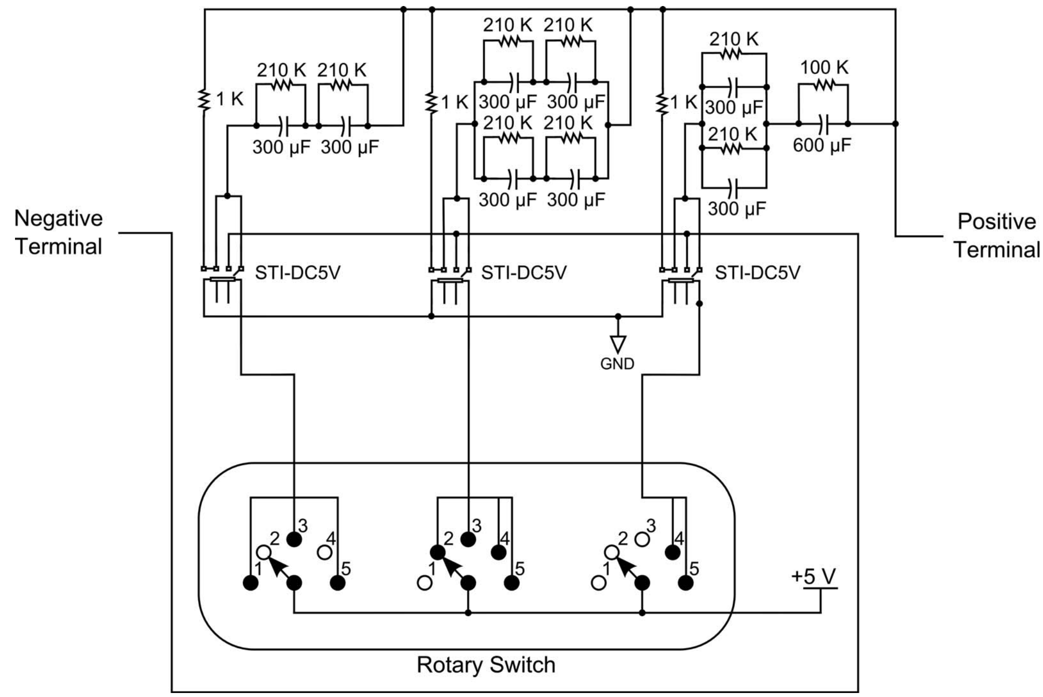

FIG. 5. Complete schematic of the medical-grade capacitor bank. The low-voltage, operator-controlled rotary switch pictured can select 150, 300, 450, 600, or 750 μF of capacitance. Each individual capacitor is rated up to at least 330 V. There are eight 300 μF and one 600 μF capacitors. The capacitors are arranged into three units rated up to 660 V that can be either activated or discharged. By using different combinations of the three blocks (1×150 μF and 2×300 μF), each of the five settings can be achieved.

timing diagram giving the device state, all the essential digital lines, and the high voltage for a sample output. Dotted lines show concurrent times and the diagonal lines of the device state represent software delays.

In describing the details of the timing, it is important to understand all the inputs and outputs to the stimulator. Figures 3 and 4 show three groups of inputs and outputs. The timing signals are two TTL inputs from the timing computer. One of these, the external state signal, is routed through the stimulator directly to the control computer and has no direct control of the stimulator. However, the external fire signal is connected directly to the bridge logic to control the synchronized timing between the stimulator and data acquisition. The computer controls are digital lines from the NI 6503 card and have already been mentioned. These include the lines to control the 12 bit DAC for voltage control of the CCS, the line to control the relays for directing the output to the S1 or S2 terminals, a line to directly control the CCS charging, and a line to control the discharging of the capacitors through the discharge resistor (see Fig. 1). There are also four lines coupling to the bridge logic that control the polarity of the output, the armed state of the device, and whether the device can be fired internally or externally (internal firing is for testing only). The device also provides eight computer readbacks that come through the NI 6025E card. There is direct readback of the S1/S2, CCS charging, polarity, and arming signals. The device also reads back two digital signals from the CCS, the end of charge signal and the fault condition signal. The end of charge line is low whenever the device is actively charging, becomes high when the CCS has fully charged the capacitors to the requested voltage, and stays high even if the CCS charging is disabled, only returning to low when charging is started again. The fault line signals a failure in the CCS, triggered by drawing too much power or failing to connect a load to the high-voltage outputs of the CCS. The last two readbacks are of the external fire signal and the external state signal TTL lines from the timing computer.

In addition to the readbacks, two pulse counters watch for proper stimuli and erroneous stimuli. Proper stimuli are those in which the output pulse terminates firing while the end of charge signal from the CCS is high. This ensures that the capacitors were fully charged. Figure 6 shows the proper firing of an S2 pulse. Erroneous fires are those in which the output pulse begins before the CCS has had time to fully charge the capacitors, for example, when a larger capacitance than allowed by the protocol has been selected. This scenario is pictured in Fig. 7.

With this stimulator, we can implement multiple software configurations, including a mode for a single output (S2 only) and another mode for two separate outputs (S1 and S2) delivered sequentially. These configurations rely on the flexibility of the software on the outboard computer and the use of the external state signal TTL pulse from the main computer. The simplest mode for the device is the S2 only mode, as pictured in Fig. 6. In this mode, the external state signal is used to control the beginning and end of charging. When the box is turned on, all peripheral component interconnect (PCI) cards are initialized and the device is placed into the safe state described above; additionally, the output is routed to the S1 terminal (which should not be connected externally). This is the device's resting state in this mode and represents the safest possible configuration of the device when powered. When the external state signal goes high, the

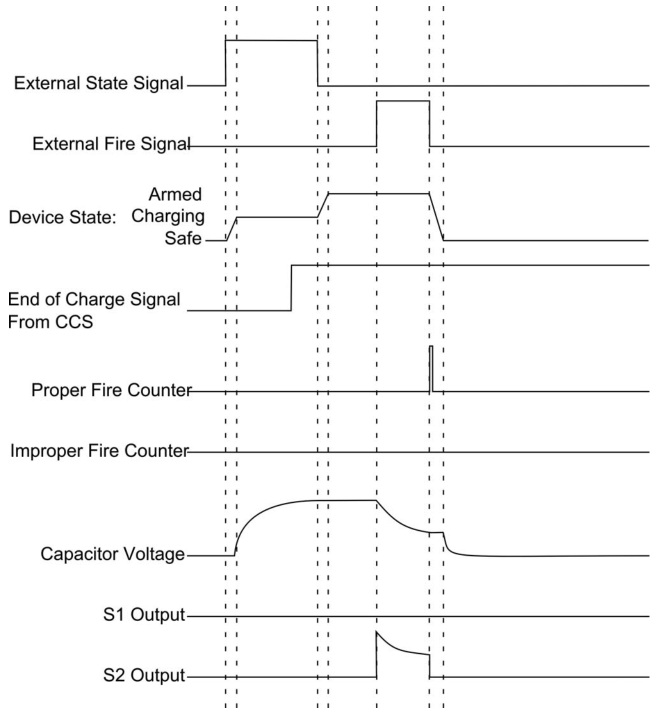

FIG. 6. A cartoon timing diagram illustrating the proper functioning of the device running in single-output (S2 only) mode. In this mode, the external state signal is used to envelop the charging, with rising edges representing the beginning of charging and falling edges representing the end of charging. The device state is a software state drawn as a three-level line diagram with diagonal lines representing software delays. Note that this is not a voltage trace. In this example, changing to the charging state is a two-step process: first the external state signal triggers the software to transition to the charging state, and some finite time later, the software changes the physical lines to put the device in the charging state. In contrast, the external fire signal has an almost immediate impact on the stimulator itself, allowing synchronized timing between the cameras and the stimulation. The proper fire counter increments when the CCS end of charge is high and when the external fire signal has a falling edge. Dashed lines represent concurrent events.

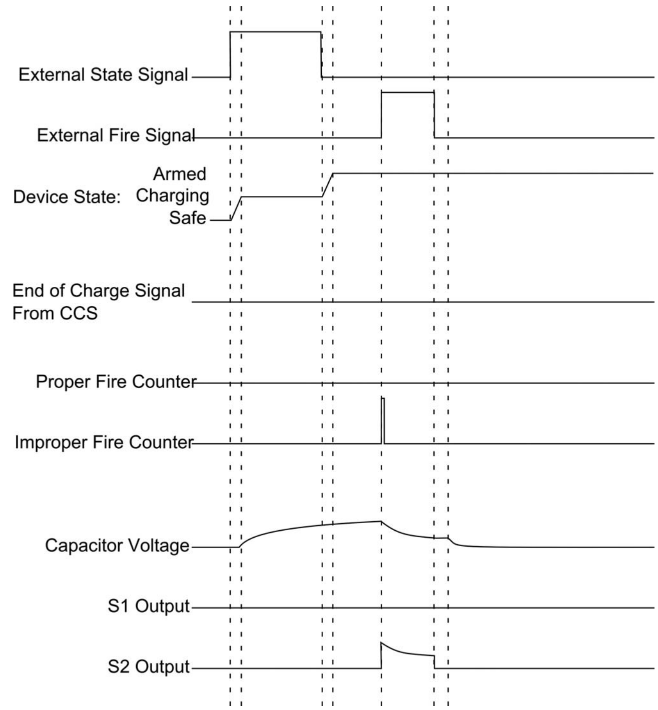

FIG. 7. An example equivalent to Fig. 6 except that the CCS has not been provided with sufficient time to fully charge the capacitors to the requested voltage. The end of charge never becomes high, causing the rising edge of the external fire signal to trigger the improper fire counter.

device enters the charging state. When the external state signal goes low, the device enters the armed state. When the external fire signal is switched to high, the capacitors discharge through the load, and when the external fire signal terminates, the output ceases and the proper fire counter is triggered, signaling for return to the safe state.

In the two-output mode (S1/S2 mode), the software responds differently to the signals, as seen in Fig. 8. Now, the external state signal is used to change between S1 and S2 outputs, with low representing the S1 output and high representing the S2 output. Here, the resting state is the armed state, and the control computer cycles through the safe and charging modes as quickly as possible, using the end of charge readback to signal the change from charging to armed. Also, unless the new request voltage is lower than the previous voltage on the capacitors, the system never discharges the capacitors, exemplified by S1 following S2 in Fig. 8. The voltage values of the S1 and S2 pulses are set independently. It is possible to have multiple S2's, although the charging time can be prohibitive if the energy demand is too high, as described above. It is also possible to quickly refire the stimulator using whatever charge is left on the capacitors.

POSSIBLE BIPHASIC OUTPUT

It is important to note that while this device is not biphasic, as described above, a small modification could easily provide that capability and add one more feature to the device that could be of great potential research value. A simplistic approach to making this device biphasic would be to add a third input from the timing computer, called "external polarity," that would directly control the bridge polarization instead of leaving this task to the outboard computer. This would allow switching the polarization during the middle of the discharge. While this solution seems reasonable because we are simply using a diode bridge, the voltages and currents can be so high in this device that any shorts created during the submicrosecond switching time of the bridge transistors might be sufficient to damage the transistors and the capacitors. To properly implement biphasic output, it is necessary only that the external fire be turned off during a small window when the polarity is flipping, but this could be on the order of 10 μs. This could be implemented in software on the timing computer, but a better alternative would be to design a circuit for this gating in hardware. While it is possible to implement a circuit to gate the external fire on changes in external polarity using a complex system of delays, a simpler solution would be to place a rising edge delay circuit at the final two outputs of the bridge logic. This would cause the active half of the bridge to turn off before the other half turned on. A delay of 1–10 μs could be implemented easily by adding an *RC* circuit and a comparator, an optical isolator, or dedicated delay chip. A diode in parallel with the delay circuit would create the rising edge delay and allow the falling edge to remain unchanged.

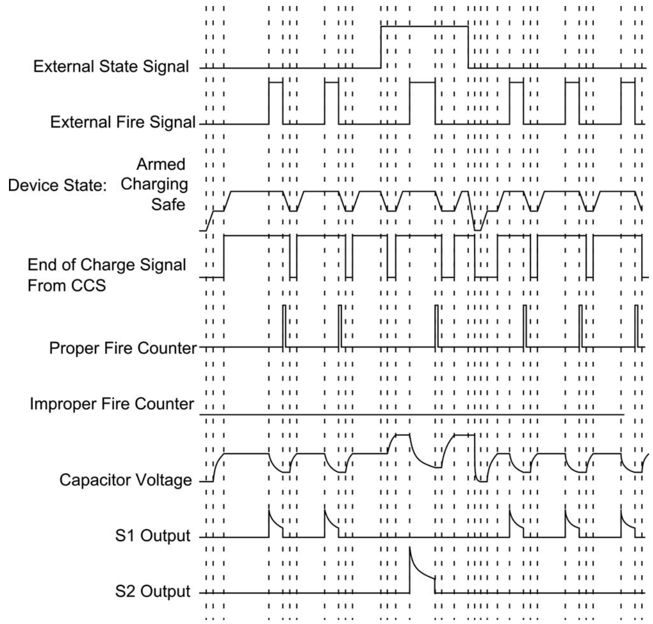

FIG. 8. A timing diagram for the two-output (S1/S2) mode. Unlike the S2 only mode, the external state signal causes a switch between charging up to two different voltages (S1 and S2). If the new voltage is equal or greater to the previously requested voltage, the capacitors are not discharged in between two pulses. However, if the voltage requested is less than the previous one, the capacitors are discharged to reset them, as can be seen in the first S1 after the S2.

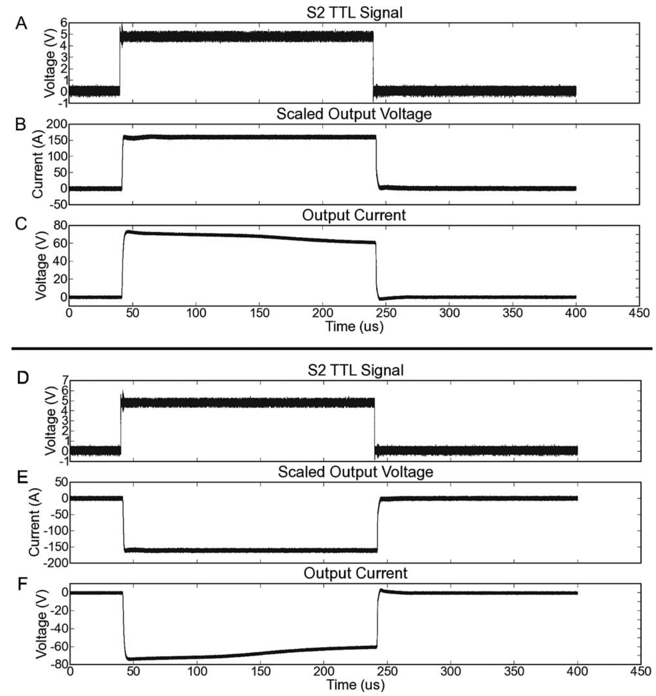

FIG. 10. Temporal voltage traces from the two movies in Fig. 9. The top of each figure is the S2 TTL pulse, the middle is the voltage trace, and the bottom is the current trace. The voltage trace is scaled from the actual voltage because the measuring apparatus involved two electrodes at an arbitrary distance apart placed on either side of the heart in the bath. In reality, the maximum voltage should be within 3% of 500 V. The current in (C) and (F) was measured with a 50 A dc current probe (Tektronix TCP305) that encircled one of the leads between the defibrillator and the heart. The voltage in (B) and (E) was measured with a 100 MHz high-voltage differential probe (Tektronix P5205) connected to Ag–AgCl electrodes in the bath and adjacent to the heart. Each curve has 2.5×10^6 data points recorded with a digital oscilloscope (Tektronix TDS5034B).

EXPERIMENTAL RESULTS

This device has been successfully used to study the field stimulation of the whole heart in a bath.[4,5] Figures 9 and 10 show the action of a very short (200 μs), very strong (500 V) shock applied to a whole heart in a bath. The optical traces were made using a voltage-sensitive fluorescent dye, a high-speed camera, and processing to normalize the signal against a background. This protocol has been described in detail previously.[6] It is clear that the heart is polarized along the direction of the field and behaves oppositely in response to fields of opposite orientation. In looking at Fig. 10, it is clear that the voltage does not decay visibly, and the current does not decay more than about 15%. Also, the pulse has very clean edges on this scale and follows the TTL pulse very accurately. Note that the voltages in the middle trace were measured with Ag–AgCl electrodes placed just around the heart (roughly 4 mm apart) and therefore did not register the full top voltage between the plate electrodes, which should be within 3% of 500 V based on prior measurements.

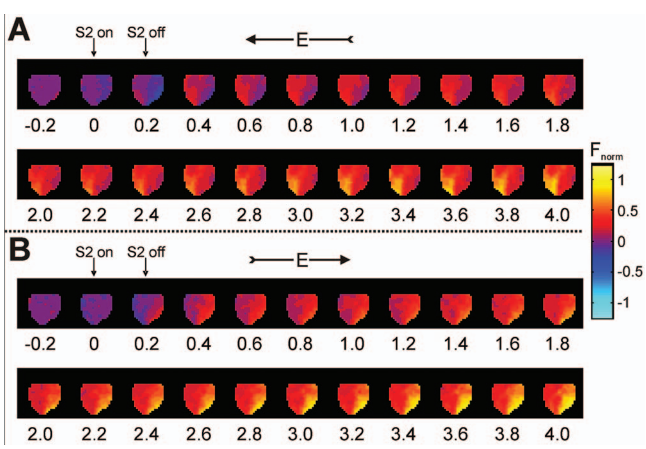

FIG. 9. (Color) An example of the spatiotemporal response of an isolated rabbit heart to strong field stimulation of short duration, as obtained with fluorescence imaging of a dye that is sensitive to the transmembrane potential following a 0.2 ms, 50 V/cm shock. In (A), the electric field is applied from right to left, and in (B), the field is applied from left to right. The numbers below frame indicate the time in ms since the shock onset. Images were acquired with a CCD camera (Redshirt, 26×26 pixels at 5051 frames/s) (from Ref. 8, with permission).

We have also been able to show that long stimuli on the order of 10 ms do not decay below 25% of maximum when stimulating a whole heart in a bath (Fig. 11). This is important when delivering very high energy pulses because fast decay rates can lead to uncertainties in charge delivery. Because these measurements are made with a heart in a large bath, we do not detect the reduction of the resistance during the shock that has been observed with transthoracic defibrillation in animals and is attributed to electroporation.[7]

CONCLUSION

We have demonstrated a versatile, computer-controlled, capacitive-discharge stimulator suitable for scientific inquiries about defibrillation. The device has proven effective in both tests and real cardiac experiments and is flexible enough

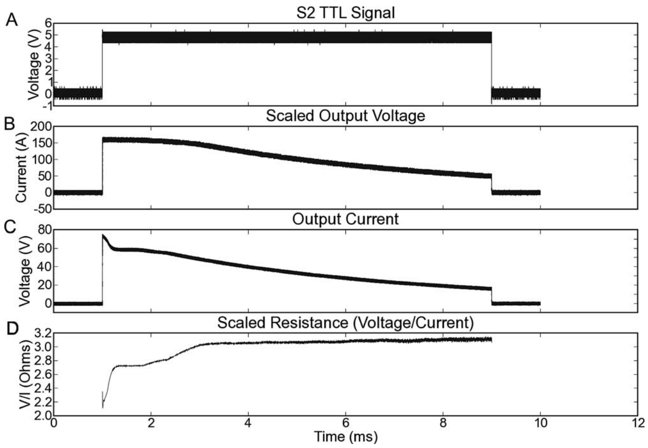

FIG. 11. Voltage and current data from the same heart, but for a longer duration shock. While stimulation strength after 10 ms is less than the maximum due to the voltage decay of the capacitors, it is still significant at almost 30% of the maximum. This was made possible by the large capacitance of the device (750 μs). Panel (D) is the ratio of part (C) to (B), clipped to only the active firing region. The curve is also Gaussian filtered with a sigma of 50 points. The fast upstroke of this curve (first 0.3 ms) is due to the response time of the current probe, and the slower upstroke between 1.5 and 3 ms is probably the result of electrode polarization. The final plateau is consistent with a constant load resistance.

to be of use in a wide range of defibrillation and other cardiac stimulation protocols. The addition of biphasic waveforms would allow the device to be capable of replicating the discharge characteristics of most current defibrillators. As with any high-voltage capacitor-energy storage device, cardiac defibrillators are capable of causing injury or death. The defibrillator design we present may not address all possible failure modes, and hence this device should be used with extreme caution. The design of this defibrillator is not certified by any individual or organization nor is the system intended for use on human subjects. The authors do not accept any responsibility for injury or death that might occur as a result of proper or improper use of this device. Given these caveats, the system we have developed is robust and well suited for a wide variety of cardiac experiments.

ACKNOWLEDGMENTS

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[1] J. Maynard Smith, *Some Consequences of Scale* (Cambridge University Press, London, 1968), Chap. 1, pp. 6–17.
[2] J. C. Newton, S. B. Knisley, X. Zhou, A. E. Pollard, and R. E. Ideker, J. Cardiovasc. Electrophysiol. **10**, 234 (1999).
[3] V. P. Nikolski, A. T. Sambelashvili, and I. R. Efimov, IEEE Trans. Biomed. Eng. **49**, 1217 (2002).
[4] M. C. Woods, V. Y. Sidorov, M. R. Holcomb, D. L. Beaudoin, B. J. Roth, and J. P. Wikswo, Heart Rhythm **3**, 751 (2006).
[5] M. C. Woods, M. M. Maleckar, V. Y. Sidorov, M. R. Holcomb, D. N. Mashburn, N. A. Trayanova, and J. P. Wikswo, Heart Rhythm **3**, S181 (2006).
[6] V. Y. Sidorov, M. C. Woods, and J. P. Wikswo, Biophys. J. **84**, 3470 (2003).
[7] R. A. Malkin, D. X. Guan, and J. P. Wikswo, IEEE Trans. Biomed. Eng. **53**, 1901 (2006).
[8] M. C. Woods, *Field Stimulation of the Diastolic Rabbit Heart: The Role of Shock Strength and Duration on Epicardial Activation and Propagation* (Vanderbilt University, 2005), Chap. 6, pp. 109–138.