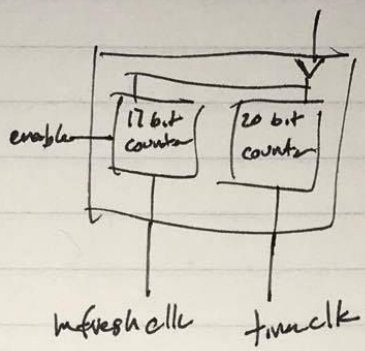
a) HLSM DESIGN

TOP:

Inputs: startstop, reset, sw[7:0], mode[1:0]

Output: an[3:0], sseg[6:0]



• Clkdivider:

in: clk, reset

out: refresh_clk, time_clk

• Stopwatch

IN - clk, startstop, reset, mode[1:0], switch[7:0]

OUT/Registers: reg_d0 - d3, corresponds to each digit.