Lab 2 Report

Name:

UT EID:

Section:

Checklist:

Part 1 –

i. Simulation waveforms for Part 1 for Structural as well as Behavioral modelling (Screenshots)

Part 2 –

ii. Truth table of the function
iii. Algebraic expression of the logic function
iv. Logic circuit schematic
v. Verilog codes for module and testbench for structural modelling
vi. Simulation waveform for structural modelling (Screenshot)
vii. Verilog codes for module and testbench for behavioral modelling
viii. Simulation waveform for behavioral modelling (Screenshot)

Note *–> The Verilog codes should be copied in your lab report, and the actual Verilog (.v) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth table, algebraic expression and circuit schematic, you are free to draw it on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*