LAB 4 Report

Name:

UT EID:

Section:

Checklist:

Part 1 -

i. Simulation waveform of the Flight Attendant Call System for behavioral as well as dataflow modelling
ii. K-map for minimizing the expression for next_state for dataflow modelling
iii. Boolean expression for next_state for dataflow modelling
iv. Completed design file (.v) for dataflow modelling

Part 2 -

v. State Diagram of the Rising Edge Detector
vi. Completed design files (.v) including the top module and clock divider
vii. Test-bench of the system
viii. Simulation waveform
ix. Constraints File (Just the uncommented portion)

Part 3 -

x. Completed design files (.v) of all the modules in the system
xi. Test-bench of the system
xii. Simulation waveform
xiii. Constraints File (Just the uncommented portion)

Note → *The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the* ***actual Verilog (.v), Constraint (.xdc)***

files and Bitstream (.bit) files *need to be zipped and submitted as well on Canvas. You are not allowed to change your codes after final submission as the TAs may download the submitted codes or bitstream files from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*