Lab 5 Report

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**Section:**

Checklist:

Part 1 –

    i.   Design file (.v) for the Ripple Carry Adder

    ii.   Test-bench

    iii.   Complete Table 1 from the simulation

A[3:0]	B[3:0]	Cin	Sum[3:0]	Cout
0001	0101	0	0110	0
0111	0111	0	1110	0
1000	0111	1	0000	1
1100	0100	0	0000	1
1000	1000	1	0001	1
1001	1010	1	0100	1
1111	1111	0	1110	1

Table 1. Testcases for Ripple Carry Adder Verification

    iv.   Constraints File (Just the uncommented portion)

    v.   Simulation waveform for the above test-cases
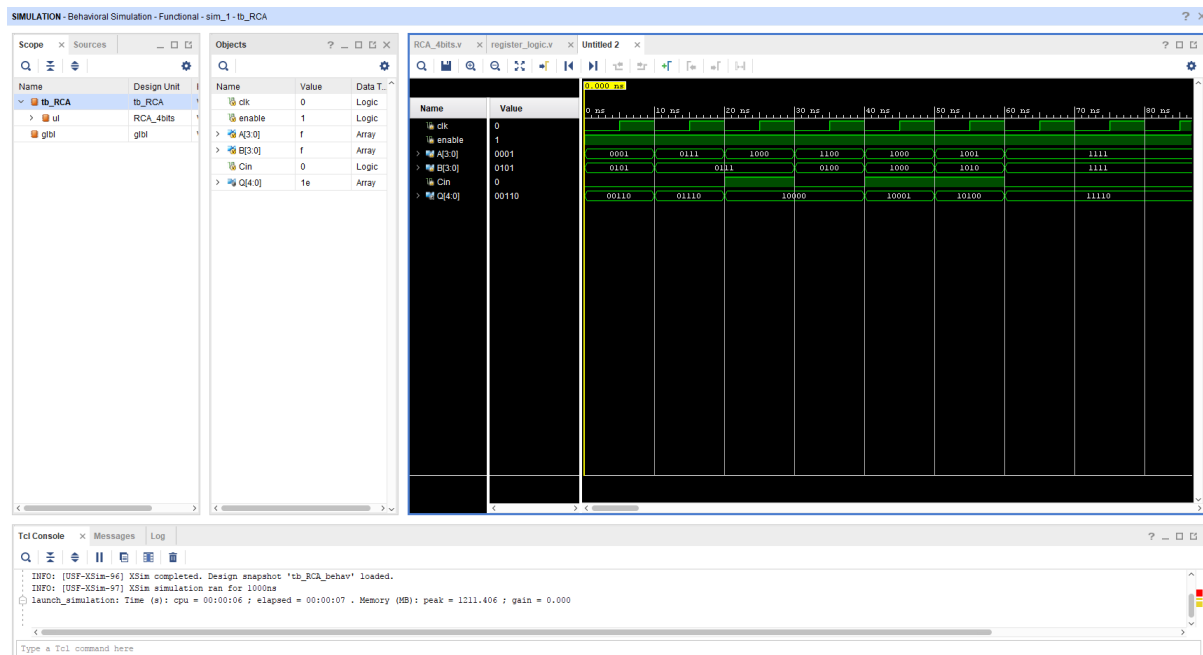
Part 2 –

vi.   All the equations for C_i's and S_i's
- C[0] = Cin
- C[1] = G[0] + (P[0]C[0])
- C[2] = G[1] + (P[1]G[0]) + (P[1]P[0]C[0])
- C[3] = G[2] + (P[2]G[1]) + (P[2]P[1]G[0]) + (P[2]P[1]P[0]C[0])
- C[4] = G[3] + (P[3]G[2]) + (P[3]P[2]G[1]) + (P[3]P[2]P[1]G[0]) + (P[3]P[2]P[1]P[0]C[0])

vii.   Design files (.v) for the Carry Lookahead Adder and Register Logic

viii.   Test-bench

ix.   Complete Table 2 from the simulation

| A[3:0]	B[3:0]	Cin	Sum[3:0]	Cout
0000	0101	0	0101	0
0101	0111	0	1100	0
1000	0111	1	0000	1
1001	0100	0	1101	0
1000	1000	1	0001	1
1101	1010	1	1000	1
1110	1111	0	1101	1

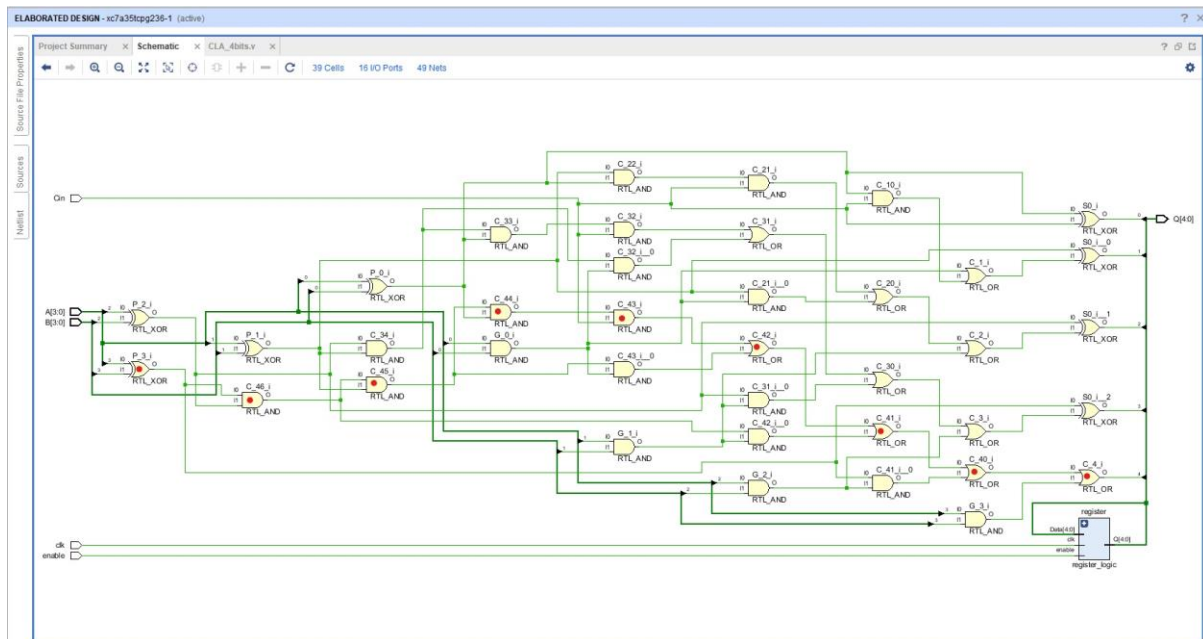**Table 2.** Testcases for Carry Lookahead Adder Verification

x.   Constraints File (Just the uncommented portion)

xi.   Simulation waveform for the above test-cases
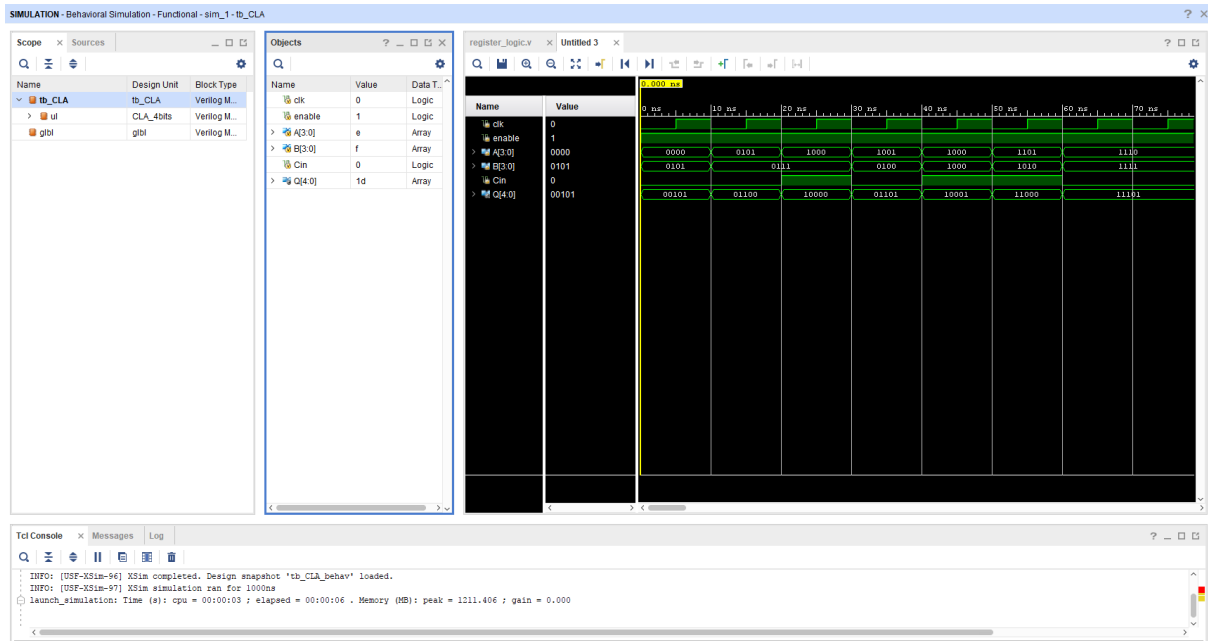
Part 3 –

xii.   Screenshots of the gate-level schematics for both the adder techniques
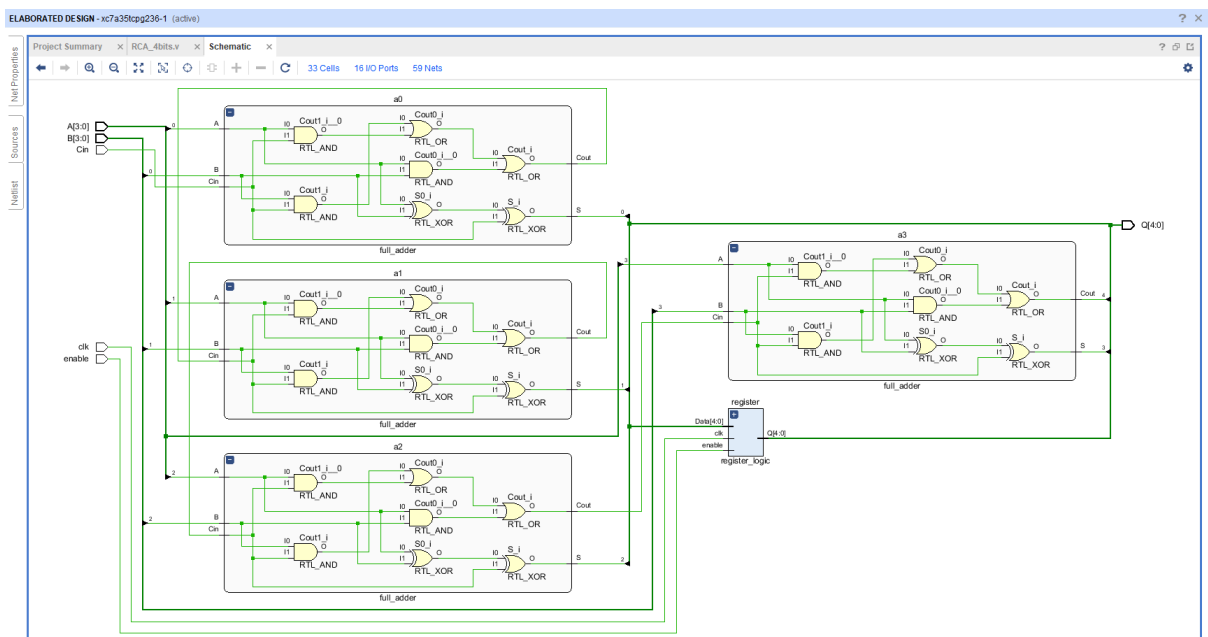
xiii. Delay and area for both the adder techniques showing all the work
- Ripple Carry Adder
  - Delay = 28 ns (By following Cin to Cout) Each full adder has a critical path going from 2nd AND -> 1st OR -> 1st OR (3+2+2 = 7ns)*4 = 28 ns
  - Each full adder contains 3 ANDs, 2 ORs, 2 XORs. Using the table and the given areas for each logic gate, we can calculate the area:
    3(4) + 2(4) + 2(6) = 12 + 8 + 12 = 32 (for 1 full adder)
    4 bit RCA area = 32 * 4 = 128
- Carry Look-ahead Adder
  - Delay = 23 ns (By following the red-dotted path) (3+3+3+3+3+2+2+2+2 = 23 ns)
  - The above RTL design of the CLA contains 20 ANDs, 10 ORs, 8 XORs.
  - 4 bit CLA area = 4(20) + 4(10) + 6(8) = 168

xiv. Brief conclusion regarding the pros and cons of each of the techniques
- RCA
  - Pros
    - Small area = less logic gates, which means that production costs will be cheaper
  - Cons
    - Relatively slow; each Cin is an output from a previous adder (other than the LSB), therefore calculating the sum will take some time in a "ripple" manner
- CLA
  - Pros
    - More efficient; since each carry signal is calculated in advance based on input signals.
  - Cons
    1. As we have higher bit CLAs, the logic blocks get more and more complex, thus having to implement more logic gates than the RCA