

a) FSM DESIGN

TOP:

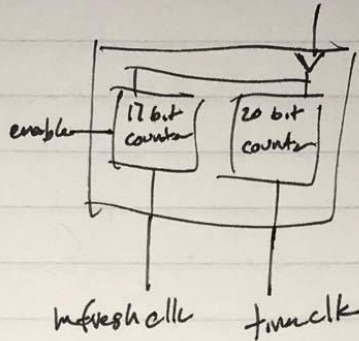
Inputs: startstop, reset, sw[7:0], mode[1:0]

Output: an[3:0], sseg[6:0]

• Clkdvdler:

in: clk, reset

out: refresh_clk, time_clk

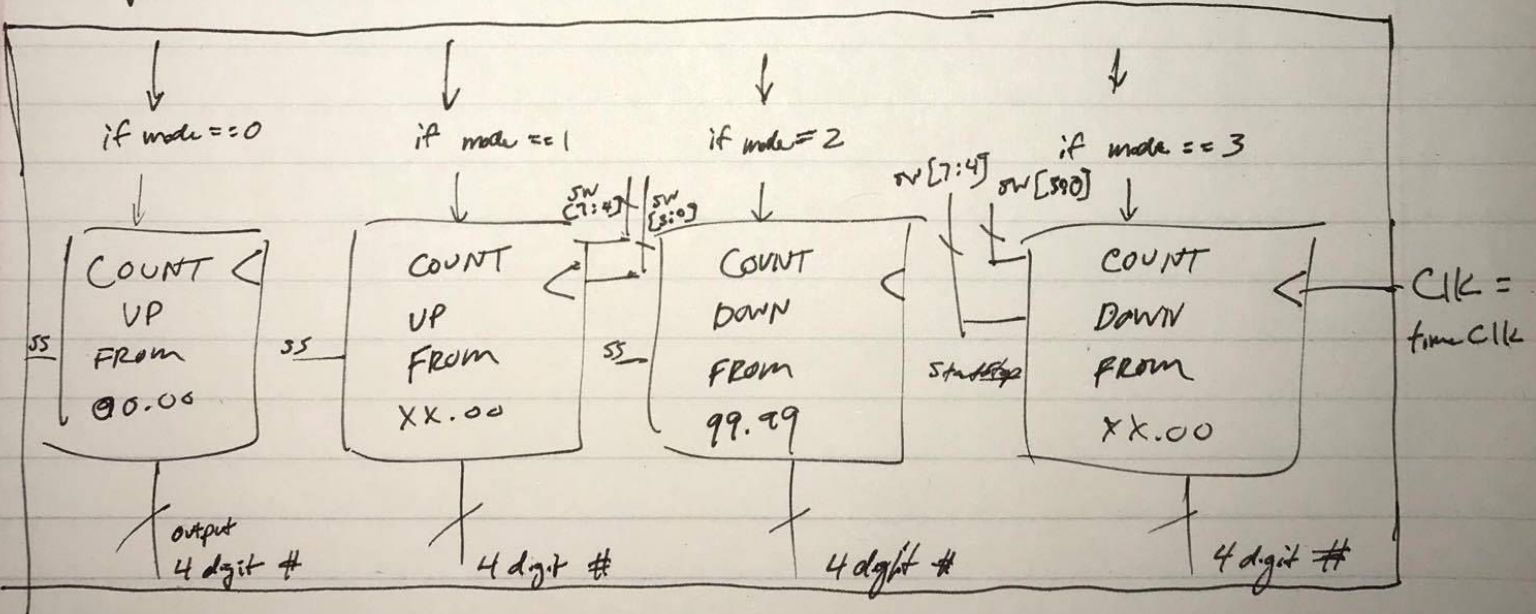


• Stopwatch

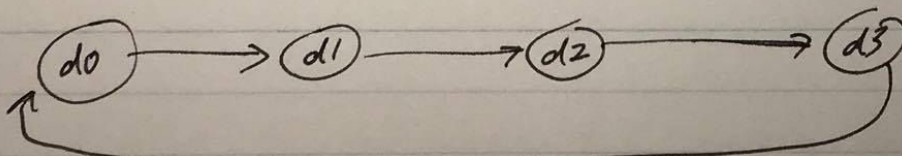
IN - clk, startstop, reset, mode[1:0], switch[7:0]

OUT / Registers: reg-d0-d3, corresponds to each digit.

mode[1:0] / sw[9:8]



sseg_refresh / time_max_state_machine



transitions on each pusedge of clk

clk = refresh_clk