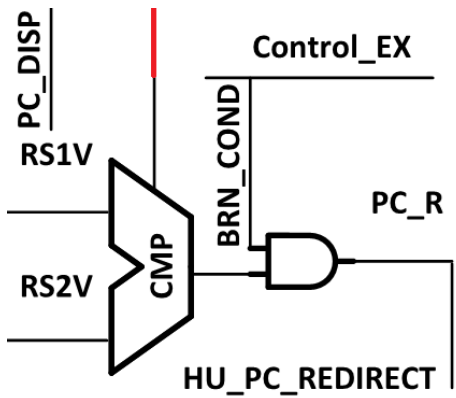
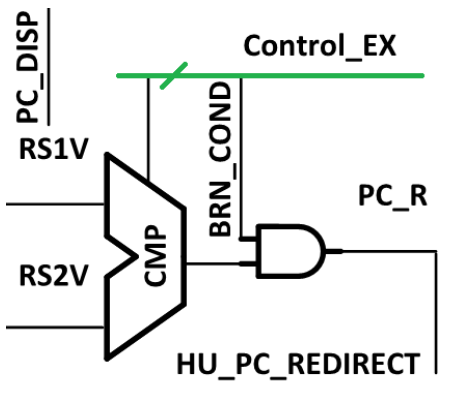


ERRATUM	Original	Fixed
#1. Invalid control signal for comparator in branch logic	 <p>The original logic diagram shows a comparator (CMP) with inputs RS1V and RS2V. Its output is connected to an AND gate along with the BRN_COND signal. The output of the AND gate is PC_R. A red line indicates the Control_EX signal is connected to the BRN_COND input.</p>	 <p>The fixed logic diagram shows the same comparator (CMP) and AND gate structure. However, the green line indicates the Control_EX signal is now connected to the RS1V input of the comparator instead of the BRN_COND input.</p>