MPI 3 RMA

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Why Change RMA?

- "Problems with using MPI 1.1 and 2.0 as compilation targets for parallel language implementations"
  - http://upc.lbl.gov/publications/bonachea-duell-mpi.pdf
  - But note the assumption of cache coherence
- Mismatch with hardware evolution
  - Or not - will GPGPUs be cache-coherent? 1000 core processors?
- Lack of support for "classical" shared-memory operations (including the misnamed "Win_lock"); active messages
- Lack of use by MPI programmers

Possible Topics

- Read-modify-update for MPI RMA
- Blocking RMA routines (with implied sync); what is memory consistency model?
- Respond to Dan Bonachea's paper on why MPI RMA unsuited to UPC with enhancements (such as a different "window" model).
  - Probably includes light-weight replacements
- Changes to MPI RMA for cache coherent systems (good idea or is it too late?) Other RMA models (remote mmap?)

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Scope must include:

- MPI "flavor"
- Portability and Ubiquity
- Performance on the fastest platforms
- Memory consistency with THREAD_MULTIPLE

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