A Physical Based Analytic Model of RRAM Operation for Circuit Simulation

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Abstract

A physical based analytic model of metal oxide based RRAM cell under DC and pulse operation modes is presented. In this model, the transport behaviors of oxygen vacancies and oxygen ions, metal conductivity, electron hopping and heat conduction and the parasitic capacitance and resistance effects are covered. The developed analytic model is verified and calibrated by measured data. Furthermore, we implement the analytic model in a 2×2 RRAM array simulation and investigate the reliability of RRAM array for the first time.

Introduction

Metal oxide based resistive-switching random access memory (RRAM) has attracted considerable interests as next generation of memory technologies [1-4]. Extensive researches have been touched to understand the resistive switching mechanisms and to improve the performance of RRAM [1-6]. For future memory application, the analytic model of a RRAM cell for circuit simulation is required. However, there are few works to address this issue [7]. In this paper, a set of physical based analytic model of the RRAM cell at DC and pulse operation modes are developed and implemented in the circuit simulator for the first time. The model can describe the main features of the RRAM cell under static and transient switching operations. The proposed model is verified and calibrated by the experimental data, and is implemented in circuit simulation. The simulation of a 2×2 RRAM array with parasitic elements is performed to investigate the critical characteristics of the RRAM array such as the reliability.

Modeling of Resistive Switching

It has been commonly accepted that resistive switching is due to formation and rupture of conductive filament (CF) and the switching characteristics are strongly correlated with the geometry of CF as a direct result of generation and recombination of oxygen vacancies (V_O) in the switching oxide layer [5-7]. The physical process of a RRAM device operation is schematically shown in **Fig.1**. In the SET process, both generation of V_O (1) and drift of oxygen ion (O^{2-}) to the top electrode (2)(3) cause the formation of CF connecting anode and cathode, which results in the cell switching to the low resistance state (LRS). For the RESET process, the recombination between O^{2-} and V_O would rupture the CF and the cell is switched to the high resistance state (HRS). The recombination between O^{2-} and electron-depleted V_O is modeled as an energy relaxation process and is described by (4). The top electrode (TE) is active electrode and acts as an O^{2-} reservoir to release or absorb O^{2-}. The electron transport is metallic-like transport along CF and hopping among the disperse V_O. The temperature distribution with multiple heating sources is also modeled by (7). Equations to describe the above physical processes of the RRAM device operation are summarized in **Table. I**.

Analytic Model of RRAM Operation

The stochastic simulation [8] of CF evolution and corresponding I-V curve during the RRAM device RESET operation is shown in **Fig.2**. The results indicate that the process of CF rupture in the RESET operation is corresponding to the whole filament disconnecting firstly at the TE then extending towards the interior step by step with voltage increasing. **Fig.3** shows the CF evolution process and correlated I-V curve obtained from the stochastic simulation [8] during the SET operation. The results reveal that CF growing process is corresponding to the formation of a fine filament in the rupture region firstly connecting the tip of the CF and TE then gradually enlarging along the radius direction with the current increase during SET operation. The final width of CF is w. Based on this insight from the stochastic simulation; we model the CF evolution as shown in **Fig.4**. The gap distance (x) between the rupture CF tip and the TE determines the resistance of HRS during the RESET process [6]. Hence x and dx/dt are the critical factors for RESET process. After RESET, x is fixed to x0, where the x0 and w of the newly grown CF determine the resistance of LRS during the SET process. The dx/dt and dw/dt are the key factors to model the SET transient operation. Here the LRS is modeled by the conduction of CF with a width of w paralleled with a non-linear hopping current as shown in **Fig.5** (a). Under the ultra-low current, w is small and the nonlinear I-V curves at LRS can be reproduced as shown in **Fig.5** (b). The I-V characteristics at HRS are shown

in **Fig.5** (c), which can be modeled as two parallel non-linear hopping currents with different x as shows in **Fig.5** (a). In order to develop the analytic model of a RRAM cell, x, w and their evolving speeds are modeled according to the physical process of RRAM operation as shown in **Fig.1**. Then the analytic model for the RRAM operations including the I-V curves of HRS/LRS and the SET/RESET operation process are set up. The equations and parameters of the model are summarized in **Table II**.

Model Verification

Both DC and transient electric characteristics of metal oxide based RRAM are modeled and compared with the measured data of the fabricated $TiN/TiO_X/HfO_X/TiO_X/HfO_X/Pt$ RRAM devices [9]. The electrical measurements were performed with Keithley 4200 and Agilent 81150A. **Figs.6-7** show the measured and calculated DC I-V curves during RESET and SET processes, respectively. The analytic model can reproduce the gradual RESET and abrupt SET processes, which is consistent with the measured data. The multi-level HRS can be achieved with different stop voltage which corresponds to the different x as shown in **Fig.6**. The relation between the SET voltage and the ambient temperature under DC sweep mode is shown in **Fig.8**. This relation can be quantified by (1); the voltage will decrease as the ambient temperature increase for an established probability of V_O generation. The model predictions agree well with the measured data.

Results and Discussion

The parasitic effects have been considered during the transient operation. The equivalent circuit including the parasitic elements is shown in **Fig.9**. It consists of a parallel capacitance, a large parallel resistance, contact resistance and the resistive switching element. **Figs.10-11** show the model calculated and measured transient response during RESET/SET process. The relations of the voltage altitude to the pulse width during SET/RESET process are shown in **Figs.12-13**. The voltage-time dilemma phenomenon is reproduced by the analytic model. Excellent agreement between the modeling and measured data indicates the validity of the developed analytic model to describe the main features of the RRAM cell operations under both static and transient conditions. By implementing the analytic model in the circuit simulator, a 2×2 RRAM array as shown in **Fig.14** is simulated with half voltage operation schemes to investigate the reliability issue of the RRAM array. The cell resistance after RESET operation with different interconnection resistance is shown in **Fig.15**. The supply voltage for the selected cell decreases with the interconnection resistance increase during the RESET operation, which result in the fail of RESET to the target resistance value. **Fig.16** shows the write operation impact on the adjacent cell. The resistance state transition of cell A from the HRS to LRS after several thousands of operation cycles on cell C is associated with a lower voltage applied on the cell A when the switching operation on the cell C is performed. Those results demonstrate that the presented analytic model will be a powerful tool for the design and optimization of RRAM array.

Conclusion

A physical based analytic model of metal oxide based RRAM cell operation is developed. The developed analytic model verified by measured data which can reproduce the characteristics of RRAM cell operation both under DC and pulse operation modes. Furthermore, we implemented the analytic model in a 2×2 RRAM array simulation, identifying the validity of the developed analytic model in larger scale circuit simulation to optimize the design of RRAM.

Acknowledgements

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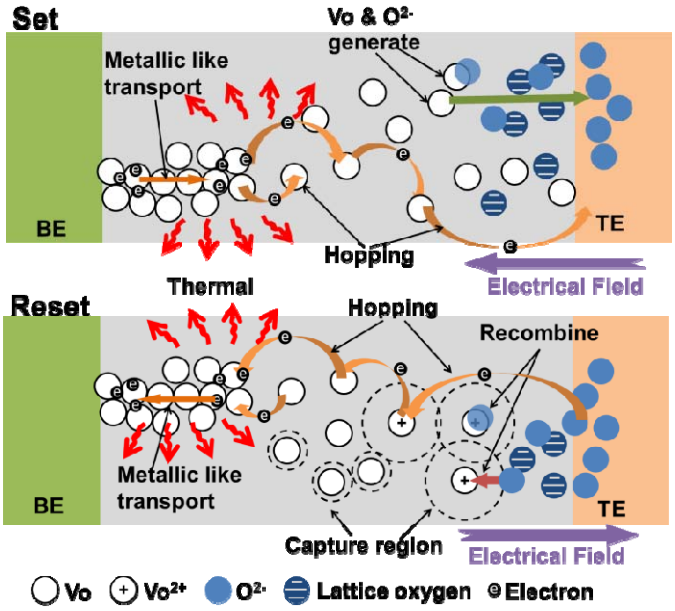

Fig.1 Schematic physical process of resistive switching used in the model, including the generation of oxygen vacancies, oxygen ions hopping, oxygen ions absorbed and released by the electrode, recombination between oxygen vacancies and oxygen ions, local temperature increase due to local current and electron transport.

Table I Equations of resistive switching behaviors

Description	Equation
Generation probability of oxygen vacancies V_O	$P_g(E,T,dt) = fdt\exp\left(-\frac{E_a - \alpha_a ZeE}{k_B T}\right)$ (1)
Probability of O^{2-} hopping from electrode to dielectric layer	$P_m(V,T,dt) = fdt\exp\left(-\frac{E_i - \gamma ZeV}{k_B T}\right)$ (2)
Probability of O^{2-} hopping in dielectric layer	$P_h(E,T,dt) = fdt\exp\left(-\frac{E_h - \alpha_h ZeE}{k_B T}\right)$ (3)
Probability of recombination between O^{2-} and depleted V_O	$P_r(T,dt) = fdt\exp\left(-\frac{\Delta E_r}{k_B T}\right)$ (4)
Transmission probability of electrons between two V_O	$W_{m\to n} = f_{ph}\exp\left(-2\alpha R_{mn} - E_{mn}/k_B T\right)$ (5)
Conductivity of CF	$\sigma = \sigma_0\exp\left(\frac{E_{AC}}{k_B T}\right)$ (6)
Temperature distribution in dielectric layer	$C\frac{\partial T}{\partial t} = \nabla(k\bullet\nabla T) + Q$ (7)

Parameters description: f & f_{ph}: vibration frequency of oxygen atom& electron in V_O; E_a: average active energy of V_O, E_i: the energy barrier between the electrode and oxide; E_h: hopping barrier of O^{2-}; ΔE_r: the relaxation energy during the recombination process; E: located electric field; V: external voltage; Z: charge number; e: unit charge; α_a&α_h: enhancement factor of electric field in the lower of E_a&E_h; γ: enhancement factor of external voltage in the O^{2-} release process. T: located temperature; α: attenuation length of the electron wave function in V_O; R_{mn}: the distance between two Vo; E_{mn}: the energy difference between two V_O; E_{AC}: the active energy of conductive; k: thermal conductivity of oxide; C: specific heat per unit volume of oxide.

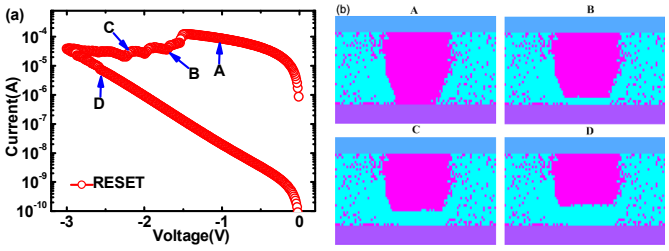

Fig.2 (a) I-V curve in RESET process under DC sweep. (b) CF geometry at different point in (a).

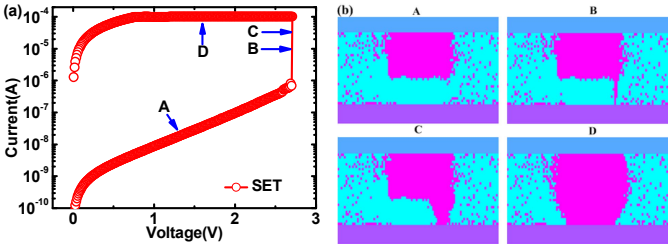

Fig.3 (a) I-V curve in SET process under DC sweep. (b) CF geometry at different point in (a).

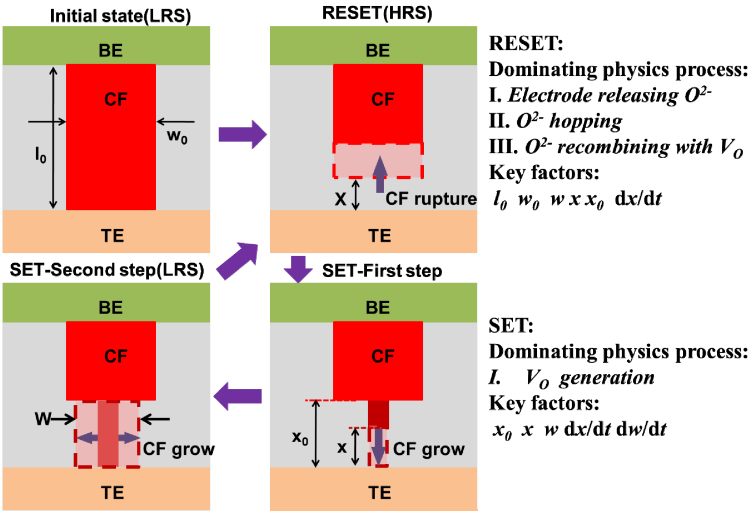

Fig.4 The schematic of CF evolution. The reduction of x in RESET process is determined by the slowest process (I-III) among the dominating processes for the RESET. The SET process is divided into two steps. 1st step: CF growth from the rupture CF tip to the electrode. 2nd step: CF extending along the radius direction of formed CF.

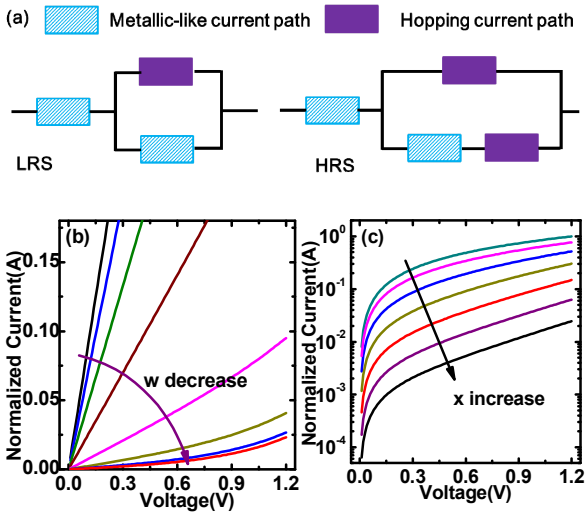

Fig.5 (a) Equivalent circuit of conduction in LRS and HRS; (b) (c) LRS/HRS I-V curves reproduced by the analytic model. The non-linear characteristic in LRS is reproduced by the developed analytic model at small LRS (w).

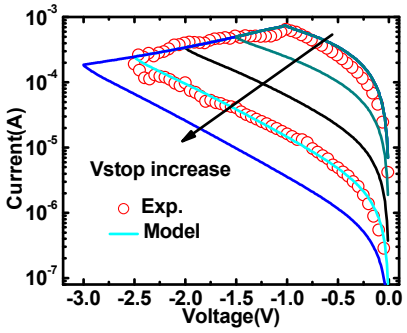

Fig.6 The modeled DC I-V curves during the RESET operation, together with the measured data.

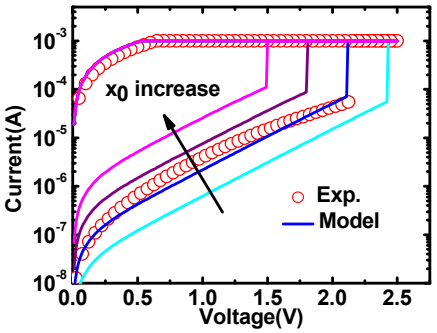

Fig.7 DC I-V curves during the SET operation, together with the measured data.

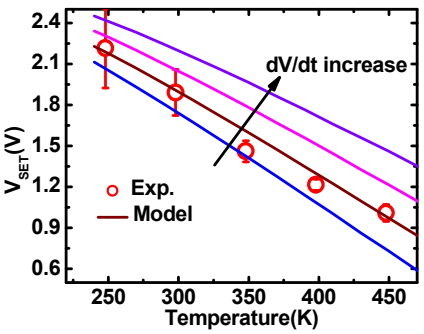

Fig.8 The dependence of SET voltage on temperature under DC sweeps, together with the measured data.

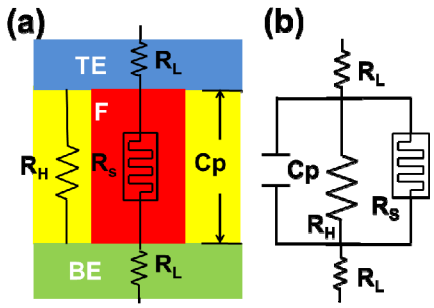

Fig.9 Equivalent circuit of a RRAM cell with parasitic elements.

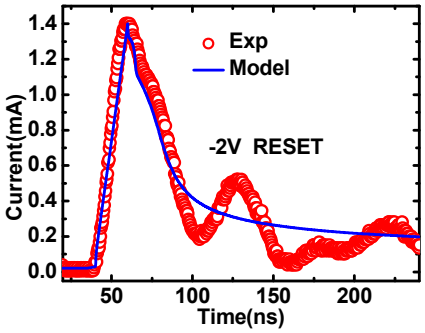

Fig.10 The transient response during RESET process. Excellent agreement between the measured and modeled data is presented.

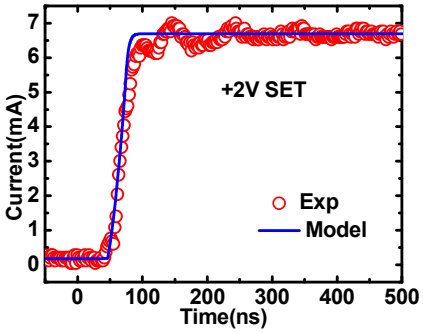

Fig.11 The transient response during SET process. Excellent agreement between measured and modeled data is observed.

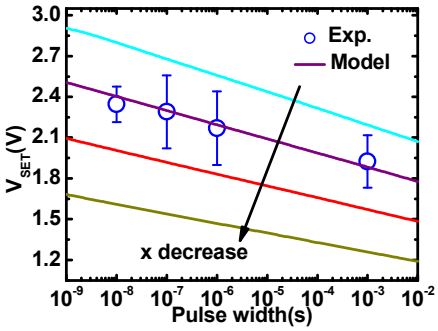

Fig.12 Relation of SET voltage to pulse width. Good fitting between model and measured data is observed.

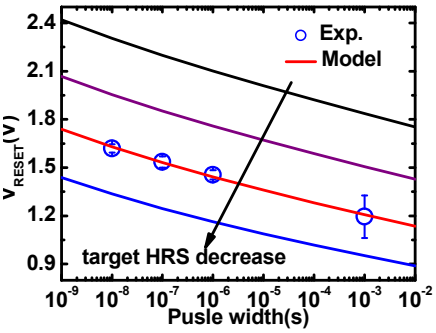

Fig.13 Relation of RESET voltage under different pulse width, which coincides with the model prediction.

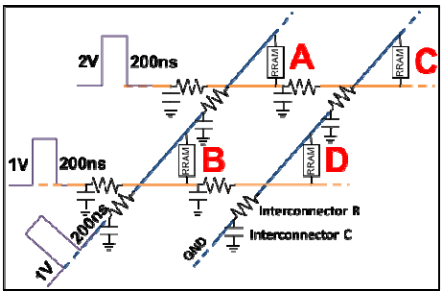

Fig.14 The schematic of 2×2 RRAM array and the operation mode in our simulation.

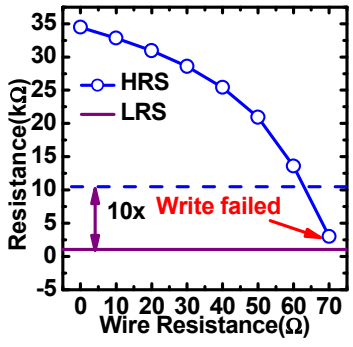

Fig.15 Dependence of the resistance of cell C after 200ns pulse RESET on the interconnection resistance, which indicates low resistance of the interconnection is critical to RRAM array of high reliability.

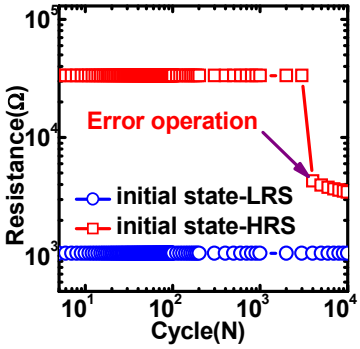

Fig.16 The impact of write cell C on the adjacent RRAM cell A, which suggests the error operation should be considered in the design of RRAM array.

Tabel II The equations in our model

Description	Equation
Rate of CF shortening when RESET process I is dominant	$\frac{dx}{dt} = af\exp(-\frac{E_i - \gamma ZeV}{k_B T})$ (8)
Rate of CF shortening when RESET process II is dominant	$\frac{dx}{dt} = af\exp(-\frac{E_h}{k_B T})\sinh(\frac{\alpha_h ZeV_r}{xk_B T})(x>0)$ (9)
Rate of CF shortening when RESET process III is dominant	$\frac{dx}{dt} = af\exp(-\frac{\Delta E_r}{k_B T})$ (10)
Changing rate of the length of CF in SET process	$\frac{dx}{dt} = af\exp(-\frac{E_a - \alpha_a ZeV_r}{xk_B T})$ (11)
Changing rate of the width of CF in SET process	$\frac{dw}{dt} = (\Delta w + \frac{\Delta w^2}{2w})f\exp(-\frac{E_a - \alpha_a ZeV}{x_0 k_B T})$ (12)
Hopping current in gap region	$I = I_0\exp(-x/x_T)\sinh(V/V_T)$ (13)
Temperature in dielectric layer	$T = T_0 + IVR_{th}$ (14)

Parameters description: a: distance between two V_O; Vr: the potential difference on the gap region; X_T&V_T: the characteristic length & voltage in hopping; R_{th}: the effective thermal resistance; Δw: the effective CF expands width.