High-performance low-power current sense amplifier using a cross-coupled current-mirror configuration

K.-S. Yeo, W.-L. Goh, Z.-H. Kong, Q-X. Zhang and W.-G. Yeo

Abstract: A high-performance current sense amplifier employing a cross-coupled current-mirror configuration is presented. The circuit is designed for low-voltage low-power SRAM applications. Its sensing speed is independent of the bit-line capacitances and is only slightly sensitive to the data-line capacitances. Simulation results have shown that the new sense amplifier gives performance leverage over the conventional sense amplifier circuits in terms of speed and power.

1 Introduction

With the ever-increasing operating frequency, escalation in chip size and growth in packing density reaching the ULSI (ultra-large-scale-integration) level, reducing power consumption becomes particularly imperative. In fact, low-voltage operation is inevitable for future ULSI applications [1–4]. The most efficient way of reducing power dissipation is by scaling down the power supply voltage. However, this leads to serious problems, especially when the capacity of the memory cells increases [5]. By reducing the supply voltage, the readout voltage amplitude on the bit-lines is reduced. As a result, sense amplifiers with high sensitivity are required to detect these signals [5].

The memory capacities of SRAMs have been quadrupling from one generation to another almost every three years [6]. Each of these generations of CMOS SRAMs has been enhanced by reducing the memory cell size by about one-third and increasing the chip size by roughly 1.5 times [6]. However, with the relentless progress in integrated circuit technology, the density of SRAMs in embedded applications has multiplied significantly in recent years [7]. This has inevitably resulted in a rise in both the bit- and data-line capacitances, and hence constituted a major design constraint in achieving higher sensing speed in memory systems.

Speed, power and area are the three most fundamental and crucial design parameters in a memory system. In most cases, a high sensing speed is often achieved by compromising both the power consumption and the silicon area. A novel current sense amplifier, which allows fast access time without sacrificing power dissipation and chip area, is presented in this paper. The performance of this novel current sense amplifier is also compared with three current sense amplifiers reported in the literature [8–10].

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2 Circuit description and operation

Fig. 1 depicts the proposed current sense amplifier, coupled with a simplified read-cycle-only memory system. It comprises seven pMOSFETs (P41, P42, P43, P44, P45, P46 and P47) and six nMOSFETs (N11, N12, N13, N14, N15 and N16). The conventional current sense amplifier [8] with (ideally) zero input resistance during sensing is shown in Fig. 2. This property makes it insensitive to changes in the bit-line capacitance. The hybrid current-mode sense amplifier reported in [9] is illustrated in Fig. 3. Its sensing speed is independent of the bit-line and data-line capacitances. Another current sense amplifier for fast CMOS SRAMs is shown in Fig. 4 [10]. It has the ability to transform into a latch soon after a differential current signal appears at nodes A and B.

The proposed current sense amplifier achieves a high sensing speed without compromising its power dissipation. Its basic idea is to amplify the bit-line current in order to increase the sensing speed. Meanwhile, the new design has extracted the gist of the conventional current sense amplifier by including transistors P41, P42, P43 and P44 forming a conventional current conveyor. As a result, the new circuit is bit-line capacitance insensitive. Fig. 1 also embraces a CMOS amplifier (N15, N16, P45, P46 and P47) and a data-line equalisation circuit.

During the read cycle, when RS2 and CS2 are activated, the memory cell at the lower row is selected, resulting in a higher current flow through BL than that at $\overline{BL}$. These differential current signals that appear at the bit-lines propagate to two pairs of current mirrors (N11, N12 and N13, N14). The current mirrors serve the purpose of increasing the current transmitted from the bit-lines by the same amplification ratio. After current intensification, the bit-line currents are considered sufficiently large to greatly enhance the sensing speed. In spite of this, the current mirrors act as current sinks instead of current sources. Hence, the conventional amplifier (N0, N4, N6, P23 and P24) portrayed in Fig. 2 is not compatible with this novel circuit. The new amplifier (N15, N16, P45, P46 and P47) is therefore designed to use the current sink. Since the current through N12 is larger than that at N13, node E is discharged to a potential lower than node F ($V_E < V_F$). The aspect ratios for N12 and N15 must be carefully designed to sink the current from

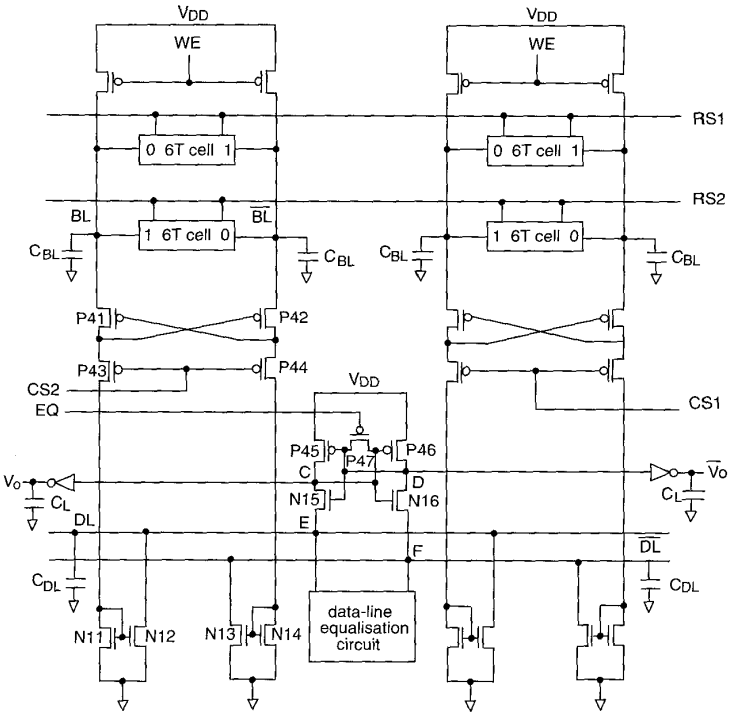

Fig. 1 *Proposed current sense amplifier and a simplified read-cycle-only memory system*

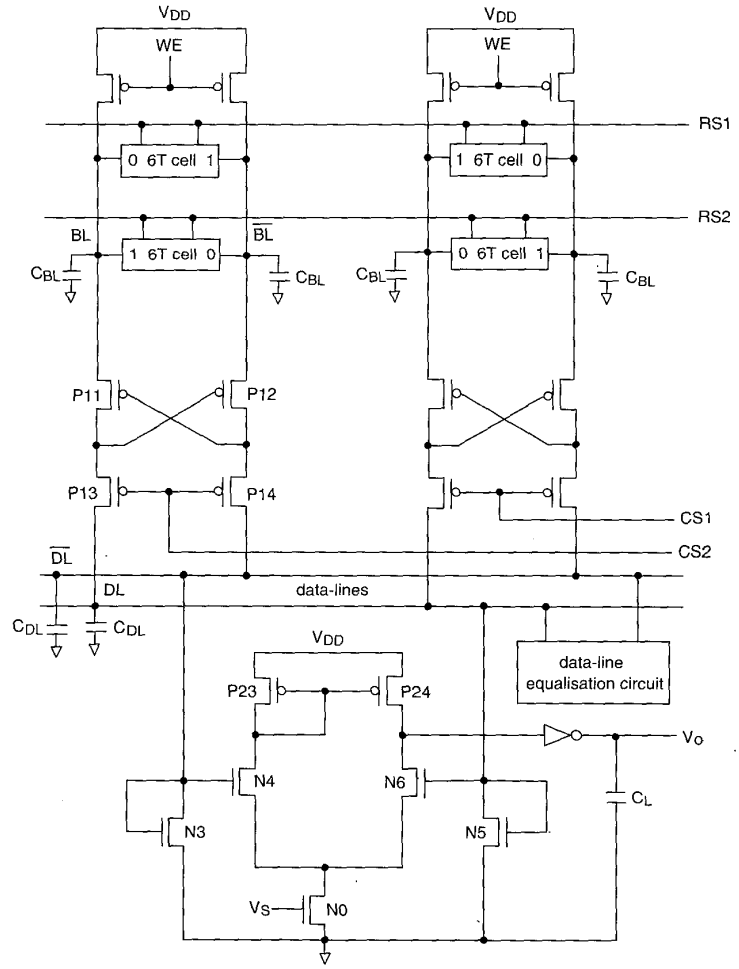

Fig. 2 *Conventional current sense amplifier and a simplified read-cycle-only memory system [8]*

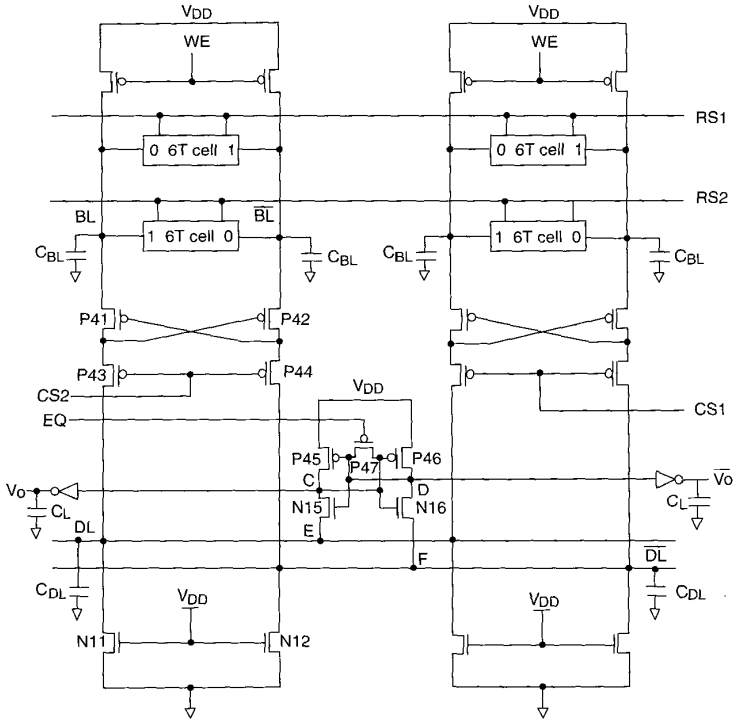

Fig. 3 *Hybrid current-mode sense amplifier and a simplified read-cycle-only memory system [9]*

node C. Coupled with the fact that the gates of N15 and N16 are initially clamped at the same potential by the signal EQ, the magnitude of the gate to source voltage of N15 ($V_{GS(N15)}$) is higher than $V_{GS(N16)}$. To ensure efficient operation of the circuit, the EQ signal can be released after only the current from the bit-lines resides at the data-lines. Owing to the sinking transistor N15 rendering higher V_{GS} than N16, the voltage at node C is lower than the voltage at node D. Furthermore, the amplifier with cross-coupled configuration implies that the source to gate voltage of P45 ($V_{SG(P45)}$) is less than $V_{SG(P46)}$. The current flowing towards node D will therefore be much higher than at node C. The voltage at node D then increases further and the voltage at node C decreases. This process continues until the output V_o reaches V_{DD}. Fig. 5 shows the voltages at the different nodes during a read cycle.

3 Simulation results and performance evaluation

Extensive circuit simulations, using HSPICE, have been carried out to verify circuit operation and characterise its performance. Simulation results are based on the 2 V/0.25 μm CMOS technology from Chartered Semiconductor Manufacturing.

All four circuits (the conventional circuit, the circuits reported in [9, 10] and the new circuit) were simulated together with a simplified read-cycle-only memory system. They were comparatively evaluated in terms of the propagation delay and average power dissipation with different bit- and data-line capacitances. The IC layouts of all four circuits are shown in Figs. 6–9. Their active chip areas are 496.02 μm^2, 340 μm^2, 445.16 μm^2 and 416.15 μm^2, respectively. The layouts are drawn according to the CSM 5M2P n-well p-substrate CMOS design rules. The aspect ratios of the three circuits are given in Table 1.

The effects of bit-line capacitances on both propagation delay and average power consumption are shown in Fig. 10. All the four circuits are insensitive to bit-line capacitances. The new circuit has the lowest propagation delay (i.e. fastest sensing speed), and its power consumption is less than the conventional circuit. Although its power consumption is higher than the circuit reported in [10], it is only 0.6 mW. For the case in which C_L has a capacitive load of 0.1 pF with $C_{BL} = C_{DL} = 1$ pF, the speed of the new circuit is 168%, 7% and 112% faster than the conventional circuit and the circuits reported in [9] and [10], respectively.

The sensing delay with respect to the data-line capacitances is illustrated in Fig. 11. Unlike the conventional circuit and the circuit reported in [10], the sensing delay of the new circuit is not so sensitive to the data-line capacitances. The improvement in speed for the new circuit is even more pronounced at higher data-line capacitances. For the case in which C_L has a capacitive load of 0.1 pF with $C_{BL} = 1$ pF, $C_{DL} = 5$ pF, the speed of the new circuit is 317%, 15% and 289% faster than the conventional circuit and the circuits reported in [9] and [10], respectively. The proposed circuit is therefore very suitable for use in high-speed low-power SRAMs.

4 Conclusion

A high-performance current sense amplifier with high sensing speed is reported. The new circuit is appropriate to applications in a low-voltage low-power environment. It has been simulated using HSPICE to confirm its superiority over existing current sense amplifier circuits. With almost equivalent chip area, the new circuit promises a much lower sensing delay and permits low power consumption based on the 2 V/0.25 μm CMOS technology. At capacitances $C_L = 0.1$ pF, $C_{BL} = 1$ pF and $C_{DL} = 5$ pF, the proposed

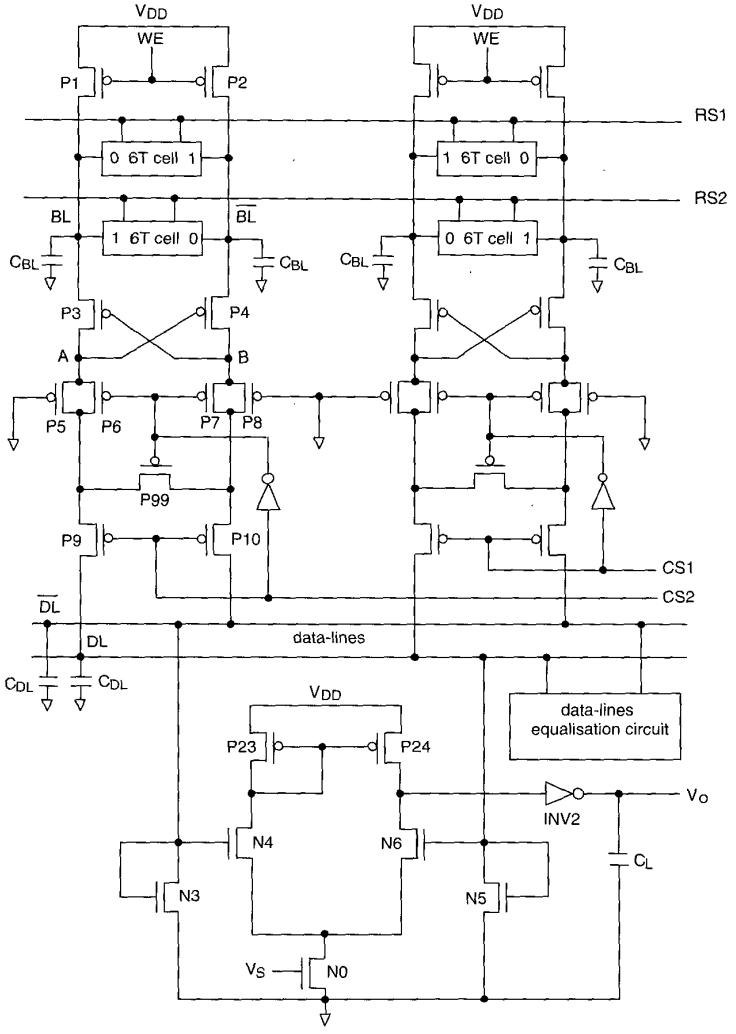

Fig. 4 *Current sense amplifier reported in [10] and a simplified read-cycle-only memory system*

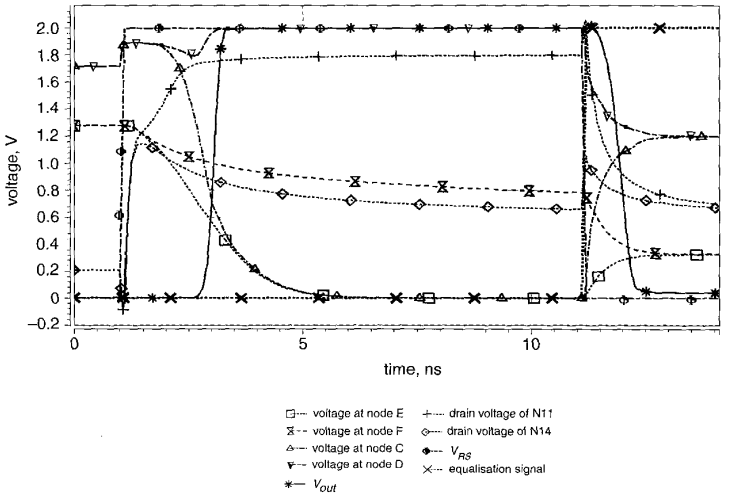

Fig. 5 *Transient waveform of voltages at various nodes for 2 V/0.25 μm technology*
$C_L = 0.1\,\text{pF}$, $C_{BL} = 1.0\,\text{pF}$ and $C_{DL} = 5.0\,\text{pF}$

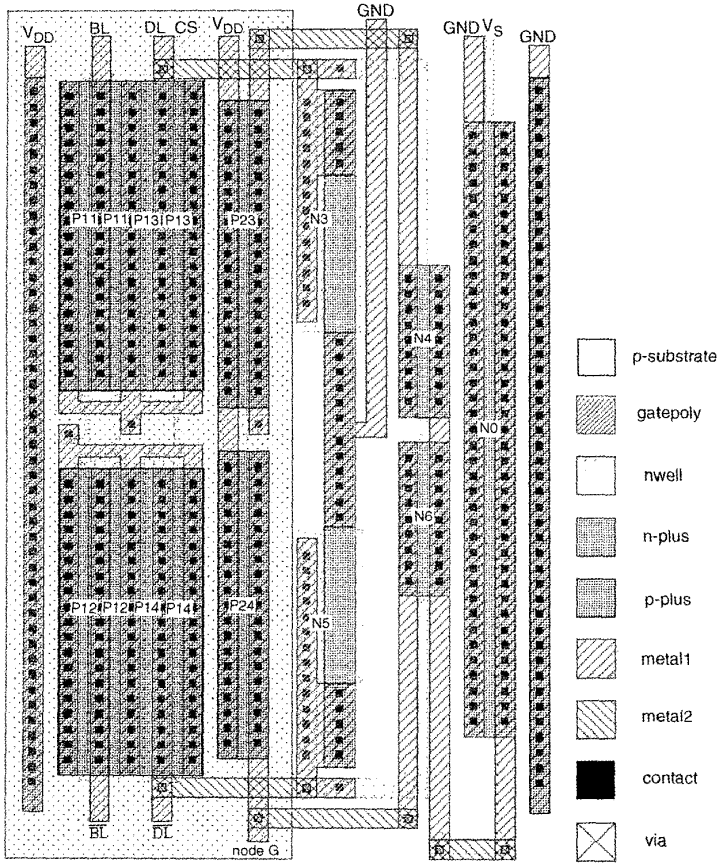

Fig. 6 *Layout of the conventional sense amplifier [8]*

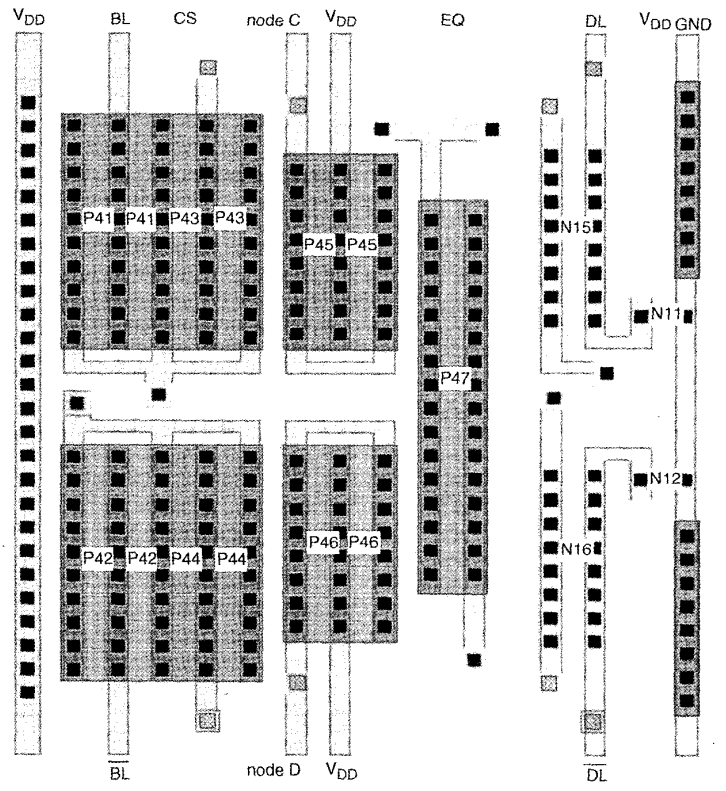

Fig. 7 *Layout of the hybrid current-mode sense amplifier [9]*

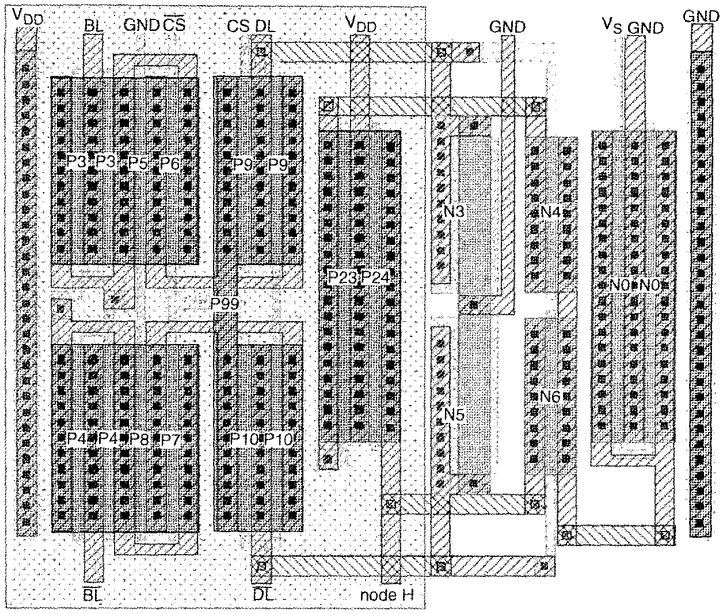

Fig. 8 *Layout of the sense amplifier reported in [10]*

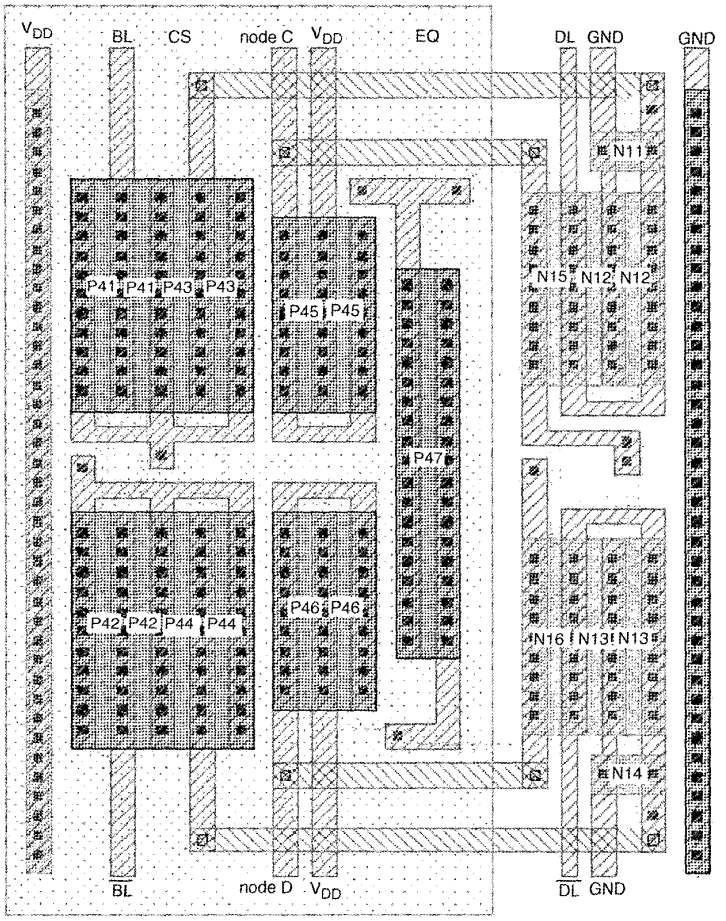

Fig. 9 *Layout of proposed sense amplifier*

Table 1: Aspect ratios of the transistors for the conventional circuit, the circuits in [9, 10] and the new sense amplifier circuit

Transistor	Conventional circuit *W/L*, μm/μm	Circuit reported in [9] *W/L*, μm/μm	Circuit reported in [10] *W/L*, μm/μm	New circuit *W/L*, μm/μm
P3	—	—	12/0.25	—
P4	—	—	12/0.25	—
P5	—	—	6/0.25	—
P6	—	—	6/0.25	—
P7	—	—	6/0.25	—
P8	—	—	6/0.25	—
P9	—	—	12/0.25	—
P10	—	—	12/0.25	—
P11	20/0.25	—	—	—
P12	20/0.25	—	—	—
P13	20/0.25	—	—	—
P14	20/0.25	—	—	—
P23	10/0.25	—	10/0.25	—
P24	10/0.25	—	10/0.25	—
P41	—	12/0.25	—	12/0.25
P42	—	12/0.25	—	12/0.25
P43	—	12/0.25	—	12/0.25
P44	—	12/0.25	—	12/0.25
P45	—	10/0.25	—	10/0.25
P46	—	10/0.25	—	10/0.25
P47	—	10/0.25	—	10/0.25
P99	—	—	0.75/0.25	—
N0	20/0.25	—	20/0.25	—
N3	1/5	—	1/5	—
N4	5/0.25	—	5/0.25	—
N5	1/5	—	1/5	—
N6	5/0.25	—	5/0.25	—
N11	—	1/0.25	—	1/0.5
N12	—	1/0.25	—	10/0.25
N13	—	—	—	10/0.25
N14	—	—	—	1/0.5
N15	—	5/0.25	—	5/0.25
N16	—	5/0.25	—	5/0.25

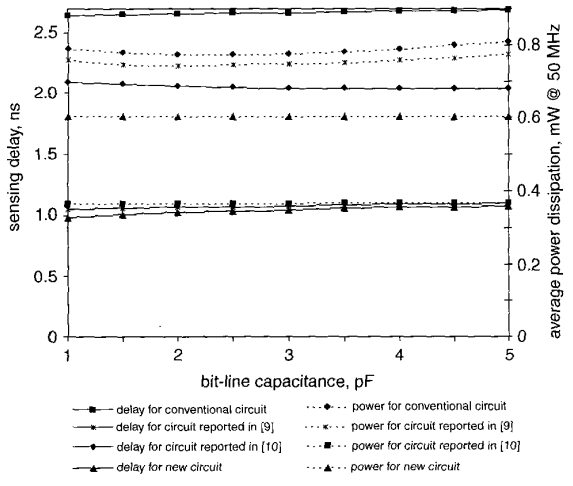

Fig. 10 *Sensing delay and average power dissipation against bit-line capacitances for 2 V/0.25 μm technology*
$C_L = 0.1$ pF, $C_{DL} = 1.0$ pF

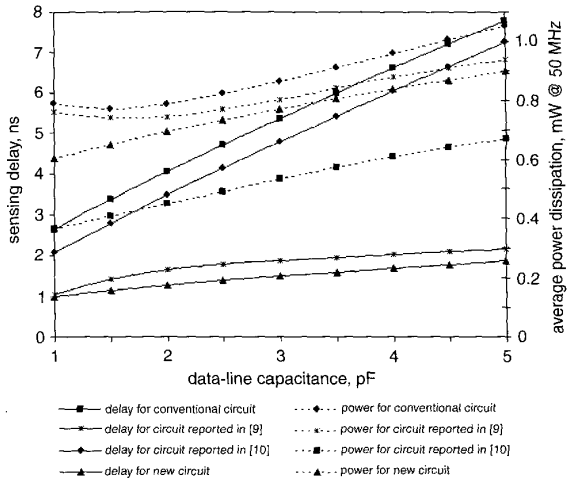

Fig. 11 *Sensing delay and average power dissipation against data-line capacitances for 2 V/0.25 μm technology*
$C_L = 0.1$ pF, $C_{BL} = 1.0$ pF

circuit improves the sensing speed by 317% compared to the conventional current sense amplifier and 15% and 289% when comparison is made with the amplifiers presented in [9] and [10], respectively. Also, the new circuit exhibits a spectacular decrease in sensing delay sensitivity with respect to the data-line capacitances, i.e. only an insignificant 220 ps/pF compared to 1292 ps/pF, 275 ps/pF and 1288 ps/pF for the conventional circuit and the circuits reported in [9] and [10], respectively.

5 Acknowledgment

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