Highly Scalable Non-volatile Resistive Memory using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses

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Abstract

Simple binary-TMO (Transition Metal Oxide) Resistive Random Access Memory named as OxRRAM has been fully integrated with 0.18μm CMOS technology, and its device as well as cell properties are reported for the first time. We confirmed that OxRRAM is highly compatible with the conventional CMOS process such that no other dedicated facility or process is necessary. Filamentary current paths, which are switched on or off by asymmetric unipolar voltage pulses, made the cell properties insensitive to cell or contact size promising high scalability. Also, OxRRAM showed excellent high temperature performance, even working at 300°C without any significant degradation. With optimized TMO material and electrodes, OxRRAM operated successfully under 3V bias voltage and 2mA switching current at a TMO cell size smaller than $0.2\mu m^2$.

Introduction

Resistive memories, which can vary their resistance depending on applied voltage, were intensively studied from the 1960s to early 1980s for device applications (1). For example, chalcogenide materials, semiconductors, various kinds of oxides and nitrides, and even organic materials were found to have resistive memory properties. However, high operation voltage and current, poor endurance, and low film handling technique made the resistive memory unfavorable in comparison with capacitive memories.

With the remarkable progress in material science, resistive memory started to attract the research community's interest again as a nonvolatile, low power, high density, and multi-bit operating memory. Perovskite oxides such as Cr-doped $SrTi(Zr)O_3$ (2), $Pr_{0.7}Ca_{0.3}MnO_3$ (3), $PbZr_{0.52}Ti_{0.48}O_3$ (4) were reported to show memory switching by electric pulses of reasonably small voltage and current. However, perovskite oxides consist of more than 3 components, and thus are not easily applicable to normal semiconductor manufacturing processes because their crystal structure and stoichiometry are hardly controllable. Moreover, the substrate should have a well-defined crystal structure for required film quality, and an efficient etching process has not been proposed yet. In this respect, binary TMOs have great advantages not only in their compatibility to CMOS processes but also in their resistance to thermal or chemical damages.

Switching Mechanism

It is well known that defects of TMO films generate impurity states in the band gap. For example, metal or oxygen vacancies generate density of states near the valance or conduction band respectively, while metallic defects do the same just above the electrode Fermi level as described in Fig. 1 (a). Clockwise and anti-clockwise V-I loop is generated when switching from high to low resistance state and from low to high resistance state respectively as in Fig. 1 (b). We propose that in the low resistance SET state, current due to empty metallic states above Fermi level in the conductive filament decreases as these states become filled with injected charges by increased bias voltage (5). In the high resistance RESET state, current increases due to the enhanced polaronic conduction in metal vacancy states, which is by heating and percolation effects as well as discharge of previously stored charge in the metallic defect states (6).

Experimental

An OxRRAM test vehicle is fully integrated based on 0.18μm CMOS technology. A TEM image and the corresponding schematic of the fabricated 1T1R OxRRAM cells as well as basic circuit diagram of memory cell array are presented in Fig. 2. Inset of Fig. 2 (a) is an active cell, which has simple MIM structure composed of a thin polycrystalline TMO layer and two noble metal electrodes. The TMO layer is deposited with either reactive sputtering or plasma oxidation of thin metal layer. TMO cells are easily patterned by conventional dry etch process, though TMO patterning is not necessary once BE or TE is isolated.

Cell and Device Properties

As-deposited TMO films are normally insulators. After a process similar to soft break down called 'forming', conducting paths showing reversible bi-stable switching are made. Fig. 3 shows typical switching characteristics of TMO cells. A voltage pulse is required to switch from low

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resistance set state to high resistance reset state, while a current-limited voltage pulse is required for switching back to the set state. It is noticeable that switching takes place independent of bias polarity. Since set voltage (V_{set}) is always higher than reset voltage (V_{reset}) and reset current (I_{reset}) is always higher than set current (I_{set}), the TMO cell can be programmed into either set or reset state from any previous state by choosing proper pulse voltage and current. Also, the cell resistance can be read by voltage pulse less than V_{reset} without affecting the stored data. Voltage and current of each programming pulse is summarized in Fig. 4.

As many binary TMOs are known to have memory switching properties, we tested several TMOs, which are easily applicable to semiconductor processes to find the one having the lowest programming voltage and current. Fig. 5 (a) and (b) show that NiO has the lowest I_{set}, I_{reset}, and forming voltage (V_{form}) among the tested materials. Also, Fig. 5 (b) shows that V_{form} depends linearly on film thickness. From these results, we chose TMO film thickness to be the thinnest possible while still conserving its switching properties. In addition, we found oxidation control is very important for low voltage and current operation. In the case of NiO, Fig. 6 (a) shows V_{form} can be reduced down to 1.5V by under-oxidation, where V_{form} and V_{set} are close enough that separate forming step is not necessary. Fig. 6 (b) shows that programming current can be reduced by oxygen control, the trend shows that the highest necessary current, I_{reset}, also decreases with under-oxidation. As for the electrodes, we would like to comment that poly Si or some non-noble metals were also tested as electrodes, but noble metals provided more reliable memory switching performance.

Cell size dependence also gives very interesting results. Fig. 7 demonstrates that the resistance of fresh cells decreases inversely proportional to the cell size, while reset resistance (R_{reset}) and set resistance (R_{set}) decrease only slightly as cell size increases. Also, threshold voltages do not change with cell size variation. This result indicates that only a finite sized filament in the active material switches between R_{set} and ~100kΩ with constant programming voltages regardless of cell or electrode size. Size insensitive performance provides a great advantage in scalability because the narrow process margin from scaling down does not matter any more.

As for programming speed, OxRRAM cells can be stably set with a 10ns pulse. A single 5μs pulse or multiple 100ns pulses are necessary for reset as shown in Fig. 8.

OxRRAM has excellent thermal property. Fig. 9 shows stable high temperature programming is possible up to 300°C without any degradation of sensing margin (R_{reset}/R_{set}) or any change in programming condition. Fig. 10 demonstrates that more than 10^4 times of set/reset cycling at 200°C does not reduce the sensing margin.

The results of cycling and reading endurance test are shown in Fig. 11 and 12. More than 10^6 times of set/reset cycles have been confirmed guaranteeing sensing margin of 10. All failures were due to shorts during cycling. For the reading endurance, no sign of degradation in cell resistance has been observed after reading more than 10^{12} times by 0.4V reading voltage.

For retention tests, pre-programmed cells are baked at high temperature as in Fig. 13. Although the number of failed cells increases for the first day, no more failures has been observed after that. As all of the failures were soft failures, annealing could effectively reduce the number of early failing cells. Fig. 14 shows that 300 hours of baking at 150 °C makes only minor change in switching curves. Long-term stability of cell resistance is being monitored. So far, the cell has remained stable for more than 8 months at room temperature as shown in Fig. 15.

Conclusion

World premier binary-TMO based RRAM (OxRRAM) has been successfully demonstrated. Operating below 3V and 2mA, 10^6 times of set/reset and 10^{12} times of reading cycles have been confirmed. Due to cell size independent properties and the simplicity of integration process, OxRRAM is proposed to be one of the most promising candidates for next generation high-density low-cost non-volatile memory. Also, OxRRAM has good tolerance for thermal budget and no contamination issue, so that it can be easily embedded in other devices.

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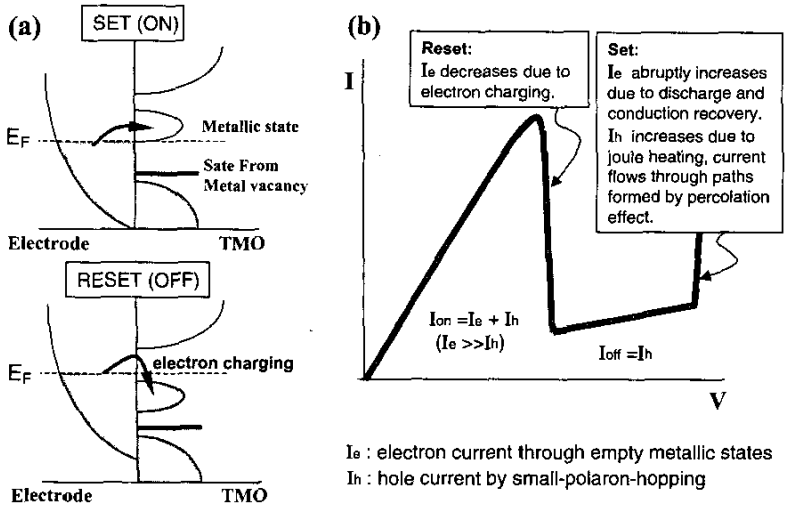

Fig.1 (a) Band diagrams of an electrode and TMO in ON and OFF states. (b) Proposed mechanisms.for reset and set switching.

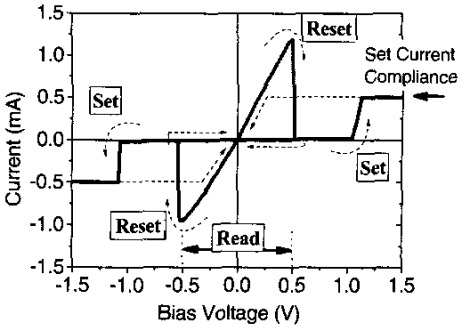

Fig.3 Typical I-V curves of the OxRRAM switching in voltage sweeping mode. Switching is possible with either positive or negative bias voltage and set current compliance. Voltage ranging from 0 to reset threshold can be used for reading.

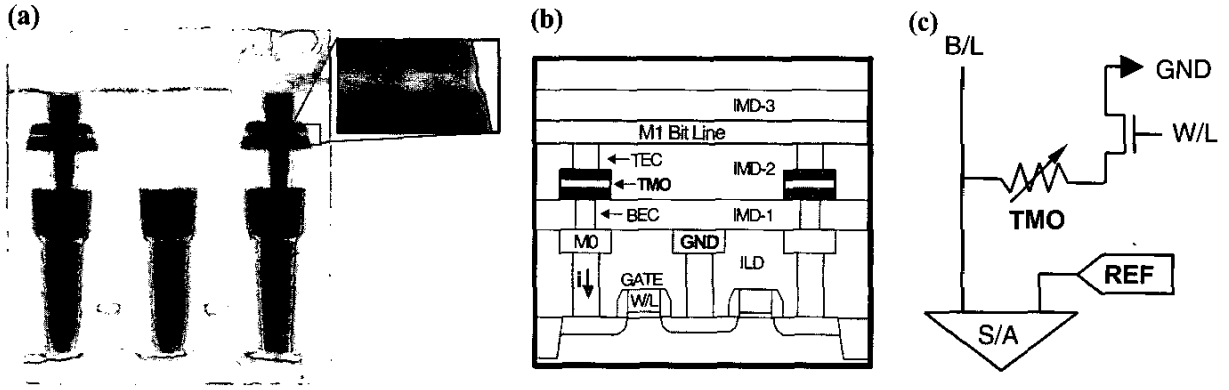

Fig.2 (a) Cross-sectional TEM image of fully integrated OxRRAM cell array with magnified polycrystalline TMO inset, (b) corresponding schematic diagram.and (c) basic circuit diagram of OxRRAM memory cell array.

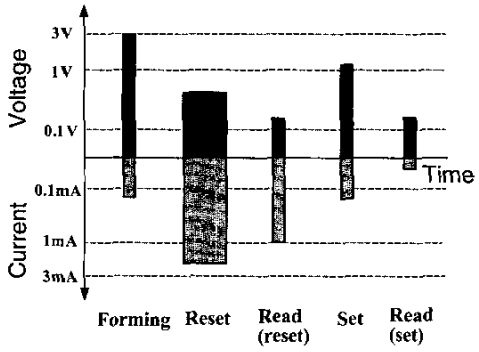

Fig.4 Voltage and current levels of test programming pulses. Pulse width is on the order of ns for forming, read and set, and is on the order of μs for reset.

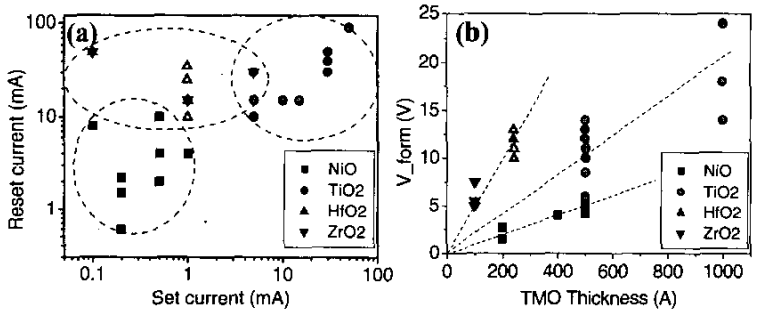

Fig.5 (a) Set and reset currents distribution at various conditions for each TMO materials. (b) Forming voltage and its thickness dependence for each TMO materials.

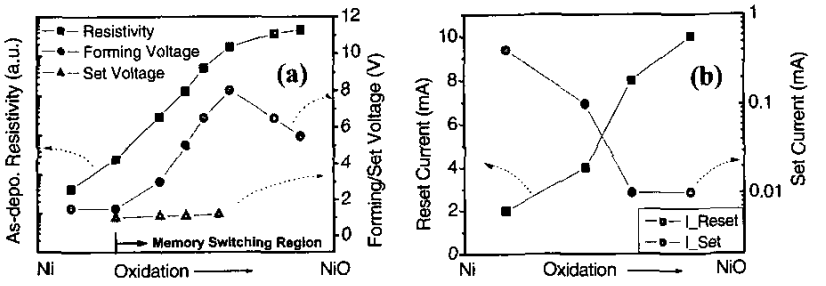

Fig.6 (a) As-deposited resistivity and forming voltage as a function of Ni oxidation. Forming voltage becomes closer to set voltage as NiO is under oxidized in the memory switching region. (b) Set and reset current changes as a function of Ni oxidation.

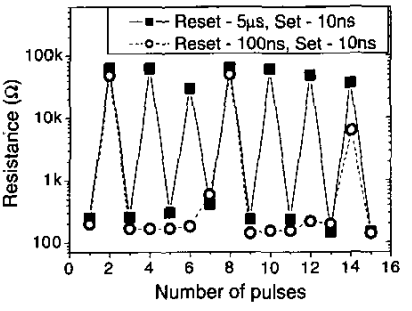

Fig.8 Pulse dependent switching behavior with 5μs/100ns reset pulses and 10ns set pulses applied one after the other.

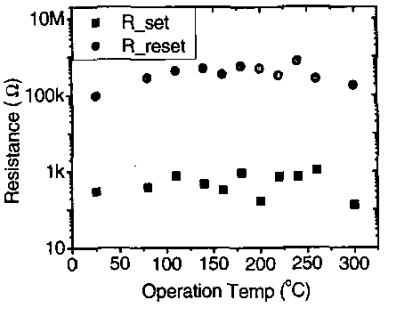

Fig.9 Resistances of set and reset cells with 0.3x0.7μm² size while switching at high temperature up to 300°C.

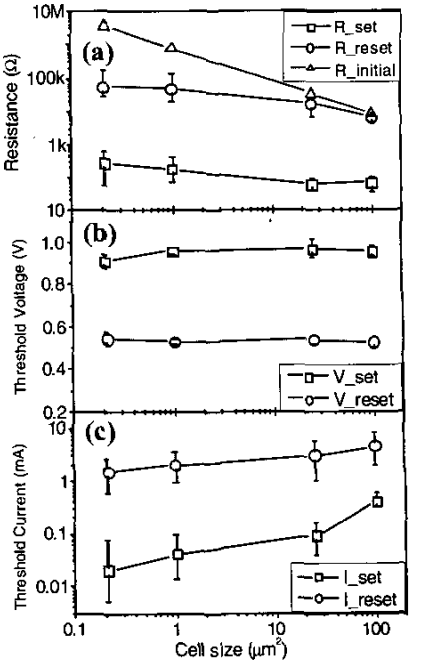

Fig.7 Cell size dependence of (a) resistance, (b) threshold voltage, and (c) threshold current in each state.

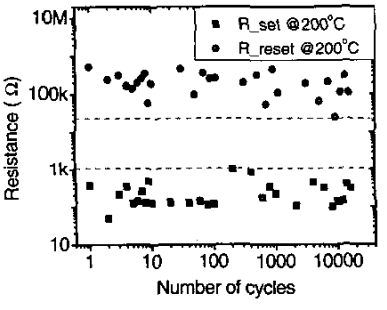

Fig.10 Set/Reset cycling endurance with 0.3x0.7μm² cell at 200°C.

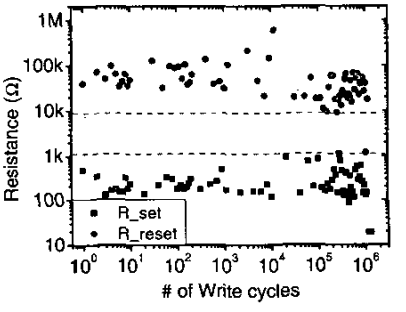

Fig.11 Set/Reset cycling endurance with 0.3x0.7μm² cell at room temperature.

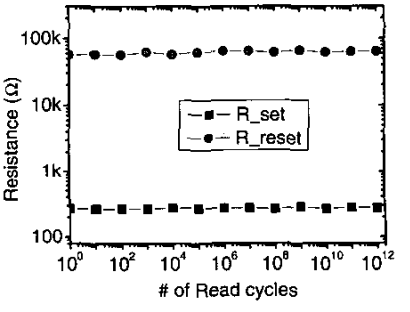

Fig.12 Reading endurance for high and low resistance states of a 0.3x0.7μm² cell with 0.4V reading pulses.

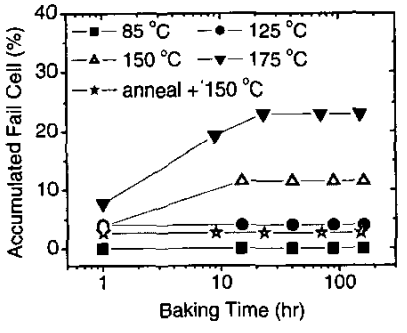

Fig.13 Accumulated failed cell percentage as a function of baking time and temperature.

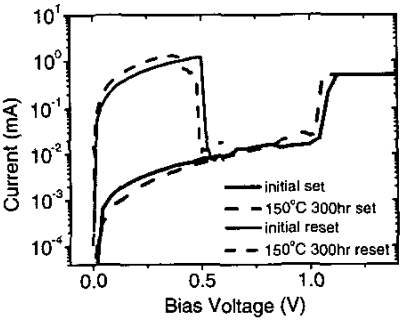

Fig.14 Set and reset I-V curves before and after 150°C-300hr baking.

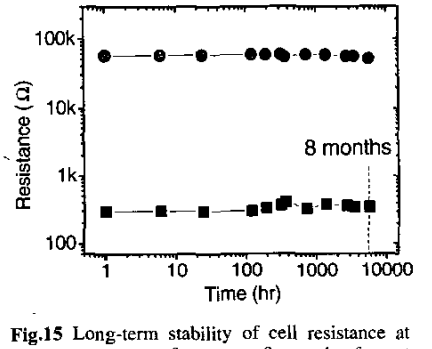

Fig.15 Long-term stability of cell resistance at room temperature for up to 8 months for set and reset cells.