The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits

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The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits

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Programmable crossbar circuits are one key architecture proposed for integrated nanoscale electronics. Emphasizing practicality of fabrication, many scenarios advocate crossbar circuits based on two-terminal devices. In this case, however, signal restoration and inversion remain critical weaknesses. Restoration is essential before the degraded output of one logic gate can drive the input of a subsequent logic gate. Inversion is required to generate a complete logic family. Here we describe and demonstrate a solution to both problems, the crossbar latch. This device stores a logic value on a signal wire, enabling logic value restoration, and inversion. In combination with resistor/diode logic gates, these operations in principle enable universal computing for crossbar circuits, and potentially, integrated nanoscale electronics.
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I. INTRODUCTION

To have fully general computing, one must have not only logic and memory functions, but also be able to place a logical variable into a memory and reuse it as the input to another logic function. One method of achieving such operations is to use a latch.[1] While latches are well known in semiconductor electronics, the advancement of molecular-scale electronics[2] will require different approaches to developing a latching functionality. An architectural paradigm gaining acceptance as both physically constructable and logically useful is the programmable crossbar array,[3] populated in the simplest case with two-terminal devices at each crosspoint. There have been previous proposals to construct bistable latches[4–6] using back-to-back two-terminal molecular devices with negative differential resistivity (NDR).[7] These ideas build on the original suggestion of Goto[8] to create a latch using paired tunnel diodes with NDR. In this paper we describe a latch that has a completely different operating principle, based on the properties of bistable electronic switches.[9,10] It enables nanometer-scale latches to be constructed and integrated with other devices using a crossbar architecture,[3,11,12] and provides storage of an arbitrary logic signal, restoration of logic signal strength, and inversion of the latched output. The combination of these features with resistor/diode logic operations allows the construction of finite state machines, which are sufficiently powerful to compute any function.[1]

The essential functionality that one must have in order to build a latch is to be able to transform back and forth between a voltage representation (logic) and a switch representation (memory) of a digital value, as illustrated schematically in Fig. 1. A given signal line L can be set to either a logical 0 or a 1 voltage state by using two control switches, S_0 and S_1. S_0 can connect L to a voltage source V_0 that pulls down, whereas S_1 can connect to a source V_1 that pulls up. If S_0 (S_1) is closed and S_1 (S_0) is open, then there will be a logical 0 (1) voltage state on L. Thus, the bit stored by the memory (switches S_0 and S_1) can be transferred to the voltage representation, V_0 or V_1, of a output logic value on L. Once the switches are set, it is also possible to invert the logic value by exchanging the voltage sources. The latch must also transform the input logic value on L (voltage) to the switch configuration of S_0 and S_1 (memory), which requires the ability to toggle the switches S_0 and S_1 with appropriate control voltages. This is essentially the same operation as setting a bit of memory in a bistable-switch crossbar array, incorporating, for example, metal/molecule/metal switches.[3,9–12]

II. THE BISTABLE-SWITCH LATCH

Standard semiconductor latch circuits use three-terminal transistors to achieve the switching illustrated in Fig. 1. Here we describe a different latching concept particularly well suited to application in two-terminal crossbar circuits. Two control lines C_A and C_B are connected to a signal line L with bistable two-terminal switches S_A and S_B, as shown schematically in Fig. 2(a). Each switch has a polarity and a voltage threshold for toggling to a closed or an open state. The

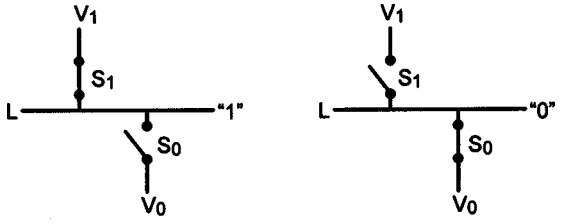

FIG. 1. Schematic diagram illustrating the basic function of a latch—to transform between the switch (memory) and voltage (logic) representations for a data value. The logic line L is connected to two control lines with voltages V_0 and V_1 representing logical 0 and logical 1, respectively. When switch S_1 is closed and S_0 is open, the line voltage is pulled up to V_1 and thus has a logical value of 1. When switch S_1 is open and S_0 is closed, the line voltage is pulled down to V_0 and thus has a logical value of 0.

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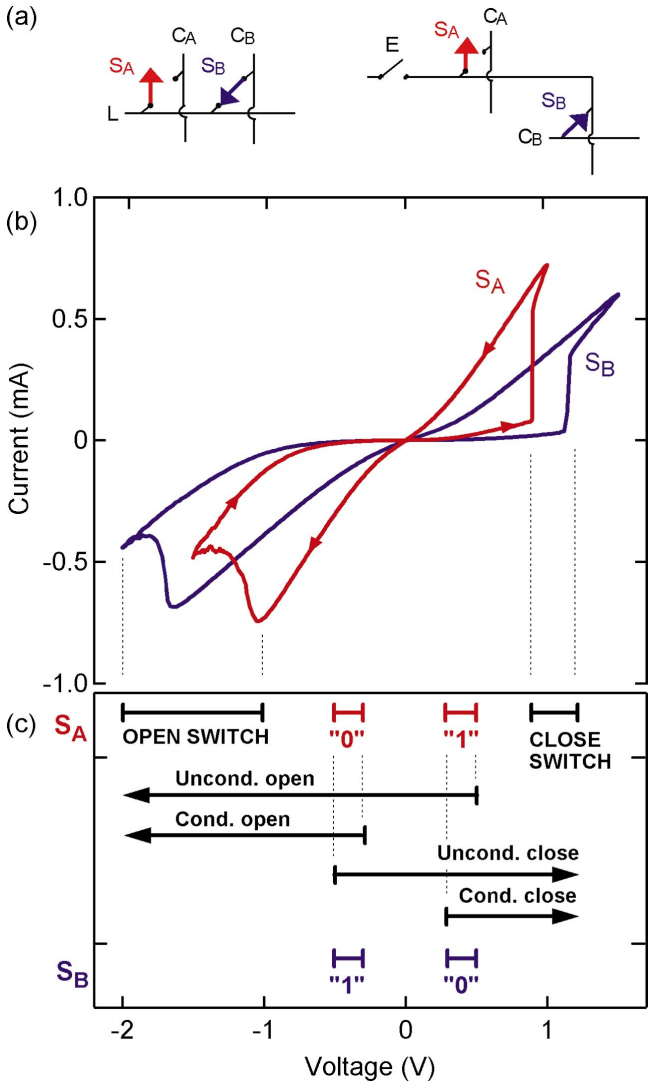

FIG. 2. (Color) (a) (left) A schematic diagram of a crossbar latch. L is the signal line, and C_A and C_B are the two control lines. The bistable electronic switches S_A and S_B connecting the two control lines to the signal line have antiparallel polarity in terms of the sign of the voltage pulses that open or close the switches. (Right) Wiring two parallel polarity switches into the antiparallel latch circuit configuration, and adding an enable switch E. (b) Experimental current-voltage characteristics for two metal/molecule/metal bistable switches that were used to construct a latch. Arrows indicate hysteresis direction. Devices of area 12 μm^2 (S_A) and 16 μm^2 (S_B). (c) Schematic illustration of the system voltage ranges for logic (0, 1) and switching (open switch, close switch), and the consequent control voltages (arrows) required to unconditionally and conditionally open and close the switches. Control voltages depend on the switch polarity (labeled at left S_A, S_B) and the input logic state (0, 1).

two switches are oriented antiparallel to each other in their polarity (indicated by the direction of the arrows). The signal line has at least two different voltage states, ranging from a logical 0 to a logical 1. If the input to the signal line represents the output value of a diode/resistor logic function, the magnitude of the potential will in general be degraded from the true 0 or 1 voltage states. A critical function of the latch will be to restore this signal value to the appropriate full potential. To perform the complete latching operation, a sequence of voltage pulses is applied to each control line, which unconditionally opens both switches, conditionally closes one of them, then restores (and optionally inverts) the signal level. This procedure is described in detail in the following.

Figure 2(b) illustrates the voltage levels of the system needed to understand the operation of the bistable-switch latch. The current-voltage (I-V) characteristics of two different molecular switches (S_A and S_B) show figure-eight-shaped hysteresis. The voltage polarity is defined such that a positive or "forward" bias results in current flowing through the switch in the direction of the arrow in Fig. 2(a). At low voltages $|V|<0.7$ V, the devices behave as stable nonlinear resistors in both the open and closed states. Switching is achieved when the applied bias exceeds the positive or negative voltage threshold for closing or opening each switch. The latch design incorporates two devices, and the variance in their I-V behaviors is accounted for by designating open and close voltage *ranges*, as shown in Fig. 2(b). A voltage exceeding the absolute maximum of the open (close) range will thus open (close) either switch. Also shown are suitably chosen voltage ranges representing a logical "0" and logical "1." The maximum of the 1 range represents a strong 1, which is the initial value of a logical 1. The minimum represents a weak 1, which is the lowest voltage to which a logical 1 is permitted to degrade via sequential resistor/diode logic operations. Correspondingly, there is a weak logical 0 and a strong logical 0. The voltage axis shown corresponds to the potential drop across the switch, i.e., the difference in voltage between the signal line and the control line for that switch [Fig. 2(a)]. The relative order of the open, 0, 1, and close ranges allows the latch to function, but the values of the voltages depend on how the ground potential is defined.

Four switching operations are now enabled by manipulating the voltage on the control line of either switch. The signal line is understood to hold a voltage that lies between a strong 0 and a strong 1. Inducing a large reverse bias will *unconditionally* open the switch, regardless of the voltage on the signal line. This is illustrated by the large amplitude arrow "Unconditionally open." Similarly, a large forward bias will unconditionally close the switch. Opening and closing metal/molecule/metal switches in such an unconditional fashion was the basic operation used to set or reset bits in a memory and to define programmable logic functions.[12] The interesting variation introduced here, at the heart of the ability to utilize the bistable-switch latch, is that one can create *conditional* open or close pulses. If the voltage on the signal line is between a weak 0 and a strong 0, then applying a conditional open pulse to the control line will open the switch, as labeled Cond. open. However, if the voltage on the signal line is between a weak 1 and strong 1, then applying the same conditional open pulse will not open the switch because the potential across the junction will not reach the open switch threshold. Conversely, a conditional close pulse can close the switch only if the voltage on the signal line is at least a weak 1, as labeled "Cond. close."

Figure 2(c) also illustrates the necessity for antiparallel switches. If the two switches were aligned with the same polarity, the 0 and 1 latched states of Fig. 1 cannot be conditionally achieved. For example, both switches could be opened unconditionally, but only a logical 1 could be used to

conditionally close a switch and thus store the 1 value. Alternatively, both switches could be unconditionally closed, but only a logical 0 could subsequently be conditionally stored. Reversing the polarity of switch S_B removes this constraint; it can be represented by inverting the polarity of the logical 0 and 1 ranges with respect to the *I-V* curve of S_B, as illustrated at the bottom of Fig. 2(c). With this circuit modification, a conditional close operation is now available for both a logical 1 and logical 0 input.

The operation of the latch then proceeds as follows (refer to Fig. 2).

(i) Unconditionally open both S_A and S_B by applying an above threshold pulse with positive bias to C_A and with negative bias to C_B.

(ii) Apply conditional close pulses to both control lines (negative for C_A and positive for C_B).

(iii) Apply the voltage for a strong logical 1 to control line C_A and the voltage for a strong logical 0 to control line C_B to restore the signal line to its full potential.

If the initial voltage on the signal line is between a weak and a strong 1, steps (i) and (ii) will close S_A and leave S_B open, whereas for an initial voltage between a weak and a strong 0, S_A will be open and S_B will be closed. Step (ii) may be performed simultaneously for both switches or in two consecutive substeps. If the input voltage on the signal line is degraded because of noise, resistive losses, or diode drops then the voltage will be restored to the full correct signal level after it has been latched. The latch can also provide a logic inversion function. In the last step (iii), after latching the signal one must disconnect from the input and then reverse the voltages on C_A and C_B.

III. EXPERIMENTAL METHODS

The fabrication and electrical characterization of the switch devices used here have been previously described in detail.[10,12] Briefly, two-terminal metal/molecular-monolayer/metal planar junction devices were fabricated by sequential deposition of the bottom electrode, Langmuir-Blodgett (LB) monolayer and top electrode on a flat insulating substrate to form individual crosspoint junctions. Bottom electrodes of 100 nm thick platinum (Pt) were formed by optical lithographic techniques. A LB monolayer of stearic acid $C_{17}H_{35}COOH$ (Aldrich) was next deposited as the cadmium stearate salt (monolayer thickness 2.8 nm by ellipsometry). The top electrode of 5 nm titanium (Ti) + 200 nm aluminum (Al) was subsequently evaporated through a shadow mask onto the LB film. Crosspoint devices were constructed with lateral wire widths of $1-10$ μm Pt and $5-20$ μm Ti/Al, yielding active junction areas of $5-200$ μm^2 and thus 10^7-10^9 molecules electrically in parallel at each junction.

In previous studies,[10,12] similar devices functioned as voltage and current controlled tunable resistors. Application of forward voltage bias (Ti electrode positive) above a certain threshold caused a reduction in the device resistance; above threshold "reverse" bias increased device resistance. These are precisely the characteristics required to implement the latch design described in Figs. 1 and 2. Physically, the latch circuit of Fig. 2(a) was constructed by externally wiring together two separate crosspoint devices. Voltage pulses were applied using a programmable digital/analog source (National Instruments, MIO-16XE); currents and voltages were measured with a parameter analyzer (Hewlett-Packard, HP4155). All current-voltage-time measurements were conducted in laboratory ambient at 300 K.

IV. RESULTS

Measured current-voltage characteristics for two metal/molecule/metal switches used to construct a latch are shown in Fig. 2(b). There is switch-to-switch variability, and the on and off thresholds are in general asymmetric. However, it is still relatively straightforward to define appropriate ranges for V_{close} and V_{open} valid for both switches. In this case, $1.2\ V < V_{close} < 1.6\ V$, and $-2\ V < V_{open} < -1.4\ V$. Based on these parameters, a set of voltage levels can be selected to permit latch operation. Strong logic levels were chosen to be $V_1 = +0.5$ V and $V_0 = -0.5$ V. The unconditional open voltage level was set at $V_{Uncond} = -2.6$ V. The conditional close voltage level was set at $V_{Cond} = +1.2$ V [Fig. 2(c)].

Figure 3 illustrates the latch operation for two switches connected as in Fig. 2(a). The control pulse sequences applied to C_A and C_B are shown in panel (a) using the pulse magnitudes selected above. The sequence $P1-P7$ implements the unconditional open on S_A, then S_B, followed by the conditional close on S_A, then S_B. This is followed by the final signal restoration and, in this case, inversion. Test pulses $P1$, $P4$, and $P7$ accurately measure the switch resistances at the beginning, middle, and end of the sequence. To allow signal inversion an additional "enable" switch [Fig. 2(a)] was connected in series to the input signal line. The enable switch is closed during latching pulses ($P2-P6$), then opened before signal inversion ($P8$).

The changing resistance state of each molecular switch is illustrated in Fig. 3(b). For this trial "*d*," the switches began with $R_A \sim 5\times10^3\ \Omega$ (closed) and $R_B \sim 10^7\ \Omega$ (open). The first control pulse ($P2$) correctly opened S_A, after which $R_A \sim 10^7\ \Omega$. S_B was already open, so the second pulse ($P3$) affected it minimally. The next control pulse ($P5$) attempted a conditional close on S_A, but failed as intended since the input voltage was a (weak) logical 0, $V_{in} = -0.3$ V. The fourth control pulse ($P6$) attempted a conditional close on S_B, and succeeded as designed; subsequently $R_B \sim 3\times10^3\ \Omega$ (closed). The degraded logical 0 input of $V = -0.3$ V was now latched; i.e., transformed into the memory state of the nonvolatile switches. Subsequent connection of C_A and C_B to the strong $V_0 = -0.5$ V and $V_1 = +0.5$ V voltage levels, respectively, ($P8$) restored and inverted the signal.

The outcomes of six successive trials using this identical control voltage protocol are shown in Fig. 4; the only parameter varied between trials was the input voltage. For trial "*a*" an input voltage of $V_{in} = +0.4$ V was latched, restored, and inverted to an output voltage of $V_{out} = -0.49$ V. Trial d, detailed in Fig. 3 above, shows an input $V_{in} = -0.3$ V inverted to an output of $V_{out} = +0.49$ V. In summary, input voltages $0.3\ V \leqslant |V_{in}| \leqslant 0.4\ V$ latched and inverted correctly with signal restoration to $|V_{out}| \sim 0.5$ V; input voltages $|V_{in}| = 0.2$ V

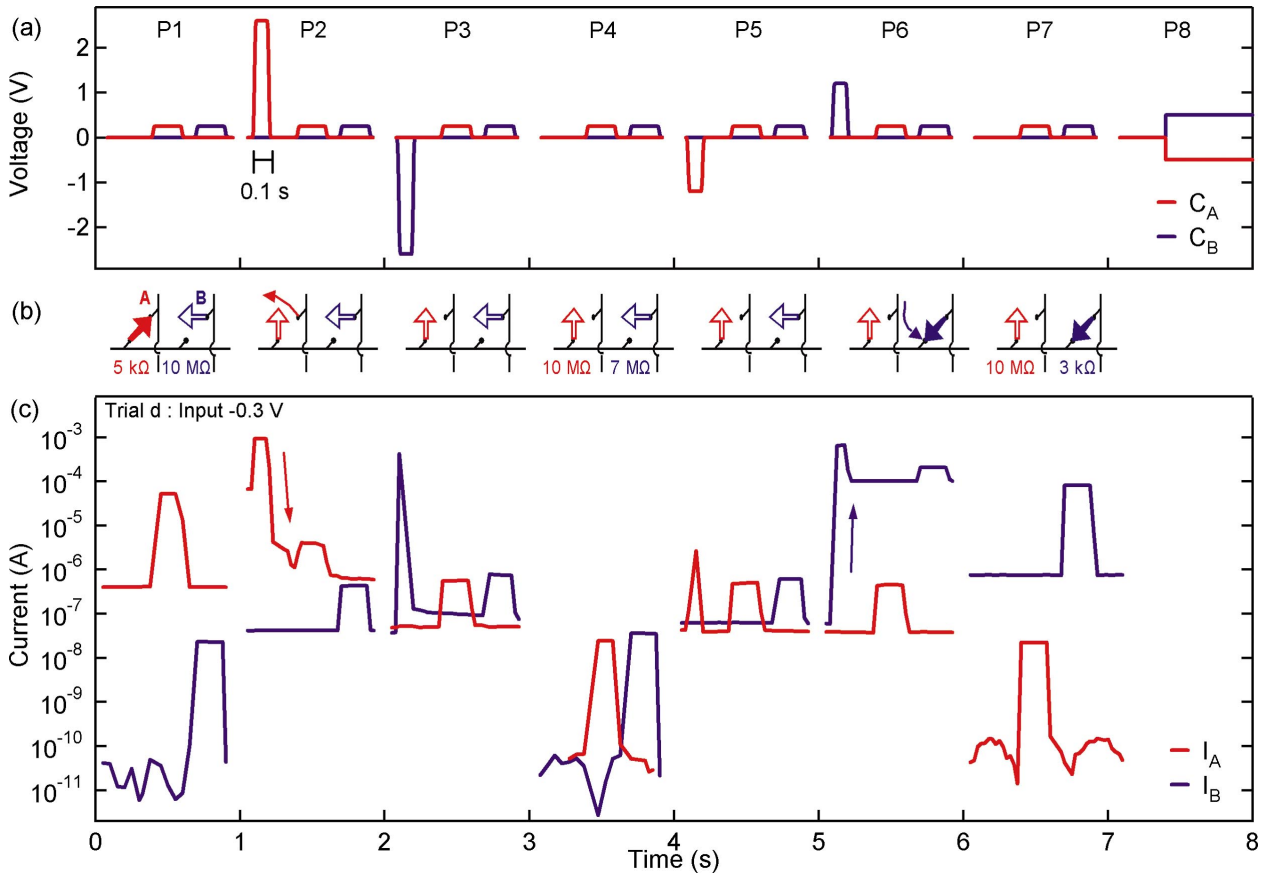

FIG. 3. (Color) Experimental demonstration of a working crossbar latch. (a) The pulse sequence on the two control lines C_A and C_B to achieve the latch function. Initial, interim, and final test pulses (unnecessary in actual operation) are labeled $P1$, $P4$, and $P7$. Unconditional opens, $|V|=2.6$ V, on S_A ($P2$) and S_B ($P3$) are followed by conditional closes, $|V|=1.2$ V, on S_A ($P5$) and S_B ($P6$), according to the switch polarities illustrated in Fig. 2. These control pulses are 0.1 s in duration (followed by additional $V=0.25$ V test pulses to verify switching). The final step ($P8$) is to restore and invert to $|V|=0.5$ V. (b) Schematic state of the switches during each period of the pulse sequence, and switch resistances R_A, R_B during this pulse sequence, for an input voltage of −0.3 V (trial d of Fig. 4). (c) Currents (absolute value) through the switches S_A and S_B during this pulse sequence. The change of state during the open operation on S_A ($P2$) and the close operation on S_B ($P6$) are both visible (arrows).

failed to latch. These results empirically define the logic voltage ranges, i.e., for the strong logical 1 or 0 defined as $|V|=0.5$ V, a weak logical 1 or 0 must be $|V|\geqslant 0.3$ V, and the input operating margin is thus $|\Delta V_{\text{in}}|\sim 0.2$ V. Finally, we note that subsequent trials deliberately alternated between positive and negative input voltages, rigorously requiring both switches to change state correctly during each trial.

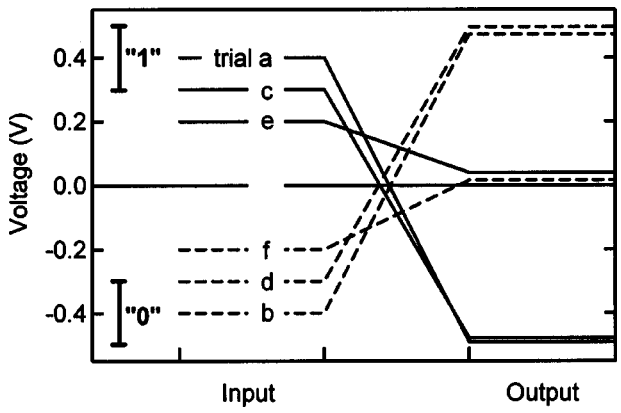

FIG. 4. Six trials run using the fixed pulse protocol of Fig. 3, varying only the input signal voltage. Input voltages $|V|=0.3$ V and $|V|=0.4$ V latched and inverted correctly with signal restoration to $|V^{\text{out}}|\sim 0.5$ V; input voltages $|V|=0.2$ V failed to latch.

V. DISCUSSION

This paper is a feasibility-level description and demonstration of the bistable-switch latch concept. Using this latching strategy in a crossbar structure has the particular advantage that the two latch control lines C_A and C_B, which may be driven by conventional circuitry outside a nanoscale circuit, can be connected to a large number of logic signal lines. Thus, a single pair of latch lines can control many latches, which is very efficient in terms of the number of connections from a nanocircuit to the outside world.

Furthermore, any type of bistable two-terminal switches can be used to implement this latch. The molecular-monolayer switches used in this demonstration are suitably bistable,[10] and operable at nanoscale device dimensions within ultrahigh density nanoelectronic circuits.[12] Unpackaged devices to date have, however, shown limited lifetimes (~100 s of cycles) and switching speeds (~0.1 kHz in Fig. 3 switching transitions), both of which require improvement before reliable application.

This latch design also requires two opposite polarity switches to form the latch. Crosspoint devices fabricated to date[9–12] have been unipolar, with polarity defined by the asymmetric electrode materials. Implementation of this latch design within a single crossbar is feasible simply by "turning

the corner" within the crossbar; i.e., connecting the lower wire output of S_A to the upper wire input of S_B, as indicted schematically in Fig. 2(a). Alternatively, a three-level crossbar consisting of control lines on top of logic lines on top of control lines would also enable implementation.

The crossbar latch is a key element for implementing logic in nanoscale circuits. We have described a two-terminal bistable switch latching function, and provided a proof-of-principles demonstration that it works.

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