A High-Speed Current Mode Sense Amplifier for Spin-Torque Transfer Magnetic Random Access Memory

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***Abstract*— A high-speed current mode sense amplifier for Spin Torque Transfer Magnetic Random Access Memory (STT MRAM) is proposed. The sense amplifier is designed in a 0.18 µm CMOS technology, and 1.8 V supply voltage. The resistance values of high state is 2132 Ω, low state is 1215 Ω, and reference state is 1512 Ω, respectively. The proposed sense amplifier decreases the dropping rate of input bias. In particular, it can reduce the sensing time and the power-delay-product (PDP). In addition, the proposed sense amplifier has higher driving ability.**

I. INTRODUCTION

Magnetic random access memory (MRAM) is one of the most promising and strongest desires for next-generation memory, which features non-volatility, high reading speed, large retention time up to 10 years and it allows more than 10^{12} re-program [1]. MRAM acts as a resistor depending on the direction of magnetization in the two ferromagnetic layers. The ferromagnetic layers include free layer and pinned layer. When the direction of the two layers is parallel, the resistance state of MRAM cell is low; on the contrary, the resistance state is high if the direction is anti-parallel.

The first generation of MRAM is toggle MRAM, which is based on magnetic field writing created by another writing current path [2]. The drawback is that it needs a larger writing current to reduce the device dimensions. The second generation of MRAM is Spin Torque Transfer Magnetic Random Access Memory (STT MRAM), which is based on the direction of writing current through the memory cell. It determines writing operation to be high state or low state. Figure 1(a) illustrates the high state of MRAM, Figure 1(b) shows the low state, and Figure 1(c) is their equivalent circuit diagram. One advantage of the second generation is that accompany the decreasing device dimensions, the writing current can be reduced. Also, the cell area can be decreased because another writing current path is not necessary.

The benefit for applying current mode sense amplifiers in sense circuits is their small input impedances, cross-coupled positive feedback structure and small common input/output impedances [3]. Consequently, the requirement of charges is smaller than the voltage mode sense amplifiers. This paper compares the sensing delay time and PDP for several conditions among the proposed, Chung's and clamped bit-line sense amplifiers.

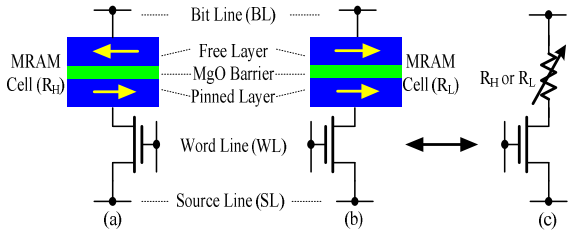

Figure 1. STT MRAM Cell Structure (a) High Resistance State (b) Low Resistance State (c) Equivalent Circuit

II. CURRENT MODE SENSE AMPLIFIER

A. *Clamped Bit-line Sense Amplifier*

The first current mode sense amplifier is illustrated in Figure 2 [4]. R_{MTJ} is the resistor of MRAM cell. When R_{MTJ} represents high resistance, it can be abbreviated as R_{AP} or R_H, and its value is 2132 Ω; on the other hand, it can be written as R_P or R_L when it symbolizes low resistance, and the value is 1215 Ω. R_{ref} is the reference resistor which is 1512 Ω. The gates of M5 and M6 are connected to V_{DD}. When EN and $\overline{SAE}$ is low, M5 and M6 are all working in deep triode region. Therefore, M5 and M6 act equally to voltage-controlled resistance. If the resistances of M5 and M6 are too small, the voltages of V_{IN_L} and V_{IN_R} would also be small. Then, the sensing delay time will increase. But if the voltages of V_{IN_L} and V_{IN_R} are too high, M1 and M2 would be turned off. Consequently, the sense amplifier will shut down. The optimal bias of V_{IN_L} and V_{IN_R} is $V_{OUT} - V_{th}$. The value of V_{OUT} is half V_{DD}. The sense amplifier needs more current difference to compensate the offset, so it takes longer sensing delay time [5].

B. *Chung's Sense Amplifier*

The second current mode sense amplifier is illustrated in Figure 3 [5]. It utilizes a cross-coupled structure by connecting the gates of the clamping MOS (M5, M6). Therefore, V_{OUT} automatically bias the gate voltage of M5 and M6. If the R_{MTJ} is R_H, the voltage of V_{IN_L} would be higher than that of V_{IN_R}, and the current density of M6 is going to be smaller than that of M5. Hence, the V_{gs} of M1 will be smaller than the V_{gs} of M2. Also, M2 has bigger

current density than M1 does. Consequently, V_{OUT_L} will be in high level and V_{OUT_R} will be in low level. While V_{OUT_L} increases, the current density of M6 is becoming bigger; while V_{OUT_R} decreases, the current density of M5 is becoming smaller. This structure can improve the performance of sensing speed by letting the voltage of V_{IN_L} and V_{IN_R} not decrease dramatically.

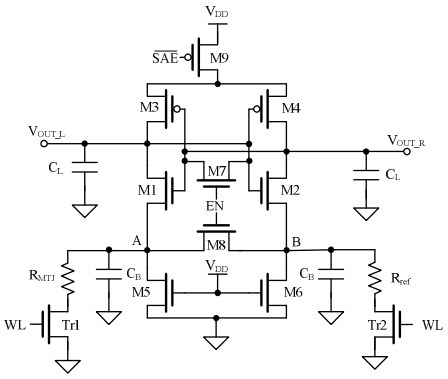

Figure 2. Clamped Bit-line Sense Amplifier

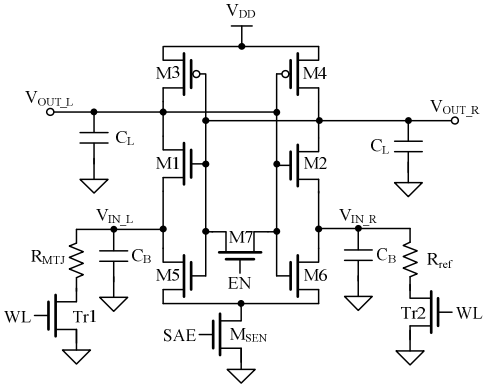

Figure 3. Chung's Sense Amplifier

III. Proposed Current Mode Sense Amplifier

The schematic diagram of the proposed current mode sense amplifier is shown in Figure 4 and the operation within the timing diagram of the current mode sense amplifiers is shown in Figure 5.

A. Structure

C_B is the loading of bit-line and C_L is the loading of outputs. V_{IN_L} and V_{IN_R} are connected to the memory and reference cells of STT MRAM. The drain of M_{SEN} exists a tiny voltage, which reduces the current density of M5 and M6 simultaneously. Hence, the dropping rate of input bias is slower. That will improve the sensing speed. M1~M4 is the cross-coupled positive feedback amplifier. The equalizer M7 makes the equal outputs in one level. In the precharge phase, V_{OUT_L} and V_{OUT_R} are all biased at half V_{DD}.

B. Operation

The following is the operation of the current mode sense amplifier. In Figure 5, EN is high and SAE is low during the first stage of precharge. The outputs of the sense amplifier are equalized by M7. Hence, V_{OUT_L} is equal to V_{OUT_R}. During the last stage of precharge, WL and SAE are high, EN is low, and the sense amplifier turns to evaluation phase from precharge phase. The evaluation phase makes the two outputs, V_{OUT_L} and V_{OUT_R}, to be in the high level and low level respectively.

When R_{MTJ} is in high resistance state and R_{ref} is in reference state, the voltage of V_{IN_L} is higher than that of V_{IN_R}, and the current density of M5 is larger than that of M6. Therefore, both the V_{gs} and the current density of M1 are smaller than those of M2. Consequently, V_{OUT_R} will be in the low level and V_{OUT_L} will be in the high level because of the positive feedback cross couple amplifier (M1-M4). Most importantly, the sources of M5 and M6 connect to the MOS M_{SEN}. It makes the bias voltage of V_{IN_L} and V_{IN_R} in Figure 4 higher than that in Figure 2. Because there is the tiny bias voltage existed in the drain of M_{SEN} (Figure 4), the current density of M5 and M6 will slightly decline. In consequence, the voltage of V_{IN_L} and V_{IN_R} drop slowly. It affects the sensing speed of the sense amplifier.

Even if Chung's sense amplifier has the mechanism that automatically adjusts the current density of M5 and M6, the sensing speed of the sense amplifier is relevant to the difference between the current density of the inputs. The sense amplifier in Figure 3 reduces the difference of current density between M5 and M6. It also means that the sensing speed will be slower than that of the proposed current mode sense amplifier.

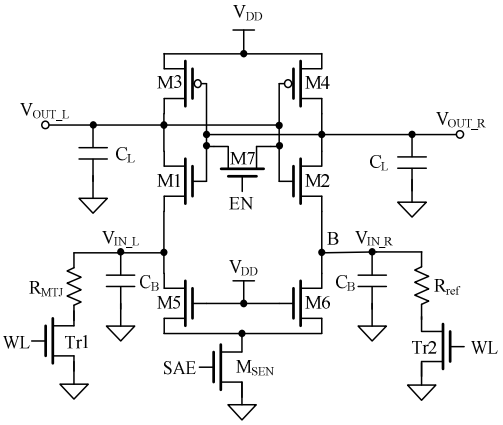

Figure 4. Proposed Current Mode Sense Amplifier

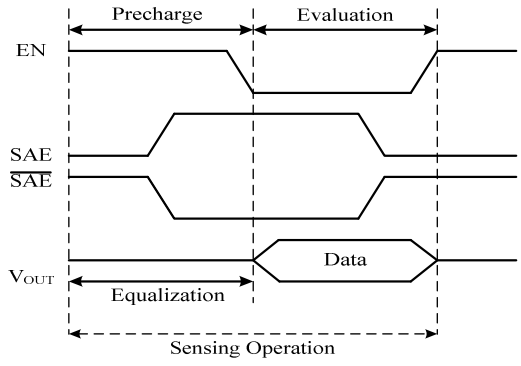

Figure 5. Timing Diagram

IV. Simulations and Comparison Results

A. SA Sensing Speed with Output Loading

The following comparisons are simulated in HSPICE with 0.18μm CMOS technology. The temperature is at 25°C and the supply voltage is 1.8V. The transistor sizes are listed in TABLE I. The maximal output loading of clamped bit-line sense amplifier is 2p at SS corner. Therefore, this sense amplifier in the following simulation would not simulate beyond 2p. Figure 6 illustrates the sensing speed of the three sense amplifiers when C_L is 2p and C_B is 0.6p [6]. When the signal SAE is open for a while, the signal EN should be closed. As soon as the signal EN is closed, the outputs generate the sensing result immediately.

It is obvious that the sensing speed of the proposed sense amplifier is faster than Chung's and clamped bit-line sense amplifiers. Figure 7 presents the sensing delay time of the three sense amplifiers while the output loading is from 0.5p to 5p and the interval of increment is 0.5p at different corners.

It illustrates that the delay time will be increased because of the output loading. It also expresses that the differences of delay time among the three current mode sense amplifiers are more obvious when the output loading is increasing.

TABLE I. Transistor W/L Sizes for the Proposed, Chung's and Clamped Bitl ine Sense Amplifier

Transistor(μm)	Proposed	Chung's	Clamped
M1,M2	2.5 / 0.18	2 / 0.18	0.42 / 0.18
M3,M4	3 / 0.18	2.5 / 0.18	2.5 / 0.18
M5,M6	0.42 / 0.18		
M7,M8	10 / 0.18		
Msen	0.42 / 0.18	0.42 / 0.18	5 / 0.18

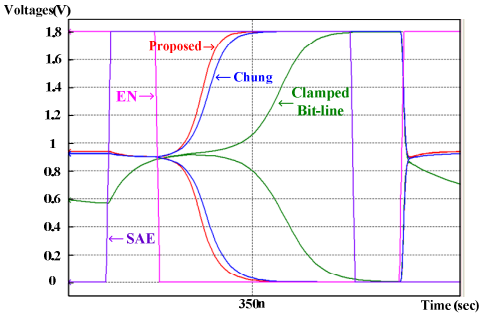

Figure 6. Simulation Result of Three Current Mode Sense Amplifier

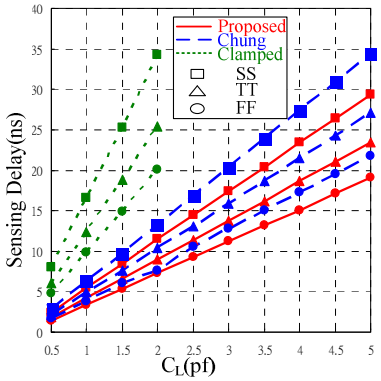

Figure 7. Sensing Delay versus Output Capacitance for Different Process Corners

B. SA Performance under Different Loading

TABLE II lists the power and sensing delay of different values of C_L and C_B with the three kinds of current mode sense amplifiers. When C_L is from 0.5p to 2p, C_B is 0.6p [6] and C_B is from 0.5p to 2p, C_L is 1p. In Figure 6 and Figure 7, the proposed sense amplifier has larger driving ability. Hence, the power dissipation of this sense amplifier is larger than the others. However, it is not objective if power condition is the only consideration. Consequently, we use the power-delay-product (PDP) to estimate total performance. In Figure 8(a) and 8(b), the different loading and value of capacitances, and PDP of the three sense amplifiers are shown. In Figure 8(a), PDP of the proposed sense amplifier is always lower than that of Chung's and clamped bit-line sense amplifiers. Furthermore, the obvious difference of PDP also accompanies the increase of C_L, and the performance of the proposed sense amplifier is more efficient than the others.

TABLE II. Power and Delay Time for the Proposed, Chung's and Clamped Bit-line Sense Amplifier

Power(mW)	C_L=0.5p	C_B=0.5p	C_L=1.5p	C_B=1.5p	C_L=2p	C_B=2p
Proposed	0.2006	0.2149	0.2296	0.2166	0.2442	0.2177
Chung's	0.1756	0.1895	0.2036	0.1907	0.2177	0.1916
Clamped	0.0445	0.09	0.0893	0.0889	0.1114	0.0889
Delay(ns)	C_L=0.5p	C_B=0.5p	C_L=1.5p	C_B=1.5p	C_L=2p	C_B=2p
Proposed	1.85	4.265	6.6	3.926	9	3.825
Chung's	2.15	4.91	7.6	4.486	10.4	4.3775
Clamped	6.02	12.36	18.83	12.2375	25.45	12.224

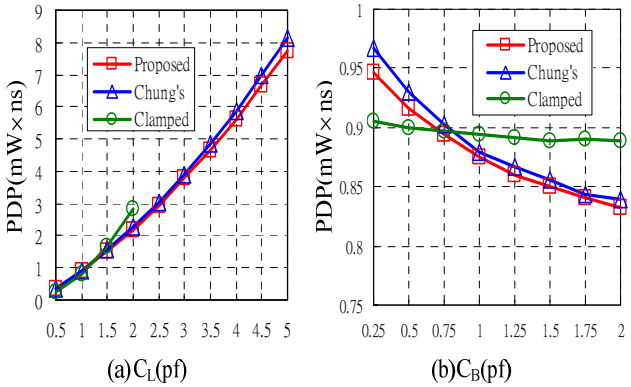

Figure 8. Power-Delay-Product of Different Loading (a) Output Loading (C_L) (b) Different Bit line Loading (C_B)

The variation of the loading on bit-line (C_B) versus PDP of the three sense amplifiers is shown in Figure 8(b). When C_B increases by degrees, PDP of Chung's sense amplifier and clamped bit-line sense amplifier are always higher than the proposed sense amplifier. Because loading on bit-line affects the sense amplifier's sensing speed, C_B also affects PDP indirectly. The increase of C_B helps bias voltage of V_{IN_L} and V_{IN_R} raise. Then, the sensing speed will be faster and the sensing delay time will decrease; hence, PDP of the sense amplifier is about to drop off.

C. Response Time Analysis of Resistive Load Vatiations

In the simulation, the value of high resistance R_H is 2132Ω, low resistance R_L is 1215Ω and reference cell R_{ref} is 1512Ω. However, the MTJ resistance values are highly

relevant in the process. Therefore, we have performed an analysis of the resistive load variations. In order to let the simulated value fit the scale. Figure 9 shows the simulated waveforms of R_{MTJ} from R_L – 50% to R_H + 68% in the transient response. It also means the value is from 0.6kΩ to 3.6kΩ and the increment is 0.6kΩ. Due to the MRAM resistance (R_{MTJ}), which sweeps from low to high, the outputs of the sense amplifier have high level and low level. The figure also presents that the variation of R_{MTJ} will affect the sensing delay time, but the function of proposed sense amplifier is still correct.

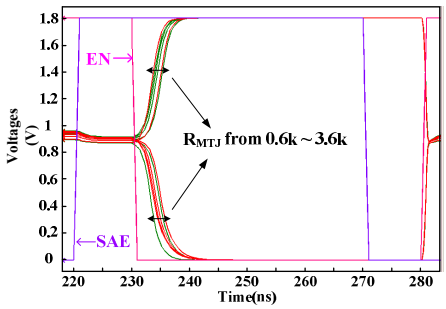

Figure 9. Simulation Result of Proposed Sense Amplifier with Various Resistances

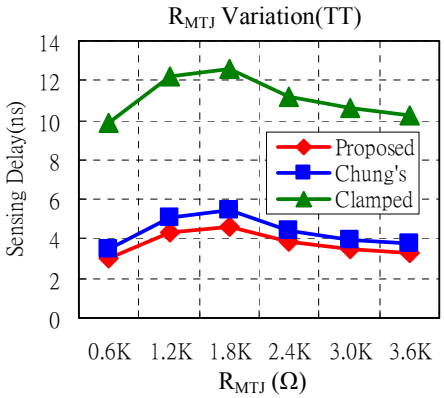

Figure 10. Sensing Delay Time of Various Resistive Loads

Figure 10 presents the sensing time of various resistive loads of the proposed, Chung's and clamped bit-line sense amplifiers. When the resistance of R_{MTJ} is close to R_{ref}, the difference of inputs is not obvious; thus, the sensing time is about to get longer relatively. If the difference of resistance between R_{MTJ} and R_{ref} is larger, the required sensing time is shorter. After R_{MTJ} exceeds 2.4k, the sensing time is almost constant. Among the various resistances of the three sense amplifiers, the sensing time of the proposed sense amplifier is shorter than Chung's and clamped bit-line sense amplifiers.

Figure 11 is the layout of the three kinds SAs for 1K MRAM cells respectively. In other words, the total cells in the layout are 3K MRAM cells.

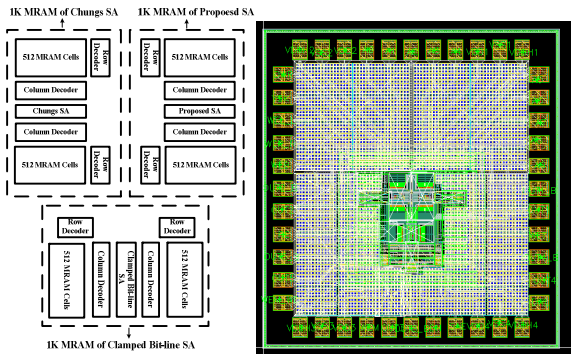

Figure 11. Layout of the Three Kinds SAs for 1K MRAM Cells respectively

CONCLUSIONS

A high-speed current mode sense amplifier of Spin-Torque Transfer MRAM is proposed in this paper. The simulation is in 0.18 μm CMOS technology, and the supply voltage is 1.8V. The input bias dropping rate is decreased in the proposed sense amplifier. It affects the sensing speed of the sense amplifier. When the loading on bit-line (C_B) is 0.6p and the output loading (C_L) is 2p, the proposed sense amplifier exhibits 15% and 182% faster sensing delay than Chung's and clamped bit-line sense amplifiers respectively. The reductions of Power-Delay-Product (PDP) are 3% and 28 %. Furthermore, the proposed sense amplifier spends less sensing delay time under various resistances than the others.

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