INVITED PAPER

Device Properties of Bernoulli Memristors

This paper explains why memristor dynamics comply with Bernoulli's equation; the mathematical framework and its usefulness are discussed.

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ABSTRACT | This paper explains why charge- and flux-controlled memristor dynamics comply with Bernoulli's nonlinear differential equation. These devices are termed Bernoulli memristors. Based on the fact that their identified nonlinear dynamics can always be treated in a linearized manner, a general mathematical framework suitable for the systematic study of individual or networks of Bernoulli memristors can be developed. The paper details the novel mathematical framework and showcases its usefulness: 1) by applying it to obtain a closed-form expression of the output as an explicit function of the input for an example memristor model whose dynamics are described by a power law; 2) by determining analytically the harmonic content of the output of a Bernoulli memristor driven by a sinewave; 3) by investigating systematically the dynamics of networks of Bernoulli memristors connected either in series or in parallel; and 4) by assessing qualitatively the impact of series parasitic ohmic resistance on the dynamics of an ideal memristor.

KEYWORDS | Bernoulli; distortion; harmonic; memristor; network; parallel; parasitic; series

I. INTRODUCTION

In his seminal 1971 paper, Leon Chua theorized a new two-terminal passive circuit element whose operation was similar to a resistor with memory [1]. Hence, he termed the new theoretical element the memristor. Unlike conventional resistors, the direct current (dc) resistance of the memristor at any instant depends upon the total charge that has passed through the device from the past until the present time. Once the driving signal is removed, the ideal device will maintain its state indefinitely, or until the driving signal is applied again [1]–[3].

In 2008, Hewlett-Packard (HP) labs reported the fabrication of a practical nanoscale solid-state device whose behavior was explained in the context of memristive behavior [4], [5]. The experimental realization of the device has led to a surge of theoretical and commercial interest in memristive electronics and their applications with several research groups demonstrating memristive behavior in different devices and systems stemming from different underlying physical mechanisms.

The device initially introduced by HP was a nanoscale solid-state metal/insulator/metal thin film built of platinum (Pt) and titanium-dioxide (TiO_2) with regions of the TiO_2 being oxygen deficient. The change in resistance results from the drift of the positively charged oxygen vacancies when a strong electric field is applied [4], [6]–[8]. The generation of such strong electric fields is a consequence of the nanoscale dimensions of the device. Based on the same metal/insulator/metal structure but using different materials, a memristive device with the insulating layer consisting of a silver (Ag) and silicon (Si) mixture has also been built. In this case, the resistance switching is caused by the motion of Ag ions when a voltage is applied across the device [9]. Memristive behavior has also been reported in nanoparticle assemblies (Fe_3O_4) [10] and in vanadium dioxide (VO_2) thin films due to the insulator-to-metal transition [11], [12]. Furthermore, the use of a class of semiconductor spintronic devices as memristive systems has been suggested. In this class of devices, the current flow modulation is achieved by the filtering of electrons

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according to their spin, allowing only electrons of a certain spin to go through [13]. Several other memristor-type devices have been reported while a variety of successfully fabricated nanostructures can now be understood within the context of memristive behavior (see [4] and references therein).

Attractive memristor properties, such as their intrinsic nonvolatile memory and their small size, suggest their use in a plethora of applications. The most obvious application is as memory elements in high-density storage units. Aiming towards this goal, Vontobel *et al.* [14] present strategies for reading from and writing to a memristor crossbar array. In [15], it is shown how memristive switches can be used as logic gates to perform logic operations while at the same time serving as memories that store logic values. The feasibility of integrating memristors with conventional silicon electronics to build programmable FPGA-like circuits is demonstrated in [16]–[18], while Pershin and Di'Ventra [19] suggest the use of memristors in programmable analog circuits by exploiting the fact that practical realizations of memristors do not change significantly their state when voltages below a certain threshold are applied. Additionally, the close resemblance of a memristor to neural synapses has elicited interest in memristor-based implementations of synaptic learning mechanisms in bioinspired circuits [9], [20]–[23].

Undoubtedly, the above developments in memristors and memristive systems are indicative of the fast growing interest in the field driven by, among others, the potential for commercial applications. Despite this remarkable progress, a big challenge in the effort to understand, and hence optimally design, memristors still remains the development of a general mathematical framework for their analysis that goes beyond mere computational simulation.

The foundations of a step in this direction can be found in our recently proposed mathematical framework [24]–[27]. References [24] and [25] were the first work linking Bernoulli dynamics with memristors. In [26], it was explained why the dynamics of a general class of memristors and other mem-elements, such as memcapacitors and meminductors, comply with the dynamics governed by Jacob Bernoulli's differential equation. For memristors falling into this category it is always possible to nonlinearly transform the differential equations describing their dynamics into a linear form. This in turn allows for their systematic study by simplifying the process of obtaining analytic input–output solutions. In [27], a further investigation is presented that generalizes these results by showing the compliance of the output dynamics with Bernoulli's equation for all possible types (from the pairwise combinations between voltage/current-driven and flux/charge-controlled) of passive memristors. The usefulness of our formalism was demonstrated using HP's ideal memristor model from [4] as an example to obtain explicit analytic expressions for the output. We have also shown how the systematic investigation of memristor properties, such as he hysteresis of the I–V characteristic, can be facilitated thanks to the derived analytic relations linking low-level device parameters with the memristor's nonlinear dynamics.

The purpose of this paper is to build on the foundations set in [26] and [27] to extend our framework and investigate further device properties of ideal Bernoulli memristors. The paper is organized as follows. In Section II, we present our framework and demonstrate its use by deriving the analytic input–output relation for a model example. Section III investigates analytically the harmonic distortion levels present at the output when a memristor is driven by a pure sinusoid. We also discuss quantitatively the interdependence of harmonic distortion levels with the I–V hysteresis, as well as the dependence on low-level device parameters and parameters of the input driving signals. It should be stressed that the analysis reported in Section III becomes feasible through our mathematical framework. Section IV focuses on the study of networks of memristors connected either in series or in parallel and shows how the framework still applies to these cases. We also evaluate the impact of an ohmic parasitic resistance upon the effective I–V curves of the memristor. Section V concludes the paper by summarizing and discussing the results presented.

II. MATHEMATICAL FRAMEWORK

A. Bernoulli Differential Equation

Bernoulli differential equations (BDEs) are a family of nonlinear ordinary differential equations (ODEs) of the general form [28]

$$y_t' + p(t)y = q(t)y^n \tag{1}$$

where $n \neq 0, 1$. They are characterized by an important property: using an appropriate substitution of the form $z = y^{1-n}$ they can always be reduced to a linear ODE. It can be shown that an exact solution, for the initial condition $z(t_0) = [y(t_0)]^{1-n}$ at $t = t_0$, is given by

$$[y(t)]^{1-n} = Bm^{-1}(t) + (1-n)m^{-1}(t)\int_{t_0}^{t} m(\tau)q(\tau)\,d\tau \tag{2}$$

where $B = z(t_0) = [y(t_0)]^{1-n}$ and $m(t)$ is the integrating factor

$$m(t) = e^{(1-n)\int_{t_0}^{t} p(\tau)d\tau}.$$

If an initial condition is not available, we can still obtain the general solution by ignoring the limits of integration and considering B as the constant of integration. We refer to devices whose dynamics are characterized by a BDE as Bernoulli devices.

B. Flux-Controlled Bernoulli Memristors

Consider the relation $Q(t) = Q[\Phi(t)]$ describing the flux-controlled memristor on the Q–Φ plane, where $Q(t)$ and $\Phi(t)$ are the charge and flux, respectively. Differentiating with respect to time leads to [1]

$$\frac{dQ(t)}{dt} = \frac{dQ[\Phi(t)]}{d\Phi(t)}\frac{d\Phi(t)}{dt} \tag{3}$$

where $\mathcal{W}[\Phi(t)] = dQ[\Phi(t)]/d\Phi(t)$ is the incremental memductance. The memductance, which is the reciprocal of the memristance $\mathcal{W}(t) = \mathcal{M}^{-1}(t)$, is expressed in units of siemens. Using the fact that $dQ(t)/dt = I(t)$ and $d\Phi(t)/dt = V(t)$, (3) can be expressed on the I–V plane as

$$I(t) = \mathcal{W}[\Phi(t)]V(t) \tag{4}$$

which together with

$$\dot{\Phi}(t) = V(t) \tag{5}$$

define the flux-controlled memristor with $I(t)$ and $V(t)$ denoting, respectively, the current and the voltage of the memristor [2], [29].

It is important to consider here the differential equation that governs the dynamics of the memristor on the I–V plane where devices are typically characterized since access on the Q–Φ plane is impractical. Substituting $\mathcal{W}(t) = I(t)/V(t)$ in the time derivative of $I(t) = \mathcal{W}(t)V(t)$ and rearranging yields

$$\dot{V}(t) - \frac{\dot{I}(t)}{I(t)}V(t) = -\frac{V^2(t)}{I(t)}\dot{\mathcal{W}}(t) \tag{6}$$

where $\dot{\mathcal{W}}(t)$ has not been expanded since the controlling internal variable is still unspecified. Depending on the form of the derivative $\dot{\mathcal{W}}(t)$, (6) may result in a BDE as in (1).

For a flux-controlled memristor mathematically represented by the pair of (4) and (5)

$$\dot{\mathcal{W}}(t) = \frac{d}{dt}\mathcal{W}[\Phi(t)] = \frac{d\mathcal{W}[\Phi(t)]}{d\Phi(t)}V(t) \tag{7}$$

is always an explicit function of $\Phi(t)$ multiplied by $V(t)$. Substituting (7) in (6) results in

$$\dot{V}(t) - \frac{\dot{I}(t)}{I(t)}V(t) = -\frac{g_1(\Phi(t))}{I(t)}V^3(t) \tag{8}$$

which is a BDE irrespective of $g_1(\Phi(t)) = d\mathcal{W}[\Phi(t)]/d\Phi(t)$. Equation (8) is the BDE describing the flux-controlled current-driven memristor. Therefore, assuming that any passive flux-controlled memristor is represented by the pair of (4) and (5), then the dynamics of flux-controlled memristors are always characterized by a BDE provided that

$$\lim_{t\to t_0}\frac{I(t)}{V(t)} = B_0 \quad \text{and} \quad \lim_{t\to t_1}\frac{V(t)}{I(t)} = B_1$$

where B_0, B_1 are finite nonzero constants and t_0, t_1 are the instants when $V(t_0) = I(t_1) = 0$.

The reader can verify in a similar manner that the output dynamics comply with a BDE for all strictly passive memristors formed from the pairwise combinations between voltage or current driven which are charge or flux controlled. Strict passivity, i.e., $\mathcal{M}(t)$ or $\mathcal{W}(t) > 0$ for all t, ensures that the representation of the memristance as a function of the dependent quantity is possible. The resulting BDEs can always be transformed into a linear time-dependent differential equation, whence we obtain the expression of the memristor output as a function of the input [27]. Table 1 summarizes all such results. The dual results incorporating the memductance can be obtained by substituting $V(t)$ for $I(t)$, $Q(t)$ for $\Phi(t)$, and $\mathcal{M}(\cdot)$ for $\mathcal{W}(\cdot)$.

C. An Example Model

To demonstrate the use of the framework, we apply it to the case of a flux-controlled memristor whose memductance dynamics are described by a general relation of the form

$$\dot{\mathcal{W}}(t) = k_1 V^{\alpha}(t) \tag{9}$$

where $\alpha \neq -1, -2$ and k_1 is a nonzero constant. $\dot{\mathcal{W}}(t) = 0$ implies a constant memductance which is equivalent to a conventional resistor. We will show how the output voltage of the particular model can be expressed analytically as a function of the input current with k_1 a proportionality constant determined by low-level device parameters (e.g., doping levels, dimensions, carrier mobility, resistivity). Note that, strictly speaking, (9) describes the dynamics of

Table 1 Governing Differential Equations and Corresponding General Solutions for All Types of Passive Memristors

Memristor Type		Constitutive Law	Governing BDE	General Solution
Flux Controlled	Current Driven	$V(t)=\mathcal{M}(\Phi)I(t)$	$\dot{V}(t)-\frac{\dot{I}(t)}{I(t)}V(t)=\frac{d\mathcal{M}(\Phi)}{d\Phi}\frac{V^2(t)}{\mathcal{M}(\Phi)}$	$V(t)=I(t)\left[\mathcal{M}_0^{-1}-\int_0^t\frac{d\mathcal{M}(\Phi)}{d\Phi}\frac{I(\tau)}{\mathcal{M}(\Phi)}d\tau\right]^{-1}$
	Voltage Driven	$I(t)=\mathcal{M}^{-1}(\Phi)V(t)$	$\dot{I}(t)-\frac{\dot{V}(t)}{V(t)}I(t)=-\frac{d\mathcal{M}(\Phi)}{d\Phi}I^2(t)$	$I(t)=V(t)\left[\mathcal{M}_0+\int_0^t\frac{d\mathcal{M}(\Phi)}{d\Phi}V(\tau)d\tau\right]^{-1}$
Charge Controlled	Current Driven	$V(t)=\mathcal{M}(Q)I(t)$	$\dot{V}(t)-\frac{\dot{I}(t)}{I(t)}V(t)=\frac{d\mathcal{M}(Q)}{dQ}\frac{V^2(t)}{\mathcal{M}^2(Q)}$	$V(t)=I(t)\left[\mathcal{M}_0^{-1}-\int_0^t\frac{d\mathcal{M}(Q)}{dQ}\frac{I(\tau)}{\mathcal{M}^2(Q)}d\tau\right]^{-1}$
	Voltage Driven	$I(t)=\mathcal{M}^{-1}(Q)V(t)$	$\dot{I}(t)-\frac{\dot{V}(t)}{V(t)}I(t)=-\frac{d\mathcal{M}(Q)}{dQ}\frac{I^3(t)}{V(t)}$	$I(t)=V(t)\left[\mathcal{M}_0^2+2\int_0^t\frac{d\mathcal{M}(Q)}{dQ}V(\tau)d\tau\right]^{-\frac{1}{2}}$

a memristor for $\alpha=1$; for any other valid value of α, it describes the dynamics of a memristive system. These memristive dynamics are inspired by the power laws governing the characteristics of amorphous materials and are intentionally generalized to stress the usefulness of our formalism.

The example described by (9) can be classified as a Bernoulli device since substituting (9) in the differential (6) results in

$$\dot{V}(t)-\frac{\dot{I}(t)}{I(t)}V(t)=-k_1\frac{V^{\alpha+2}(t)}{I(t)} \tag{10}$$

which is a BDE for any $\alpha\neq-1,-2$. Establishing this as a Bernoulli device allows us to follow the procedure described in Section II-A. By comparing (10) with (1), we can identify the functions $p(t)$ and $q(t)$ and use (2) to obtain the output voltage $V(t)$ as

$$V(t)=\frac{I(t)}{\left[\mathcal{W}_0^{\alpha+1}+k_1(\alpha+1)\int_0^t I^\alpha(\tau)\,d\tau\right]^{\frac{1}{\alpha+1}}} \tag{11}$$

where we have assumed the initial condition $I(0)/V(0)=\mathcal{W}_0$ at $t=t_0=0$.

Assuming that the input is a periodic signal with period $T_0=2\pi/\omega_0$, amplitude A, and mean value over a period equal to zero, then we can reexpress the current as $I(t)=A\hat{I}(t)$ and the output voltage in normalized time $x=\omega_0 t$ as

$$V(x)=\frac{A\hat{I}(x)}{\mathcal{W}_0\left[1+\beta_1\int_0^x\hat{I}^\alpha(x)\,dx\right]^{\frac{1}{\alpha+1}}} \tag{12}$$

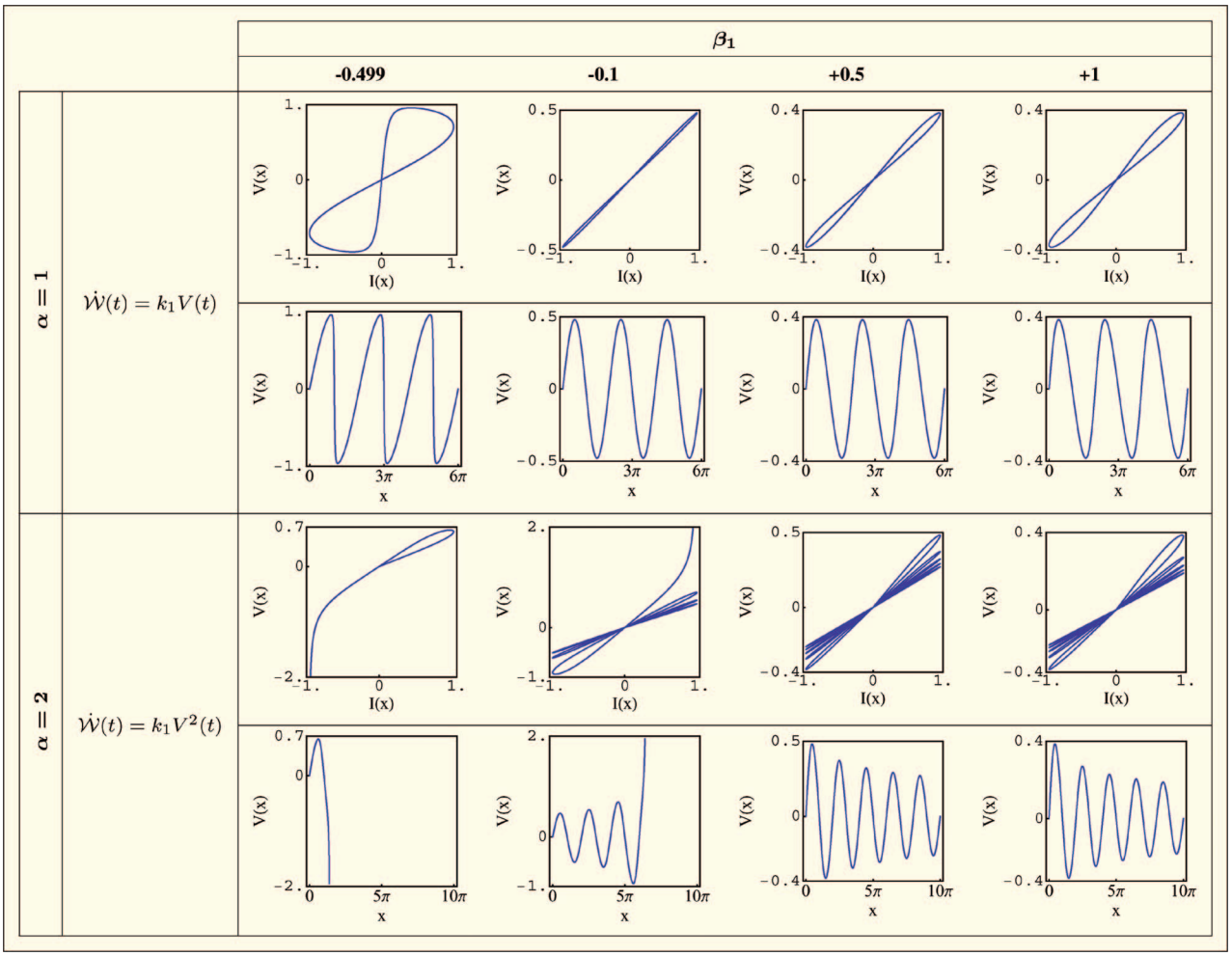
where $\beta_1=(\alpha+1)k_1A/(\omega_0\mathcal{W}_0^{\alpha+1})$ and $\hat{I}(t)$ is the same periodic input with unit amplitude. In this way, we succeed in lumping into a single quantity β_1 both low-level device parameters (e.g., $k_1,\mathcal{W}_0,\alpha$) and parameters related to the input (A and ω_0). Ignoring the scaling factor $A/\mathcal{W}_0$, it is clear from (12) that β_1 governs the output waveform for a given input signal. By further restricting the output to be real and finite, we can determine the range of β_1 values which satisfy this requirement. Allowing β_1 to vary only in this range of values will result in sets of possible waveforms for which the output is real and finite. Conversely, each real and finite output response corresponds to a specific β_1 value which means that if the physical system is configured in a manner such that all its parameters evaluate to a specific β_1 value, then the response corresponding to this β_1 can be anticipated.

Consider now the model of (9) driven by the waveform $I(t)=A\sin(\omega_0 t)$ for $\alpha=1$ and $\alpha=2$. Using (12), the output voltage can be determined analytically. The results are summarized in Table 2 including the example model and its general solution. For completeness, we have also listed the analogous results for the charge-controlled case for a voltage input. It can be shown [27] that the

Table 2 Analytical Solutions for Bernoulli Models With Dynamics of the Form $\dot{\mathcal{W}}(t)=k_1V^\alpha(t)$ or $\dot{\mathcal{M}}(t)=k_2I^\alpha(t)$

Type	Model	Output	$\alpha=1$	$\alpha=2$	
Flux Controlled	$\dot{\mathcal{W}}(t)=k_1V^\alpha(t)$	$V(x)=\frac{A\hat{I}(x)}{\mathcal{W}_0\left[1+\beta_1\int_0^x\hat{I}^\alpha(x)dx\right]^{\frac{1}{\alpha+1}}}$	$\frac{A\sin(x)}{\mathcal{W}_0[1+\beta_1(1-\cos(x))]^{\frac{1}{2}}}$	$\frac{A\sin(x)}{\mathcal{W}_0\left[1+\beta_1(\frac{x}{2}-\frac{1}{4}\sin(2x))\right]^{\frac{1}{3}}}$	$\beta_1=\frac{(\alpha+1)k_1A}{\omega_0\mathcal{W}_0^{\alpha+1}}$
Charge Controlled	$\dot{\mathcal{M}}(t)=k_2I^\alpha(t)$	$I(x)=\frac{A\hat{V}(x)}{\mathcal{M}_0\left[1+\beta_2\int_0^x\hat{V}^\alpha(x)dx\right]^{\frac{1}{\alpha+1}}}$	$\frac{A\sin(x)}{\mathcal{M}_0[1+\beta_2(1-\cos(x))]^{\frac{1}{2}}}$	$\frac{A\sin(x)}{\mathcal{M}_0\left[1+\beta_2(\frac{x}{2}-\frac{1}{4}\sin(2x))\right]^{\frac{1}{3}}}$	$\beta_2=\frac{(\alpha+1)k_2A}{\omega_0\mathcal{M}_0^{\alpha+1}}$

Table 3 *V–I* Characteristics and Time Response Plots $V(x)$ for Flux-Controlled Bernoulli Memristors With Different Values of α and β_1



memristance dynamics of HP ideal memristor reported in [4] comply with the form of the charge-controlled model shown in Table 2 when $\alpha = 1$.

Table 3 depicts the V–I and V–x curves for the two flux-controlled cases ($\alpha = 1, 2$) shown in Table 2, for four different values of β_1. For $\alpha = 1$, we obtain the familiar symmetric double-valued V–I hysteresis curves and the periodic $V(x)$ output expected from a memristor. In this case, β_1 controls the hysteretic pinch of the device. For $\alpha = 2$, the device diverges from the memristor regime. Although the input is a symmetric zero mean waveform, the effect of the positive half-wave cycle of the input is not undone by the negative half-cycle. The results are V–I curves which are not symmetric. On the V–x plane, the output is an oscillatory waveform of increasing or decreasing amplitude, depending on the value of β_1.

III. HARMONIC ANALYSIS: DISTORTION

In the previous section, it was shown how the value of β_1 affects the I–V characteristic of a flux-controlled memristor. In [27], we have shown that β_2 has the same effect on charge-controlled memristors and we have articulated a method for quantifying the hysteretic pinch of the I–V curves in terms of the work done by the driving signal. We also showed that the parameters of the model can be lumped in the single quantity β_2, which directly controls the hysteretic pinch of the memristor. Here, we investigate a different aspect of memristor behavior that is more relevant to signal processing, namely, the harmonic distortion introduced by the memristor at the output. This will be related to low-level device parameters as well as input driving signal parameters through β_2.

Single, linear, time-invariant, passive components such as the resistor, the inductor, and the capacitor (or combinations of such components) lead to linear time-invariant networks. When driven by a sinusoid, such networks output a replica of the input scaled in magnitude and shifted in phase. When a nonlinear element like the memristor is driven by a pure sinusoid, its output spectrum will be characterized by the presence of the input frequency and higher harmonics. Harmonic distortion refers to these additional components that were not present in the original spectrum. In what follows, the

Table 4 Quantity γ_m in the Recursion Relation for the Harmonics

γ_m	m
$K(k)$	0
$\frac{1}{\beta_2}\left[(\beta_2+1)K(k)-E(k)\right]$	1
$\frac{1}{3\beta_2^2}\left[(3\beta_2^2+4\beta_2+2)K(k)-2(\beta_2+1)E(k)\right]$	2
$\frac{2(m-1)(1+\beta_2)\gamma_{m-1}+\beta_2(2m-3)\gamma_{m-2}-2(m-2)(1+\beta_2)\gamma_{m-3}}{(2m-1)\beta_2}$	$m \geq 3$

spectrum of the output of the memristor will be obtained analytically when driven by a sine wave. We will then use the total harmonic distortion (THD) index to quantify the harmonic distortion and relate it to the basic device parameters.

For the purpose of our analysis, we use here the charge-controlled model from Table 2 with $\alpha = 1$

$$\dot{\mathcal{M}}(t) = k_2 I(t). \tag{13}$$

As already shown in [27], the HP ideal memristor is a charge-controlled Bernoulli memristor whose memristance dynamics comply with (13). Therefore, $k_2 = (1 - \mathcal{R}_{\mathrm{OFF}}/\mathcal{R}_{\mathrm{ON}})(\mathcal{R}_{\mathrm{ON}}/D)^2\mu_v$ where $\mathcal{R}_{\mathrm{ON}}$ corresponds to the resistance of the device when fully doped while $\mathcal{R}_{\mathrm{OFF}}$ is the resistance when completely undoped, D is the thickness of the device, μ_v is the mobility of the charge carriers (average ion mobility), and $k_2 < 0$ because $(\mathcal{R}_{\mathrm{OFF}}/\mathcal{R}_{\mathrm{ON}}) > 1$.

According to Table 2, when the model of (13) is excited by a pure sine wave of the form $V(t) = A\sin(\omega_0 t)$, the output current is given by

$$I(t) = \frac{A\sin(\omega_0 t)}{\mathcal{M}_0[1+\beta_2(1-\cos(\omega_0 t))]^{\frac{1}{2}}}. \tag{14}$$

The output waveform is also a periodic signal of period $T_0 = 2\pi/\omega_0$, the same as the input voltage, since $I(t+T_0) = I(t)$ for all t. Therefore, Fourier analysis can be employed in order to decompose the output response into its constituent harmonics. The following form of the trigonometric Fourier series is exploited here [30]:

$$g(t) = \frac{a_0}{2} + \sum_{n=1}^{+\infty}[a_n\cos(n\omega_0 t) + b_n\sin(n\omega_0 t)] \tag{15}$$

with

$$a_0 = \frac{2}{T_0}\int_{T_0} g(t)\,dt, \quad a_n = \frac{2}{T_0}\int_{T_0} g(t)\cos(n\omega_0 t)\,dt$$
$$b_n = \frac{2}{T_0}\int_{T_0} g(t)\sin(n\omega_0 t)\,dt \tag{16}$$

and $g(t)$ is a periodic signal of period $T_0 = 2\pi/\omega_0$.

We now analyze the output response $I(t)$, as given in (14), and determine the coefficients of the Fourier series according to (16). Because $I(-t) = -I(t)$, for (14), the output waveform is odd symmetric, thus $a_0 = a_n = 0$. To determine the b_n analytically we need to expand the terms $[\sin(\omega_0 t)\sin(n\omega_0 t)]$ into integer powers of $\cos(\omega_0 t)$ [31]. The result is a sum of integrals with a finite number of terms of the following form:

$$\int_0^{\pi} \frac{\cos^m(x)}{\sqrt{\delta+\epsilon\cos(x)}} = 2\gamma_m \tag{17}$$

with $\delta = 1+\beta_2$, $\epsilon = -\beta_2$, $m = 0, 1, 2, 3, \ldots$, and x denoting the normalized time. These terms lead to a recurrence relation in terms of elliptic integrals of the first kind [denoted $F(\phi, k)$] and of the second kind [denoted $E(\phi, k)$] [32]. Table 4 presents the first three terms required to initiate the recursion and the general mth term, noting that $k = \sqrt{-2\beta_2}$ and $F(\pi/2, k) = K(k)$ and $E(\pi/2, k) = E(k)$ are the complete elliptic integrals of the respective kind. Table 5 presents the amplitude of the first three harmonics at the frequencies ω_0, $2\omega_0$, and $3\omega_0$, calculated by employing the recurrence relation. The amplitude of each harmonic b_i is multiplied by $\pi\mathcal{M}_0/A$ to eliminate the scaling factor $A/(\pi\mathcal{M}_0)$. The solution presented assumes that $\delta > \epsilon > 0$, a condition satisfied by HP's memristor since $-0.5 < \beta_2 < 0$ [27]. In a similar manner, the amplitude b_i of any frequency component can be obtained analytically.

Fig. 1 shows the amplitude spectrum of the memristor output for three different β_2 values. Each plot includes the first ten harmonics normalized according to $\bar{b}_n = b_n/b_1$, where b_1 is the amplitude of the fundamental component.

Table 5 Amplitude of First Three Harmonics of the HP Memristor Under Sinusoidal Drive

i	$\left(\frac{\pi\mathcal{M}_0}{A}\right)\mathbf{b}_i$
1	$4(\gamma_0-\gamma_2)=$ $\frac{8}{3\beta_2^2}\left[(\beta_2+1)E(k)-(1+2\beta_2)K(k)\right]$
2	$8(\gamma_1-\gamma_3)=$ $\frac{16}{15\beta_2^3}\left[(\beta_2^2+8\beta_2+4)E(k)-4(2\beta_2^2+3\beta_2+1)K(k)\right]$
3	$4(-\gamma_0+5\gamma_2-4\gamma_4)=$ $\frac{8}{35\beta_2^4}\left[(3\beta_2^3+67\beta_2^2+96\beta_2+32)E(k)-(54\beta_2^3+155\beta_2^2+128\beta_2+32)K(k)\right]$

Having also in mind Table 3, the amplitude spectra show that as β_2 approaches zero the memristor becomes more linear, behaving almost like an ordinary resistor and causing less distortion at the output. On the other hand, as β_2 tends to -0.5, which corresponds to the most hysteretic behavior [27], the distortion increases considerably with higher harmonics becoming more significant as the device becomes also more nonlinear.

In each of the spectra in Fig. 1, the total harmonic distortion (THD) is also indicated [33]. The definition of the THD index used is

$$\mathrm{THD}=\frac{\sqrt{\sum_{n=2}^{\infty}C_n^2}}{C_1} \tag{18}$$

where $C_n=\sqrt{a_n^2+b_n^2}$ denotes the magnitude of the nth harmonic component. Equation (18) evaluates the index considering the contribution of each harmonic component individually. The more linear the response is, the lower the THD value is. Hence, Fig. 1(a) corresponds to the highest THD index while Fig. 1(c) to the lowest of the three. Moreover, for the particular memristor under investigation it is interesting to observe that the index is an explicit function of β_2 since $a_0=a_n=0$ and b_n can be expressed as a function of β_2. Fig. 2 illustrates the THD against β_2 while β_2 varies in the range $-0.5<\beta_2<0$: as the memristor becomes more linear, or equivalently, as β_2 approaches zero the THD decreases. This behavior is in agreement with the dependence of the hysteresis on β_2 which also decreases monotonically as β_2 tends to zero [27].

The harmonic analysis performed here reveals the explicit dependence of the memristor spectrum upon the parameter β_2. The analytic expressions obtained for evaluating the amplitude of the frequency components show that β_2 governs the spectrum of the device. This becomes clear by looking at the first three harmonics listed in Table 5. The significance of this observation lies in the fact that β_2 combines into a single quantity $\beta_2=(\alpha+1)k_2A/(\omega_0\mathcal{M}_0^{\alpha+1})$ all of the parameters of the model. Therefore, it is the combination of these parameters that determines the spectral content at the output and not each one individually. In other words, many different combinations of parameters have the same effect on the observable output. A similar conclusion was reached for hysteresis in [27]. Such observations, which correlate device parameters (e.g., doping, dimensions, mobility) with driving conditions (e.g., amplitude and frequency of the input), constitute a characteristic example of useful and practical insights gained by the adoption of our mathematical framework.

One may exploit the explicit dependence of the THD upon β_2 to: 1) either tune a specific memristor technology in such a manner that β_2, for an anticipated range of input frequencies and amplitudes, takes values within a range such that THD remains below a certain desired level; or 2) determine the anticipated THD levels for a given memristor technology under different combinations of input frequencies and input amplitude values.

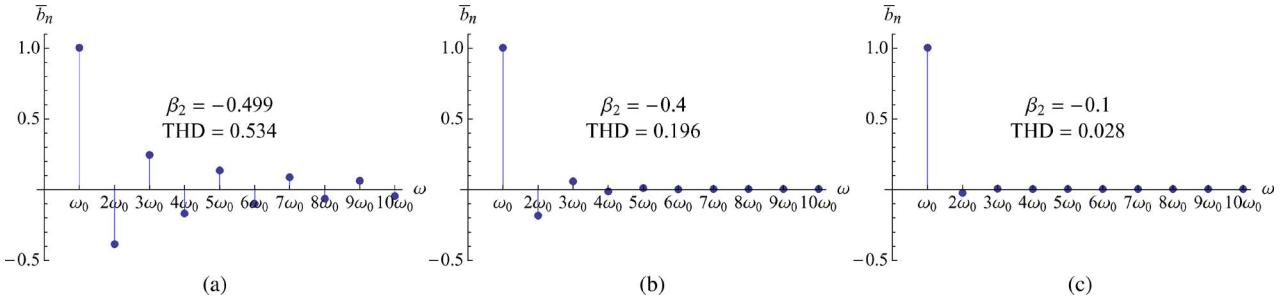


Fig. 1. *The amplitude spectrum of the output of an HP memristor given by (14) when driven by a pure sinusoid. Each subfigure depicts the first ten harmonic components for three different β_2 values. The spectra illustrate that the larger the algebraic value of β_2, or equivalently, the more linear is the resistor, the less its harmonic distortion. The THD index is also reported, evaluated using (18). The amplitude of each component is normalized with respect to the fundamental: $\bar{b}_n=b_n/b_1$.*

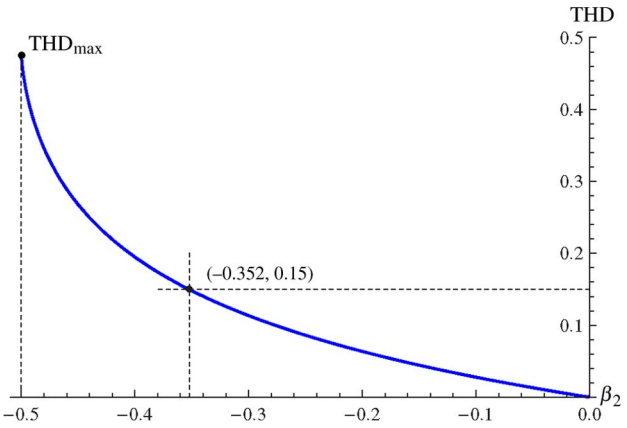


Fig. 2. *Dependence of the THD upon the renormalized parameter β_2 of the HP memristor. The THD decreases monotonically for $-0.5 < \beta_2 < 0$ as the memristor tends to linearity. On the one extreme, as $\beta_2 \to -0.5$, the device becomes more nonlinear and THD is maximized. On the other extreme, as $\beta_2 \to 0$, the device approaches linearity and THD $\to 0$.*

For example, consider a fabricated memristor modeled by (13) and characterized by the THD $-\beta_2$ curve of Fig. 2. For this specific memristor, we require, for example, a THD value less than 15%. The only parameters that can be adjusted in this case are the amplitude and frequency of the excitation. Therefore, as indicated in Fig. 2, if we select the amplitude and frequency of the input such that $\omega_0/A = (\alpha+1)k_2/(\beta_2 \mathcal{M}_0^{\alpha+1})$ with $\beta_2 \in [-0.352, 0)$, then at the output THD levels of less than 15% should be expected.

IV. NETWORKS OF BERNOULLI MEMRISTORS

The analysis in Sections II and III focused on the properties of single memristors. In this section, we further progress the study of memristor properties by investigating systematically the behavior of networks of memristors. In what follows, it is shown that a network containing either charge- or flux-controlled Bernoulli memristors is equivalent to a single Bernoulli memristor. The result is verified for series and parallel networks for which the equivalent memristance is also derived. In each case, the output is calculated as an explicit function of the input for the example configurations. Finally, we study the effect of a series parasitic resistance on the output of the memristor.

A. Compliance of Memristor Networks With Bernoulli's Differential Equation

A network containing only charge-controlled memristors defined by

$$\begin{aligned} \dot{Q}(t) &= I(t) \\ V(t) &= \mathcal{M}(Q(t))I(t) \end{aligned} \tag{19}$$

or flux-controlled memristors defined by

$$\begin{aligned} \dot{\Phi}(t) &= V(t) \\ I(t) &= \mathcal{W}(\Phi(t))V(t) \end{aligned} \tag{20}$$

with positive incremental memristance (memductance) is equivalent to a single Bernoulli memristor characterized by a Bernoulli differential equation. This follows directly from Chua's Closure Theorem and Existence and Uniqueness Theorem [1], which show that any network of only memristors is equivalent to a single unique memristor, and the fact that any single passive memristor described by (19) or (20) is a Bernoulli memristor (see Section II-B and [27]). Consequently, networks consisting of either charge- or flux-controlled Bernoulli memristors can be transformed into a linear form and in some cases their output can be expressed as an explicit function of the input using the procedure detailed in Section II-A.

B. Memristors in Series

Consider first a network of N charge-controlled Bernoulli memristors configured in series, as shown in Fig. 3, with each one having memristance $\mathcal{M}_j(Q(t))$, where $j = 1, 2, 3, \ldots, N$. If we let $V_j(t)$ denote the voltage across the jth memristor and $I(t)$ the common current passing through the network then we can write N Bernoulli differential equations, one for each memristor

$$\dot{I}(t) - I(t)\frac{\dot{V}_j(t)}{V_j(t)} = -I^2(t)\frac{\dot{\mathcal{M}}_j(t)}{V_j(t)}. \tag{21}$$

If we multiply both sides of (21) by its corresponding voltage $V_j(t)$ and then add them together, it results in

$$\dot{I}(t)\sum_{j=1}^{N} V_j(t) - I(t)\sum_{j=1}^{N}\dot{V}_j(t) = -I^2(t)\sum_{j=1}^{N}\dot{\mathcal{M}}_j(t). \tag{22}$$

Relying on Kirchhoff's voltage law (KVL) and the linearity of differentiation, we can write for the total voltage $V(t)$

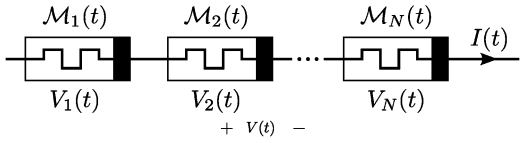


Fig. 3. *Memristors in series. A network with N Bernoulli memristors configured in series. $\mathcal{M}_j(t)$ and $V_j(t)$ denote the memristance and the voltage across the jth memristor, respectively, where $j = 1, 2, 3, \ldots, N$. $I(t)$ is the current passing through the memristors and $V(t) = V_1(t) + \ldots + V_N(t)$ is the total voltage across the network.*

across the network

$$\dot{V}(t) = \frac{d}{dt}\left[\sum_{j=1}^{N} V_j(t)\right] = \sum_{j=1}^{N} \dot{V}_j(t). \tag{23}$$

Hence, we can express (22) in terms of the total voltage $V(t)$ and the common current $I(t)$

$$\dot{I}(t) - I(t)\frac{\dot{V}(t)}{V(t)} = -\frac{I^2(t)}{V(t)}\sum_{j=1}^{N}\dot{\mathcal{M}}_j(t). \tag{24}$$

Because we have initially assumed that the network consists of charge-controlled memristors, i.e., $\dot{\mathcal{M}}_j(t) = (d\mathcal{M}_j(Q)/dQ)I(t)$, it follows that (24) is a BDE. Equating the right-hand side (RHS) of (24) with the RHS of the corresponding BDE of a single charge-controlled voltage-driven memristor from Table 1 and integrating with respect to t shows that (24) describes a network that is equivalent to a single memristor with memristance

$$\mathcal{M}(t) + \mathcal{M}_0 = \sum_{j=1}^{N}\int_0^t \dot{\mathcal{M}}_j(\tau)\,d\tau = \sum_{j=1}^{N}\left[\mathcal{M}_j(t) + \mathcal{M}_{0j}\right] \tag{25}$$

where $\mathcal{M}_{0j} = \mathcal{M}_j(0)$ and $\mathcal{M}_0 = \mathcal{M}(0)$ and we have used $\dot{\mathcal{M}}(Q) = (d\mathcal{M}Q/dQ)I(t)$.

As an example, assume that the series network in Fig. 3 consists of three charge-controlled Bernoulli memristors whose memristance dynamics are modeled by[1]:

$$\dot{\mathcal{M}}_j(t) = k_{2j}I(t), \qquad j = 1, 2, 3 \tag{26}$$

and the input voltage is a sine wave. By applying the procedure in Section II-A, we can obtain an analytic expression describing the output current $I(t)$ in terms of the total input voltage $V(t) = V_1(t) + V_2(t) + V_3(t)$. The resulting expression is as follows:

$$I(t) = \frac{V(t)}{\left[\left(\sum_{j=1}^{3}\mathcal{M}_{0j}\right)^2 + 2\left(\sum_{j=1}^{3}k_{2j}\right)\int_0^t V(\tau)d\tau\right]^{\frac{1}{2}}} \tag{27}$$

[1]The index 2 in the subscript of the constant k_{2j} denotes the charge-controlled case in agreement with Table 2.

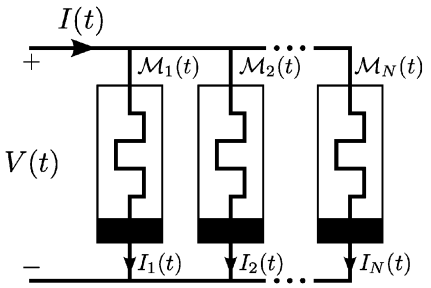


Fig. 4. *Memristors in parallel. A network of N Bernoulli memristors configured in parallel. $\mathcal{M}_j(t)$ and $I_j(t)$ denote the memristance and the current through the jth memristor, respectively, where $j = 1, 2, 3, \ldots, N$. $V(t)$ is the voltage across the memristors and $I(t) = I_1(t) + \ldots + I_N(t)$ is the total current passing through the network.*

which has the same general form as the output expression for a single charge-controlled memristor (Table 2 with $\alpha = 1$).

C. Memristors in Parallel

Consider now a network of N charge-controlled Bernoulli memristors connected in parallel, as shown in Fig. 4, with each one having memristance $\mathcal{M}_j(Q(t))$, where $j = 1, 2, 3, \ldots, N$. If we let $V(t)$ denote the common voltage across the network and $I_j(t)$ the current passing through the jth memristor branch then we can write N Bernoulli differential equations, one for each memristor

$$\dot{I}_j(t) - I_j(t)\frac{\dot{V}(t)}{V(t)} = -I_j^2(t)\frac{\dot{\mathcal{M}}_j(t)}{V(t)} \tag{28}$$

which added together yield

$$\sum_{j=1}^{N}\dot{I}_j(t) - \frac{\dot{V}(t)}{V(t)}\sum_{j=1}^{N}I_j(t) = -\frac{1}{V(t)}\sum_{j=1}^{N}I_j^2(t)\dot{\mathcal{M}}_j(t). \tag{29}$$

Exploiting Kirchhoff's current law (KCL) and the linearity of differentiation we can write for the total current $I(t)$

$$\dot{I}(t) = \frac{d}{dt}\left[\sum_{j=1}^{N}I_j(t)\right] = \sum_{j=1}^{N}\dot{I}_j(t). \tag{30}$$

Hence, we can express (30) in terms of $I(t)$ as

$$\dot{I}(t) - I(t)\frac{\dot{V}(t)}{V(t)} = -\frac{I^2(t)}{V(t)}\mathcal{M}^2(t)\sum_{j=1}^{N}\frac{\dot{\mathcal{M}}_j(t)}{\mathcal{M}_j^2(t)} \tag{31}$$

where we have also used $I_j^2(t) = V^2(t)/\mathcal{M}_j^2(t) = I^2(t)\mathcal{M}^2(t)/\mathcal{M}_j^2(t)$ with $\mathcal{M}(t)$ denoting the equivalent memristance of the network. Based on our initial assumption that the network consists of charge-controlled memristors, $\dot{\mathcal{M}}_j(t) = (d\mathcal{M}_j(Q_j)/dQ_j)I_j(t) = d\mathcal{M}_j(Q_j)/dQ_j(V(t)/\mathcal{M}_j(Q_j))$, which substituted in (31) verifies that (31) is a BDE. Equating the RHS of (31) with the RHS of the BDE governing the single charge-controlled voltage-driven memristor from Table 1 shows that

$$\dot{\mathcal{M}}(t) = \mathcal{M}^2(t)\sum_{j=1}^{N}\frac{\dot{\mathcal{M}}_j(t)}{\mathcal{M}_j^2(t)}$$

from which we can determine, after integrating with respect to t, the equivalent memristance of the network

$$\mathcal{M}^{-1}(t) + \mathcal{M}_0^{-1} = \sum_{j=1}^{N}\int_0^t \frac{\dot{\mathcal{M}}_j(\tau)}{\mathcal{M}_j^2(\tau)}d\tau = \sum_{j=1}^{N}\left[\mathcal{M}_j^{-1}(t) + \mathcal{M}_{0j}^{-1}\right] \quad (32)$$

where $\mathcal{M}_{0j} = \mathcal{M}_j(0)$ and $\mathcal{M}_0 = \mathcal{M}(0)$ and we have used $\dot{\mathcal{M}}(Q) = (d\mathcal{M}Q/dQ)I(t)$.

Assume, as an example, that the parallel network in Fig. 4 consists of three charge-controlled Bernoulli memristors with memristance dynamics described again by (26) and it is excited by a sinusoidal voltage. In this example, it is straightforward to obtain the output current in terms of the input voltage by employing KCL and substituting, for the individual currents, the output expression for charge-controlled memristors as shown in Table 2 for $\alpha = 1$. The resulting output expression is given by

$$I(t) = \sum_{j=1}^{3} I_j(t) = \sum_{j=1}^{3}\frac{V(t)}{\left[\mathcal{M}_{0j}^2 + 2k_j\int_0^t V(\tau)d\tau\right]^{\frac{1}{2}}}. \quad (33)$$

Fig. 5 shows the I–V response of a single charge-controlled memristor driven by a sine wave (solid line). Its output current is given in Table 2 ($\alpha = 1$). The figure compares the response of the single memristor to that of a series (dotted line) and a parallel network (dashed line). Each of the two networks consists of three memristors identical to the single one, arranged in series and parallel, respectively. The output current for the series configuration is given by (27) and for the parallel by (33). Note that for the parallel network the equivalent memristance of the circuit is smaller compared to that of the single memristor, therefore the amplitude of the output current increases. The opposite occurs in the case of the series network.

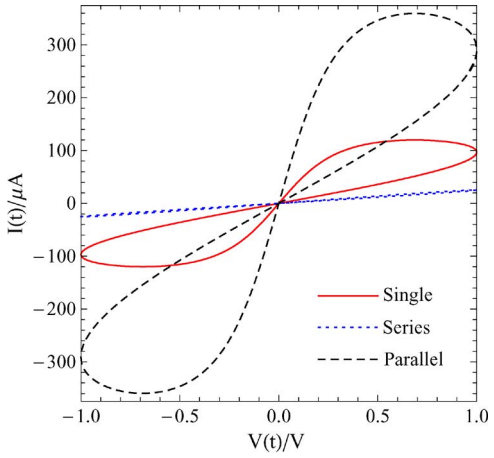


Fig. 5. *I–V characteristic curves of a network of memristors in series (dotted line) and in parallel (dashed line) compared to that of a single memristor (solid line). The series and parallel circuits consist of three memristors identical to the single one. The excitation in all three cases is the sine wave $v(t) = v_0\sin(2\pi f_0 t)$. The output for the single memristor is given by Table 2 ($\alpha = 1$); the series, by (27); and the parallel, by (33). The equivalent memristance of the series network is larger than the single memristor so that the amplitude of the output current decreases causing the I–V to collapse almost to a straight line. The opposite happens for the parallel network. These plots have been generated with parameters from the HP memristor [4] given in detail in Fig. 7.*

Although we have assumed charge-controlled memristors for the networks in parallel and series, one may derive analogous results for the flux-controlled case. For completeness, the results for both flux- and charge-controlled networks of memristors are summarized in Table 6. It is interesting to observe that the series charge-controlled network is the dual of the parallel flux-controlled network, whereas the parallel network of charge-controlled memristors appears as the dual of the series flux-controlled network.

D. Parasitic Resistance

The results derived in Section IV-B for the network of memristors connected in series can also be used to model the output when Bernoulli memristors are connected in series with constant resistors. A particular case, which is of practical interest, is the modeling of the parasitic series resistance appearing when the ideal device is physically realized. Among others, a common cause of parasitic resistance are the ohmic contacts connecting the device with the rest of the circuit. Our framework can be employed to investigate the impact of such parasitics upon the behavior of our ideal Bernoulli memristor.

Assume a constant parasitic resistance connected in series with an ideal charge-controlled Bernoulli memristor,

Table 6 Series and Parallel Memristor Networks

Network Type		Governing Bernoulli	Equivalent Mem-property
Flux Controlled	Series	$\dot{V}(t) - V(t)\frac{\dot{I}(t)}{I(t)} = -\frac{V^2(t)}{I(t)}\mathcal{W}^2(t)\sum_{j=1}^{N}\frac{\dot{\mathcal{W}}_j^2(t)}{\mathcal{W}_j^2(t)}$	$\mathcal{W}^{-1}(t) + \mathcal{W}_0^{-1} = \sum_{j=1}^{N}\left[\mathcal{W}_j^{-1}(t) + \mathcal{W}_{0j}^{-1}\right]$
	Parallel	$\dot{V}(t) - V(t)\frac{\dot{I}(t)}{I(t)} = -\frac{V^2(t)}{I(t)}\sum_{j=1}^{N}\dot{\mathcal{W}}_j(t)$	$\mathcal{W}(t) + \mathcal{W}_0 = \sum_{j=1}^{N}[\mathcal{W}_j(t) + \mathcal{W}_{0j}]$
Charge Controlled	Series	$\dot{I}(t) - I(t)\frac{\dot{V}(t)}{V(t)} = -\frac{I^2(t)}{V(t)}\sum_{j=1}^{N}\dot{\mathcal{M}}_j(t)$	$\mathcal{M}(t) + \mathcal{M}_0 = \sum_{j=1}^{N}[\mathcal{M}_j(t) + \mathcal{M}_{0j}]$
	Parallel	$\dot{I}(t) - I(t)\frac{\dot{V}(t)}{V(t)} = -\frac{I^2(t)}{V(t)}\mathcal{M}^2(t)\sum_{j=1}^{N}\frac{\dot{\mathcal{M}}_j^2(t)}{\mathcal{M}_j^2(t)}$	$\mathcal{M}^{-1}(t) + \mathcal{M}_0^{-1} = \sum_{j=1}^{N}\left[\mathcal{M}_j^{-1}(t) + \mathcal{M}_{0j}^{-1}\right]$

as shown in Fig. 6. Then, the time derivative of the equivalent memristance of the circuit is given by

$$\dot{\mathcal{M}}(t) = \dot{\mathcal{M}}_1(t) + \frac{d}{dt}[\mathcal{R}_p] = \frac{d\mathcal{M}(Q(t))}{dQ(t)}I(t) \tag{34}$$

with $\mathcal{R}_p$ representing the total parasitic resistance value. Therefore, the BDE describing the circuit in Fig. 6 is not affected by the presence of the constant parasitic resistance in the model because $d[\mathcal{R}_p]/dt = 0$. Hence, assuming that $\dot{\mathcal{M}}_1(t)$ is given by (26), the output current can be evaluated using (27) and is given analytically by

$$I(t) = \frac{V(t)}{\left[(\mathcal{M}_{01} + \mathcal{R}_p)^2 + 2k_2\int_0^t V(\tau)d\tau\right]^{\frac{1}{2}}} \tag{35}$$

where $\mathcal{M}_{01} = \mathcal{M}_1(0)$, k_1 is a constant, and $V(t) = V_e(t) + V_p(t)$. $V_e(t)$ denotes the effective voltage applied across the ideal memristor and $V_p(t)$ is the voltage drop across the parasitic resistance.

Fig. 7 illustrates the effect of the parasitic resistance value on the I–V plane [Fig. 7(a)], as well as on the I–t and V_e–t [Fig. 7(b)] plane when the circuit in Fig. 6 is driven by a sine wave $V(t) = V_0\sin(\omega_0 t)$, whose output is given by (35). The two plots compare the response of the circuit with (solid lines) and without (dashed lines) the presence of parasitic resistance. It is clear that the effective voltage applied on the memristor $V_e(t)$ is reduced when $\mathcal{R}_p > 0$, which results in an output current of reduced amplitude. The parameters used for generating these plots were extracted from HP's ideal TiO_2 memristor [4] since its memristance can be described by (26) [27]. Therefore, $k_2 = (1 - \mathcal{R}_{OFF}/\mathcal{R}_{ON})(\mathcal{R}_{ON}/D)^2\mu_v$ and $\mathcal{M}_{01} = \mathcal{R}_{ON}(w_0/D) + \mathcal{R}_{OFF}(1 - w_0/D)$ and we have chosen $\mathcal{R}_p = (2.5/100)\mathcal{R}_{OFF}$. This indicative choice of $\mathcal{R}_p$ facilitates to illustrate clearly the effect of $\mathcal{R}_p$ upon the memristor behavior.

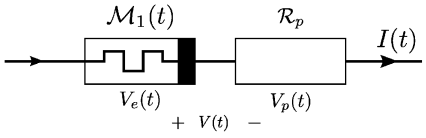


Fig. 6. *Series parasitic resistance. A memristor with memristance $\mathcal{M}_1(t)$ and its series constant parasitic resistance $\mathcal{R}_p$. $V_e(t)$ is the effective voltage across the memristor and $V_p(t)$ is the voltage across the parasitic resistance. The total voltage is denoted by $V(t) = V_e(t) + V_p(t)$ and the total current through by $I(t)$.*

V. CONCLUSION

With the above treatment, we have highlighted the usefulness of the introduction and application of the Bernoulli mathematical framework in the study of memristors. The direct consequence of the identification of the Bernoulli dynamics is the fact that the expression of the memristor output as a function of the input in a closed-form becomes feasible in some cases.

Such closed-form expressions allow for a systematic and insightful evaluation of the behavior of memristors shedding light from a perspective significantly different from the one afforded when only numerical simulations of memristors are employed. For example, as shown in this paper, the derivation of closed-form I–V characteristics of memristors allows both for the quantitative determination of the THD levels at the output of a sinusoidally driven device and the determination of deviations from ideality when series parasitic resistors are considered. The value of the formalism is further exemplified through the systematic consideration of the behavior of memristors for which the time derivative of the memristance is proportional not only to $V(t)$ [or $I(t)$] but also to $V^\alpha(t)$ [or $I^\alpha(t)$].

In addition to the above, the closed-form expressions derived describing the I–V characteristic of the memristor progress the field by revealing in an analytic and insightful manner the role of the parameter β in the behavior of the device. In particular, it was shown that properties such as the harmonic content at the memristor's output (see Table 5) and the hysteresis pinch of the device's I–V [27] are controlled by adjusting β. This quantity lumps together both low-level device parameters related to the underlying physical mechanism and fabrication of the memristor and parameters related to the input signal. According to the

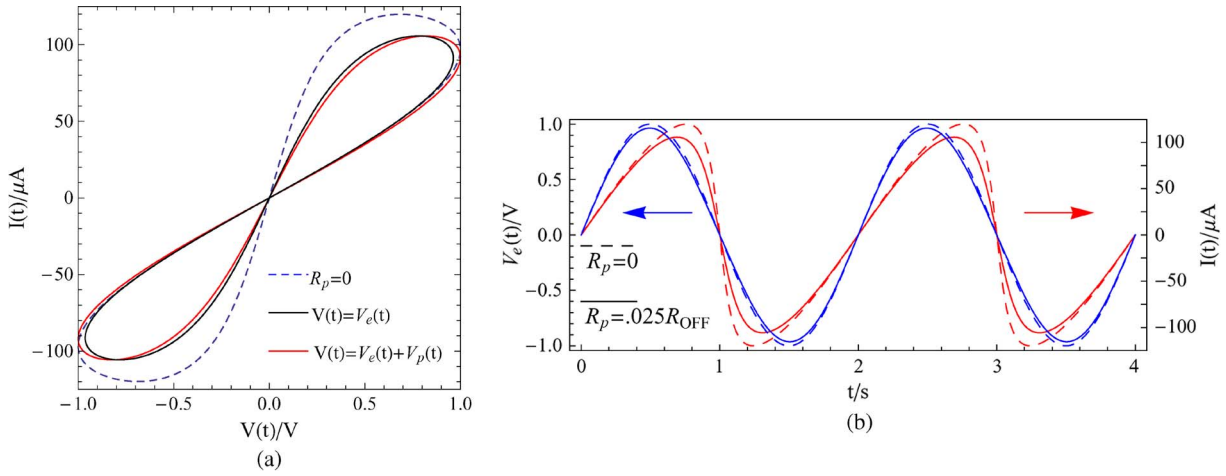


Fig. 7. ***Effect of series parasitic resistance. (a) An illustration of the input/output characteristic curve in two different situations. The blue dashed curve corresponds to the case where the parasitic resistance is completely ignored. The two solid lines correspond to the case when*** $\mathcal{R}_p = 0.025\mathcal{R}_{\rm OFF}$***. The black solid curve is a plot of the effective voltage across the memristor against the output current whereas the red solid curve is a plot of the total voltage across the circuit against the output current. (b) A plot of the effective voltage across the memristor and the output current against time, when*** $\mathcal{R}_p = 0$ ***(dashed curves) and*** $\mathcal{R}_p = 0.025\mathcal{R}_{\rm OFF}$ ***(solid curves). Both, (a) and (b) clearly indicate that the effective voltage across the memristor is reduced as a result of the parasitic resistance. This causes the amplitude of the output current to decrease. For these simulations, the input used was a sine wave of the form*** $V(t) = V_0 \sin(2\pi f_0 t)$ ***and the output as given by (35). The parameters used were the following:*** $V_0 = 1$ **V,** $f_0 = 0.5$ **Hz,** $D = 10$ **nm,** $d = \mathcal{R}_{\rm OFF}/\mathcal{R}_{\rm ON} = 160$**,** $\mathcal{R}_{\rm ON} = 100\ \Omega$**,** $\mathcal{R}_{\rm OFF} = d\mathcal{R}_{\rm ON}$**,** $\mu_v = 10^{-14}$ **ms**$^{-1}$ **V**$^{-1}$**, and** $w_0/D = 0.1$**.**

analysis presented here it is the combination of the above parameters in β and not any of these parameters individually which define the behavior of a specific memristor.

This work has also extended the framework beyond single memristors to cover also networks of memristors. It was shown that networks consisting of either charge- or flux-controlled Bernolli memristors are equivalent to a single Bernoulli memristor. Exploiting the compliance with Bernoulli dynamics it was demonstrated how the mathematical framework allows the systematic treatment of series and parallel networks of memristors.

The research question which emerges naturally from the above discussion has to do with the theoretical and practical implications of extending our general mathematical framework for the analysis of networks (other than series and parallel) of memristors and other mem-elements (memcapacitors and meminductors) which also comply with Bernoulli dynamics [26]. The authors will report on these elsewhere. ■

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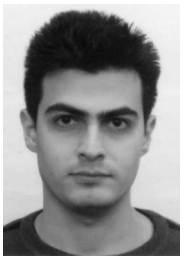

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