25nm 64Gb MLC NAND Technology and Scaling Challenges

Invited Paper

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Introduction: This paper describes the Intel-Micron 25nm NAND technology including the key process advances, scaling challenges, and cell electrical results. This technology is used for the manufacturing of a world leading edge 64Gb MLC NAND memory. This cell is the smallest cell in production.

Cell: The ½ pitch of the cell is 24.5nm in the WL direction and 28.5nm in the BL direction resulting in a cell size of $0.0028\mu m^2$. The asymmetric cell was used to enable advanced ONO IPD and room for the control gate to fit between FGs. The NAND string has 64 active and 2 dummy cells next to the select gate. The select gate is scaled to 0.14µm. The BL contacts are staggered for lithographic reasons. The cell size with overhead is $0.0034\mu m^2$ (22% overhead). Cross sections in the BL and WL directions are shown in Figs. 1, 2 and 3.

Process Technology: The cell is patterned using advanced pitch reduction techniques employing wet 193nm lithography optimized to minimize line edge roughness and cd variation. At a 25nm dimension, a 5% cd variation is ~3 Si lattices. Fig. 5 shows the production cd control capability. The AA trench depth cannot be scaled significantly because of the ~6V isolation requirements during inhibit, resulting in a 7:1 aspect ratio for the STI trench. Any structural imbalance can lead to the AA bending resulting in displacement of the channel by as much as 10nm for a 3nm cd offset. An example of a non-optimized STI fill is shown in Fig. 4. Controlling the structural bending is critical for achieving good electrical distributions of the cells in the NAND array. The aggressive WL pitch scaling leads to increased WL to WL capacitance as well as increased cell to cell interference [1, 2]. An airgap is introduced between the WLs to overcome both these problems. Fig 6 shows the airgap benefits. An airgap is also used between the BLs (Fig 7).

Die: A photograph of the 64Gb die is shown in Fig. 8. The die size is 167 mm^2 (4.8GB/cm^2) which is an increase of 103% in bit density over the Intel-Micron 34nm 32Gb technology. The small die allows use of a standard TSOP package.

Cell Scaling and Electrical Results: One of the critical scaling problems for the NAND cell is the reduction in the number of stored electrons per level with scaling. Fig. 9 shows the number of electrons required for a 100mV Vt shift as a function of the technology node. As the FG capacitance is scaled and the number of electrons stored on the FG decreases, electrons located outside the floating gate starts to dominate the cell Vt shift. Fig. 10 shows various locations within a NAND cell where charge can become trapped, and the results of a TCAD simulation showing the number of electrons at each of these locations needed to shift the Vt of a cell by 100mV. The results show that the cell Vt is more sensitive to charge trapped in several of the parasitic locations than if the charge were on the FG. The tunnel oxide, IPD, and other dielectrics were optimized to minimize charge leakage and trapping resulting in performance similar to previous generations. Fig. 11 shows cycling characteristics of the cell demonstrating very little trap-up through 10K cycles. Many challenges of cell fluctuation become pronounced at these small feature sizes. One of these is the issue of dopant fluctuation. Fig. 12 shows the mean and $\pm 3\sigma$ for the number of dopant atoms vs. feature size. At 25nm, the Vt can be expected to vary by ~30% purely due to the random dopant fluctuation. This gets reflected in the NAND cell Vt distributions requiring additional optimization of the programming algorithms for achieving MLC performance similar to prior generations. Small cells also suffer from "Giant" RTS noise caused by an interaction of random dopant fluctuation ($\propto 1/\sqrt{WL}$) with interface traps ($\propto 1/WL$) [4]. Fig. 13 shows the variation in cell Vt due to RTS for multiple generations of NAND technology. The degradation is obvious. Fig. 14 shows the normalized value of RTS for a 4.7σ cell plotted against $1/\sqrt{WL}$ showing a reasonable fit. Program noise [5] also degrades the σ of the Vt distribution due to a variation in the number of electrons injected with each programming pulse. This problem degrades with scaling as the total number of electrons on the FG is reduced. Fig. 15 shows the degradation in Vt placement with scaling at a constant pulse step. Fig. 16 shows a monte carlo simulation showing the impact of program noise on the Vt distribution. The scaling problems discussed previously are partially addressed through careful process optimization and partially though the used of increased error correction (Fig 17). BCH code, however, starts to show diminishing returns with increased ECC (Fig. 18) and future NAND will require more advanced ECC.

Conclusion: A highly manufacturable 25nm 64Gb NAND technology has been developed. Many physical and electrical scaling challenges were overcome. Severe scaling challenges have to be overcome to continue NAND scaling.

Acknowledgement: The authors gratefully acknowledge the Intel-Micron IMFT team that performed the work presented.

References:

[1] Tsukamoto, et. al, JJAP, Vol.46, No 4B 2007, pg. 2184
[2] Lee, et. al., EDL, May 2002, pg. 264
[3] Prall, NVSMW 2007, pg. 5
[4] Tega, et. al., IEDM '06 , pg. 460
[5] Compagnoni, et. al, TRED, Oct. 2008, pg. 2695

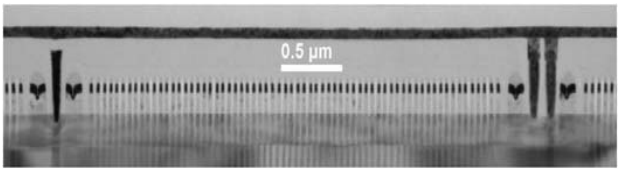


Fig. 1 Cross-section of complete string.

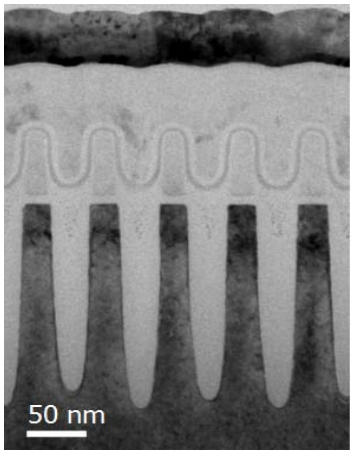


Fig. 2 Cross-section of the cell in the active area (width) direction. The variation in trench depth is due to cd variation.

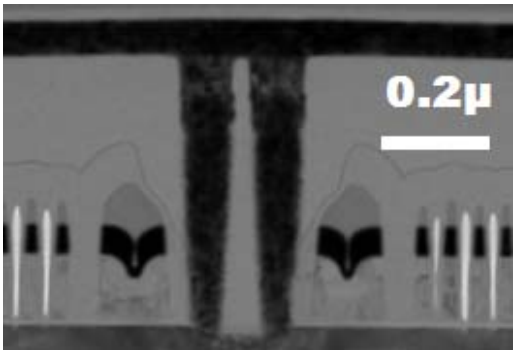


Fig. 3 Cross-section of the cell in the Wordline (WL) L direction showing select gate and contacts.

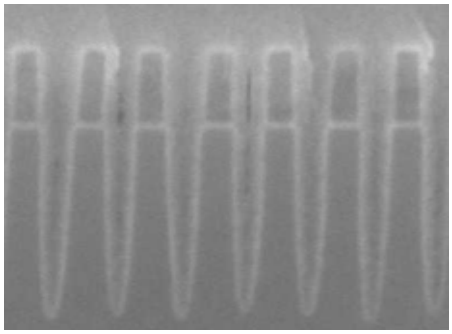


Fig. 4 Cross-section of the cell in the AA direction showing severe AA bending for a non optimized process.

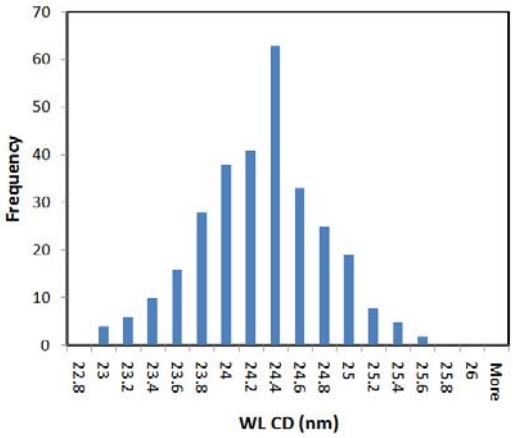


Fig. 5 Production CD control over several days showing CD control capability of better than +/- 3nm for a total range of better than 6 Si lattice constants (+/-5%)

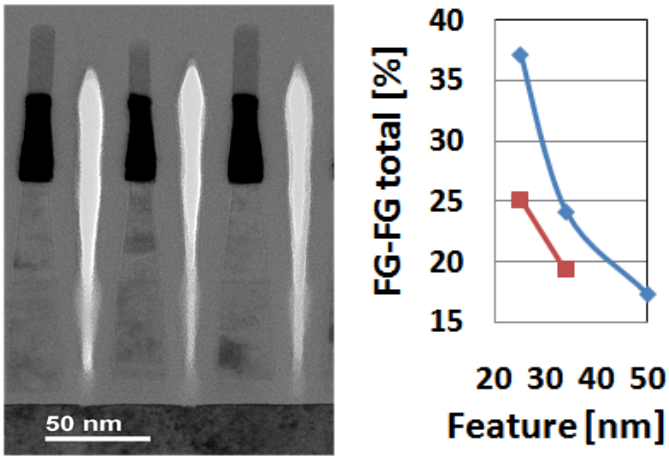


Fig. 6 Cross-section of the cell in the WL direction showing the WL airgap and reduction in total FG-FG coupling with airgap (red square) and without (blue diamond). WL bending is caused by sample preparation. A 25% reduction in total interference is achieved with the airgap.

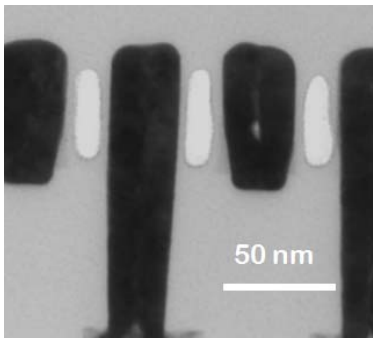


Fig. 7 Cross-section of the cell in the BL direction showing the bit line airgap. A 30% reduction in BL capacitance was achieved.

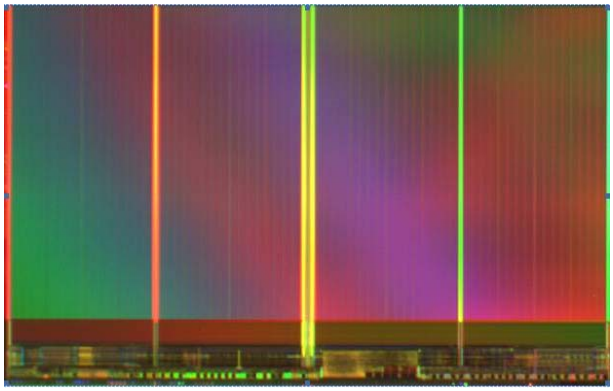


Fig. 8 Die photo of the 25nm 64Gb MLC die

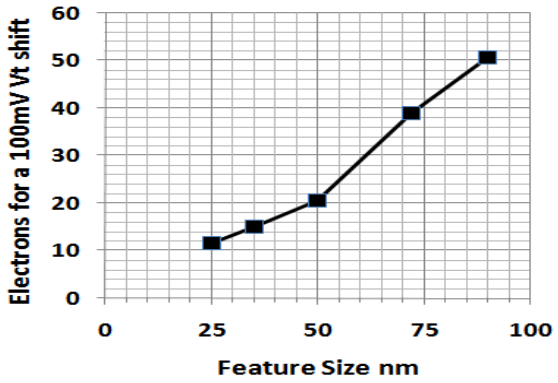
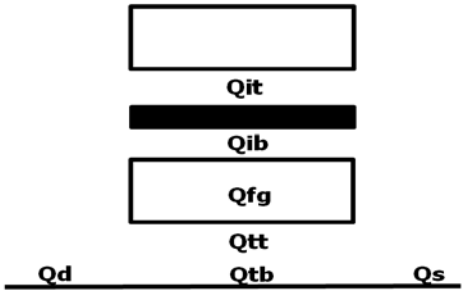


Fig. 9 Electrons required for a 100mV Vt shift vs. cell feature size. In an MLC cell, the separation between levels is typically 300-500mV or about 30-50 electrons at 25nm.



	50nm	35nm	25nm
Qtb	4	2	1
Qtt	9	7	4
Qib	22	17	9
Qit	149	103	100
Qs	33	9	5
Qd	61	16	10
Qfg	18	12	10

Fig. 10 Locations of parasitic charge in a NAND cell and the required number of electrons at these locations to shift the cell Vt by 100mV.

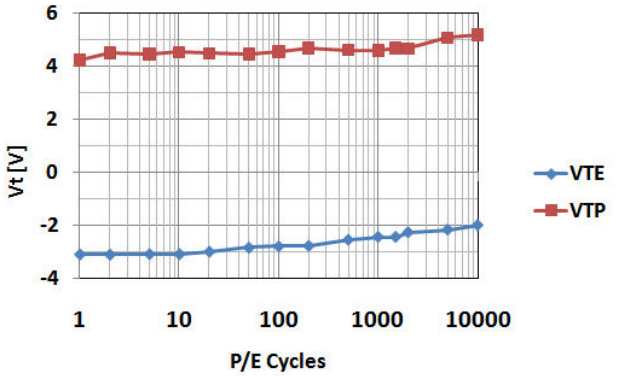


Fig. 11. NAND cell cycling characteristics showing very little trap-up.

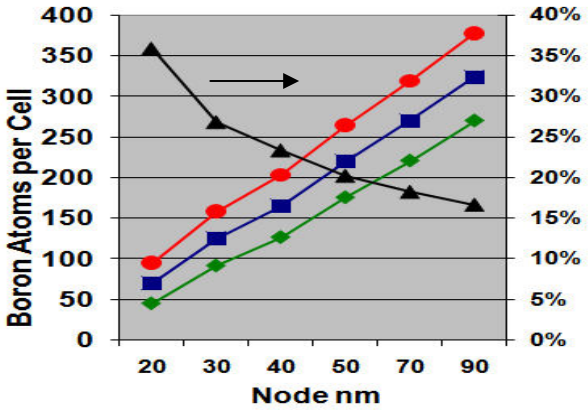


Fig. 12 Number of Boron atoms per cell (mean: square, -3σ : diamond, +3σ: circle vs. feature size. The triangle shows the ±3σ percentage divided by the mean.

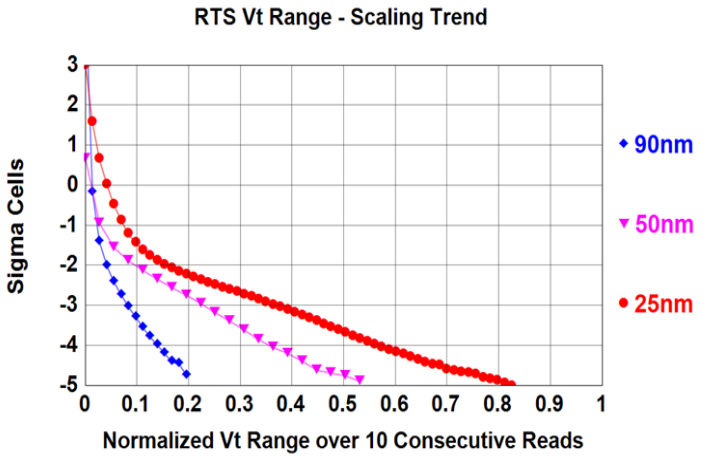


Fig. 13. RTS noise vs. cell feature size for 3 generations of NAND technology. Ten reads per cell were performed.

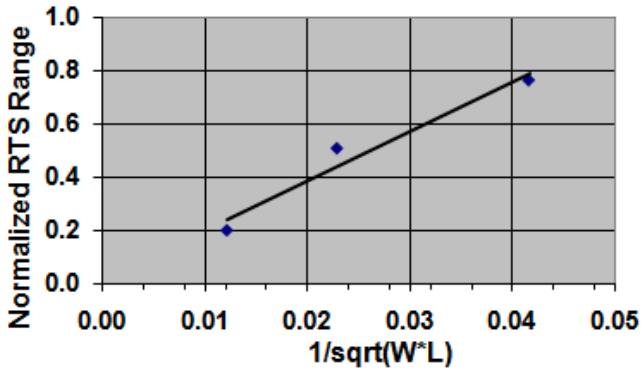


Fig. 14 4.7σ RTS noise vs. 1/sqrt(WL) showing RTS scaling as 1/sqrt(WL)

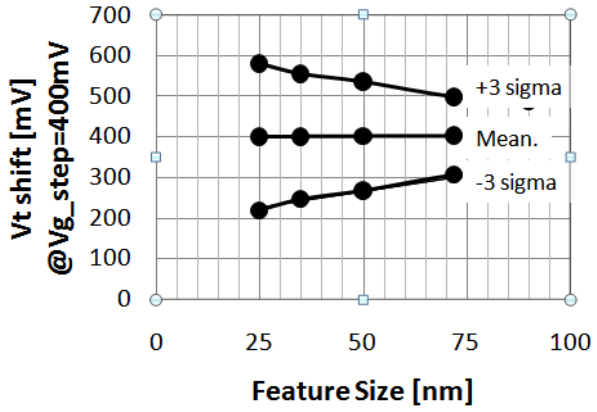


Fig. 15. Program Noise variation in Cell Vt shift vs. feature size for a constant 400mV increase in the programming pulse voltage showing an increasing variation in Vt shift with scaling. This is due to random quantum mechanical tunneling because of the small number of electrons tunneling to the floating gate during the programming event.

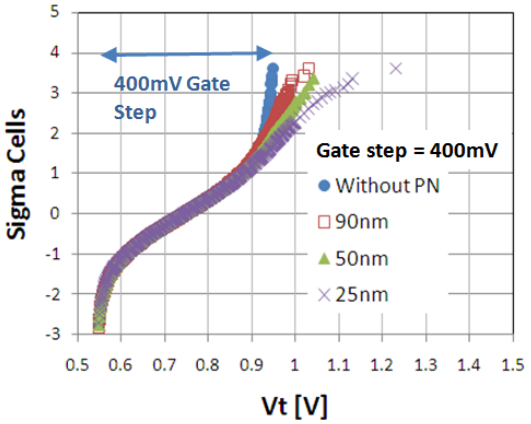


Fig. 16. Monte Carlo simulation of Vt distribution due to PN. The -3σ tail is the program verify level at .55V.

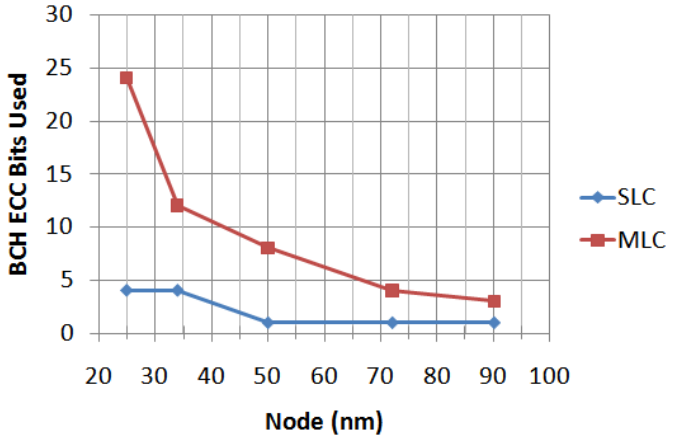


Fig. 17 Trend of increasing error correction with NAND scaling to compensate for scaling issues including: few electrons, dopant fluctuations, RTS, and program noise. The code word size was 512B for all points except 25nm MLC which uses a code word of 1024B for improved error coverage.

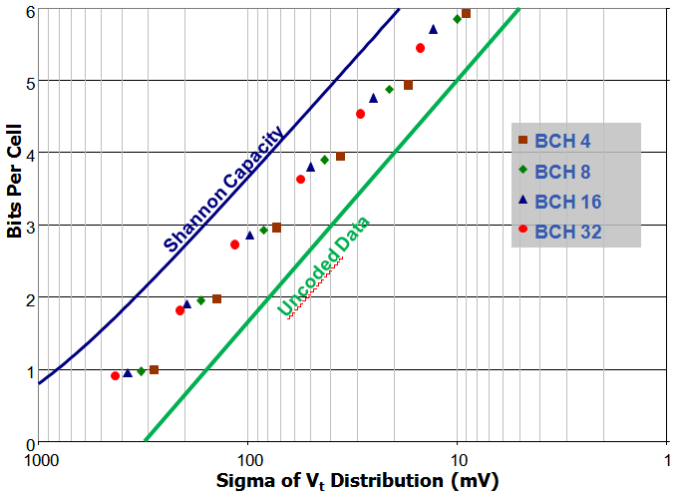


Fig. 18. Multi-bit per cell capability plotted vs. the standard deviation of the Vt distribution showing the critical need to tightly control the cell Vt distribution to continue scaling and to achieve MLC and multi-bit per cell capability. Note that the effectiveness of the BCH incrementally decreases with increasing ECC bits. The effectiveness of BCH ECC is reaching its limits requiring more advanced ECC algorithms.