KATHOLIEKE UNIVERSITEIT LEUVEN

ESAT

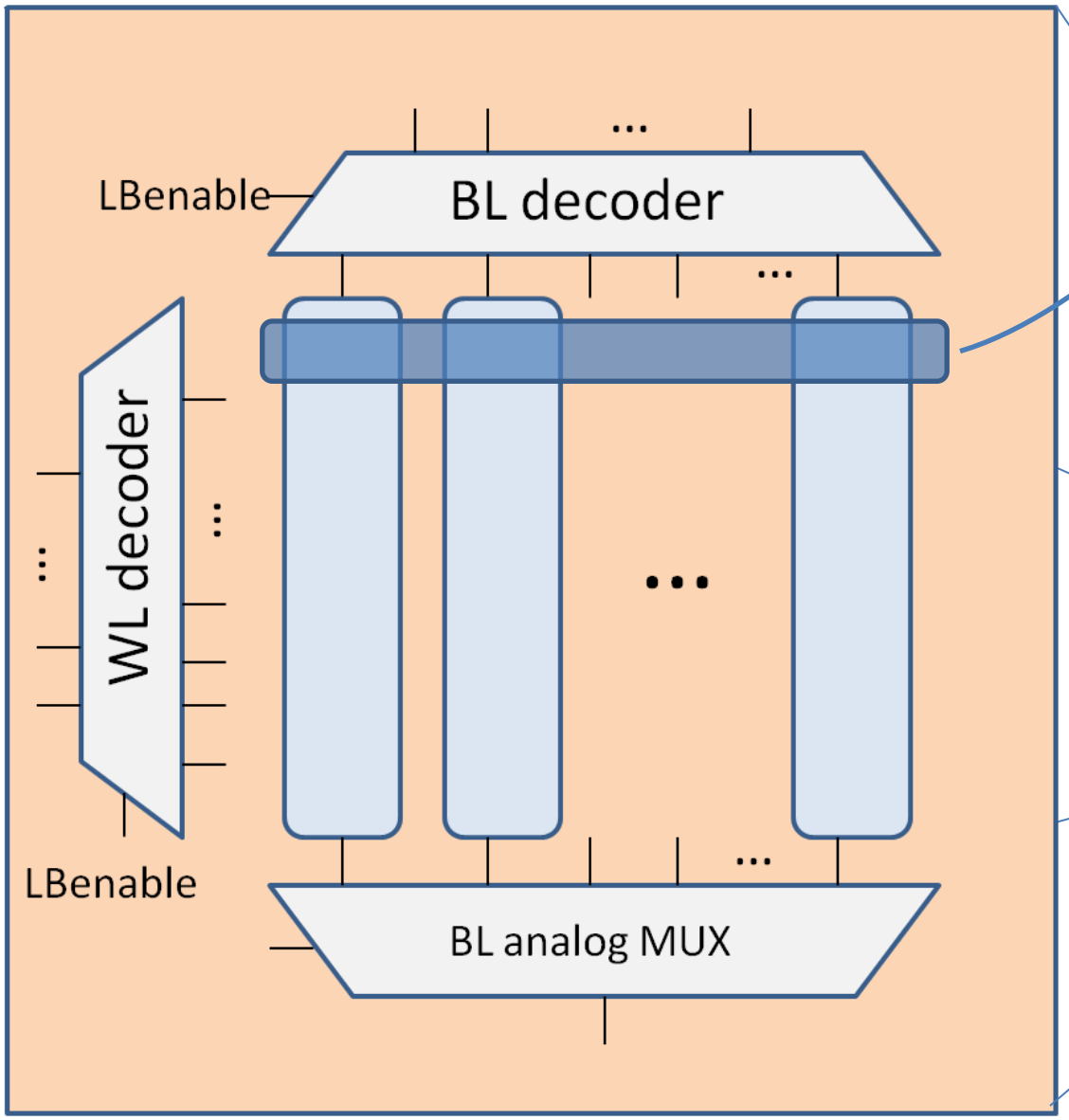
Architecture Design

Alexander Standaert
Wouter Diels

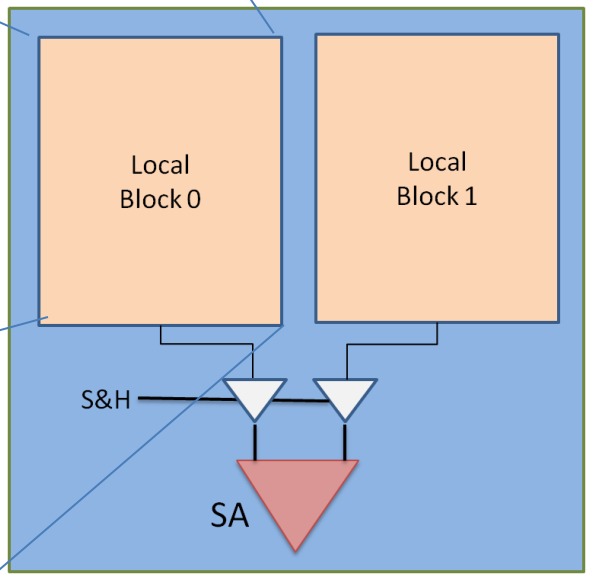
OUTLINE

- REFERENCE ARRAY
- DECODERS + BUFFERS
- VDD/SPEED TEST
- CONDOR
- ARCHITECTURE ANALYSIS
- CONCLUSION : Conclusion and Future work

REFERENCE ARRAY



Reference now inside Localblock:



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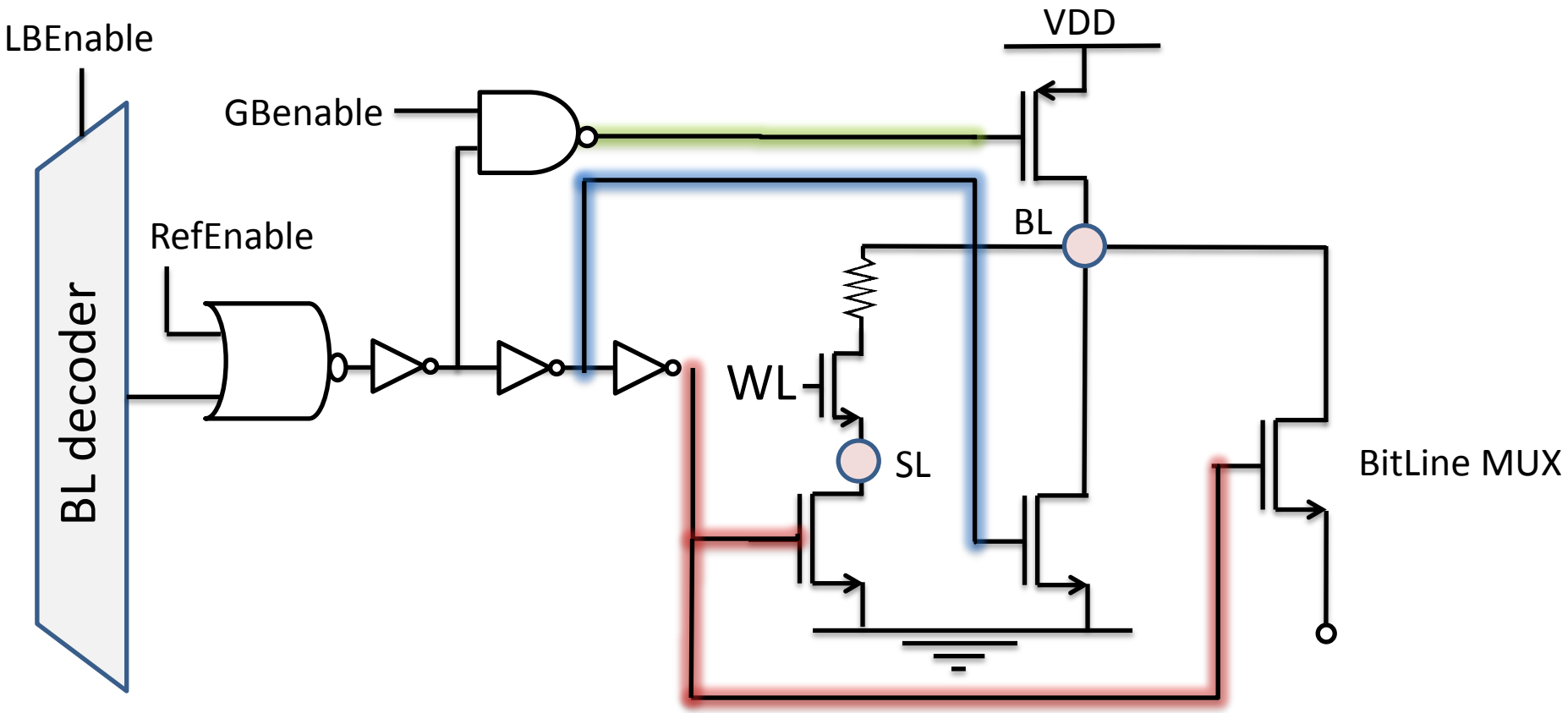

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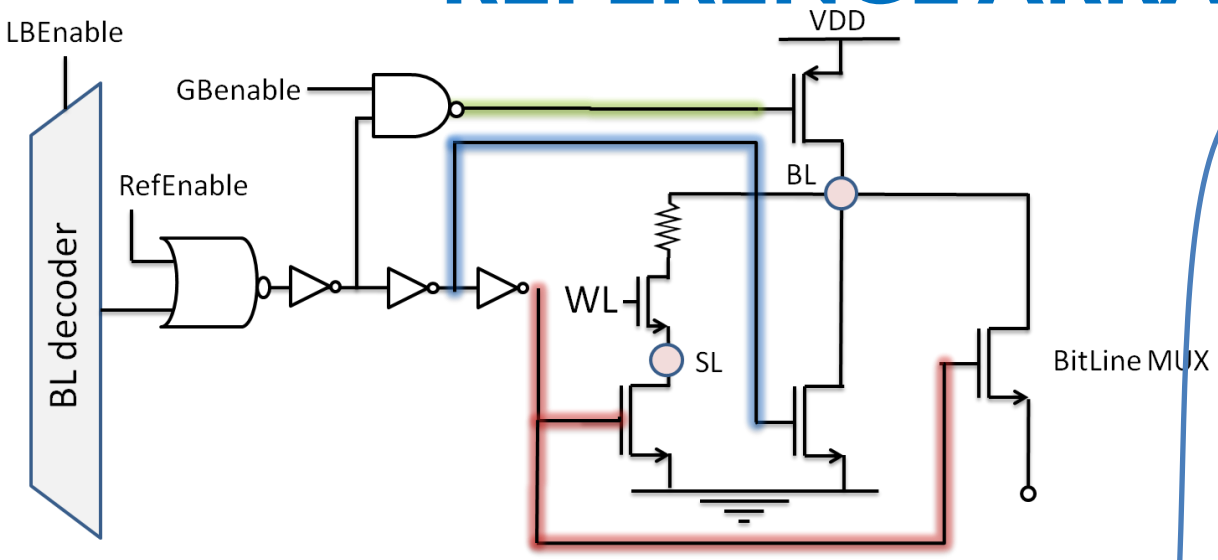
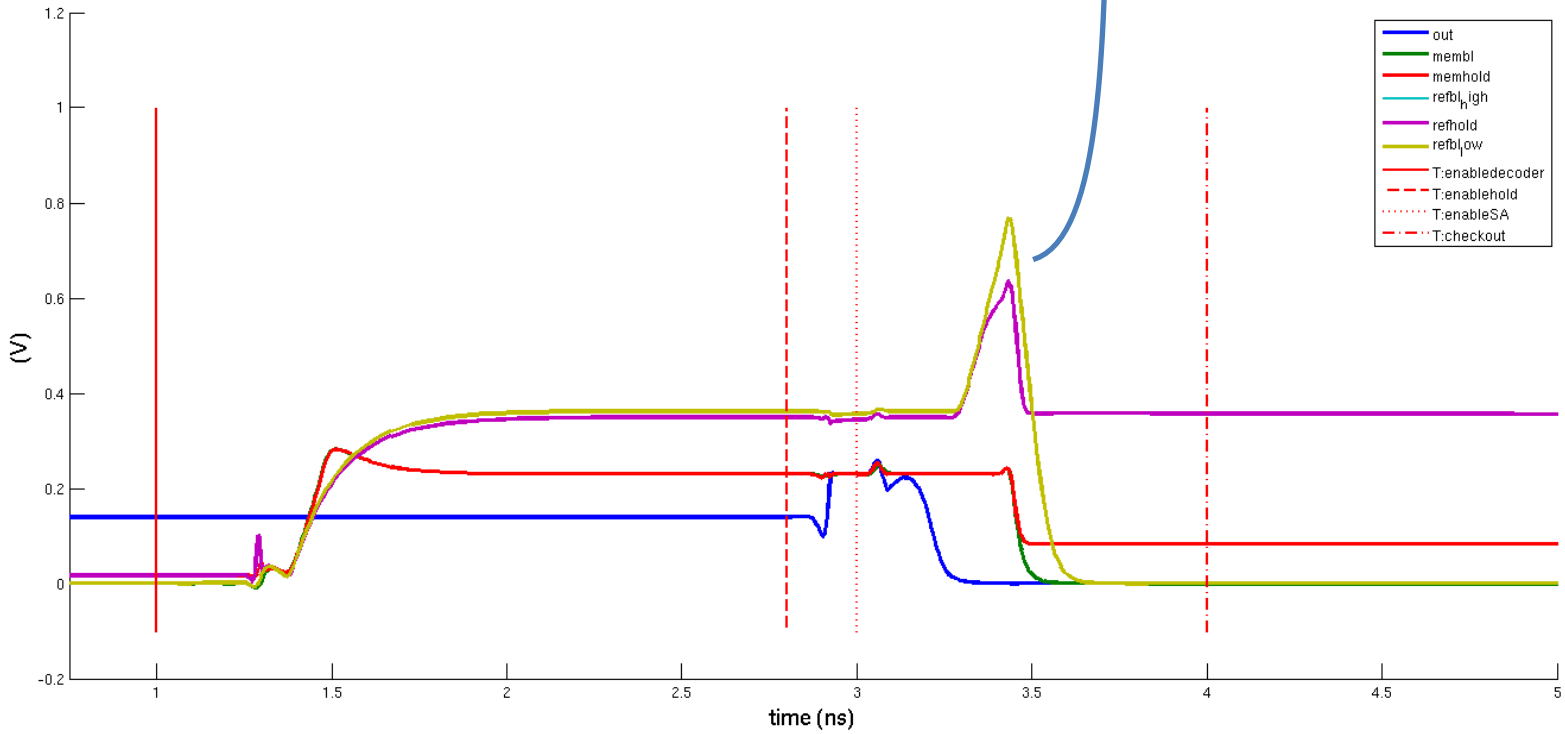


WL_ref = RefEnable
→ Load is still on when all the rest is of



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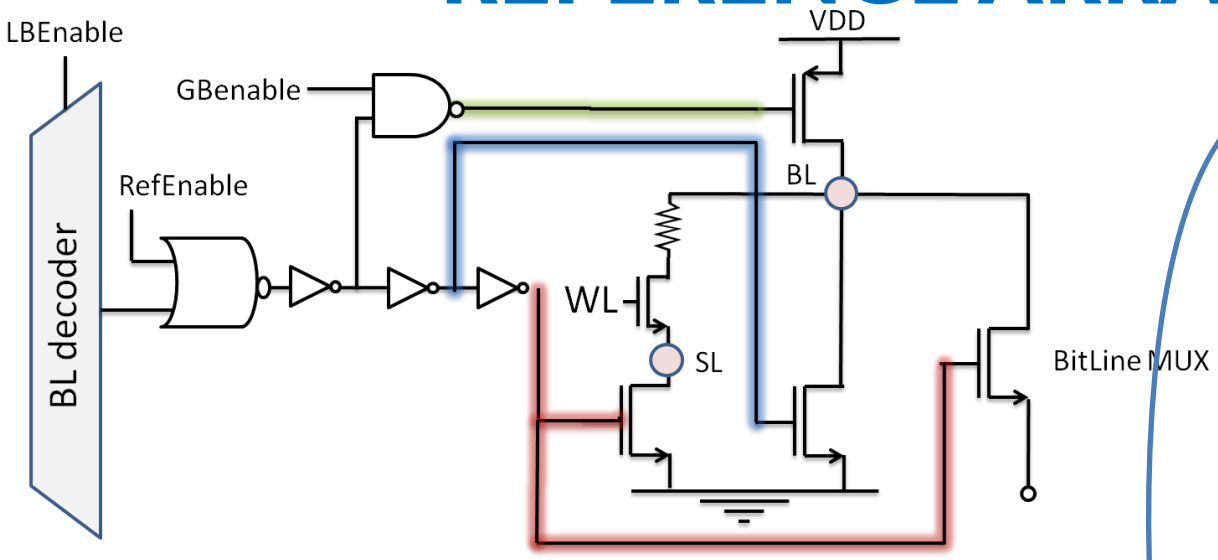
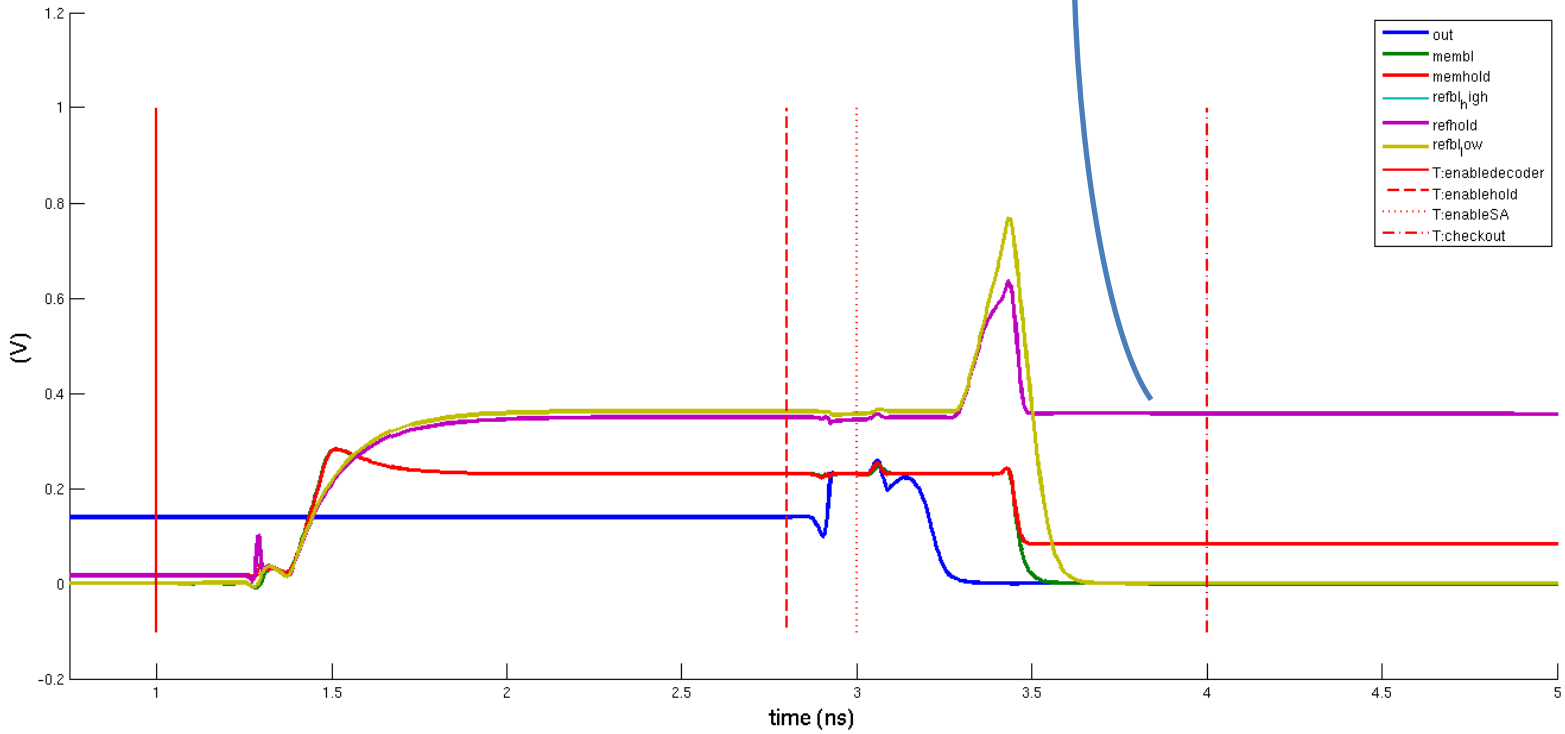


BitLine Mux is turned off before the node is fully discharged. Charge trapped is really small and doesn't affect next read cycle



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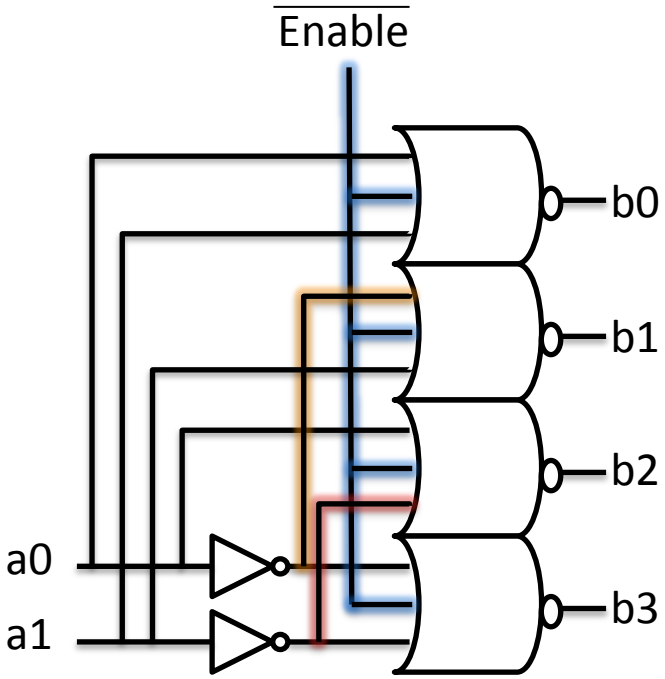
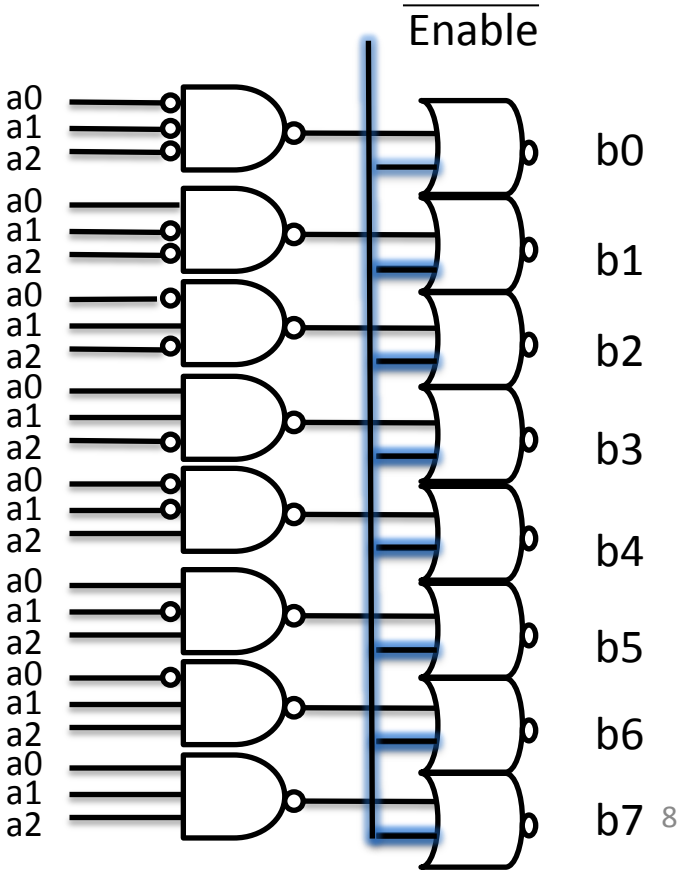
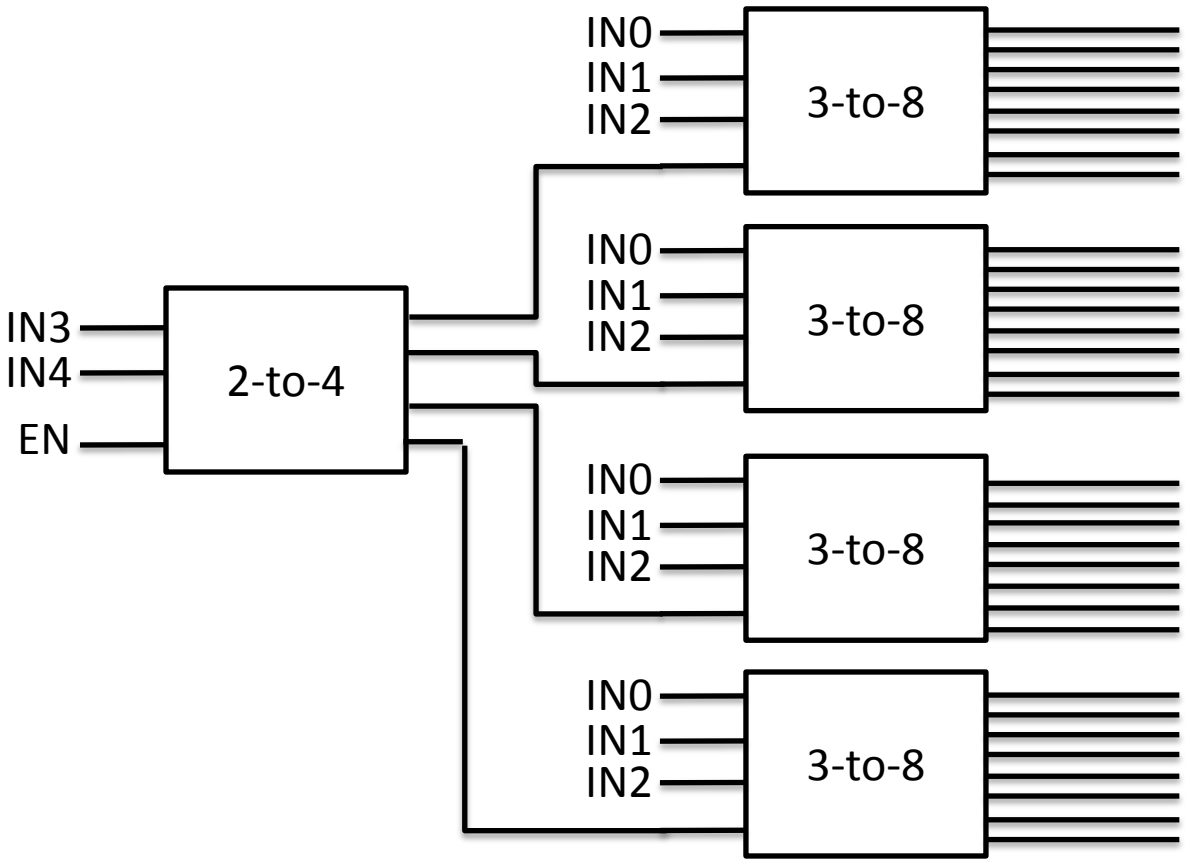
- Based on cascading 2-to-4 decoders and 3-to-8 decoders

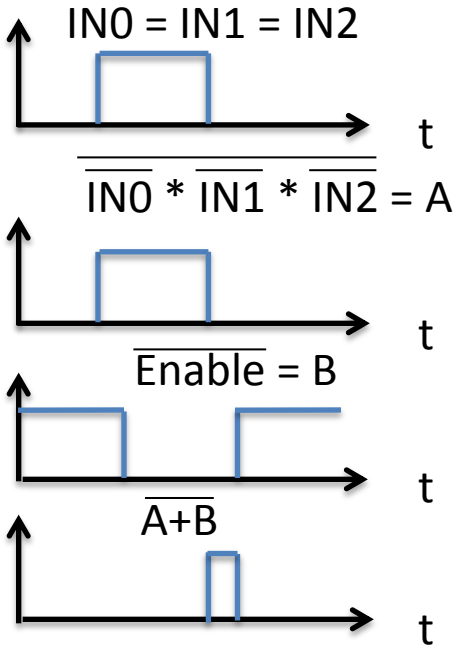




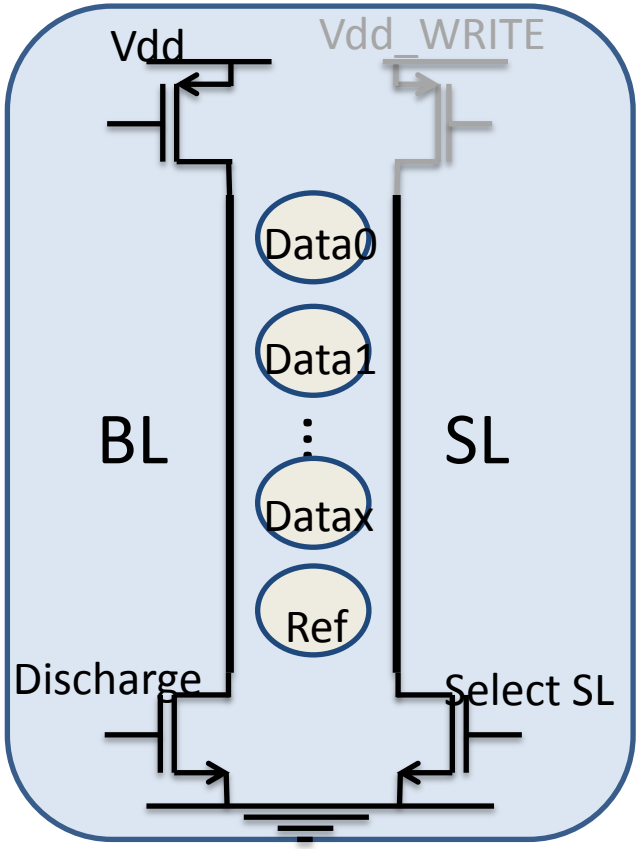
Decoders

- Glitches because NOR-gated output
- Solve by using NAND + Inverter Decoder topology, more area, worth it?





BL Decoders



- BL capacitance increases when more cells per BL
- Delay increases too
- Can't decrease Pull-Up resistance because BL will be charged to VDD
- Limited #WLpB
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WL Decoders: optimization

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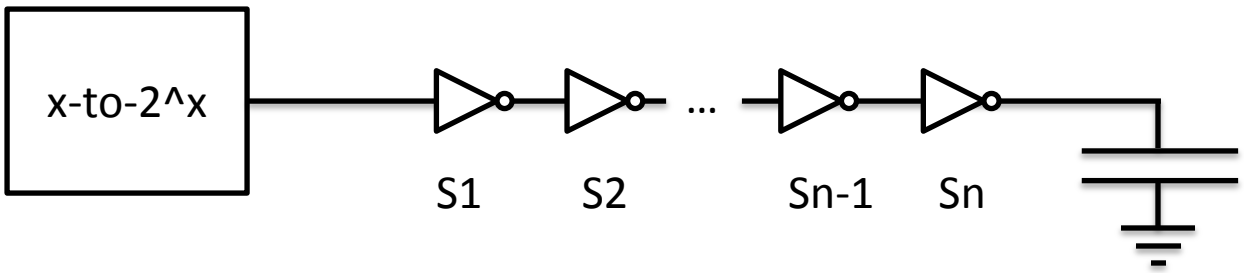
  - Different paths towards output consisting of different amount of stages and logical efforts
- Solution: Minimal decoder with sized inverter chain at output towards WL?



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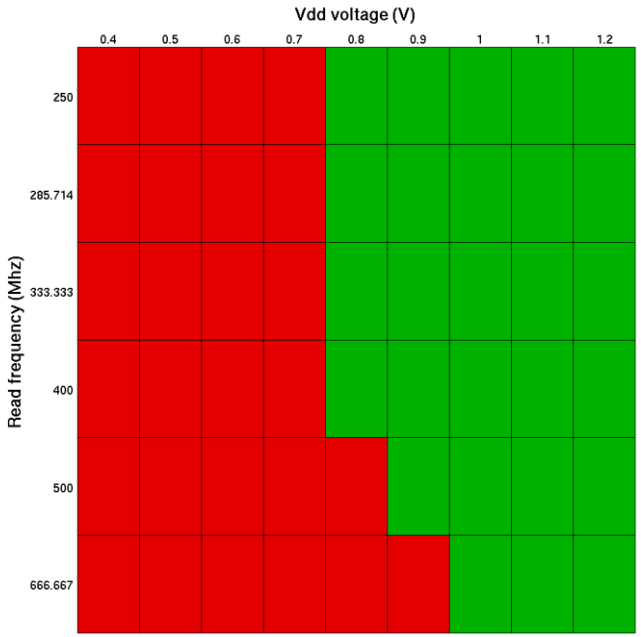
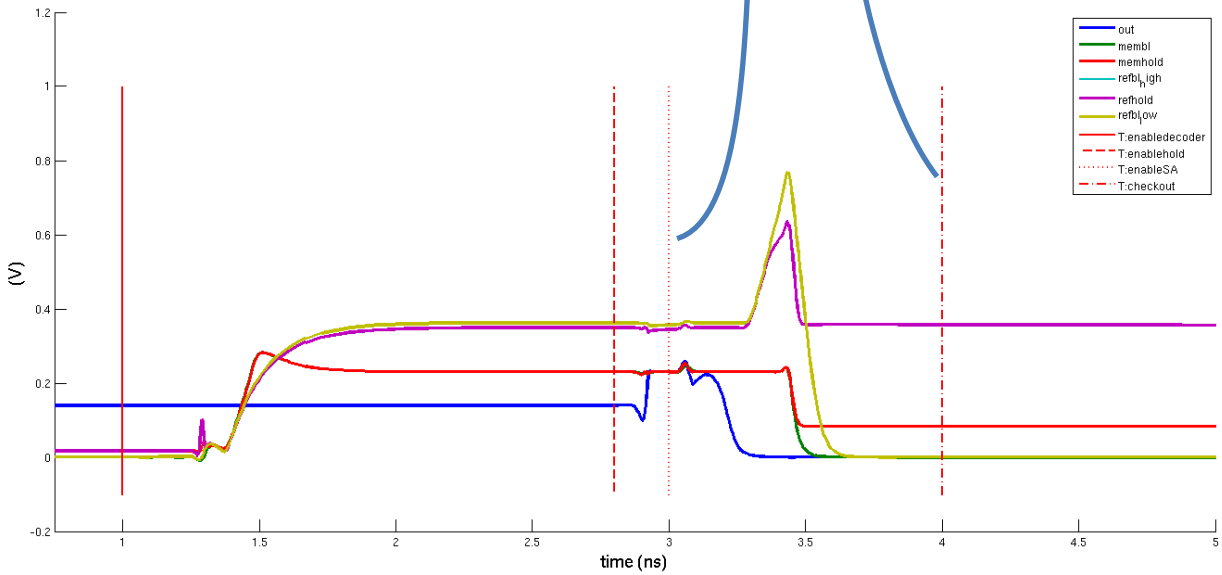
VDD/SPEED TEST



Reduce t_Saenable for different values of vdd till system fails.

t_checkout is cnt for now, but we should be able to decrease it to push speed limit futher



NOTE : no mismatch yet because SA is not yet sized !!!

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CONDOR

- Grid computing system
- Introduced at VISICS by Bert Deknuydt
- Last week we got it working with Mat2Spice and Spectre
- Documentation and new version Mat2Spice can be found on the wiki https://wiki.esat.kuleuven.be/visics/condor
- It is currently looked into getting it installed in the pc rooms

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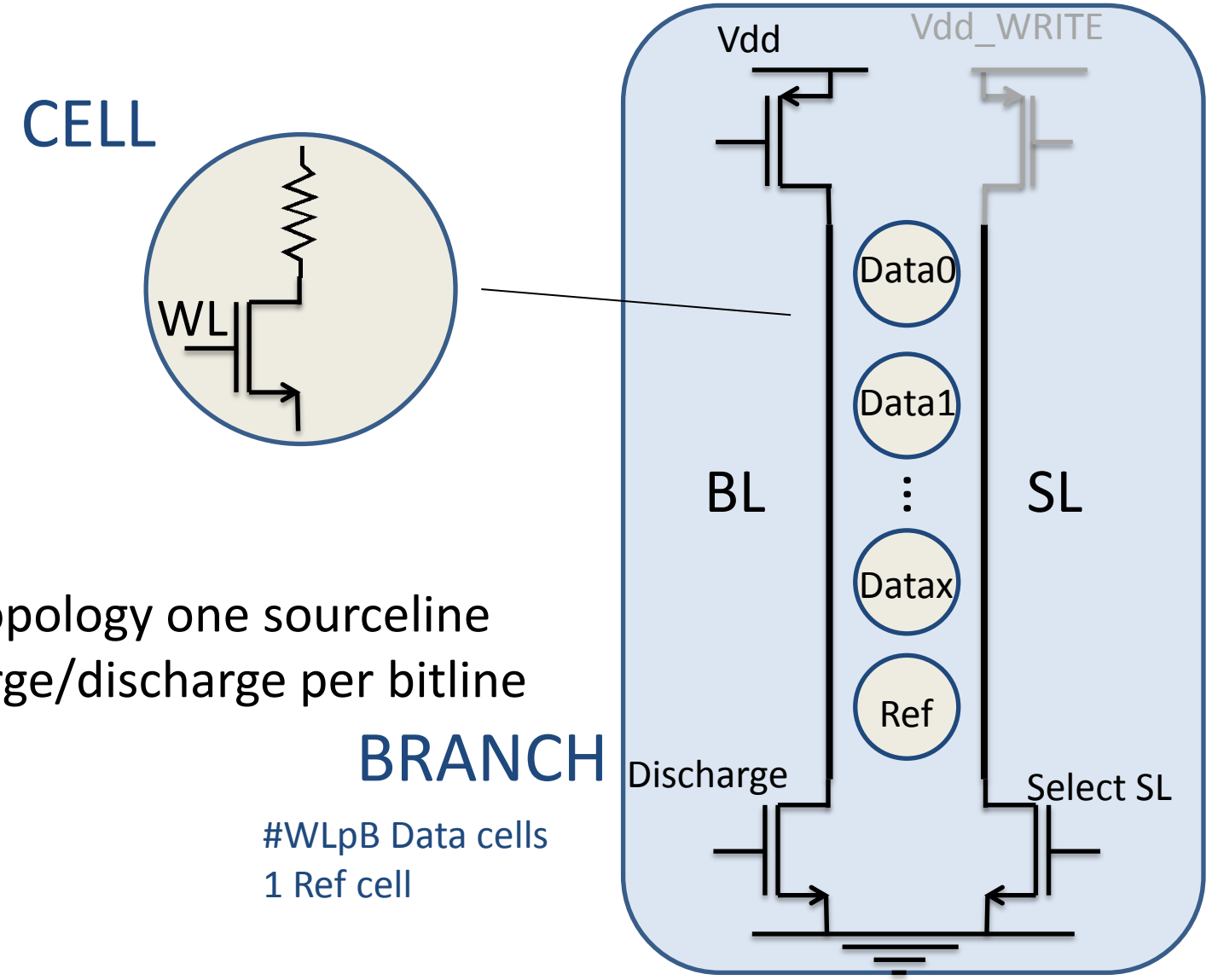
- Research optimal architecture parameters
  Probably need to trim netlist to achieve acceptable simulation time
- Inverter chain to buffer RefEnable (huge load to drive)
- Optimize decoders? (and calculate decoder area)
- Automate timing signals for Sense Amplifier

Main architecure

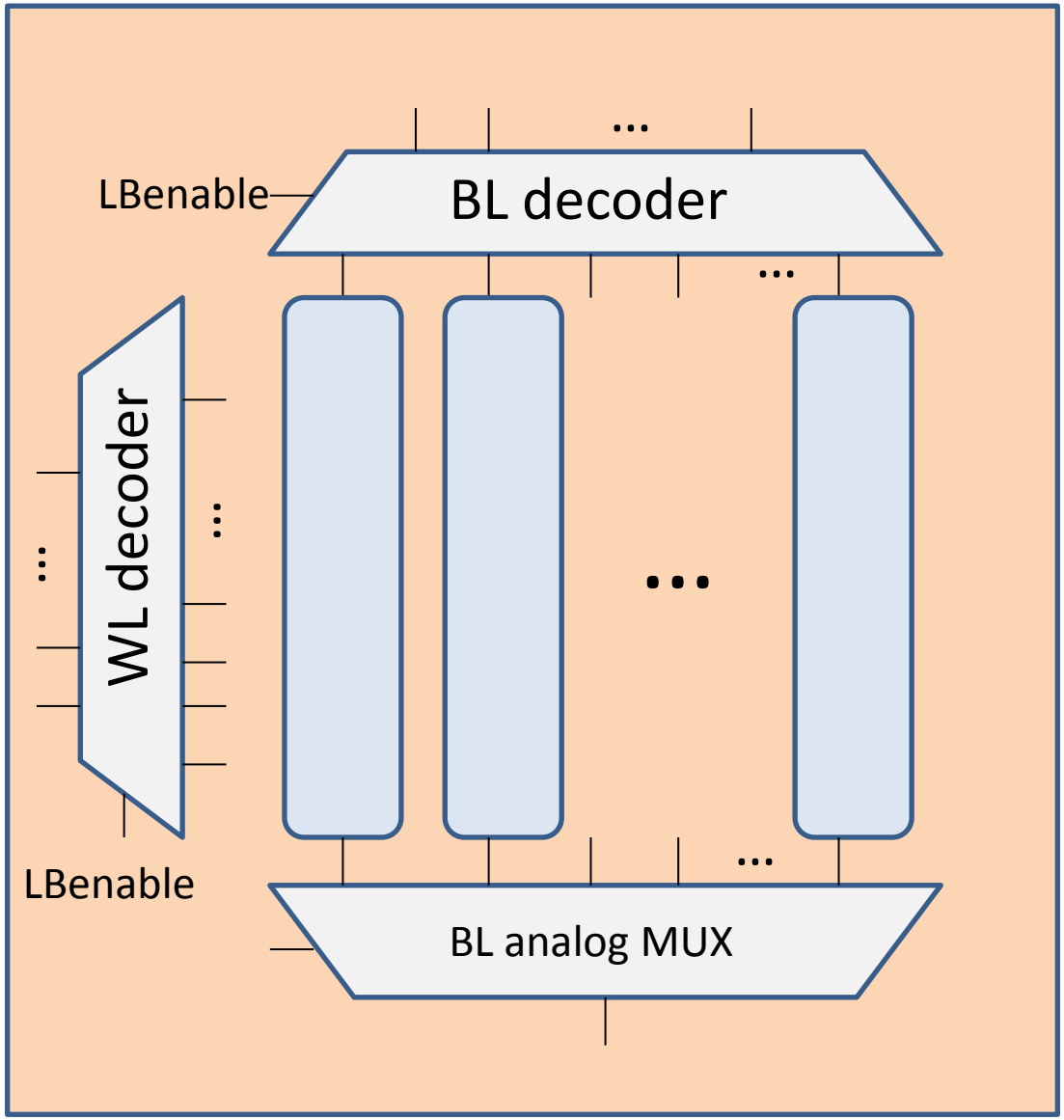


In this topology one sourceline and charge/discharge per bitline Ideal?

BRANCH

#WLpB Data cells
1 Ref cell

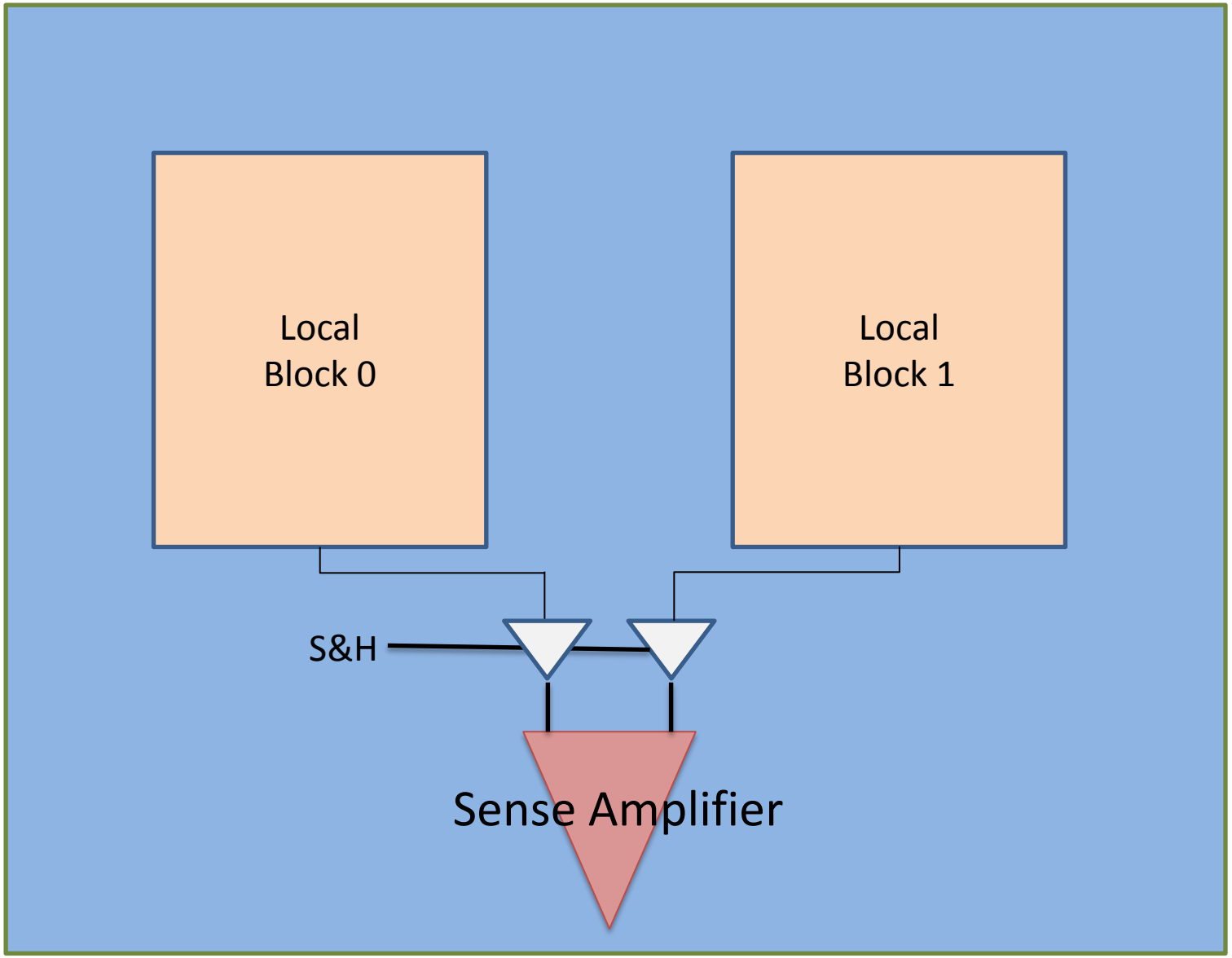
Main architecure (cont.)



Local Block

#BLpLB Branches
→#BLpLB*#WLpB Data cells
→#BLpLB Ref cells

Global Block **Main architecure (cont.)**



Architecture parameters

- # Global Blocks
- # BitLines per Local Block
- # WordLines per Branch

Total number of cells = 2*NoGB*NoBLpLB*NoWLpB

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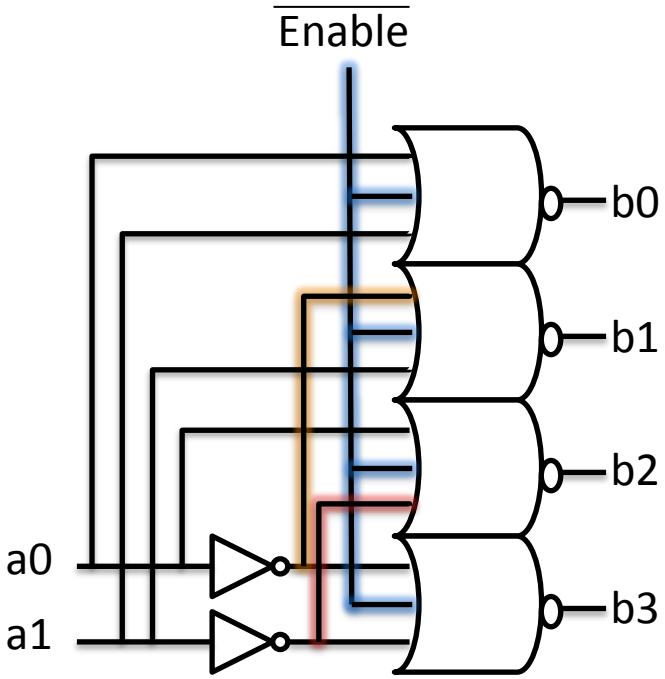

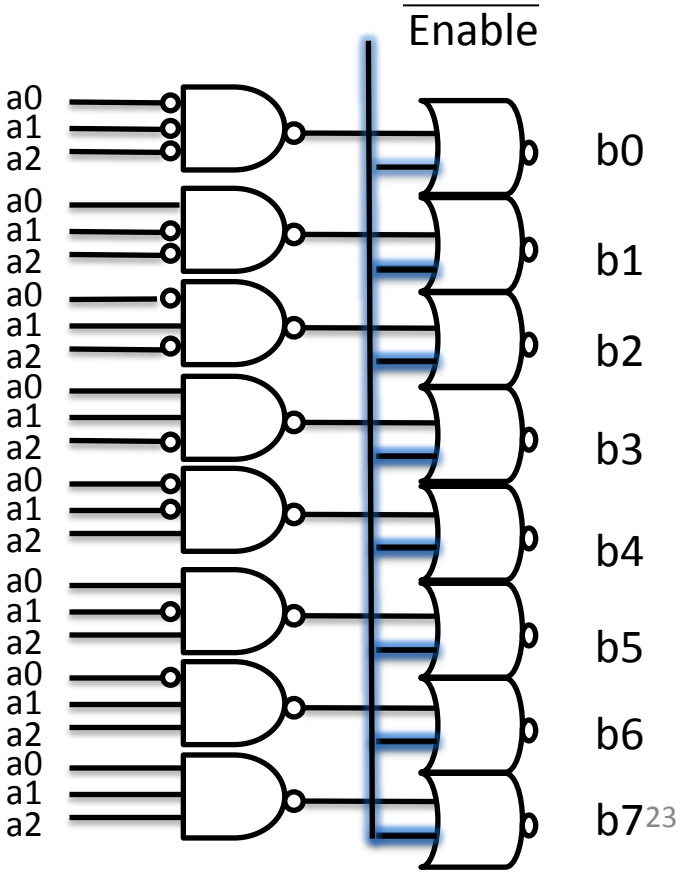

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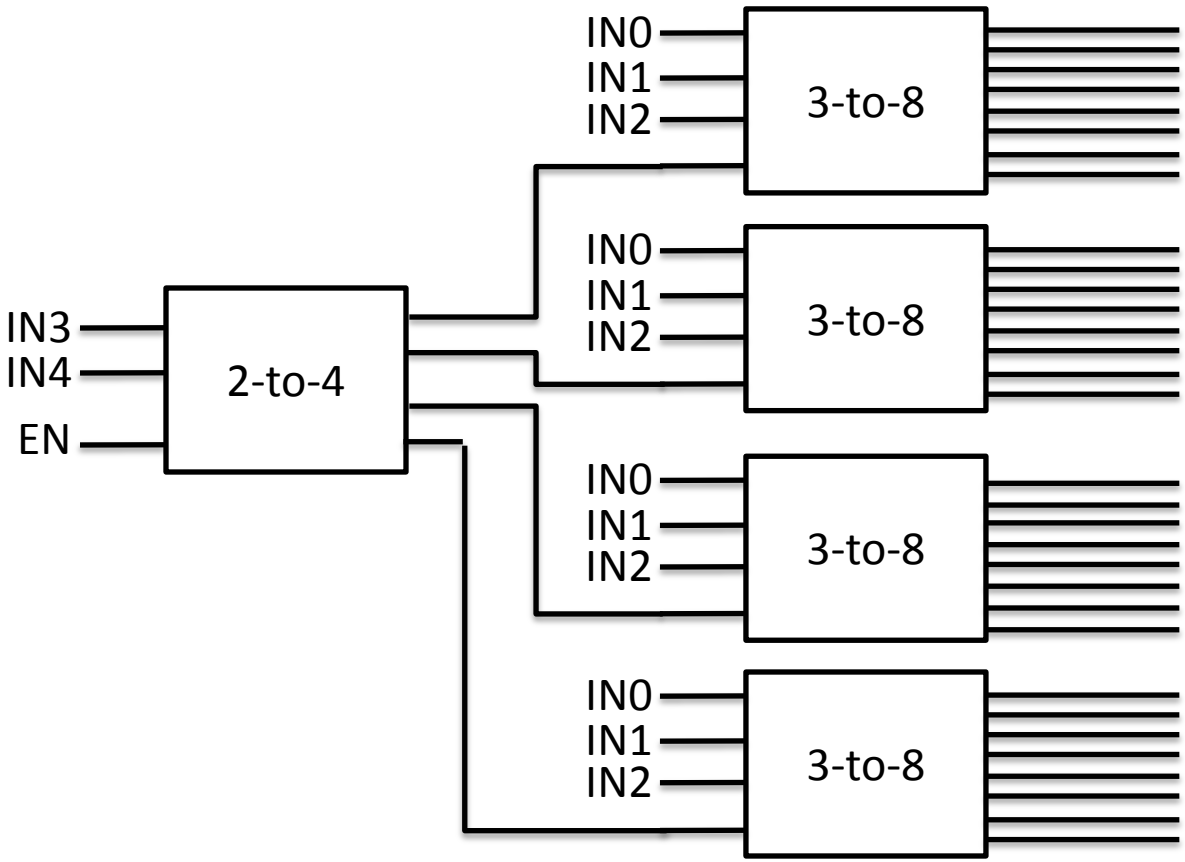

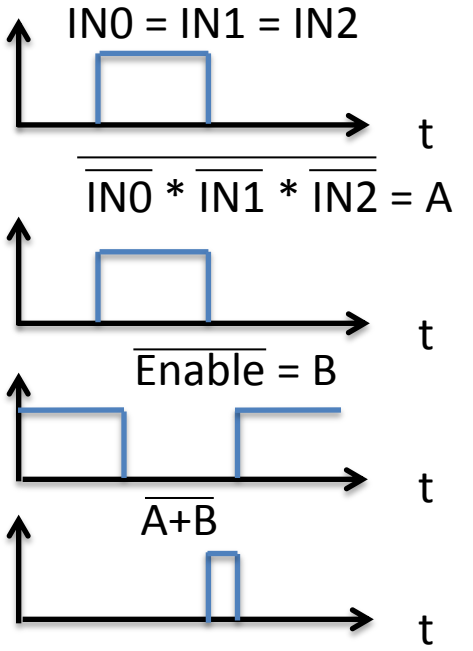

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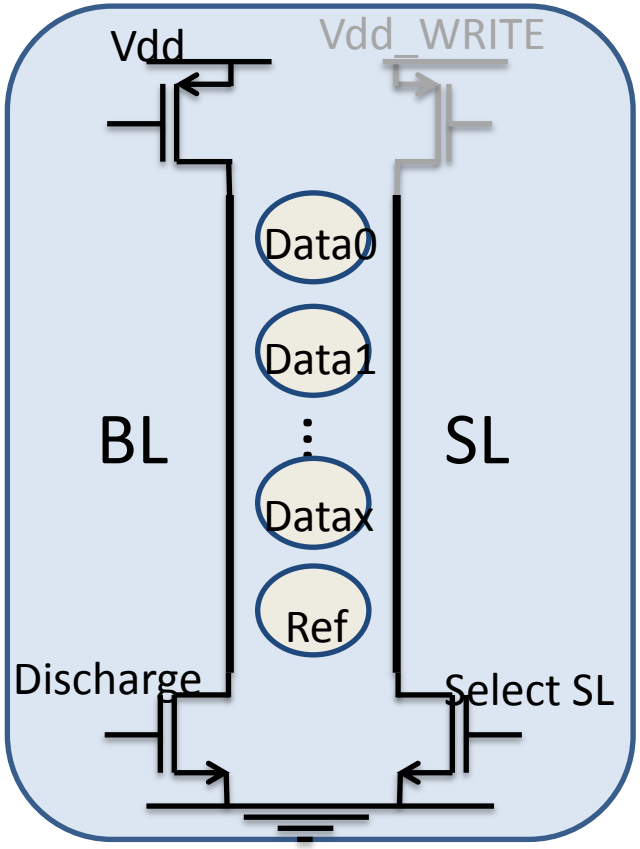

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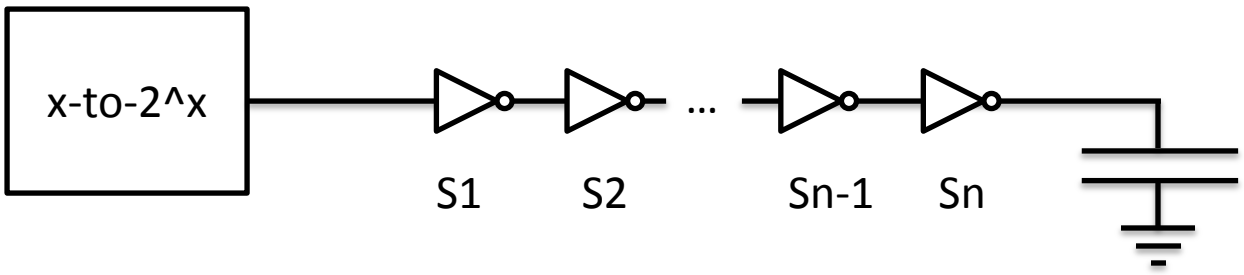
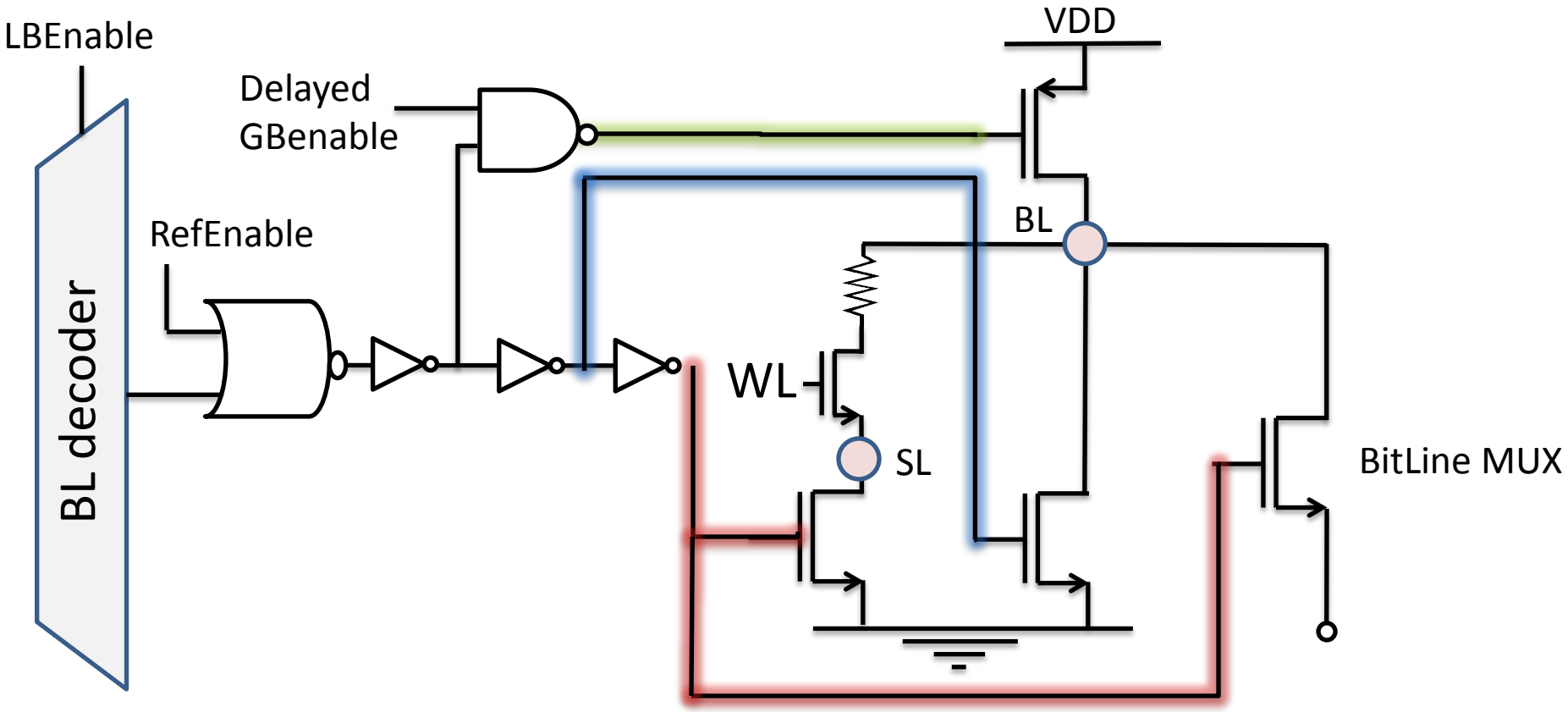


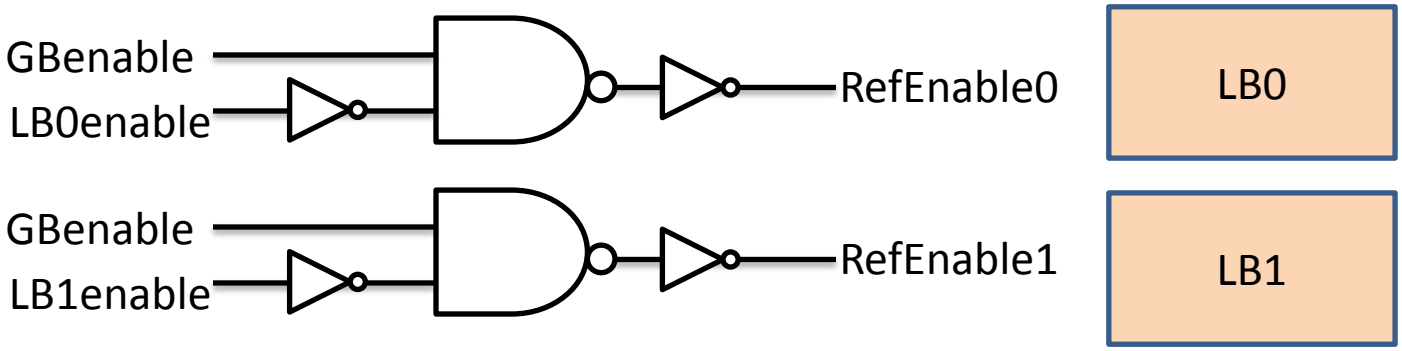
Timing

- Invertors as delay elements
- Note: in case one Source Line Discharge per Local Block, Discharge gate connected to delayed LBEnable



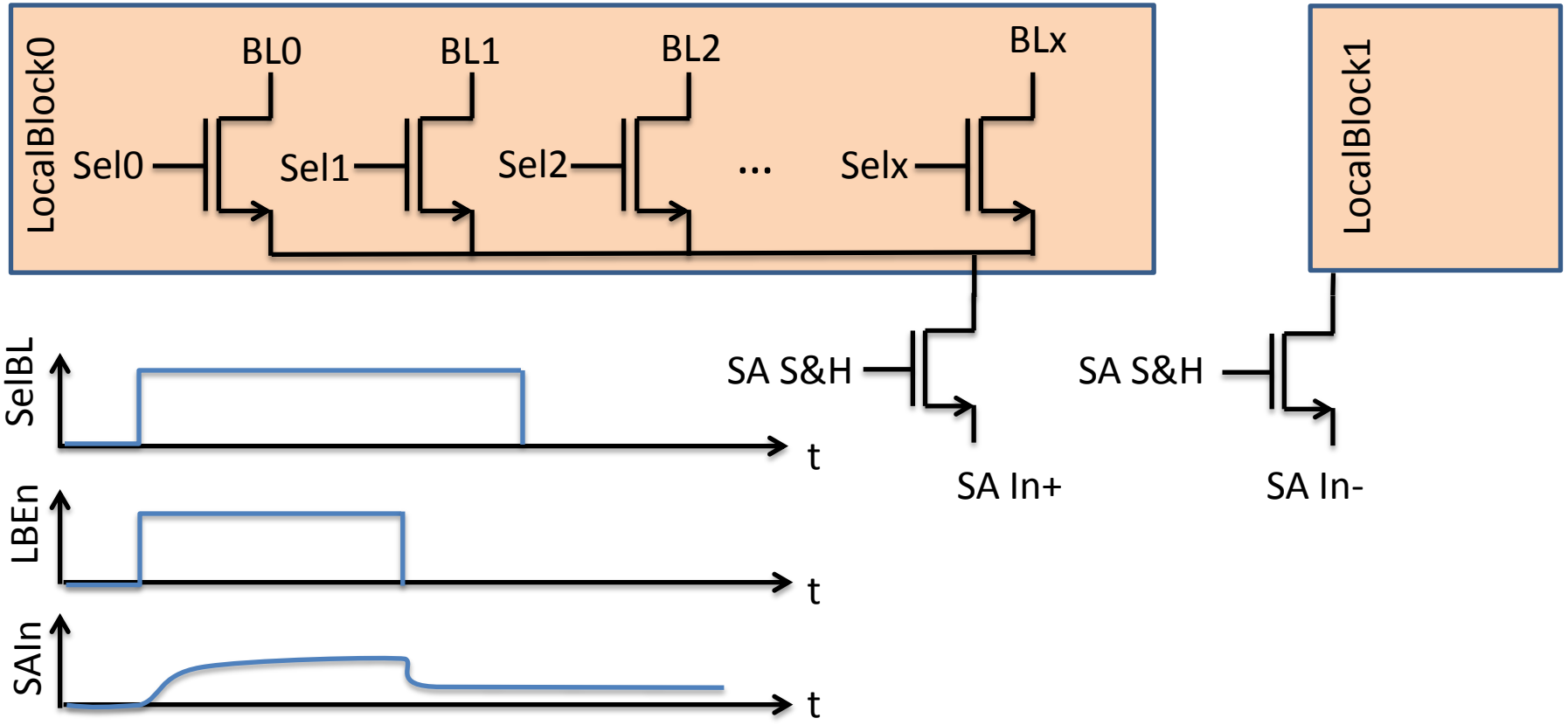
Timing

- RefEnable: AND-gated Gbenable + $\overline{\text{Lbenable}}$
- Delayed Gbenable: inverter chain
- RefEnable connected to RefWL



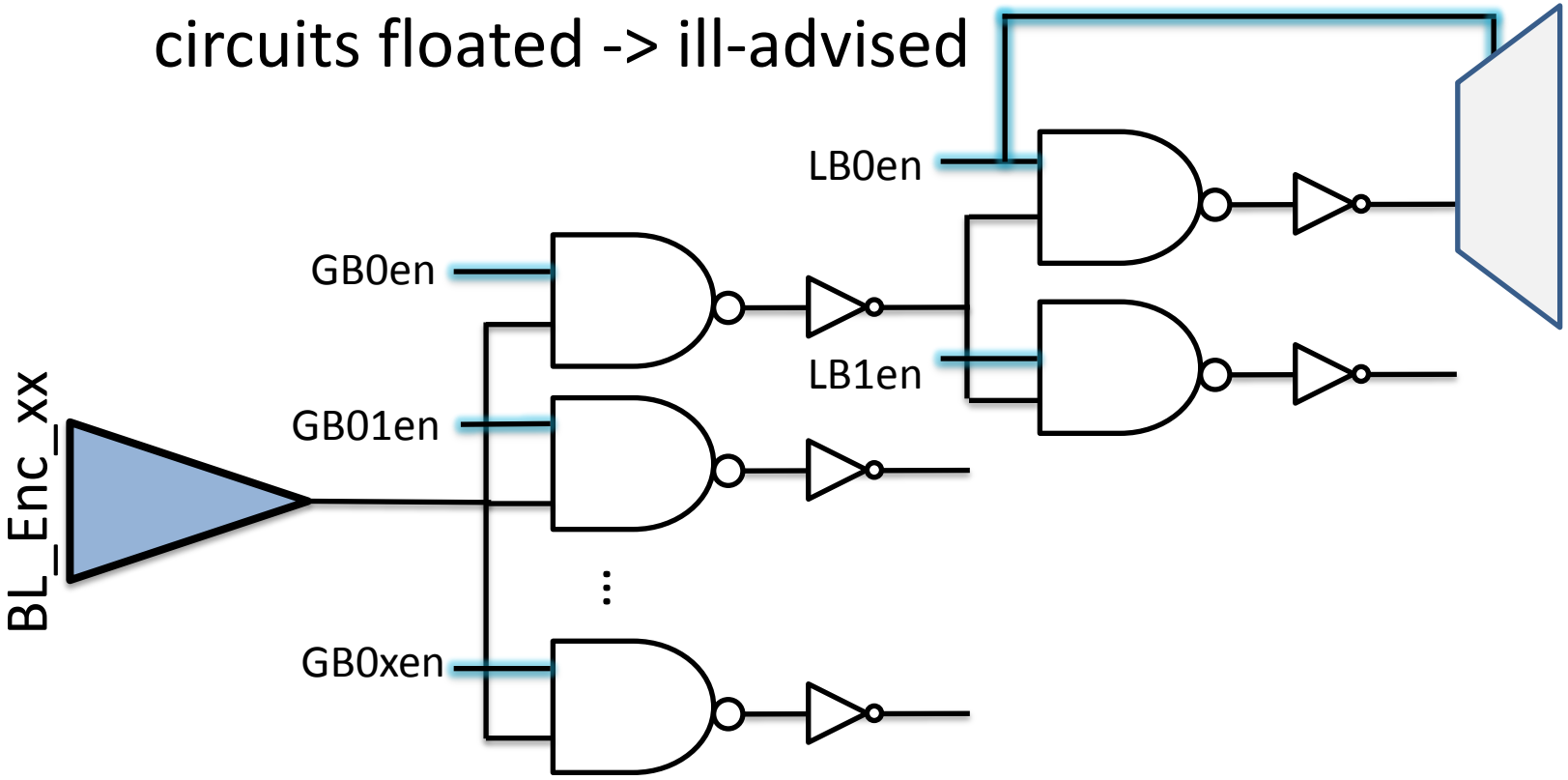
Passgates

- Just n-MOS (justified as long as Vsignal < 1V – Vt)
- Low Vt!
- Timing so only one charge injection occurs



Line Drivers

- AND-gates
- Passgates would leave nodes connected to digital circuits floated -> ill-advised



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