LECTURE 140 – THE MOS SWITCH AND MOS DIODE

LECTURE ORGANIZATION

Outline

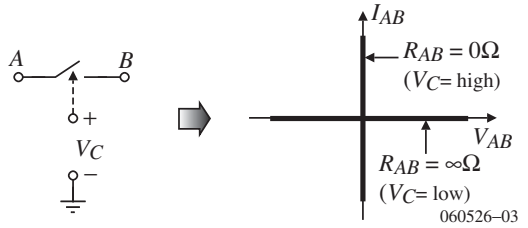
- MOSFET as a switch
- Influence of the switch resistance
- Influence of the switch capacitors
  - Channel injection
  - Clock feedthrough
- Using switches at reduced values of V_{DD}
- MOS Diode
- Summary

***CMOS Analog Circuit Design*, 2nd Edition Reference**

Pages 113-124

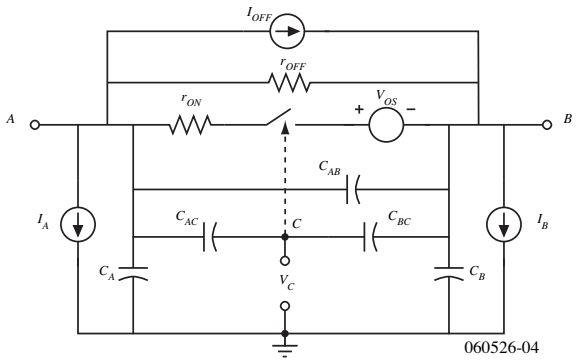
Switch Model

- An ideal switch is a short-circuit when ON and an open-circuit when OFF. V_C = controlling terminal for the switch (V_C high ⇒ switch ON, V_C low ⇒ switch OFF)

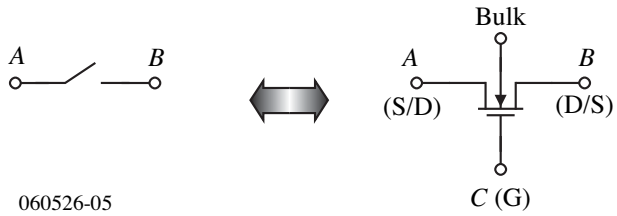


- Actual switch:

r_{on} = resistance of the switch when ON
r_{off} = resistance of the switch when OFF
V_{OS} = offset voltage when the switch is ON
I_{off} = offset current when the switch is OFF
I_A and I_B are leakage currents to ground
C_A and C_B are capacitances to ground
C_{AC} and C_{BC} = parasitic capacitors between the control terminal and switch terminals



MOS Transistor as a Switch



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On Characteristics of a MOS Switch

Assume operation in active region ($v_{DS} < v_{GS} - V_T$) and v_{DS} small.

$$i_D = \frac{\mu C_{ox} W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS} \approx \frac{\mu C_{ox} W}{L}(v_{GS} - V_T)v_{DS}$$

Thus,

$$\boxed{R_{ON} \approx \frac{v_{DS}}{i_D} = \frac{1}{\frac{\mu C_{ox} W}{L}(v_{GS} - V_T)}}$$

OFF Characteristics of a MOS Switch

If $v_{GS} < V_T$, then $i_D = I_{OFF} = 0$ when $v_{DS} \approx 0\text{V}$.

If $v_{DS} > 0$, then

$$\boxed{R_{OFF} \approx \frac{1}{i_D \lambda} = \frac{1}{I_{OFF}\lambda} \approx \infty}$$

MOS Switch Voltage Ranges

If a MOS switch is used to connect two circuits that can have analog signal that vary from 0 to 1V, what must be the value of the bulk and gate voltages for the switch to work properly?

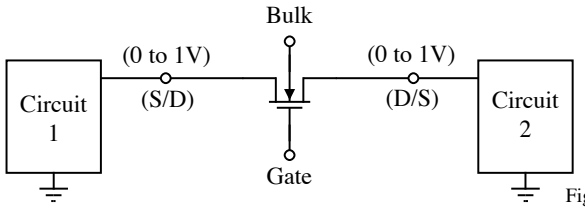


Fig.4.1-3

- To insure that the bulk-source and bulk-drain *pn* junctions are reverse biased, the bulk voltage must be less than the minimum analog signal for a NMOS switch.
- To insure that the switch is on, the gate voltage must be greater than the maximum analog signal plus the threshold for a NMOS switch.

Therefore:

$$V_{Bulk} \leq 0\text{V}$$
$$V_{Gate}(\text{on}) > 1\text{V} + V_T$$
$$V_{Gate}(\text{off}) \leq 0\text{V}$$

Unfortunately, the large value of reverse bias bulk voltage causes the threshold voltage to increase.

Current-Voltage Characteristics of a NMOS Switch

The following simulated output characteristics correspond to triode operation of the MOSFET.

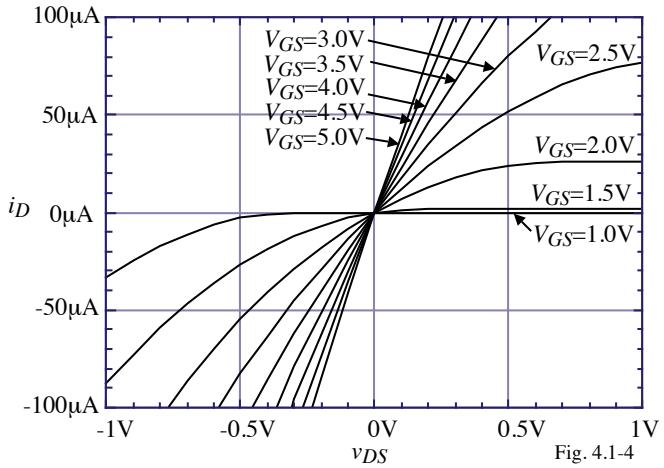


Fig. 4.1-4

SPICE Input File:

```
MOS Switch On Characteristics
M1 1 2 0 3 MNMOS W=1U L=1U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4 PHI=0.7
VDS 1 0 DC 0.0
VGS 2 0 DC 0.0
VBS 3 0 DC -5.0
.DC VDS -1 1 0.1 VGS 1 5 0.5
.PRINT DC ID(M1)
.PROBE
.END
```


MOS Switch ON Resistance as a Function of Gate-Source Voltage

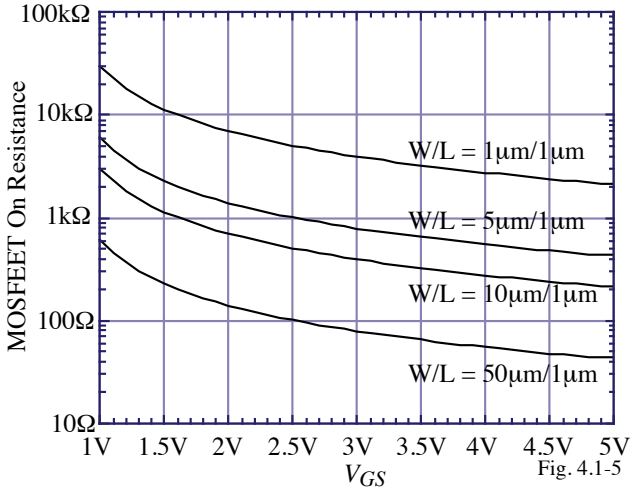


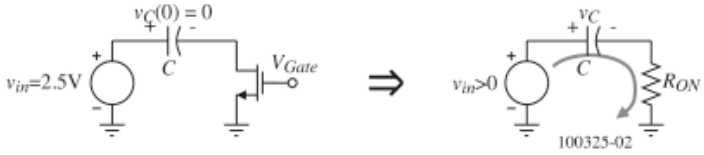
Fig. 4.1-5

SPICE Input File:

```
MOS Switch On Resistance as a f(W/L)
M1 1 2 0 0 MNMOS W=1U L=1U
M2 1 2 0 0 MNMOS W=5U L=1U
M3 1 2 0 0 MNMOS W=10U L=1U
M4 1 2 0 0 MNMOS W=50U L=1U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4, PHI=0.7
VDS 1 0 DC 0.001V
VGS 2 0 DC 0.0
.DC VGS 1 5 0.1
.PRINT DC ID(M1) ID(M2) ID(M3) ID(M4)
.PROBE
.END
```

Influence of the ON Resistance on MOS Switches

Finite ON Resistance:



Example

Initially assume the capacitor is uncharged. If V_{Gate}(ON) is 5V and is high for 0.1μs, find the W/L of the MOSFET switch that will charge a capacitance of 10pF in five time constants.

Solution

The time constant must be 100ns/5 = 20ns. Therefore R_{ON} must be less than 20ns/10pF = 2kΩ. The ON resistance of the MOSFET (for small v_{DS}) is

$$R_{ON} = \frac{1}{K_N'(W/L)(V_{GS}-V_T)} \Rightarrow \frac{W}{L} = \frac{1}{R_{ON} \cdot K_N'(V_{GS}-V_T)} = \frac{1}{2\text{k}\Omega \cdot 110\mu\text{A/V}^2 \cdot 4.3}$$

$$= 1.06$$

Comments:

- It is relatively easy to charge on-chip capacitors with minimum size switches.
- Switch resistance is really not constant during switching and the problem is more complex than above.

Including the Influence of the Varying On Resistance

Gate-source Constant

$$g_{ON}(t) = \frac{K'W}{L}[(v_{GS}(t)-V_T) - 0.5v_{DS}(t)]$$

$$g_{ON}(\text{aver.}) = \frac{1}{r_{ON}(\text{aver.})} \approx \frac{g_{ON}(0) + g_{ON}(\infty)}{2}$$

$$= \frac{K'W}{2L}(V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L} + \frac{K'W}{2L}(V_{GS}-V_T)$$

$$= \frac{K'W}{L}(V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L}$$

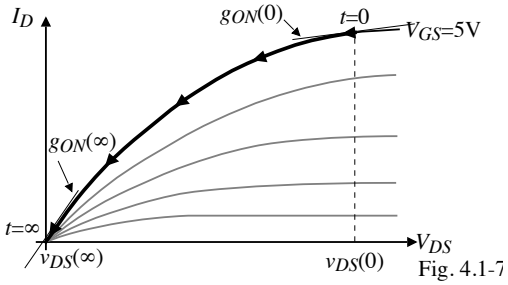


Fig. 4.1-7

Gate-source Varying

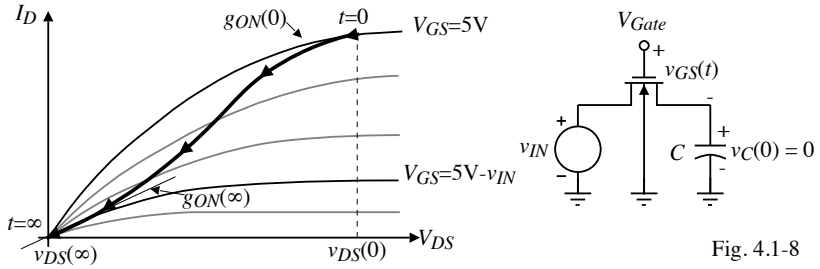


Fig. 4.1-8

$$g_{ON} = \frac{K'W}{2L}[V_{GS}(0)-V_T] - \frac{K'WV_{DS}(0)}{4L} + \frac{K'W}{2L}[V_{GS}(\infty)-v_{IN}-V_T]$$

Example 1 - Switch ON Resistance

Assume that at $t = 0$, the gate of the switch shown is taken to 5V. Design the W/L value of the switch to discharge the C_1 capacitor to within 1% of its initial charge in 10ns. Use the MOSFET parameters of Table 3.1-2.

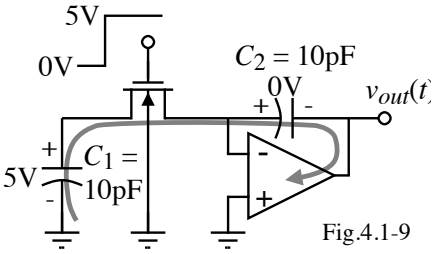


Fig.4.1-9

Solution

Note that the source of the NMOS is on the right and is always at ground potential so there is no bulk effect as long as the voltage across C_1 is positive. The voltage across C_1 can be expressed as

$$v_{C1}(t) = 5\exp\left(\frac{-t}{R_{ON}C_1}\right)$$

At 10ns, v_{C1} is 5/100 or 0.05V. Therefore,

$$0.05=5\exp\left(\frac{-10^{-8}}{R_{ON}10^{-11}}\right) = 5\exp\left(\frac{-10^{3}}{R_{ON}}\right) \Rightarrow \exp(G_{ON}10^{3})=100 \Rightarrow G_{ON} = \frac{ln(100)}{10^{3}}$$

$$=0.0046\text{S}$$

$$\therefore\ 0.0046 = \frac{K'W}{L}(V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L} = \left(110\text{x}10^{-6}\cdot 4.3-\frac{110\text{x}10^{-6}\cdot 5}{4}\right)\frac{W}{L} = 356\text{x}10^{-6}\frac{W}{L}$$

$$\text{Thus, } \frac{W}{L} = \frac{0.0046}{356\text{x}10^{-6}} = 13.71 \approx 14$$

Influence of the OFF State on MOS Switches

The OFF state influence is primarily in any current that flows from the terminals of the switch to ground.

An example might be:

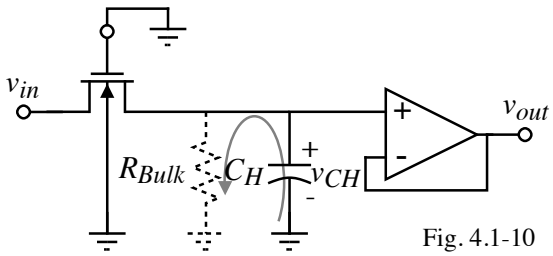


Fig. 4.1-10

Typically, no problems occur unless capacitance voltages are held for a long time. For example,

$$v_{out}(t) = v_{CH}\, e^{-t/(R_{Bulk}C_H)}$$

If $R_{Bulk} \approx 10^9\Omega$ and C_H = 10pF, the time constant is $10^9\cdot 10^{-11} = 0.01$seconds

Influence of Parasitic Capacitances

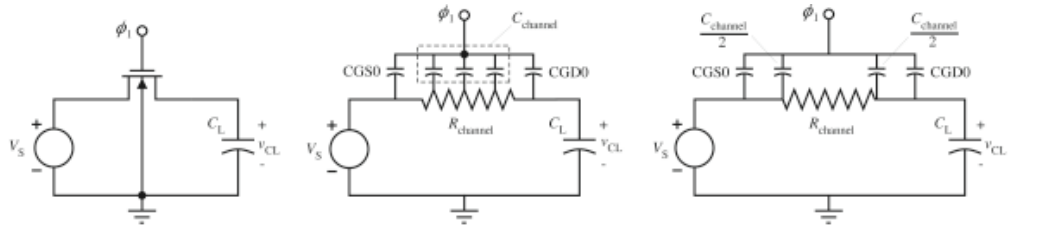
The parasitic capacitors have two influences:

- Parasitics to ground at the switch terminals (C_{BD} and C_{BS}) add to the value of the desired capacitors.

  This problem is solved by the use of stray-insensitive switched capacitor circuits
- Parasitics from gate to source and drain cause *charge injection* and *clock feedthrough* onto or off the desired capacitors.

  This problem can be minimized but not eliminated.

Model for studying gate capacitance:



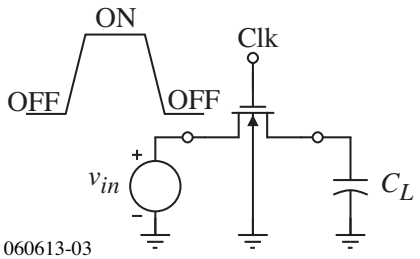
A simple switch circuit useful for studying charge injection.

A distributed model of the transistor switch.

A lumped model of the transistor switch. 100325-03

Channel Charge Injection

Consider the simple switch configuration shown:



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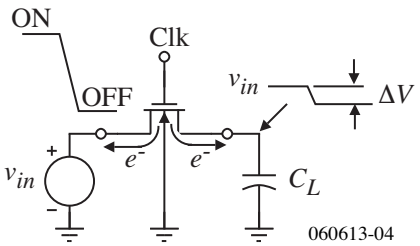
When the switch is ON, a charge is stored in the channel which is equal to,

$$Q_{ch} = -WLC_{ox}(V_H - v_{in} - V_T)$$

where V_H is the value of the clock waveform when the switch is on ($V_H \approx V_{DD}$)

When the switch turns OFF, this charge is injected into the source and drain terminals as shown.



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Assuming the charge splits evenly, then the change of voltage across the capacitor, C_L, is

$$\Delta V = \frac{Q_{ch}}{2C_L} = \frac{-WLC_{ox}(V_H - v_{in} - V_T)}{2C_L}$$

The charge injection does not influence v_{in} because it is a voltage source.

Clock Feedthrough

In addition to the charge injection, the overlap capacitors of the MOSFET couple the turning off part of the clock to the load capacitor. This is called *clock feedthrough*.

The model for this case is given as:

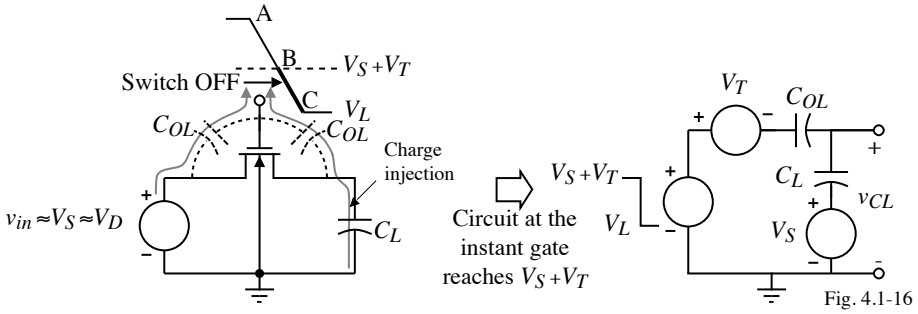


Fig. 4.1-16

The gate decrease from B to C is modeled as a negative step of magnitude $V_S + V_T - V_L$. The output voltage on the capacitor after opening the switch is,

$$v_{CL} = \left(\frac{C_L}{C_{OL}+C_L}\right)V_S - \left(\frac{C_{OL}}{C_{OL}+C_L}\right)V_T - (V_S+V_T-V_L)\left(\frac{C_{OL}}{C_{OL}+C_L}\right) \approx V_S - (V_S+2V_T-V_L)\left(\frac{C_{OL}}{C_L}\right)$$

if $C_{OL} < C_L$.

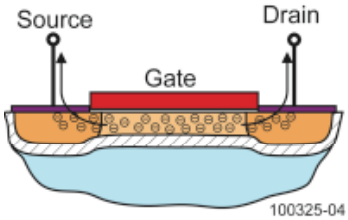
Therefore the error voltage is,

$$V_{error} \approx -(V_S + 2V_T - V_L)\left(\frac{C_{OL}}{C_L}\right) = -(v_{in} + 2V_T - V_L)\left(\frac{C_{OL}}{C_L}\right)$$

Modeling the Influence of Charge Injection and Clock Feedthrough

The influence of change injection and clock feedthrough on a switch is a complex analysis which is better suited for computer analysis. Here we will attempt to develop an understanding sufficient to show ways of reducing these effects.

To begin the model development, there are two cases of charge injection depending upon the transition rate when the switch turns off.



1.) Slow transition time – the charge in the channel can react instantaneously to changes in the turning-off, gate-source voltage.

2.) Fast transition time – the charge in the channel cannot react fast enough to respond to the changes in the turning-off, gate-source voltage.

Slow Transition Time

Consider the following switch circuit:

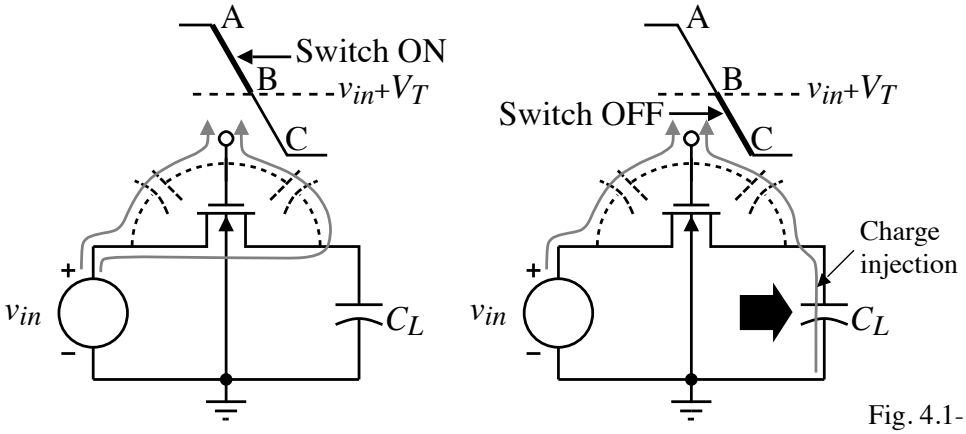


Fig. 4.1-13

1.) During the on-to-off transition time from A to B, the charge injection is absorbed by the low impedance source, v_{in}.

2.) The switch turns off when the gate voltage is $v_{in}+V_T$ (point B).

3.) From B to C the switch is off but the gate voltage is changing. As a result charge injection occurs to C_L.

Fast Transition Time

For the fast transition time, the rate of transition is faster than the channel time constant so that some of the charge during the region from point A to point B is injected onto C_L even though the transistor switch has not yet turned off.

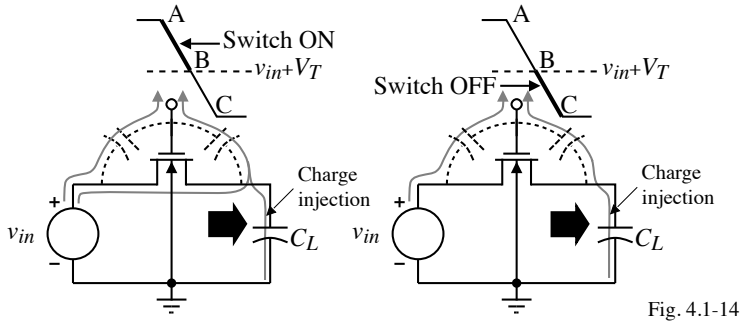


Fig. 4.1-14

A Quantized Model of Charge Injection/Clock Feedthrough†

Approximate the gate transition as a staircase and discretized in voltage as follows:

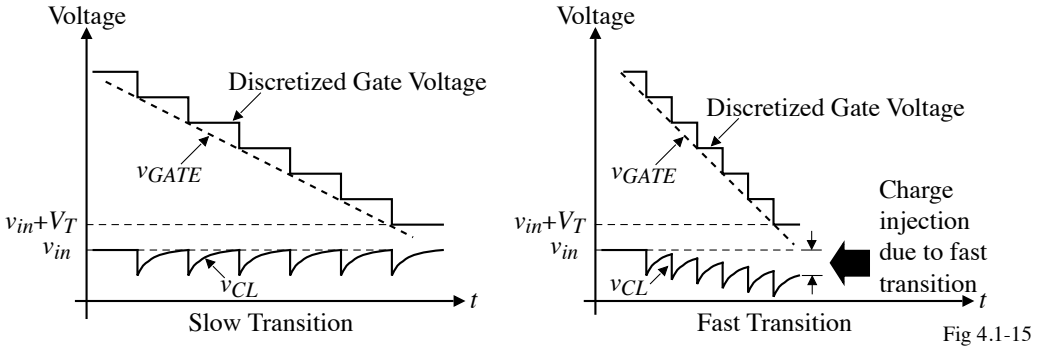


Fig 4.1-15

The time constant of the channel, $R_{channel} \cdot C_{channel}$, determines whether or not the capacitance, C_L, fully charges during each voltage step.

† B.J. Sheu and C. Hu, "Switched-Induced Error Voltage on A Switched Capacitor," *IEEE J. Solid-State Circuits*, Vol. SC-19, No. 4, pp. 519-525, August 1984.

Analytical Expressions to Approximate Charge Injection/Clock Feedthrough

Assume the gate voltage is making a transition from high, V_H, to low, V_L.

$\therefore \quad v_{Gate} = v_G(t) = V_H - Ut$ where U = magnitude of the slope of $v_G(t)$

Define $V_{HT} = V_H - V_S - V_T$ and $\beta = \dfrac{K'W}{L}$.

The error in voltage across C_L, V_{error}, is given below in two terms. The first term corresponds to the feedthrough that occurs while the switch is still on and the second term corresponds to feedthrough when the switch is off.

1.) Slow transition occurs when $\dfrac{\beta V_{HT}^2}{2C_L} >> U$.

$$V_{error} = -\left(\frac{W \cdot CGD0 + \frac{C_{channel}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} - \frac{W \cdot CGD0}{C_L}(V_S + 2V_T - V_L)$$

2.) Fast transition occurs when $\dfrac{\beta V_{HT}^2}{2C_L} << U$.

$$V_{error} = -\left(\frac{W \cdot CGD0 + \frac{C_{channel}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta V_{HT}^3}{6U \cdot C_L}\right) - \frac{W \cdot CGD0}{C_L}(V_S + 2V_T - V_L)$$

Example 2 - Calculation of Charge Feedthrough Error

Calculate the effect of charge feedthrough on the previous circuit where $V_S = 1\text{V}$, $C_L = 1\text{pfF}$, $W/L = 0.8\mu\text{m}/0.8\mu\text{m}$, and V_G is given below for the two cases. Use model parameters from Tables 3.1-2 and 3.2-1. Neglect ΔL and ΔW effects.

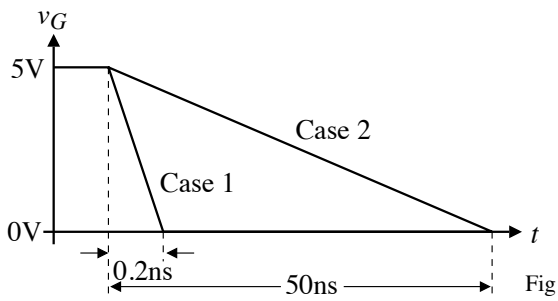


Fig. 4.1-17

Solution

Case 1:

The value of U is equal to 5V/0.2nS or $25\text{x}10^9$. Next we must test to see if the slow or fast transition time is appropriate. First calculate the value of V_T as

$$V_T = V_{T0} + \gamma\sqrt{2|\phi_F| - V_{BS}} - \gamma\sqrt{2|\phi_F|} = 0.7 + 0.4\sqrt{0.7+1} - 0.4\sqrt{0.7} = 0.887\text{V}$$

Therefore,

$$V_{HT} = V_H - V_S - V_T = 5\text{-}1\text{-}0.887 = 3.113\text{V} \Rightarrow \frac{\beta V_{HT}^2}{2C_L} = \frac{110\text{x}10^{-6}\cdot 3.113^2}{2\cdot 1\text{pF}} = 5.32\text{x}10^8 < 25\text{x}10^9$$

which corresponds to the fast transition case. Using the previous expression gives,

$$V_{error} = -\left(\frac{176\text{x}10^{-18}+0.5(1.58\text{x}10^{-15})}{1\text{x}10^{-12}}\right)\left(3.113-\frac{3.32\text{x}10^{-3}}{30\text{x}10^{-3}}\right) - \frac{176\text{x}10^{-18}}{1\text{x}10^{-12}}(1+1.774-0) = -3.39\text{mV}$$

Example 2 - Continued

Case 2:

In this case U is equal to 5V/50ns or $1\text{x}10^8$ which means that the slow transition case is valid ($1\text{x}10^8 < 5.32\text{x}10^8$).

Using the previous expression gives,

$$V_{error} = -\left(\frac{176\text{x}10^{-18}+0.5(1.58\text{x}10^{-15})}{1\text{x}10^{-12}}\right)\left(\sqrt{\frac{314\text{x}10^{-6}}{220\text{x}10^{-6}}}\right) - \frac{176\text{x}10^{-18}}{1\text{x}10^{-12}}(1+1.774-0)$$

$$= -1.64\text{mV}$$

Comment:

These results are not expected to give precise answers regarding the amount of charge feedthrough one should expect in an actual circuit. Rather, they are a guide to understand the effects of various circuit elements and terminal conditions in order to minimize unwanted behavior by design techniques.

Solutions to Charge Injection

1.) Use minimum size switches to reduce the overlap capacitances and/or increase C_L.

2.) Use a dummy compensating transistor.

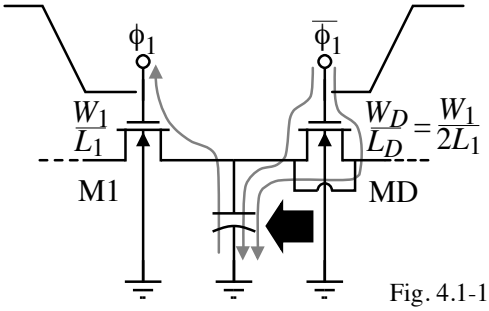


Fig. 4.1-19

- Requires complementary clocks
- Complete cancellation is difficult and may in fact may make the feedthrough worse

3.) Use complementary switches (transmission gates)

4.) Use differential implementation of switched capacitor circuits (probably the best solution)

Input-Dependent Charge Injection

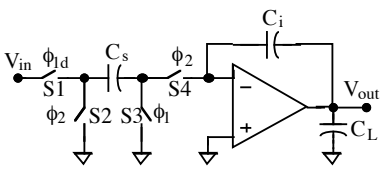
Examination of the error voltage reveals that,

Error voltage = Component independent of input + Component dependent on input

This only occurs for switches that are floating and is due to the fact that the input influences the voltage at which the transistor switches ($v_{in} \approx V_S \approx V_D$). Leads to spurious responses and other undesired results.

Solution:

Use delayed clocks to remove the input-dependence by removing the path for injection from the floating switches.



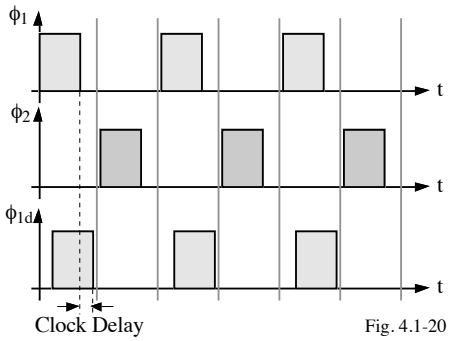


Fig. 4.1-20

Assume that C_s is charged to V_{in} (both ϕ_1 and ϕ_{1d} are high):

1.) ϕ_1 opens, no input-dependent feedthrough because switch terminals (S3) are at ground potential.

2.) ϕ_{1d} opens, no feedthrough occurs because there is no current path (except through small parasitic capacitors).

CMOS Switches (Transmission Gate)

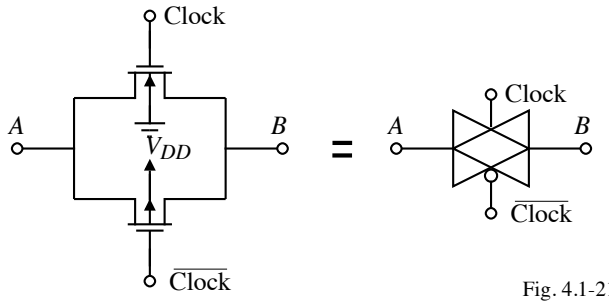


Fig. 4.1-21

Advantages:

- Feedthrough somewhat diminished
- Larger dynamic range
- Lower ON resistance

Disadvantages:

- Requires a complementary clock
- Requires more area

Example 3 - Charge Injection for a CMOS Switch

Calculate the effect of charge feedthrough on the circuit shown below. Assume that U = 5V/50ns = 10^8V/s, v_{in} = 2.5V and ignore the bulk effect. Use the model parameters from Tables 3.1-2 and 3.2-1.

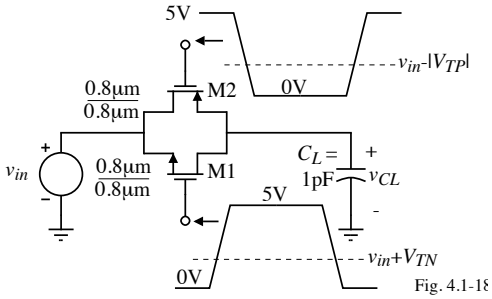


Fig. 4.1-18

Solution

First we must identify the transition behavior. For the NMOS transistor we have

$$\frac{\beta_N V_{HTN}^2}{2C_L} = \frac{110\text{x}10^{-6}\cdot(5\text{-}2.5\text{-}0.7)^2}{2\cdot 10^{-12}} = 1.78\text{x}10^8$$

For the PMOS transistor, noting that

$$V_{HTP} = V_S - |V_{TP}| - V_L = 2.5\text{-}0.7\text{-}0 = 1.8$$

we have $\frac{\beta_P V_{HTP}^2}{2C_L} = \frac{50\text{x}10^{-6}\cdot(1.8)^2}{2\cdot 10^{-12}} = 8.10\text{x}10^7$. Thus, the NMOS transistor is in the slow transition and the PMOS transistor is in the fast transition regimes.

Example 3 - Continued

Error due to NMOS (slow transition):

$$V_{error}(\text{NMOS}) = -\left(\frac{176\text{x}10^{-18}+0.5(1.58\text{x}10^{-15})}{10^{-12}}\right)\sqrt{\frac{\pi\cdot 10^{8}\cdot 10^{-12}}{2\cdot 110\text{x}10^{-6}}} - \frac{176\text{x}10^{-18}}{10^{-12}}(2.5+1.4-0)$$

$$= -1.840\text{mV}$$

Error due to PMOS (fast transition):

$$V_{error}(\text{PMOS}) = \left(\frac{176\text{x}10^{-18}+0.5(1.58\text{x}10^{-15})}{10^{-12}}\right)\left(1.8-\frac{50\text{x}10^{-6}(1.8)^3}{6\cdot 10^{8}\cdot 10^{-12}}\right)+\frac{176\text{x}10^{-18}}{10^{-12}}(5+1.4-2.5)$$

$$= 1.956\text{mV}$$

Net error voltage due to charge injection is 116μV. This will vary with V_S.

Dynamic Range of the CMOS Switch

The switch dynamic range is the range of voltages at the switch terminals ($V_A \approx V_B = V_{A,B}$) over which the ON resistance is small.

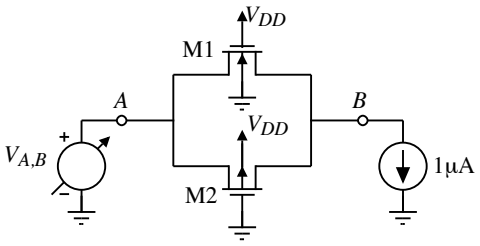


Fig. 4.1-22

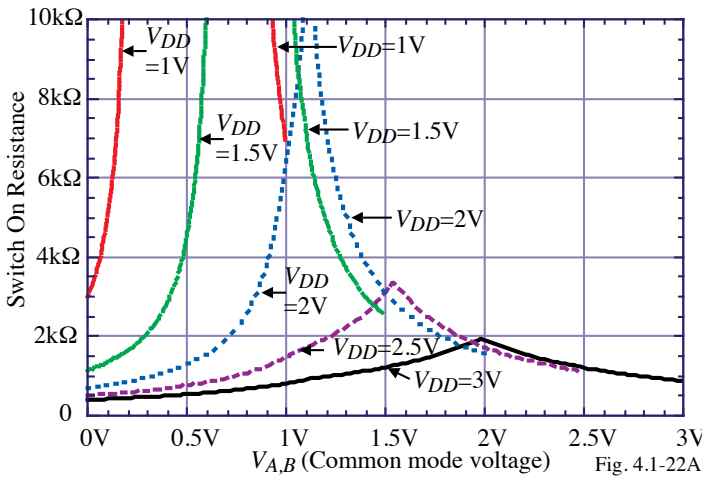


Fig. 4.1-22A

Spice File:

```
Simulation CMOS transmission switch resistance
M1 1 3 2 0 MNMOS L=1U W=10U
M2 1 0 2 3 MPMOS L=1U W=10U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4, PHI=0.7
.MODEL MPMOS PMOS VTO=-0.7, KP=50U,
+ LAMBDA=0.05, GAMMA=0.5, PHI=0.8
VDD 3 0
VAB 1 0
IA 2 0 DC 1U
.DC VAB 0 3 0.02 VDD 1 3 0.5
.PRINT DC V(1,2)
.END
```

Result:

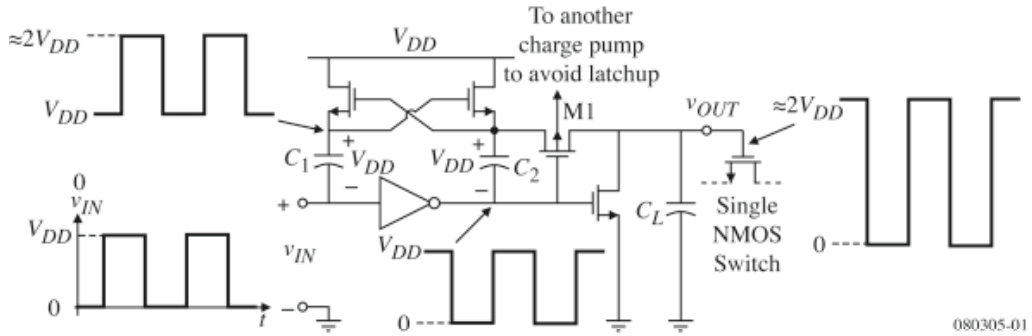
Low ON resistance over a wide voltage range is difficult as the power supply decreases.

Charge Pumps for Switches with Low Power Supply Voltages

As power supply voltages decrease below 2V, it becomes difficult to keep the switch on at a low value of on-resistance over the range of the power supply. The result is that r_{ON} becomes a function of the signal amplitude and produces harmonics.

Consequently, charge pumps are used to provide a gate voltage above power supply.

Principle of a charge pump:



$$v_{OUT} = 2V_{DD}\frac{C_2}{C_2 + C_L + C_{\text{NMOSswitch}}}$$

Simulation of the Charge Pump Circuit†

Circuit:

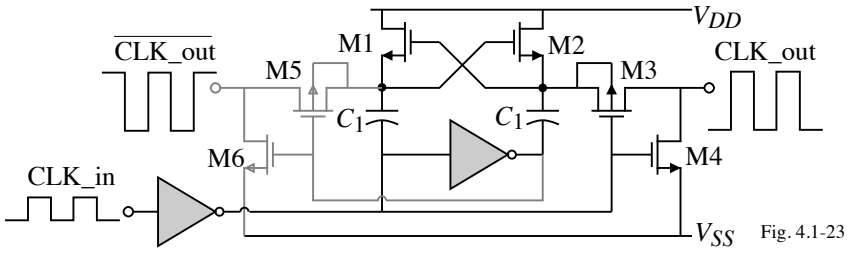


Fig. 4.1-23

Simulation:

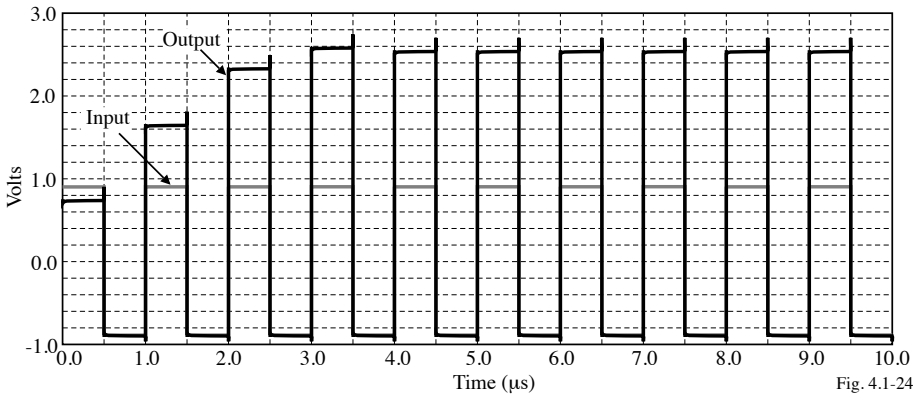


Fig. 4.1-24

† T.B. Cho and R.R. Gray, "A 10b, 20 Msample/s, 35mW Pipeline A/D Converter," *IEEE J. of Solid-State Circuits*, Vol. 30, No. 3m March 1995, pp. 166-172.

Bootstrapped Switches with High Reliability[†]

In the previous charge pump switch driver, the amount of gate-source drive depends upon the input signal and can easily cause reliability problems because it becomes too large for low values of input signal.

The solution to this problem is a bootstrapped switch as shown. →

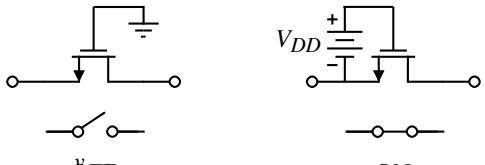
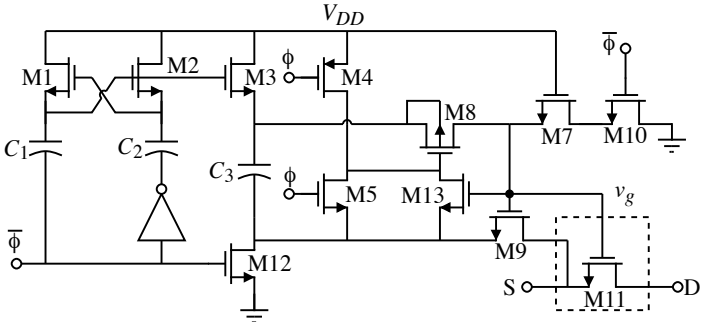


Fig. 4.1-25

Actual bootstrap switch:



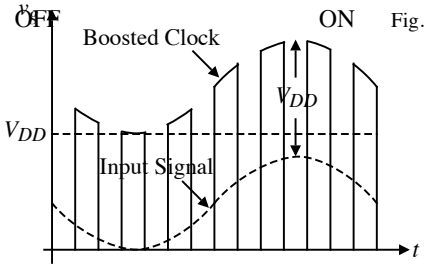


Fig. 4.1-26

ϕ low: M7 and M10 make v_g=0 and C_3 charges to V_{DD}, ϕ high: C_3 connected to v_{GS11}.

M7 reduces the v_{DS} and v_{GS} of M10 when $\phi = 0$. M13 ensures that $v_{GS8} \leq V_{DD}$.

The parasitics at the source of M11 require this node to be driven from a low impedance.

[†] A.M. Abo and P.R. Gray, "A 1.5V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter, *IEEE J. of Solid-State Circuits*, Vol. 34, No. 5, May 1999, pp. 599-605.

MOSFET DIODE

MOS Diode

When the MOSFET has the gate connected to the drain, it acts like a diode with characteristics similar to a pn-junction diode.

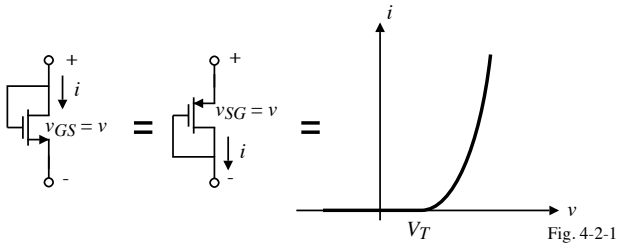


Fig. 4-2-1

Note that when the gate is connected to the drain of an enhancement MOSFET, the MOSFET is *always* in the saturation region.

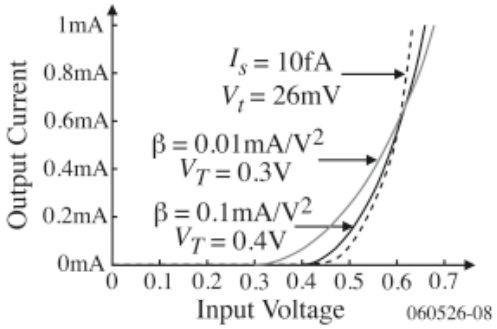
$$v_{DS} \geq v_{GS} - V_T \quad \Rightarrow \quad v_D - v_S \geq v_G - v_S - V_T \Rightarrow \quad v_D - v_G \geq -V_T \quad \Rightarrow \quad v_{DG} \geq -V_T$$

Since V_T is always greater than zero for an enhancement device, then $v_{DG} = 0$ satisfies the conditions for saturation.

- Works for NMOS or PMOS
- Note that the drain could be V_T less than the gate and still be in saturation

How Does the MOS Diode Compare with a *pn* Diode?

The comparison is basically the difference between an exponential and a square-law function. However, if the designer is willing to spend W/L, the comparison becomes more interesting as shown below.



If the threshold voltage is less than 0.4V, the MOS diode is a clear winner over the *pn* junction diode even for modest W/L ratios.

SUMMARY

- Symmetrical switching characteristics
- High OFF resistance
- Moderate ON resistance (OK for most applications)
- Clock feedthrough is proportional to size of switch (W) and inversely proportional to switching capacitors.
- Output offset due to clock feedthrough has 2 components:

  Input dependent

  Input independent
- Complementary switches help increase dynamic range.
- Fully differential operation should minimize the clock feedthrough.
- As power supply reduces, floating switches become more difficult to fully turn on.
- Switches contribute a kT/C noise which can get folded back into the baseband.
- The gate-drain connected MOSFET can make a good diode realization