Sub-10 µA reset in NiO-based resistive switching memory (RRAM) cells

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Abstract— **NiO-based resistive-switching memory (RRAM) is attracting a growing research interest for high-density non-volatile storage applications. One of the most difficult challenges for RRAM-based high-density memories is the high current necessary for the reset operation (I_{reset}), which limits the possibilities of scaling for the select diode in the cross-bar memory array. This work addresses the scalability of the reset current I_{reset} in NiO-based RRAM by limiting the set current through an integrated series MOSFET. I_{reset} is shown to be controllable down to below 10 µA. The consequences of these findings for the select diode in the cross-bar array structure are finally discussed.**

Keywords – Resistive switching memory (RRAM), transition metal oxide, crossbar architecture, nonvolatile memory.

I. INTRODUCTION

Resistive-switching memory (RRAM) is attracting a growing interest for scalable, 3D-stackable cross-bar memory arrays. RRAM operation mechanism is based on the resistance change in an active material, usually a transition metal oxide. The resistance is electrically and reversibly switched between a low and a high value, corresponding to the set and the reset states, respectively. Among the wide range of materials which have shown this peculiar ability, nickel oxide (NiO) has been selected as a potential active material for RRAM due to its unipolar and stable switching [2], compatible with high-density diode-selected cross-bar arrays. In NiO-based RRAM the resistance switching effect is due to the reversible formation and dissolution of a conductive filament (CF) through the active layer. This has been interpreted by redox chemical reactions driven by Joule heating and/or electric fields [1].

In the reset process, the CF is disrupted by thermally-activated oxidation, thus restoring the high resistance state. The reset current I_{reset} for CF dissolution is typically large, thus raising a potential issue for RRAM implementation in a cross-bar memory circuit. Indeed, the need for a high I_{reset} limits the dimension of the select-diode in the cross-bar array [3]. Therefore, reducing I_{reset} is mandatory for the development of a cross-bar structure. Due to the presence of a CF in the set state, I_{reset} does not scale with device area A: this is shown in Fig. 1, reporting the measured I_{reset} as a function of cell size. This can be explained by the Joule-heating induced reset transition, from which I_{reset} can be written as:

$$I_{reset} = \alpha(\Delta T_{crit})^{1/2}(RR_{th})^{-1/2}, \quad (1)$$

where ΔT_{crit} is the critical temperature increase for CF oxidation, α is a constant, R and R_{th} are the effective electrical and thermal resistances of the CF, respectively. Both R and R_{th} are inversely proportional to the area A_{CF} of the CF, thus from Eq. (1) we obtain $I_{reset} \propto A_{CF}$. This indicates that an effective way to reduce I_{reset} is by properly decreasing A_{CF}. This can be achieved reducing the available current during the CF formation (set operation). Indeed, experiments with 1 transistor – 1 resistor (1T1R) devices indicated that limiting the available drain current I_D during the set operation allowed for a relatively large resistance R of the set state and a subsequent reset current I_{reset} below 100 µA, both consistent with a reduction of A_{CF} [4,5].

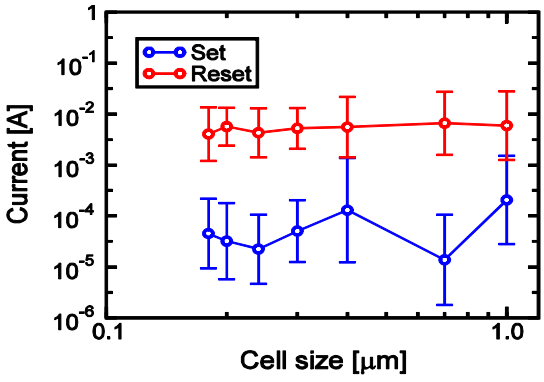

Figure 1. Measured set and reset current, I_{set} and I_{reset}, respectively, as a function of cell size.

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In this work, we show I_{reset} can be controlled down to below 10 µA, discussing the impact of such low reset currents on the scaling of diode-selected crossbar RRAMs.

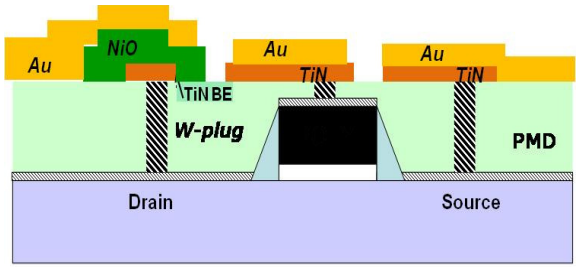

Figure 2. Schematic of the 1T-1R structure used in this work.

II. Experimental Samples and Characteristics

In order to study I_{reset} scalability, we fabricated 1T1R devices as schematically shown in Fig. 2. The n-MOSFET was made by a 130 nm process, with a channel length L = 1 µm, width W = 10 µm and a gate oxide thickness of 1.6 nm. The memory element, i.e. a NiO-based RRAM, was integrated on the drain and consisted of a stack of a 90 nm-width W-contact plug obtained by PVD and dry-etch patterning, a 30 nm-thick TiN bottom electrode with area 0.24 µm^2, an electron beam evaporated polycrystalline cubic NiO [6]. The NiO thickness was 35 nm, and NiO was capped by an Au top electrode obtained by lift-off technique.

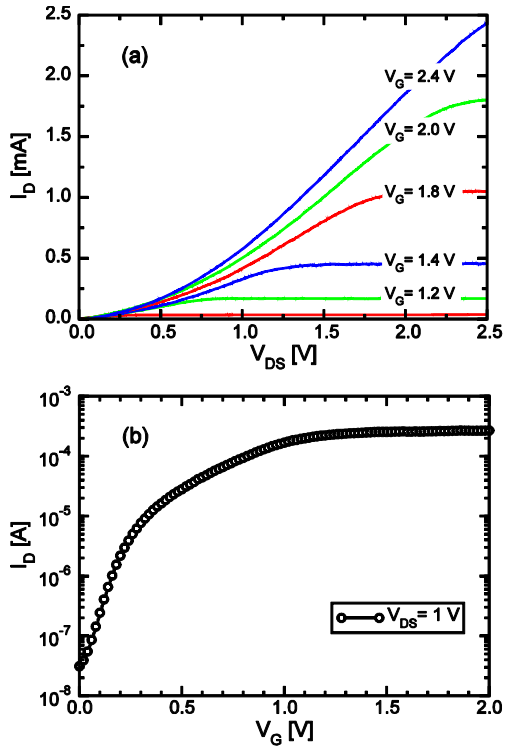

Figure 3. Measured characteristics of the select transistor, namely I_D-V_{DS} curves at various V_G (a) and measured saturated I_D-V_{GS} curve (b). I_D can be controlled over about 4 decades.

Fig. 3a shows the measured I_D of the integrated series MOSFET as a function of drain-source voltage V_{DS} for increasing gate voltage V_G, from 0 to 2.6 V. Fig. 3b shows the measured I_D-V_G curve for a fixed V_{DS} = 2.5 V. I_D displays a relatively large on-off swing from about 0.1 µA to about 300 µA, allowing for a good control of the current during the set operation.

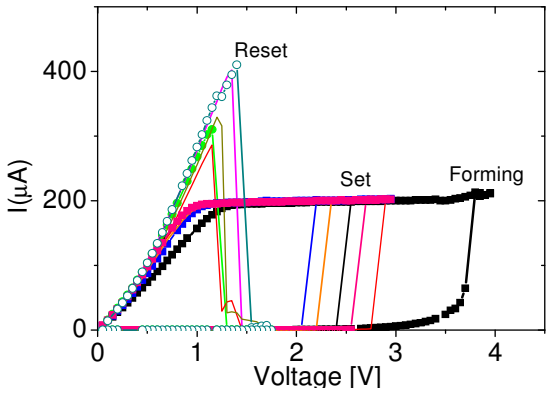

Figure 4. Forming/reset/set characteristics for 1T-1R devices. A low V_G is used during forming/set for minimum I_D and A_{CF}, while a high V_G is used during reset for minimum V_{reset}.

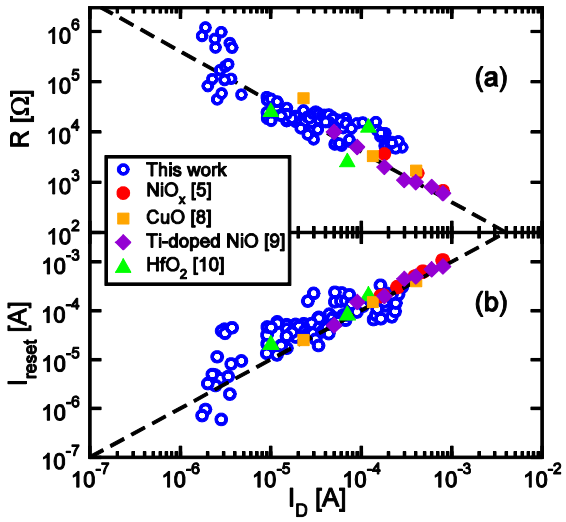

Figure 5. Measured R for the set state (a) and I_{reset} as a function of I_D. R decreases and I_{reset} increases for increasing I_D, as a result of the increasing A_{CF}. Reference data from [5, 8-10] are shown.

Fig. 4 shows the typical measured I-V characteristics of forming/reset/set operations for the 1T-1R samples. The MOSFET was biased to low V_G during forming and set operations in order to reduce the current through the oxide layer during set, thus to minimize the area of the CF. A high V_G was instead used for biasing the MOSFET during the reset operation, in order to enhance the available current for the CF dissolution and to minimize the cell voltage drop after reset. This allows to prevent an unwanted set, requiring a relatively large voltage, after the reset operation, which may result in cell programming instability.

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It has been demonstrated that the presence of a parasitic capacitance C_p in parallel to the RRAM cell may lead to a current overshoot during set operation [7]. To limit C_p, we adopted an integrated series MOSFET instead of a wire-bonded transistor. The consequently small C_p avoids unwanted parasitic current overshoots and allows an optimal control of the CF size [5]. This is demonstrated in Fig. 5a, where the measured R for the set state is shown as a function of I_D during the set operation. R decreases for increasing I_D, as a result of the increasing size of the CF. The figure also evidences a slope of about -1 on the log-log plot: This can be understood considering that R is inversely proportional to the CF area A_{CF}, which is proportional to the area A_{EF} of the electronic filament generated at threshold switching, in the first stage of the set process [7]. In turn, A_{EF} is proportional to the available current I_D during set operation, thus yielding to $R \propto A_{CF}^{-1} \propto I_D^{-1}$. The figures also clarifies that intermediate resistive values between set and reset states can be tuned by a properly I_D control: This is useful in view of possible multilevel programming of NiO RRAMs to allow for further cost scaling.

Fig. 5b shows the measured I_{reset} as a function of I_D. I_{reset} increases linearly with I_D during the set operation, as a result of $I_{reset} \propto A_{CF}$ in Eq. (1). Literature data for RRAM cells with other active metal oxides are shown for reference [5,8–10]. The comparison indicates almost universal R-I_D and I_{reset}-I_D characteristics for different active materials, namely NiO_x [5], CuO [8] Ti-doped NiO [9] and HfO_2 [10]. With respect to earlier reports, our data demonstrate the controllable scaling of I_{reset} to below 10 µA. The unprecedented small I_{reset} can be clearly seen in Fig. 6, showing the measured I-V curves for set states with variable resistance. In the figure, I_{reset} decreases for increasing set resistance (R_{set}). This trend is further shown in Fig. 7 for a wider range of resistive values. The figure compares the scatter plot of I_{reset} as a function of R_{set}, both taken from Fig. 5, with data obtained from 1R samples where the resistance was controlled by a change in the reset voltage [11]. The two sets of data show similar behaviors, although variable-set data cover smaller resistive values which are more significant in view of RRAM scaling.

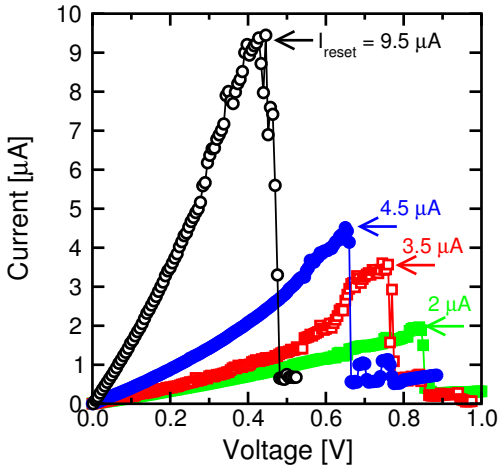

Figure 6. Measured I-V curves for set states with variable resistance, demonstrating sub-10 µA reset.

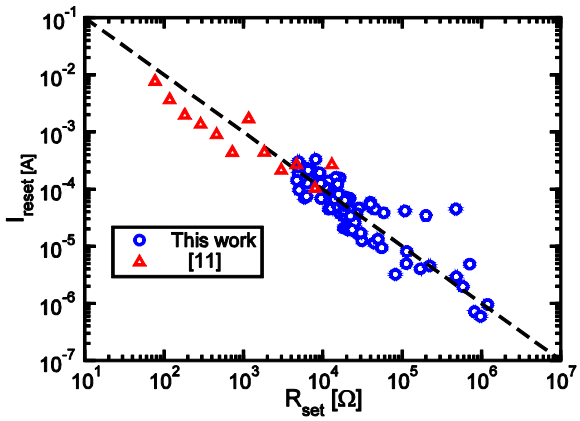

Figure 7. Scatter plot of I_{reset} as a function of R_{set} from Fig. 5, also including data for states obtained at variable reset voltage [11]. Note the consistency between the two set of data.

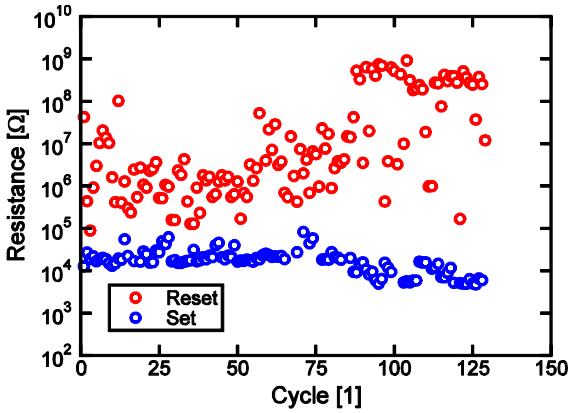

Figure 8. Measured set and reset R as a function of the number of cycles. Endurance is about 130 cycles, with good set/reset R window.

Fig. 8 shows the resistance of set and reset state as a function of the number of cycles. Endurance is about 130 cycles, with good set/reset R window. The marked change of reset-state resistance at about 80 cycles is probably due to an aging effect of the NiO layer, which however does not negatively affect the resistance window.

Fig. 9 shows a summary of currents and voltages for set and reset operations. I_{set} decreases and the set voltage increases for increasing R, in agreement with recent reports on NiO RRAMs [11]. This can be explained by the growth of the activation energy for conduction for increasing resistance. For large values of R, a change in behaviour is seen, where both I_{set} and the set voltage increase following the pre-forming I-V characteristics. This is due to the fact that the CF current becomes increasingly negligible with respect to the uniform current through the NiO layer, given by the pre-forming I-V curve (dashed line in the figure). On the other hand, both reset voltages and I_{reset} increase for decreasing R in the set state. This is attributed to series resistances due to the MOSFET and/or interconnects in our sample. Series resistances contribute an additional voltage drop at reset, causing relatively large reset voltages. The presence of this series resistance is also apparent

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in Fig. 8, where the reported set-state resistance is relatively higher as compared to usual values for similar devices [11].

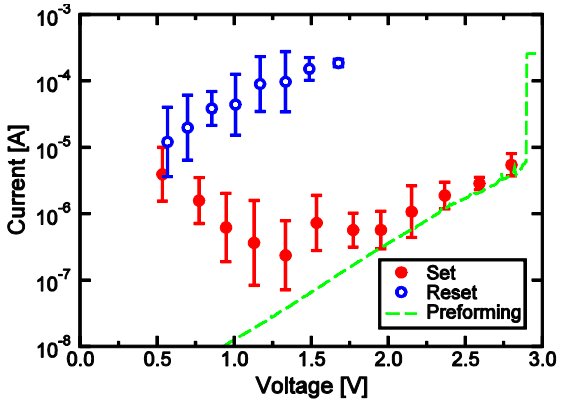

Figure 9. Scatter plot of currents and voltages for set (filled) and reset (open). I_{set} first decreases for increasing R, then increases as the CF current merges into the uniform NiO current (dashed curve). I_{reset} increases for increasing R.

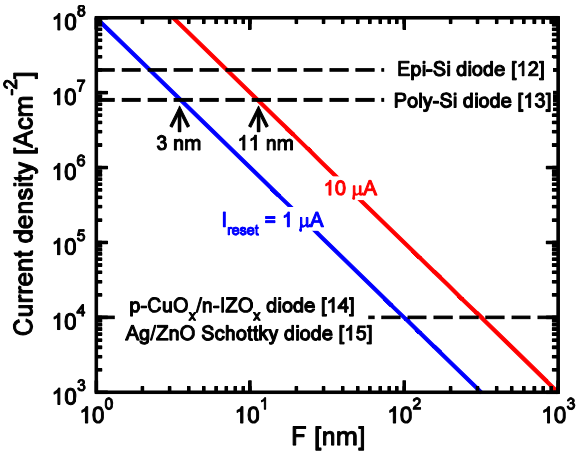

Figure 10. Calculated reset current density $j = I_{reset}/F^2$ as a function of technology node F, for I_{reset} = 1 and 10 μA. Reported j values for diode technologies [12-15] allow for scaling projections for crossbar RRAMs.

III. SCALING PERSPECTIVE

Achieving sub-10 μA current for the reset operation is crucial for the development of scalable crossbar memory arrays. In fact, the maximum I_{reset} necessary for the reset operation directly impacts the area of the select diode through the available current density j in the forward bias [3]. Fig. 10 shows the calculated $j = I_{reset}/F^2$ as a function of the technology node F where I_{reset} = 1 and 10 μA are assumed as examples of reset currents. Low I_{reset} could be achieved limiting the current during set by the MOSFET drivers which are available for decoding/selecting wordlines/bitlines. Reference current densities for already reported diodes are shown, including epitaxial Si [12], poly-Si [13], oxide-based [14] and Ag-ZnO Schottky diodes [15]. While Si-based diode allows for scaling to at least F = 11 nm, further improvement of oxide-based diodes is currently needed to allow for scalable/stackable cross-bar arrays.

IV. CONCLUSIONS

We have studied the scaling of reset current I_{reset} in NiO-based RRAMs through the limitation of the current during the set operation by an integrated MOSFET. I_{reset} was shown to be controllably reduced below 10 μA. Such low currents may allow for extremely high-density crossbar RRAM with diode selectors. In particular, our results show that a cross-bar RRAM with Si-based select diodes may be scaled down to at least 11 nm node.

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