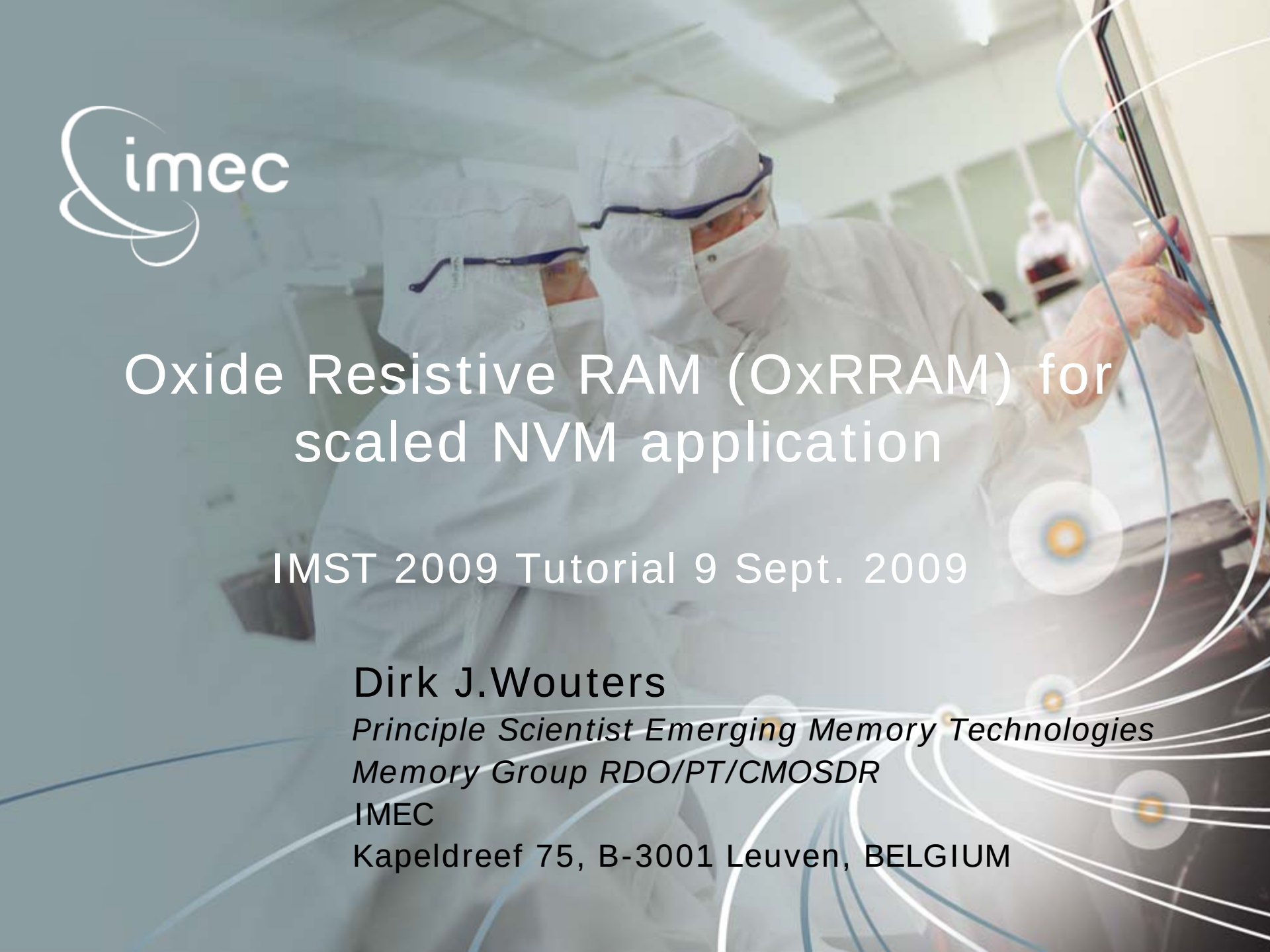


# Oxide Resistive RAM (OxRRAM) for scaled NVM application

IMST 2009 Tutorial 9 Sept. 2009


Dirk J.Wouters

*Principle Scientist Emerging Memory Technologies*

*Memory Group RDO/PT/CMOSDR*

IMEC

Kapeldreef 75, B-3001 Leuven, BELGIUM

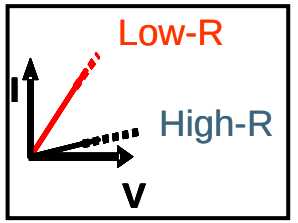
# Introduction

- Focus on non-volatile resistive switching in binary oxides (TMO), for possible use in scaled NVM
- Focus on unipolar switching (because of cell size), though same materials also show bipolar switching → related mechanism?
- Focus on scaling potential and potential issues:
  - Most experimental data still on large devices
  - Application introduction only at 10nm technology node
  - Can we extrapolate and scale? What changes ?
- *Though about 10yrs of (renewed) RRAM research, many items remain that need further investigation by the research community !*

# Outline

- Introduction
- What is a resistive switching device (concept)
  - Focus on unipolar switching RRAM
- Short History of switching in oxide films for memory application
  - Revival of on old idea
- Mechanisms of resistive switching in oxides
  - Unipolar (vs. bipolar) switching in TMO's
- Scaled OxRRAM for FLASH memory replacement?
  - Scaling prospects of RRAM
- Conclusions

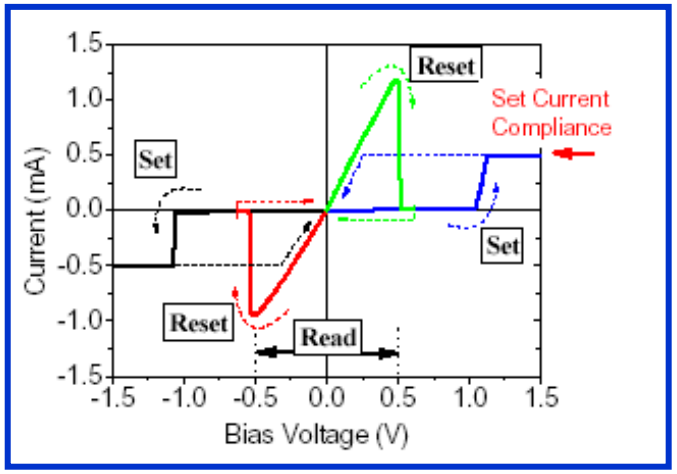
# What is a resistive switching device (concept)

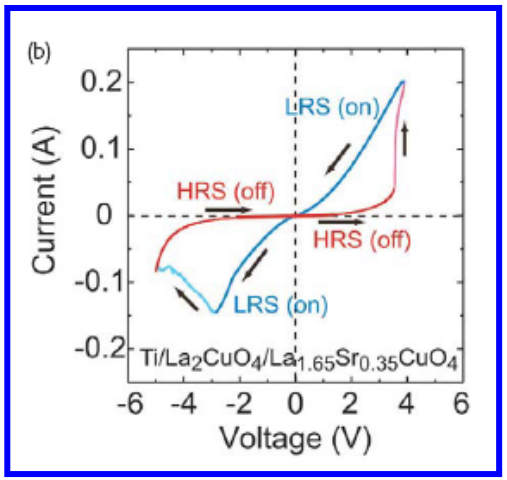



- **A 2-terminal resistor element with electrically alterable resistivity**
  - typically a low and high conductive state, although (controllable) multi conductive states would be an asset (MLC)
  - Focus on programming with an electrical signal (e.g. not magnetic)
- **Focus on non-volatile resistivity change**
  - Different from Ovonic switching (electronic switching from low to high-conductive state, but requiring a hold current to remain in high-conductive state), and also of typical Mott transition element (as VOx)
- **Focus on elements that can switch repeatedly from low to high conductive state.**
  - Different from typical Fuse or anti-Fuse element (limited application to OTP)
- **I-V characteristics not critical**
  - Typical I-V switching characteristics do not obey memristor theory

# What is a resistive switching device (concept)

- **Focus on UNIPOLAR switching**
  - **Both unipolar and bipolar switching devices**
    - **Unipolar:**
      - Set/Reset programming independent of voltage polarity write pulse
      - OK using only 1 type of voltage polarity
    - **Bipolar:**
      - Reset requires opposite polarity of write voltage then Set

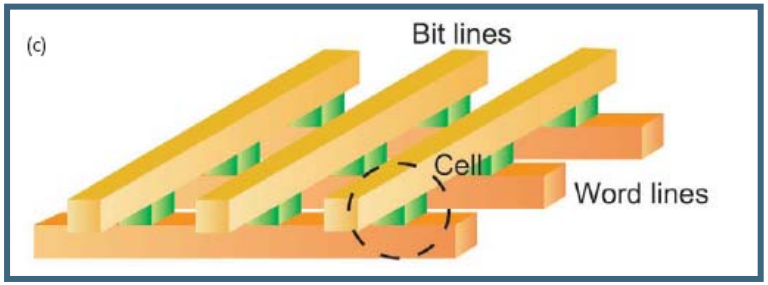



  - **Main importance**:
    - Effect on memory cell selector device → cell size and array/periphery design

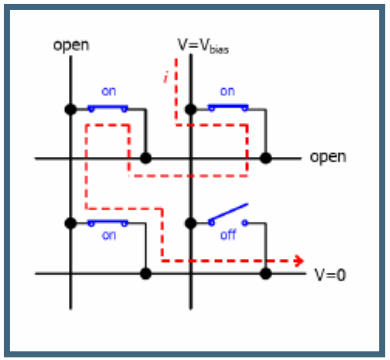
# Cell and array configuration

- RRAM target application = NAND Flash replacement for <2X technology node. Requirements:
  - → Small cell size (~$4F^2$/cell)
- Cross-bar array concept (TE lines ⊥ BE lines) results in $4F^2$ cell



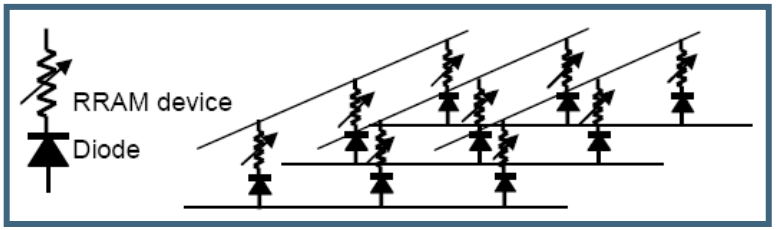

A.Sawa,
Materials Today, Vol11(6), 2008, p. 28

- However, raw cross-bar array not feasible because possible read errors (Sneak currents)
  - → Need for selector element



# Selector element : general constraints

- MOSFET transistor :
  - Good current drive capability
  - Both uni- and bi-polar switching elements possible
  - Large cell (3-terminal device)
- DIODE :
  - Small footprint, $4F^2$ cell size by vertical stack
  - Only for unipolar switching devices



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- Conclusions

# Discovery resistive switching in oxides : 1960's !

**SiO !**

**Vol 11, May 1964, p. 243**

*IEEE TRANSACTIONS ON ELECTRON DEVICES*

## The Reversible Voltage-Induced Initial Resistance in the Negative Resistance Sandwich Structure

P. H. NIELSEN
N. M. BASHARA
Dept. of Elec. Engrg.
University of Nebraska
Lincoln, Neb.

Recently the authors have found that a high initial resistance can be read out for long periods of time as long as the voltage is kept well below that for maximum current.

The above obviously suggests use of this device as a memory element which can read out nondestructively and which can be "erased" at will by increasing the voltage to a value beyond that for maximum current. The upper frequency limit of this effect has not been determ neither has the usable read-out time.

Au/SiO/Au structure

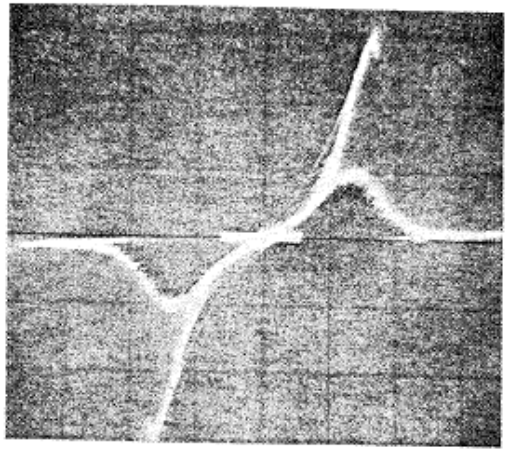

Fig. 1—Current-voltage locus, 60 cps. Ordinate scale is 40 ma/div, abcissa 2v/div. Superimposed is the high initial resistance locus resulting from *sudden* voltage removal at about 7-volts peak. The upper negative resistance curve is for voltage increasing, the lower for voltage decreasing.

*The Radio and Electronic Engineer, August 1967*

## New Thin-film Resistive Memory

*By*
J. G. SIMMONS,
B.Sc., Ph.D., F.Inst.P.†
AND
R. R. VERDERBER,
B.Sc., M.Sc.‡

**Summary:** A new thin-film metal–insulator–metal device is described. After the insulator has undergone a forming process, which consists of the electrolytic introduction of gold ions from one of the electrodes, its conductivity is observed to have increased quite markedly. In addition the sample displays negative-resistance and memory phenomena. It is shown that under the appropriate switching conditions the device can be used as a non-volatile analogue memory with non-destructive read-out. The theory of operation of the device is also presented.

# Discovery resistive switching in oxides : 1960's !

- Main characteristics of RRAM already described:

**"forming process"**

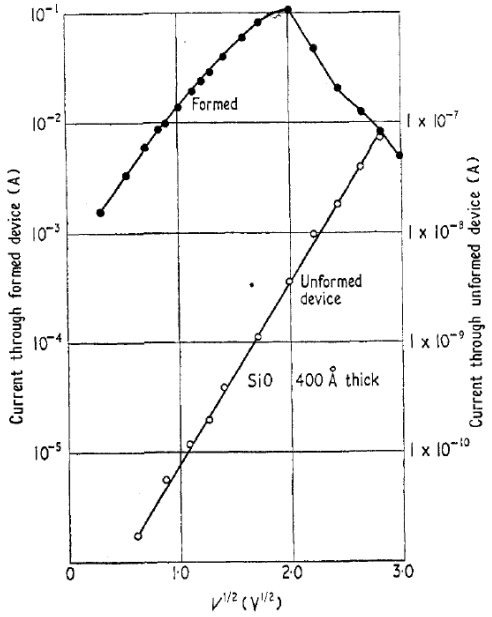


Figure 5. Current–voltage characteristics of unformed and formed device (after Simmons and Verderber 1967).

**"switching characteristics"**

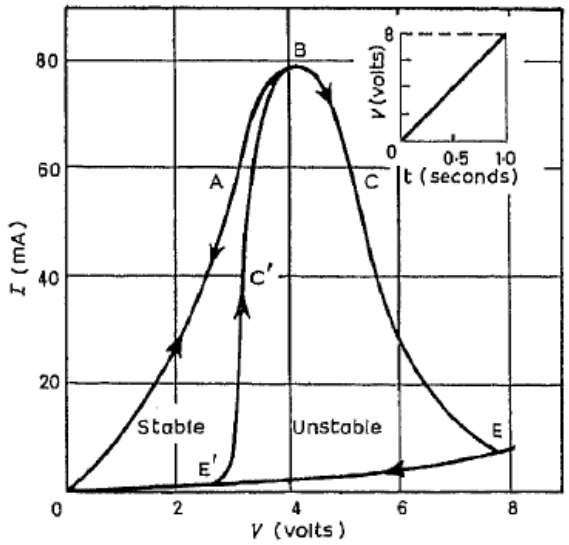


**Fig. 5.** Schematic illustrating the stable and unstable areas of the *V–I* characteristic.

G. DEARNALEY,† A. M. STONEHAM,† AND D. V. MORGAN‡

*Rep. Prog. Phys.*, 1970, **33**, 1129–1191

J. G. SIMMONS, B.Sc., Ph.D., F.Inst.P.†
AND
R. R. VERDERBER, B.Sc., M.Sc.‡

*The Radio and Electronic Engineer, August 1967*

# Resistive switching effect in *Transition Metal Oxides*

- First switching of NiO was already reported in 1964!

*Solid-State Electronics* Pergamon Press 1964. Vol. 7, pp. 785–797. Printed in Great Britain

## SWITCHING PROPERTIES OF THIN NiO FILMS*

**J. F. GIBBONS and W. E. BEADLE†**
Stanford Electronics Laboratories, Stanford, California
(*Received* 30 *March* 1964)

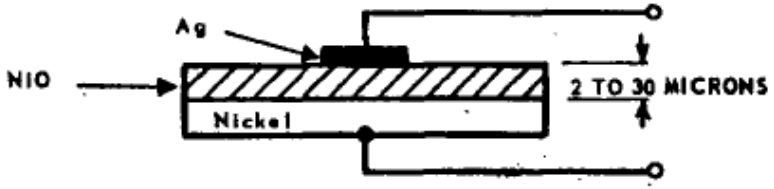


FIG. 1. Schematic representation of basic NiO thin-film device.

# *Whatever happened to….*

**Resisitive switching memories based on these concepts eventually never developed :**

- problems of stability
- scaling questioned
- **emergence & rapid successful development of Si-based memories**

# Recent surge of interest

- 4 important events that put oxide RRAM again in the picture :

1. A.Beck, B.J.Bednorz et al, IBM Zurich, APL 2000

# 1. A.Beck, B.J.Bednorz et al, IBM Zurich, APL 2000

- Thin oxide films for memory are back !

33 yrs

The Radio and Electronic Engineer, August 1967

U.D.C. 537.226

## New Thin-film Resistive Memory

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APPLIED PHYSICS LETTERS VOLUME 77, NUMBER 1 3 JULY 2000

## Reproducible switching effect in thin oxide films for memory applications

A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel,[a] and D. Widmer
*IBM Research, Zurich Research Laboratory, CH–8803 Rüschlikon, Switzerland*

(Received 13 March 2000; accepted for publication 15 May 2000)

Thin oxide films with perovskite or related structures and with transition metal doping show a reproducible switching in the leakage current with a memory effect. Positive or negative voltage pulses can switch the resistance of the oxide films between a low- and a high-impedance state in times shorter than 100 ns. The ratio between these two states is typically about 20 but can exceed six orders of magnitude. Once a low-impedance state has been achieved it persists without a power connection for months, demonstrating the feasibility of nonvolatile memory elements. Even multiple levels can be addressed to store two bits in such a simple capacitor-like structure. © *2000 American Institute of Physics.* [S0003-6951(00)04327-8]

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1. A.Beck, B.J.Bednorz et al, IBM Zurich, APL 2000
2. W.Zhuang et al, Sharp/Univ Houston, IEDM 2002

# 2. W.Zhuang et al, Sharp/Univ Houston, IEDM 2002

- coined the term RRAM
- realization 1D1R array

## Novell Colossal Magnetoresistive Thin Film Nonvolatile Resistance Random Access Memory (RRAM)

W. W. Zhuang[1], W. Pan[1], B. D. Ulrich[1], J. J. Lee[1], L. Stecker[1], A. Burmaster[1], D. R. Evans[1], S. T. Hsu[1], M. Tajiri[2], A. Shimaoka[2], K. Inoue[2], T. Naka[2], N. Awaya[2] K. Sakiyama[2], Y. Wang[3], S. Q. Liu[3], N. J. Wu[3], and A. Ignatiev[3]

1: Sharp Laboratories of America, 5700 NW Pacific Rim Blvd, Camas, WA 98607, USA
2: Sharp Corporation, IC Group, 2613-1 Ichinomoto-cho, Tenri, Nara 632, Japan
3: Texas Center for Superconductivity and Advanced Material , University of Houston, Houston, Texas 77204-5002 USA

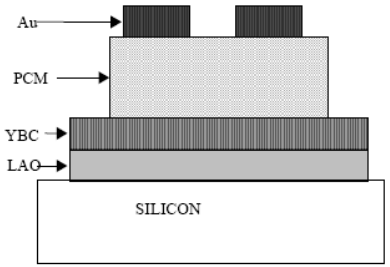


Fig.1 Pulsed Laser Deposited (PLD) test memory resistor structure. The memory material is PCMO ($Pr_{0.7}Ca_{0.3}MnO_3$). The double bottom electrode is formed with YBCO ($YBa_2Cu_3O_{7-x}$) on LAO ($LaAlO_3$)

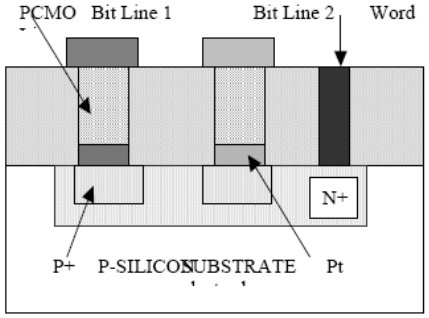


Fig.3 Resistor/diode memory array cell structure. Both top and bottom electrode of the memory resistor is made of Pt. The cell size can be as small as $4F^2$ This memory array required positive pulse for bot write and reset programming

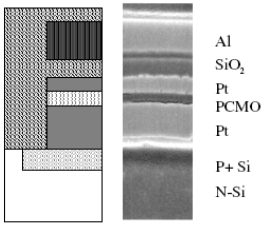


Fig.5 TEM microphotograph of a 1R1D memory cell. Shallow P+ layer is formed onto n bit line. The memory array interconnect is copper doped Al.

*Principle on bulk crystals published by A.Asamitsu et al., Nature, 1997*

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1. A.Beck, B.J.Bednorz et al, IBM Zurich, APL 2000
2. W.Zhuang et al, Sharp/Univ Houston, IEDM 2002
3. I.G.Baek et al., Samsung, IEDM 2004

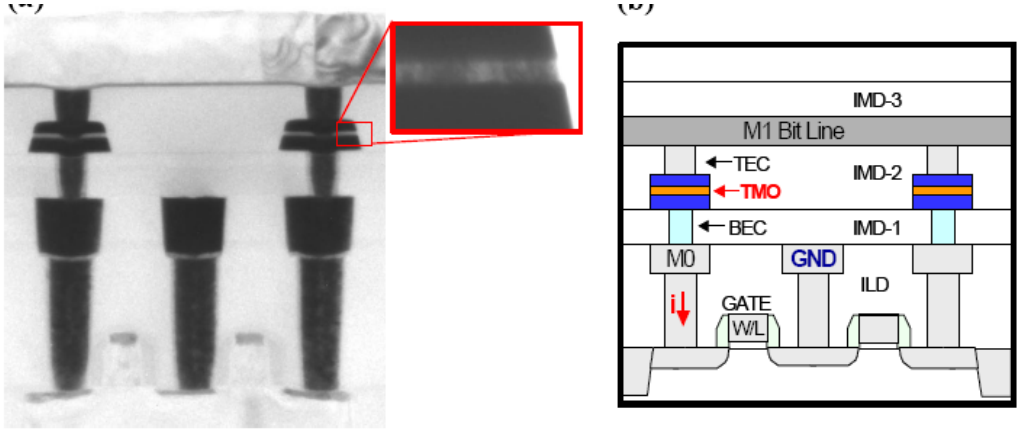
# 3. I.G.Baek et al., Samsung, IEDM 2004

- 1st advanced work (integrated device) with simple binary oxide (NiO)
- Coined the term OxRRAM (unipolar switching in TMO)

**Highly Scalable Non-volatile Resistive Memory using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses**

I. G. Baek, M. S. Lee, S. Seo*, M. J. Lee*, D. H. Seo*, D.-S. Suh*, J. C. Park*, S. O. Park, H. S. Kim, I. K. Yoo*, U-In Chung and J. T. Moon

IEDM 2004



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3. I.G.Baek et al., Samsung, IEDM 2004
4. D.B.Strukov et al., HP labs, Nature 2008

- Since then, resistive switching observed in many different oxides…

# 4. D.B.Strukov et al., HP labs, Nature 2008

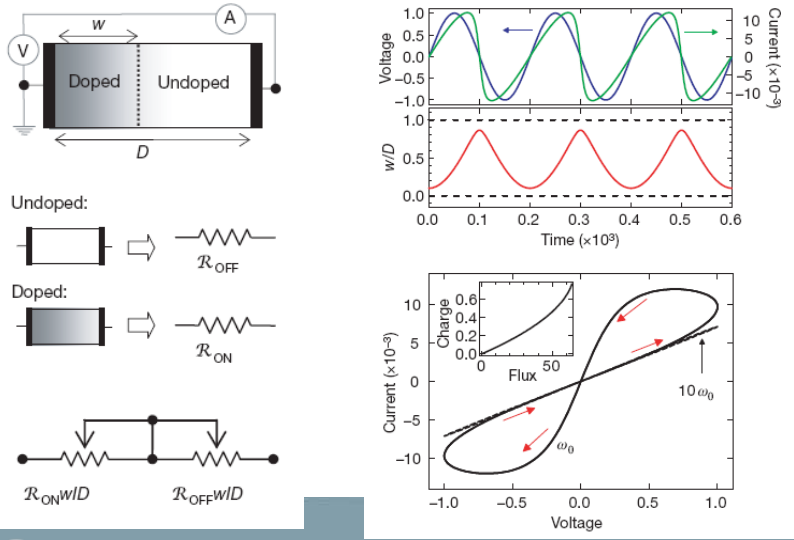
- Memristor concept applied to RRAM
- Triggered a lot of interest, especially in EE (design) world

Vol 453|1 May 2008|doi:10.1038/nature06932

## The missing memristor found

Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]

$$M(q) = \mathcal{R}_{OFF}\left(1 - \frac{\mu_V \mathcal{R}_{ON}}{D^2} q(t)\right)$$



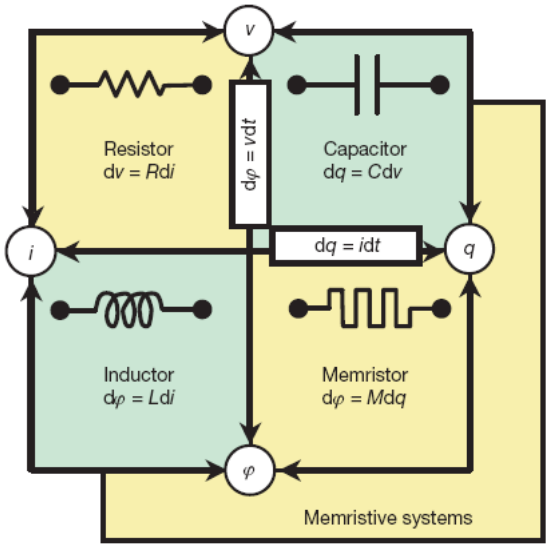




**Figure 1 | The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor.** Resistors and memristors are subsets of a more general class of dynamical devices, memristive systems. Note that $R$, $C$, $L$ and $M$ can be functions of the independent variable in their defining equations, yielding nonlinear elements. For example, a charge-controlled memristor is defined by a single-valued function $M(q)$.

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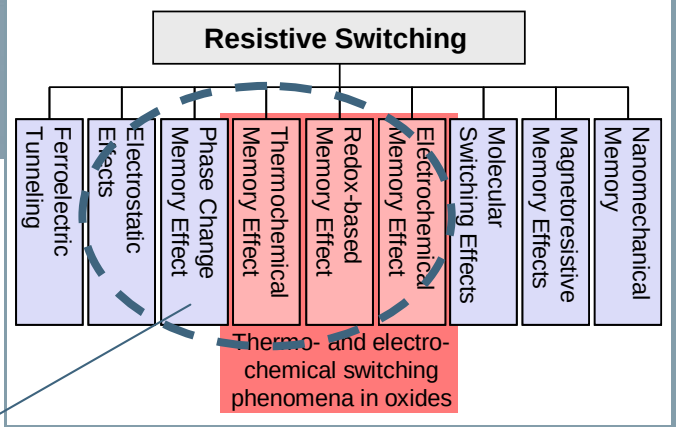
# Classification of mechanisms

Ref. R.Waser and M.Aono, Nature Materials 2007




R.Waser IEDM 2008

Resistive switching

Thermal effect

Ionic effect

PCM

Phase change

Cation migration – electrometallization

CBRAM

Fuse-Antifuse effect

Anion migration – redox effect

VCM (?)

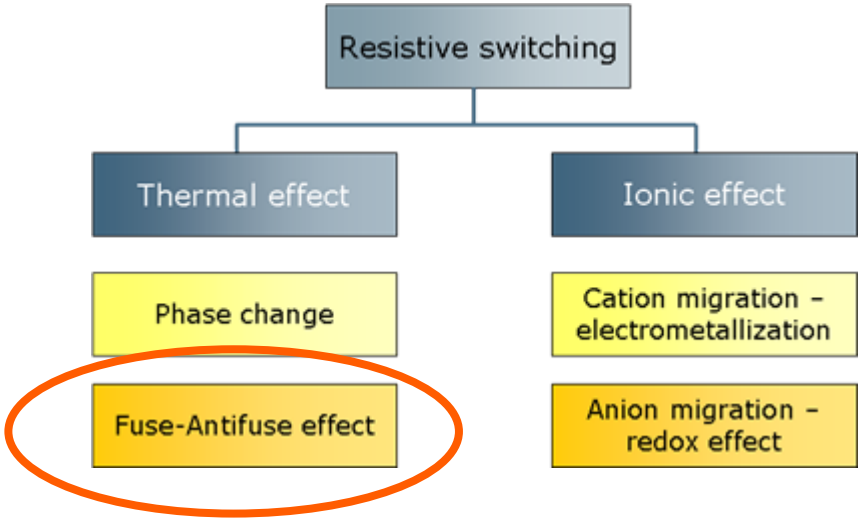
Electrostatic effect *

OxRRAM

(Not considered)

CT, Mott

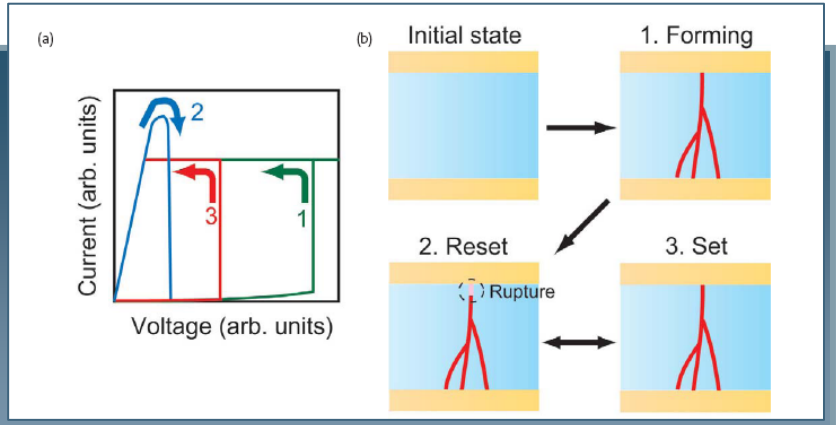
# Thermochemical (Fuse-/Antifuse) OxRRAM




***Unipolar switching***

- ***Filamentary nature (metallic filaments?)***
- ***Mechanism:***
  - ***(soft) voltage breakdown to create/restore filaments***
  - ***(local) thermal dissolution by high current to break filament***

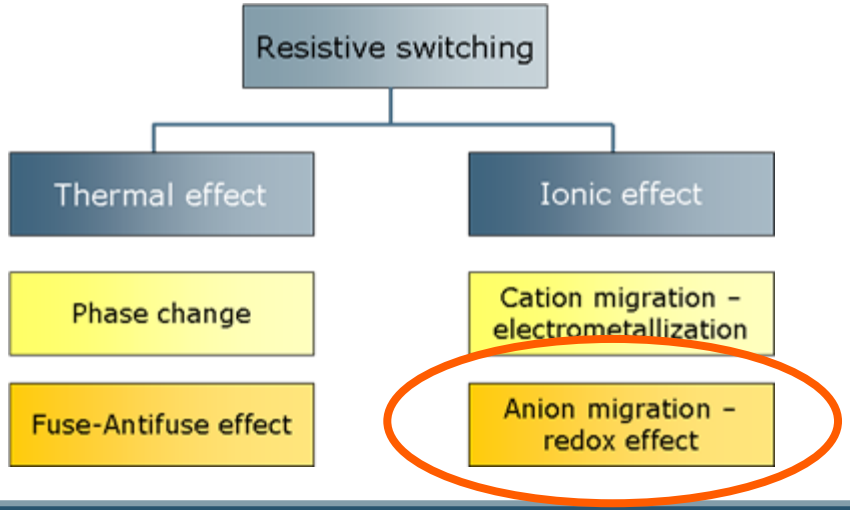
- ***materials : TMO's : NiO, TiO, CuO, ZrO , HfO...***




Akihito Sawa

materialstoday JUNE 2008 | VOLUME 11 | NUMBER 6

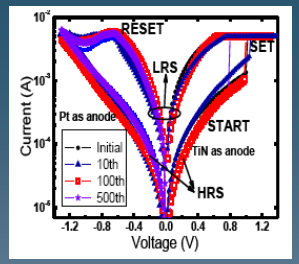
# Anion migration : Type I



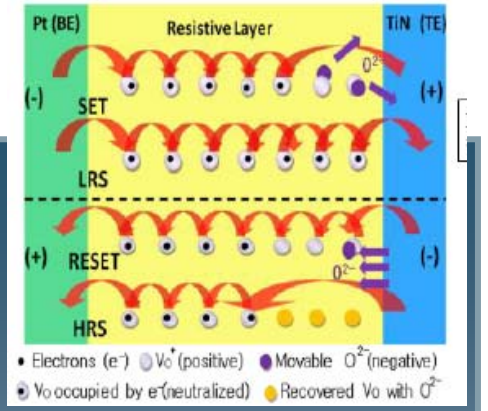

- ***Bipolar switching***
- ***Filamentary nature (oxygen vacancies)***
- ***Mechanism:***

  ***(i) Oxygen vacancies form hopping conduction path (ZnO)***

  - **SET process is similar as dielectric soft breakdown which generates and moves oxygen vacancies to form CFs, like a percolation effect**
  - **RESET is due to the depletion of electrons in some *VO+* along CFs @*VRESET* and the recovery of the electron-depleted *VO+* with *O2***




N.Xu et al, VLSI Tech 2008

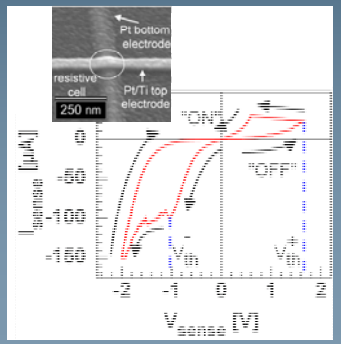



  ***(ii) Oxygen vacancies locally acts as dopants making the MO conductive (TiO)***

  - ***oxygen vacancies pile up near cathode → reduce metal valency by trapping electrons***
  - ***Form conductive region (virtual cathode) that moves up to anode***

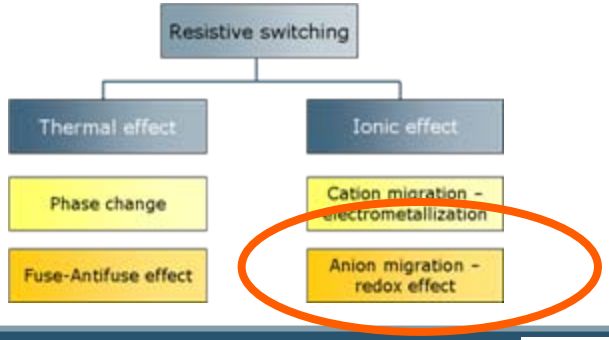
- ***TMO's (NiO,HfO, TiO...), but also STO***

VCM




*R.Waser, IEDM2009*

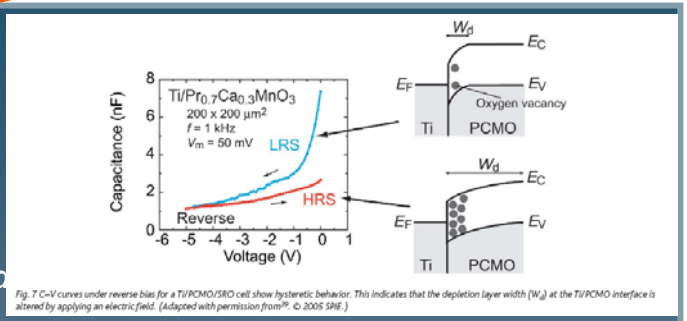
# Anion migration : Type II




- ***Bipolar switching***
- ***INTERFACE effect***

-***Mechanism:***

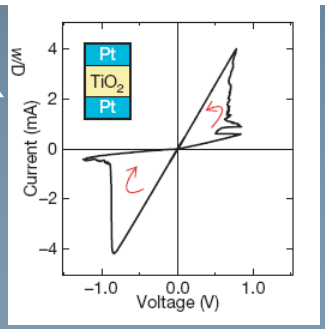
-***Oxygen Vacancy diffusion results in oxygen depleted zone near cathod***
→***Effective $V_O$+ doping effect:***
→***change of barrier height modifies electron injection from electrode***



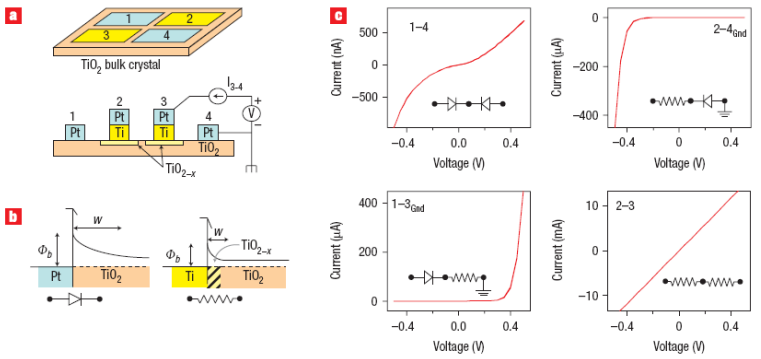

A.Sawa,
Materials Today, Vol11(6), 2008, p. 28

-***Mostly complex oxides (PCMO, doped STO), but also TiO ("Memristor")***

D.Strukov et al, Nature, May 2008



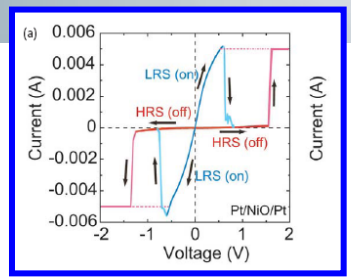

VCM




J.J.Yang et al, Nature Nanotechnology, Vol.3, July 2008

# RRAM Mechanisms : overview

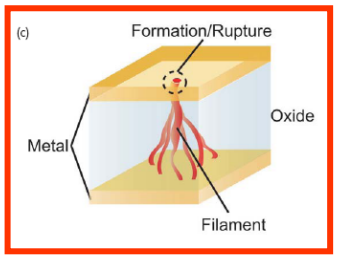
- **Thermal**
  - Fuse-antifuse processes [thermochemical]
    - Conductive filaments cf. dielectric breakdown



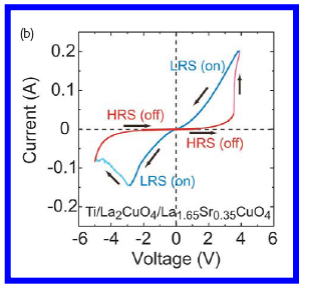

unipolar

bipolar

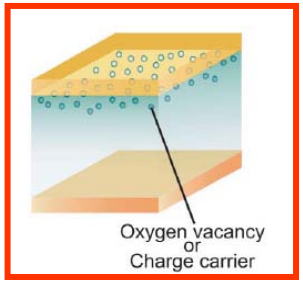
- **Ionic**
  - Ionic transport + redox reactions
    - Anion migration (oxygen vacancies)
      - TYPE I
        → conduction through **filament** of localized oxygen vacancies
      - TYPE II
        Oxygen vacancies affect SB height in metal/semiconductor-like **interface** (Uniform view)




filament



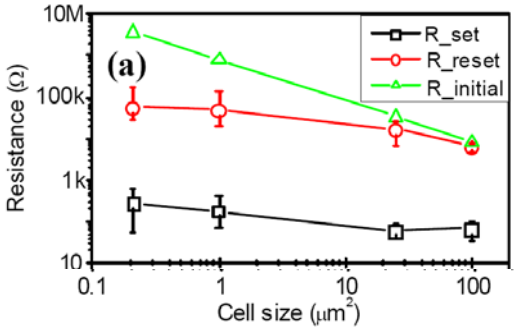

interface



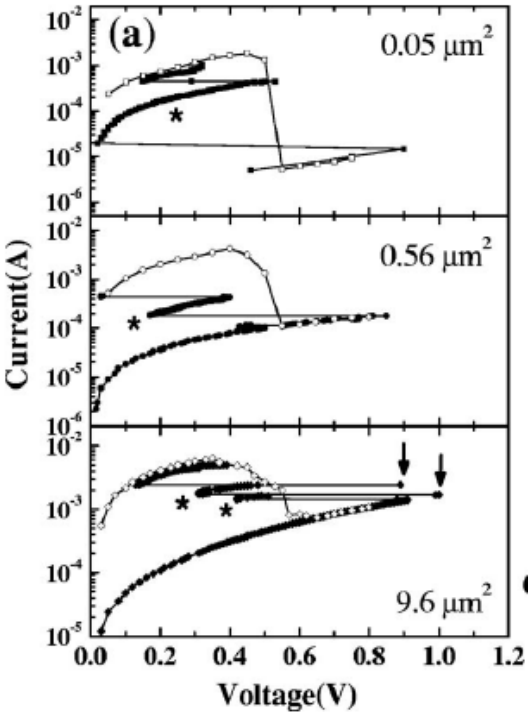

**Because of unipolar mechanism, Focus on Fuse/antifuse type**

# Unipolar switching in OxRRAM

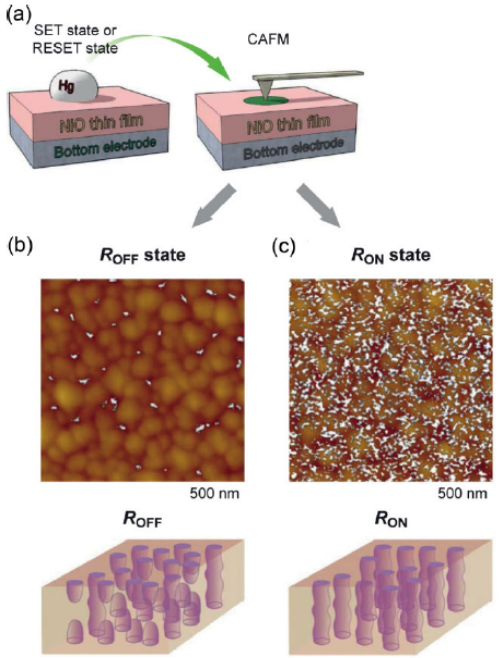
- Many indications of filamentary switching found:
  - (non) scaling of Ron with cell area
  - Intermediate and anomalous switching states
  - C-AFM




*Baek et al, IEDM 2004*



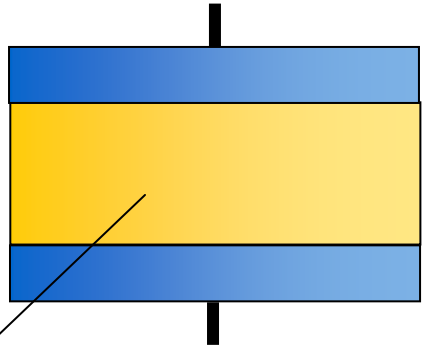

*Kim et al, APL 88, 202102 (2006)*




[162] J. Y. Son, Y.-H. Shin, *Appl. Phys. Lett.* **2008**, *92*, 222106.

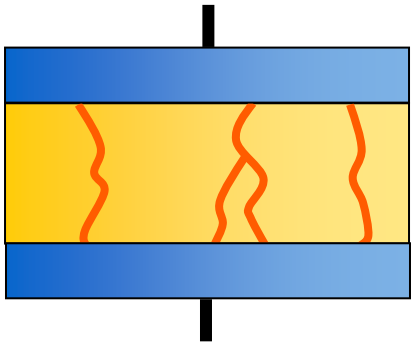
# Area scaling of LRS/HRS resistance in OxRRAM

**Initial state**



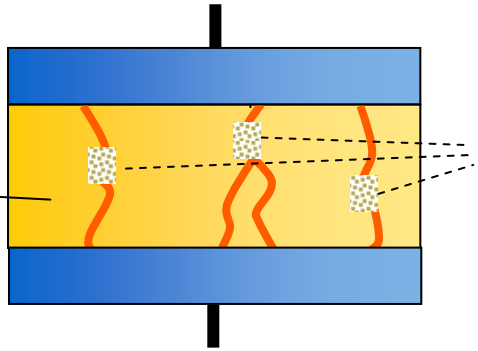
$R_{init}$ ~ 1/Area

**SET state**



$R_{LRS}$ ~ 1/#filaments

**RESET state**



$R_{HRS}^{2} = R_{init}$

$R_{HRS}^{1}$ ~ 1/#filaments

$R_{HRS}^{2} = R_{HRS}^{1} // R_{init}$

**1/#filament**
**OR**
**1/Area**

# Unipolar switching in OxRRAM

- indications of metallic nature of filaments:
  - Positive temperature coefficient of resistance
  - XTEM/EELS: observation of pure Ni peak w/o O

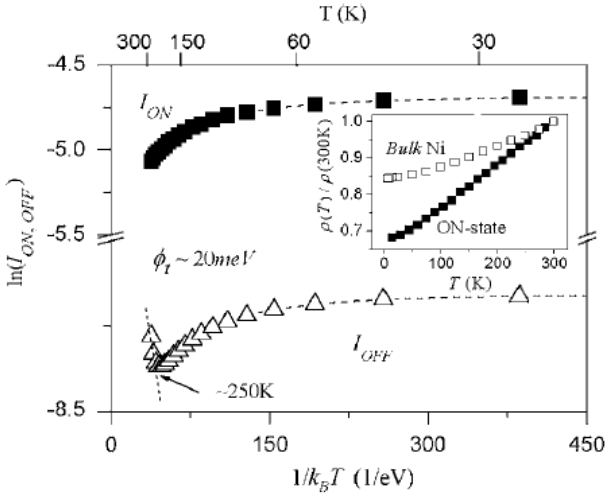



FIG. 4. $\ln(I)$ vs $1/k_BT$ curves of $I_{off}$ and $I_{on}$ whose temperature dependences were obtained separately without switching at each temperature. $V = \pm 0.2$ V. The inset shows the temperature dependence of the normalized resistivity, $\rho(T)/\rho(300\ K)$, for $I_{on}$ and a bulk Ni film.

*Jung et al, APL 90, 052104 (2007)*

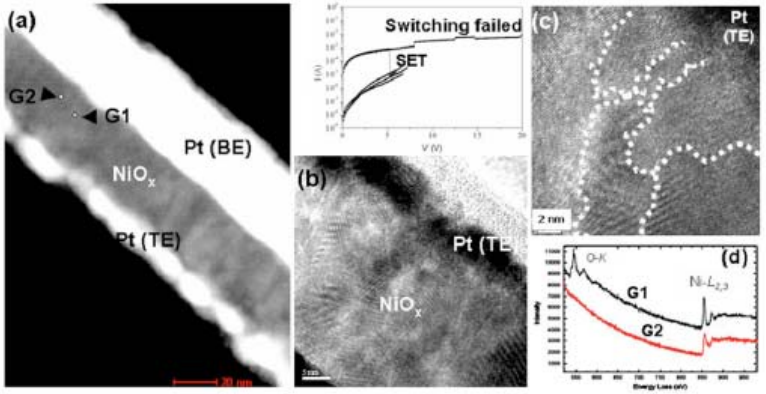
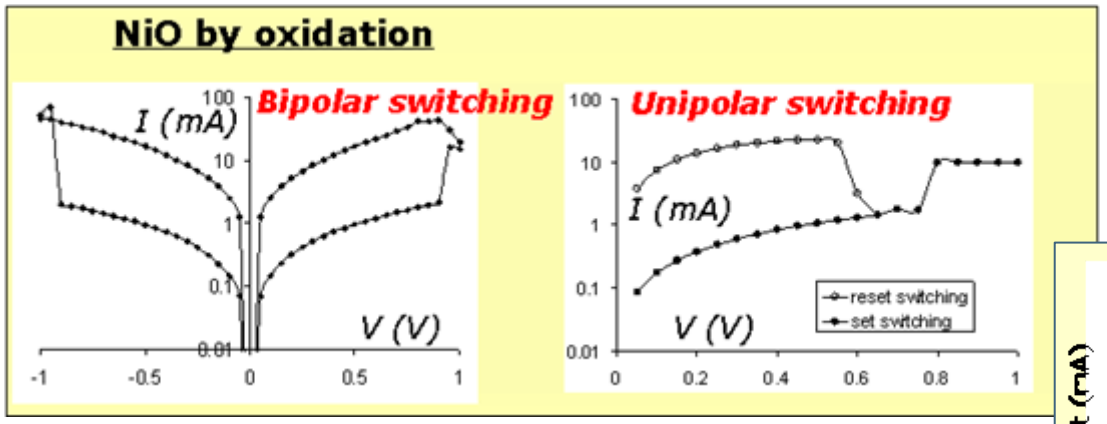


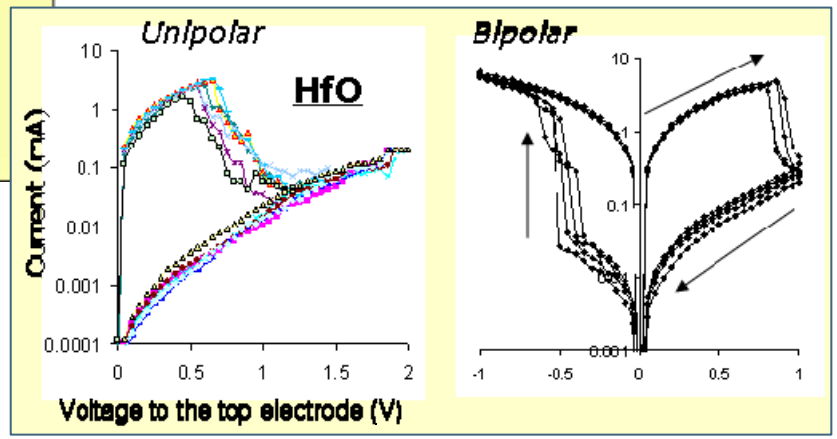

FIG. 2. (Color online) Cross-sectional HAADF-STEM (a) and HR-TEM (b) images of the switching failed $NiO_x$ film showing the $NiO_x$ grains generally broken from the columnar shapes. (c) Typical HR-TEM image obtained at the $NiO_x$ film near the top Pt electrode, which clearly illustrates irregularly broken $NiO_x$ grains as indicated by the dotted line. (d) Electron energy-loss spectra taken from the area G1 (grain) and area G2 (grain boundary) of (a) with the probe size of ~1 nm.

*Park et al, APL 91, 222103 (2007)*

# (No) link between material and switching mechanism ?

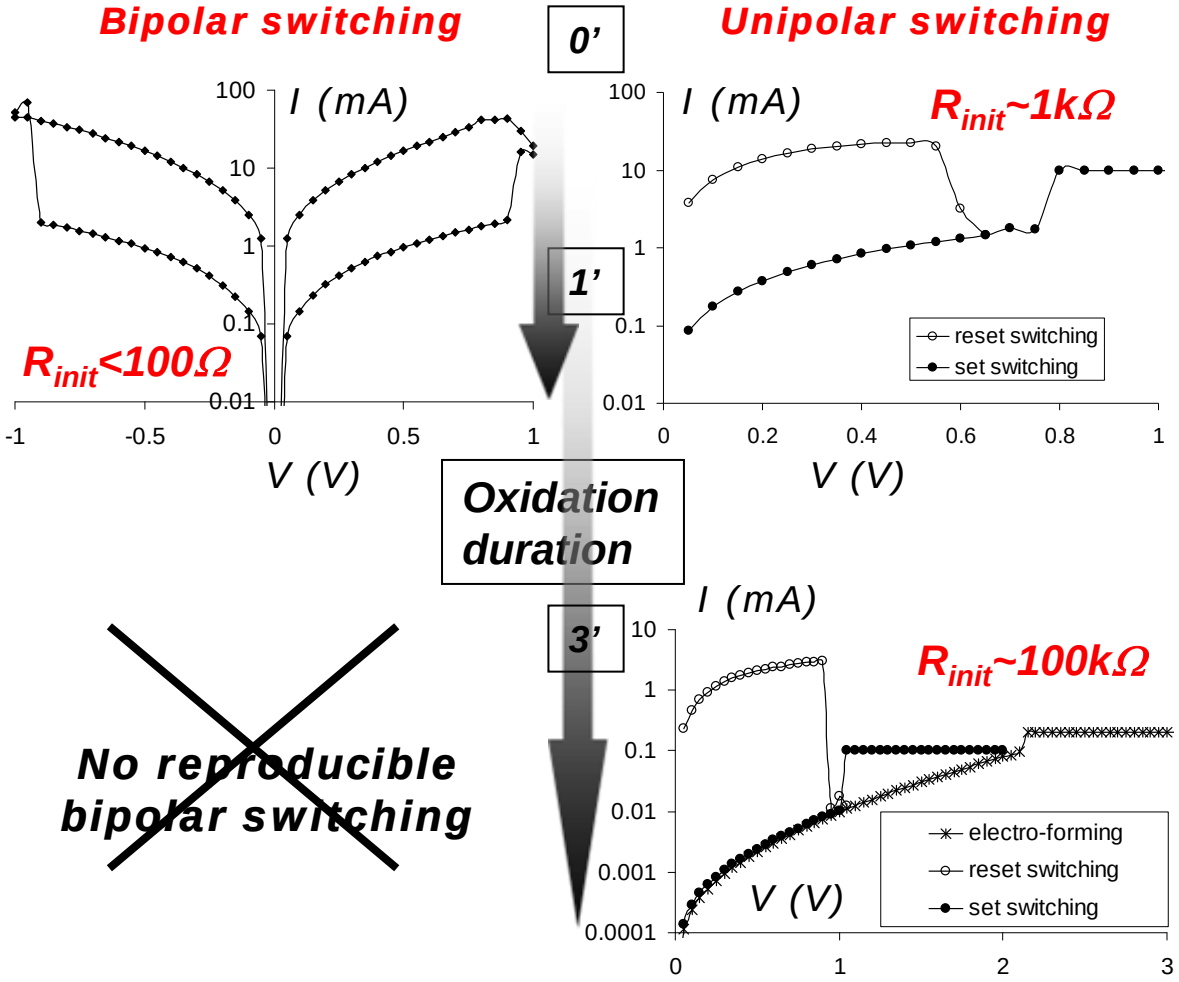
- Both unipolar and bipolar switching has been observed on same TMO material : depending on program procedure !?
  - Pt/TiOx/Pt *(D.S. Jeong et al.; ECS 2007)*
  - Ni/NiO/Ni : L.Goux et al (IMW 2009)
  - TiN/HfO/Pt (IMEC, unpublished results)



# Co-existance unipolar/bipolar OxRRAM in NiO

**Oxidation at 500C for different durations in oxygen:**




**No reproducible bipolar switching**

**Short oxidation:**

**Low** initial resistance $R_{init}$

- No forming process
- Coexistence of both switching modes

**Longer oxidation:**

**Higher $R_{init}$**, due to thicker NiO, change of microstructure…

*(J.G. Lisoni et al.; MRS 2009)*

- Forming needed
- Difficult bipolar mode

# Similarity/Link between 2 mechanisms

Fuse/antifuse: typically ***metallic*** filament

Anionic type: ***oxygen vacancy*** filament

**Speculation**

More qualitative than quantitative difference ?

→ If local [$V_O$+] increases: closer to metal !

Oxygen vacancies play crucial role in both mechanisms !

**Observation**

→ Nature of filament changes for high or low power UNIPOLAR programming

low Rset = high power

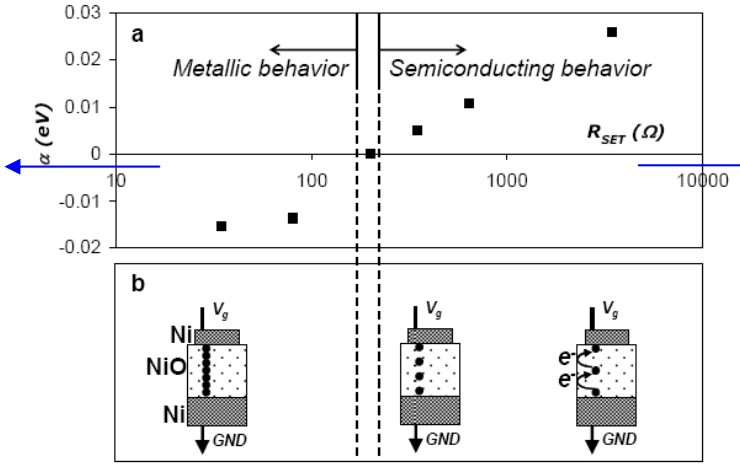



Fig. 5 a) $R_{SET}$ dependence of the extracted activation energy $\alpha$ defined in Fig. 4; b) sketches of the associated amounts of oxygen vacancies created during set switching and affecting the conduction mechanism

High Rset = low power

*L.Goux et al, IEEE TED 2009*

# Outline

- Introduction
- What is a resistive switching device (concept)
  - Focus on unipolar switching RRAM
- Short History of switching in oxide films for memory application
  - Revival of on old idea
- Mechanisms of resistive switching in oxides
  - Unipolar (vs. bipolar) switching in TMO's
- Scaled OxRRAM for FLASH memory replacement?
  - Scaling prospects of RRAM
- Conclusions

# Non-volatile solid-state memory

## USB flash drives

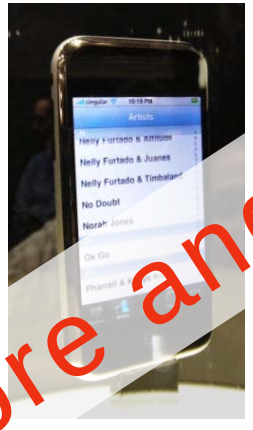
http://en.wikipedia.org/wiki/USB_flash_drive

## MP3 Players

http://en.wikipedia.org/wiki/MP3_Player

http://en.wikipedia.org/wiki/Ipod

## Mobile phones



http://en.wikipedia.org/wiki/IPhone

## Solid state hard disks

http://en.wikipedia.org/wiki/Solid-state_drive

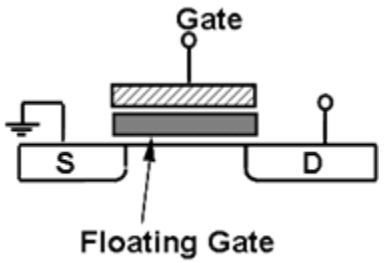
## Laptops without magnetic HD

http://en.wikipedia.org/wiki/Eeepc

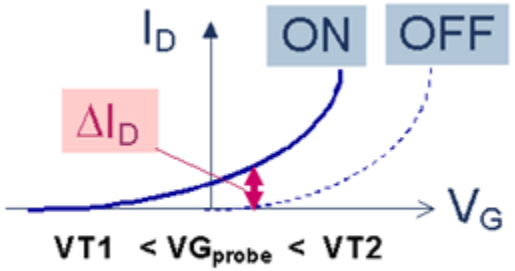
More and more memory is required

# Current main NVM technology = (NAND) Flash

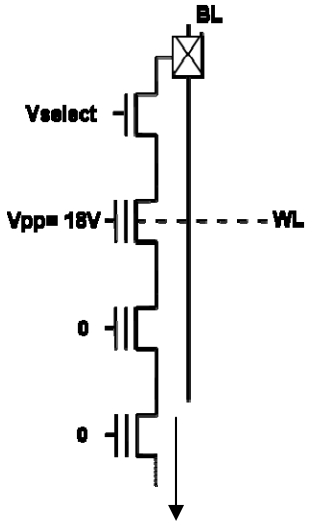
- Basic device = Si floating gate transistor, 1T cell



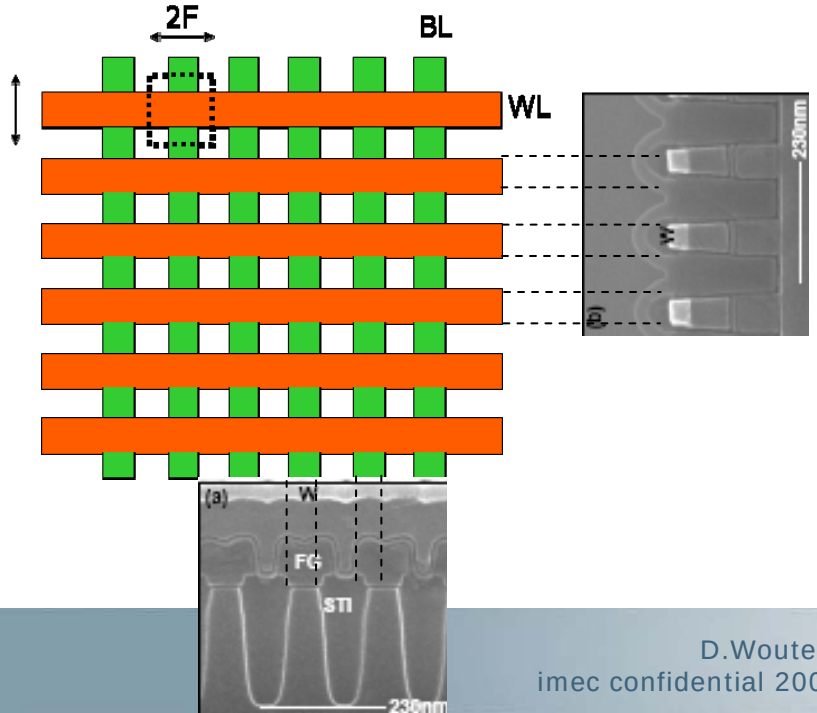

**- WRITE** : threshold voltage is shifted by putting (**PROGRAM**) or removing (**ERASE**) charge from the floating gate (by *hot carrier injection* or *tunneling*)
**- READ-OUT** by selecting element and current sensing




- NAND Flash array: *true cross point array* of WL (poly) over BL (diffusion) = $4F^2$/cell !

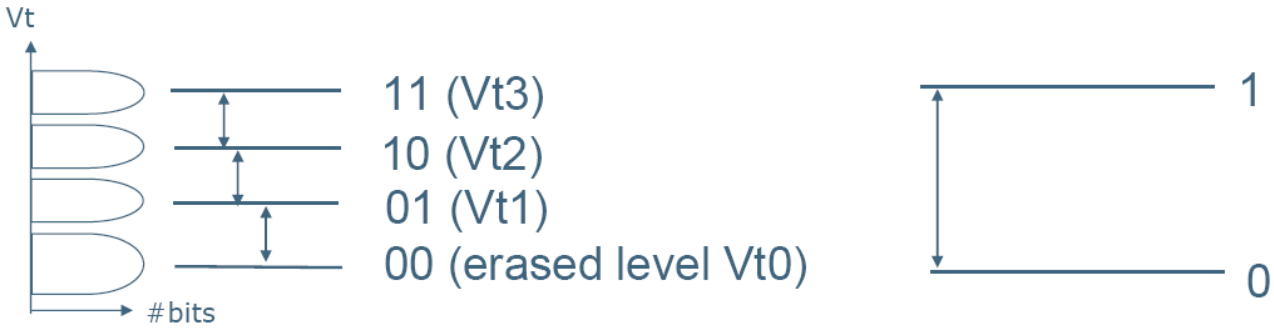



"NAND" string configuration
*(>< "NOR")*



# Current main NVM technology = (NAND) Flash

- Flash also uses MultiLevel
  - Programming to 3 different Vt levels allows to store 2bits/cell (2n levels = n bits): margins divided by 3!

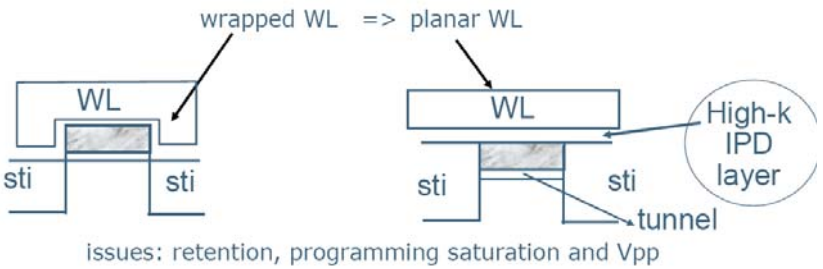



  - This multilevel capability of floating gate memory allowed for a unique step in bit size scaling : **$2F^2$ / bit**

- Current status:
  - NAND (Samsung,Toshiba/Sandisk, Hynix, Micron/Intel), now @ 64Gb, 4X-3X technology node

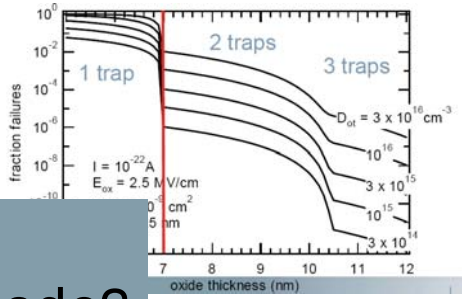
# Flash scaling limitations (1)

- Scaling limitations
  - Reduced FG coupling of scaled device




issues: retention, programming saturation and Vpp

  - Limit of tunnel ox scaling



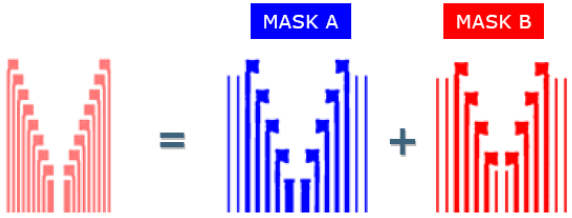

*Degraeve et al, IEDM 2001*

    - Nu further voltage scaling

**Limits of Flash scaling beyond 30nm node?**

  - Electros
    neighbo

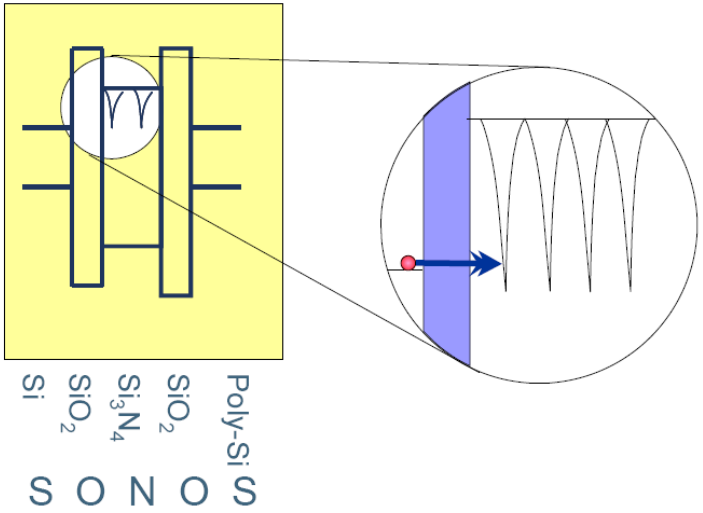
  - Dense patterning requirements ahead of advanced litho



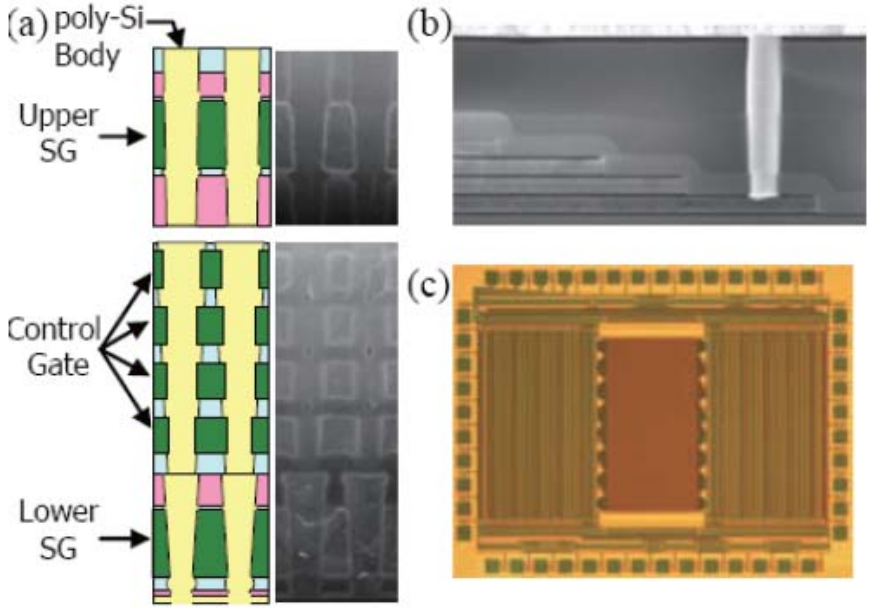

    - Dual patterning developments

# Flash scaling solutions : (1) Evolutionary

1. Charge Trap Flash
   - Use of charge trap layer instead of FG



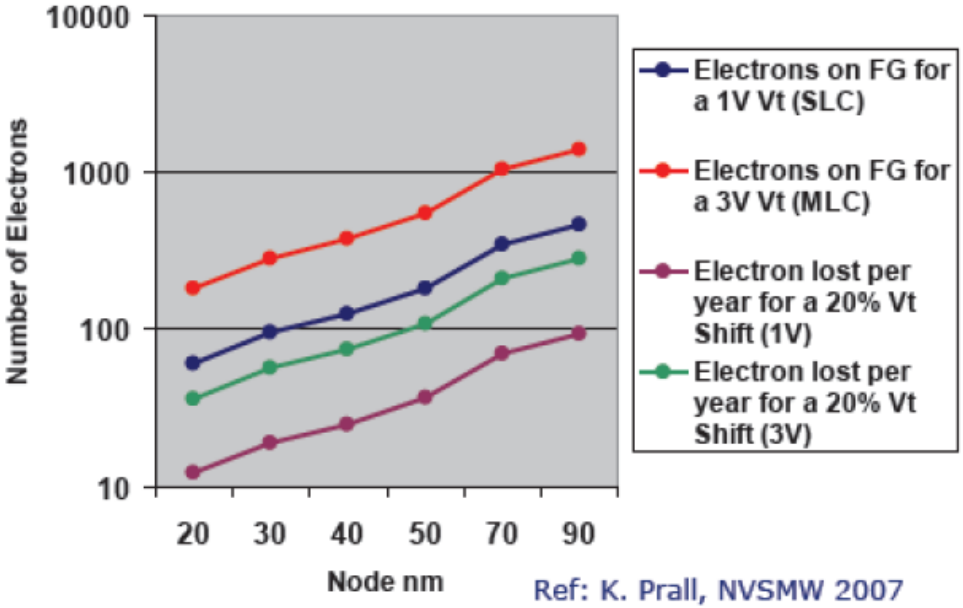

2. 3D flash
   - Vertical poly-Si SONOS




*True vertical NAND string integration (Toshiba, VLSI 2007)*

# FLASH scaling limitations (2)

- Fundamental limitations ?
  - At 20nm, less than 100 electrons are present on the FG for Vt=1
  - If 20% charge loss is the spec, we talk about ~10 electrons…
    → for 10 yrs retention, Ileak<<1e/yr…

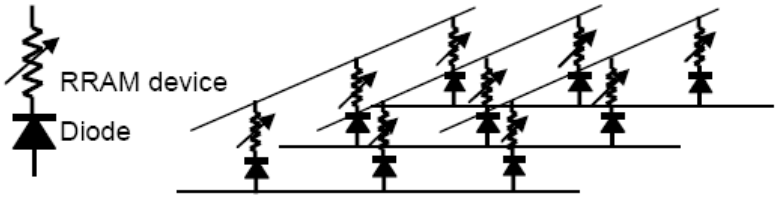


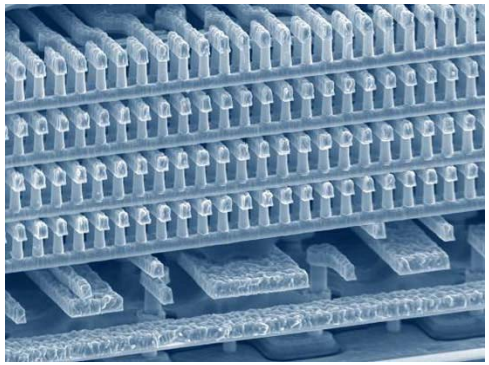

Ref: K. Prall, NVSMW 2007

# Flash scaling solutions : (2) Revolutionary

- Resistive RAM ?

- Requirements:
  - Small cell size
    - $4F^2$ : only for 1D-1R cell configuration
    - Requires unipolar switching
  - Scalability
    - Not limited by minimum charge
    - Limitations of RRAM operation principle ?
    - Scaling of program current ?
  - MLC and/or easy 3-D stacking
    - Relatively easy to write in different R-states
      - But control/distributions & retention questionable
    - 3D stacking critical on selector device
      - Non-1Xtal Si:
        - » Poly-Si diode
        - » Oxide diode



*3D Matrix*
*Semiconductor International* , 7 Jan. 2005

# Program Current Scaling

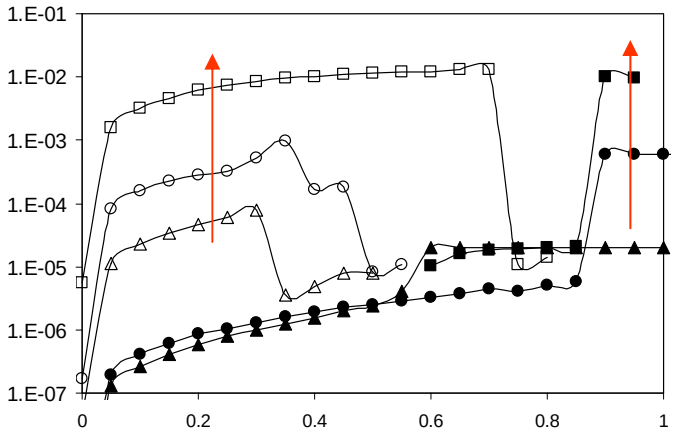
- "simple picture" :

  **$I_{Reset}$ scales 1:1 with compliance current during Set**

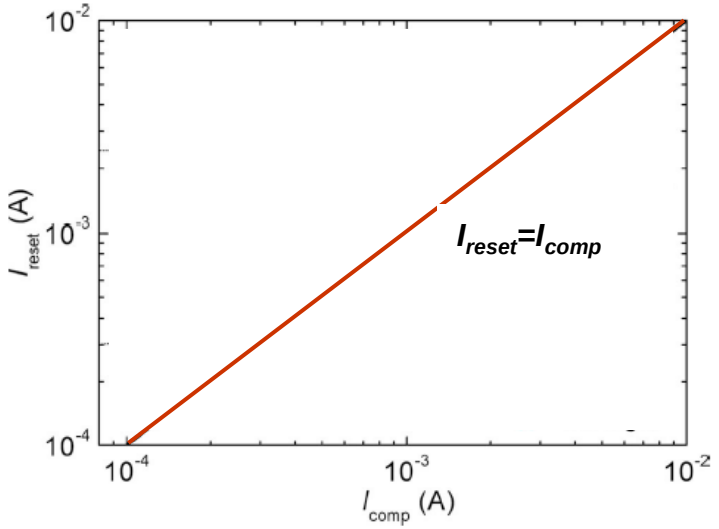
  – *Rational:*

    - Max. current during Set operation determines the "strength/number" of filaments
    - Filament configuration in turn determines the current level for RESET

  – *NOT dependent on cell area*



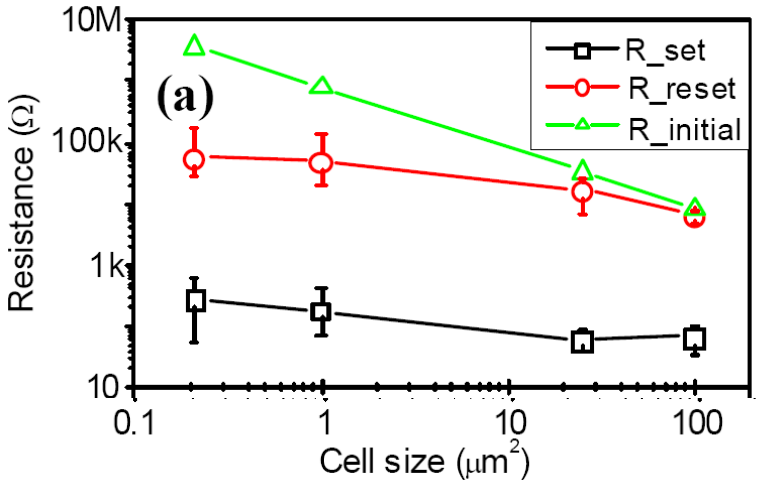

*NiO*
*L.Goux et al, IEEE TED 2009*




*Adapted from K.Kinoshita et al APL 93, 033506, 2008*

# Experimental current scaling

- As a result, typically observed :
  - **No area scaling of ON resistance**



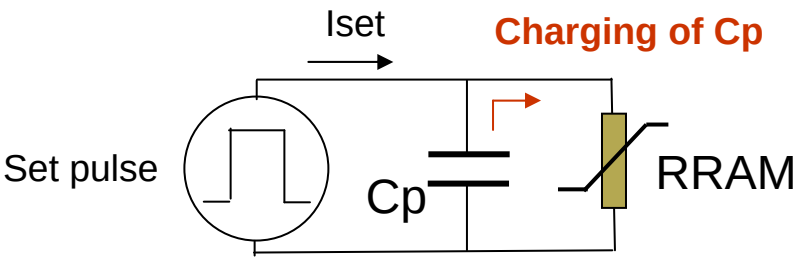

*Baek et al, IEDM 2004*

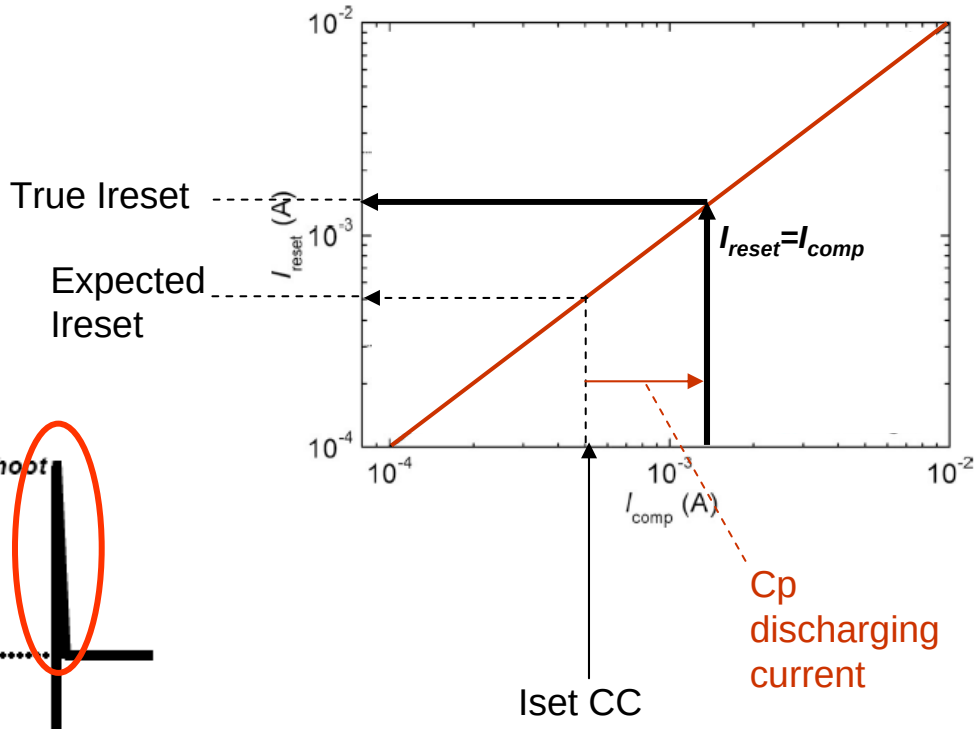
  - **Program current density increases !**

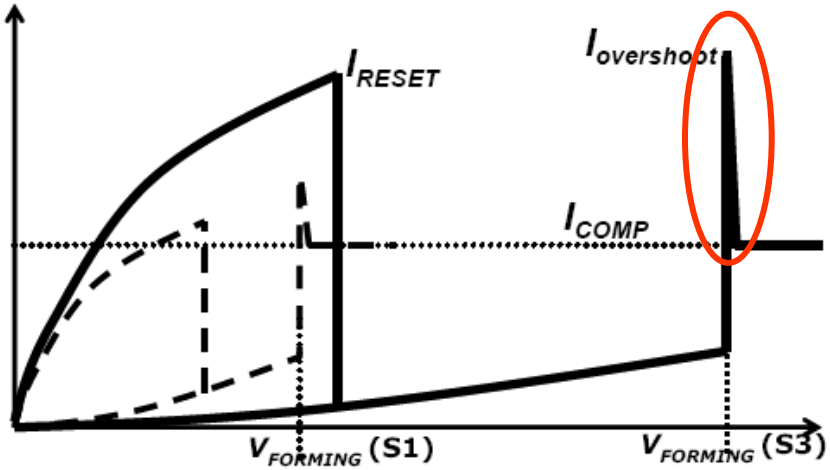
*But, following the current scaling rule, we should be able to lower the program current just by controlling the Set current compliance ??*

# Experimental current scaling

- Explanation : influence of parasitic capacitance on the minimum RESET current




L.Goux et al, IEEE TED 2009 (sept 09)

# Experimental current scaling

- E.g, off vs on-chip measurements

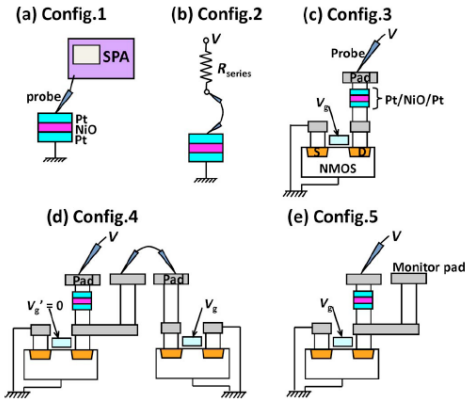
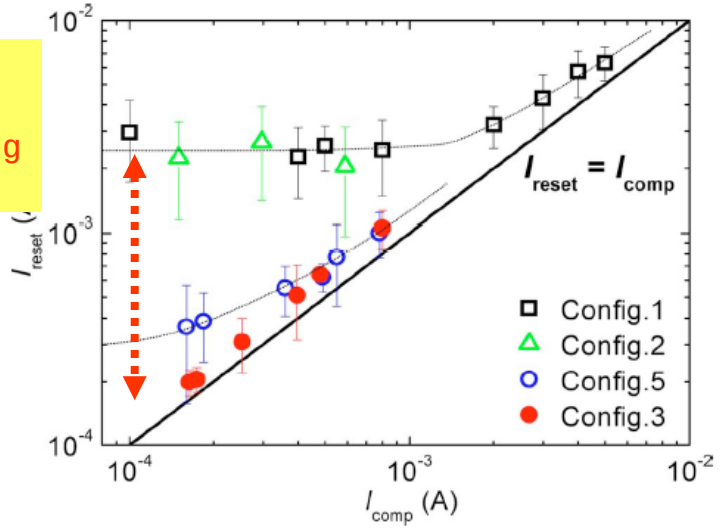



FIG. 1. (Color online) Five configurations used to measure $I_{reset}$-$I_{comp}$ characteristics: The circuit composed by connecting (a) a current limiter built into the SPA and (b) a resistance, respectively, to the Pt/$NiO_x$/Pt structure. (c) The 1T1R cell consisting of the Pt/$NiO_x$/Pt structure and the cell transistor. (d) The circuit composed by connecting the drain of 1T to the Pt/$NiO_x$/Pt structure of the 1T1R cell with the monitor pad via probes and a coaxial line. (e) The 1T1R cell with the monitor pad.

Change from 2mA to 200uA just by improving compliance

*Element size:*
Config 1 and 2: 1um2
Config 3 to 5: 0.5um2




**K. Kinoshita et al.,** APPLIED PHYSICS LETTERS 93, 033506, 2008, "*Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance*"

By controlling the parasitic capacitance, we can reduce program current for a small cell!

# Limitations of current = ?

## Target current :

- Program current < current drive of selector device
  - E.g., @10nm technology node (Area ~100nm2):
  - I reset < 8uA !
  - If VReset ~1V,
    → Ron > 200kOhm

•1Xtal Si diode :
(Samsung, IEDM06)
>20MA/cm$^2$
•Poly-Si p-n diode,
(Hitachi VLSI 09)
~8MA/cm$^2$

**Poly-Si diode**

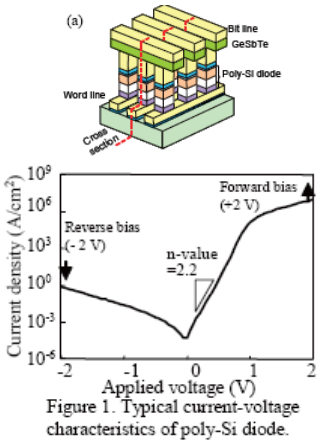


Figure 1. Typical current-voltage characteristics of poly-Si diode.

Y.Sasago et al, VLSI Tech.Symp. 2009

- Minimum read current
  - If I reset 8uA
  - Vread ~ 0.2V (1/5$^{th}$ of $V_{Reset}$)
  - Iread ~1uA only: close to limit of Sense Amplifier !

Current drive of selector device = critical factor !

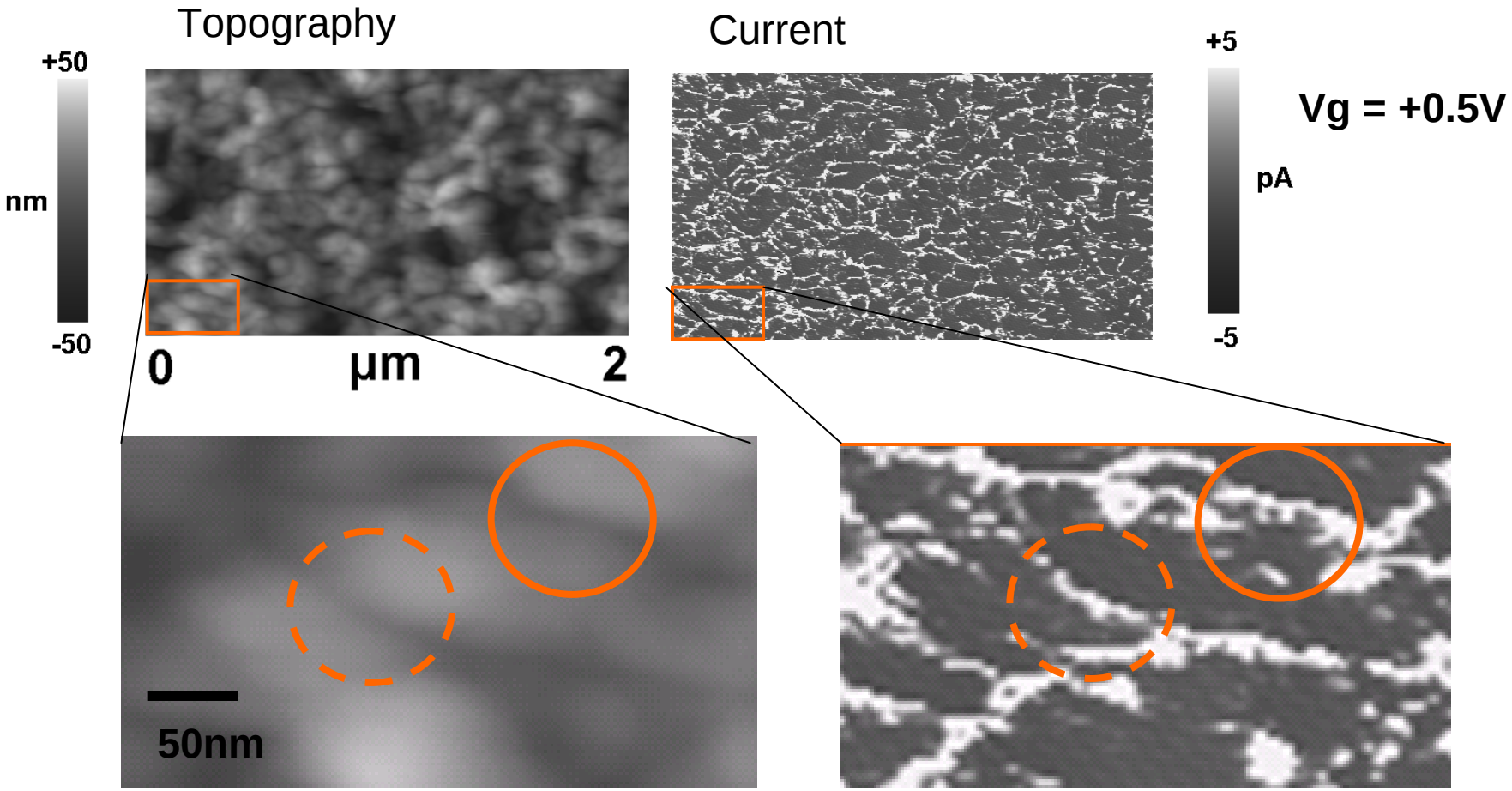
# Fundamental limitations of OxRRAM

- Due to filamentary nature:
  - Size/current of minimum filament (1-10nm?)
  - If nucleation is defect controlled (e.g. GB):
    - Statistical spread in small cells f(defect density)
    - Amorphous MOx could be preferred ?
  - ...

# Role of defects in filament formation ?

- C-AFM results in NiO

  Very non-uniform leakage distribution.
  Regions of high current are mostly situated at the grain boundaries



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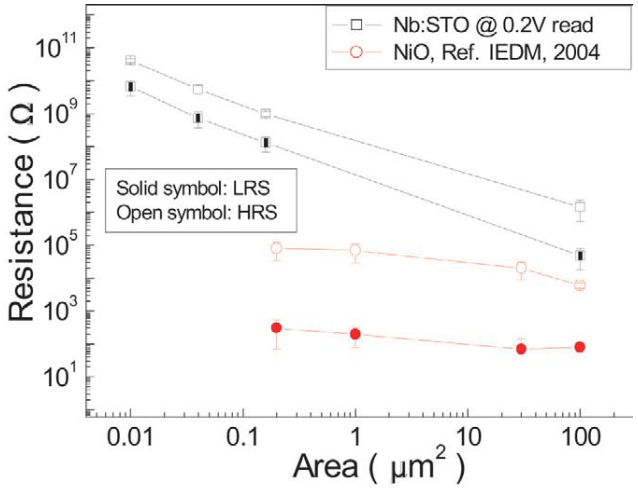
- Interfacial mechanism better for scalability ?




A.Sawa,
Materials Today, Vol11(6), 2008, p. 28

  - But bipolar programming maybe issue…

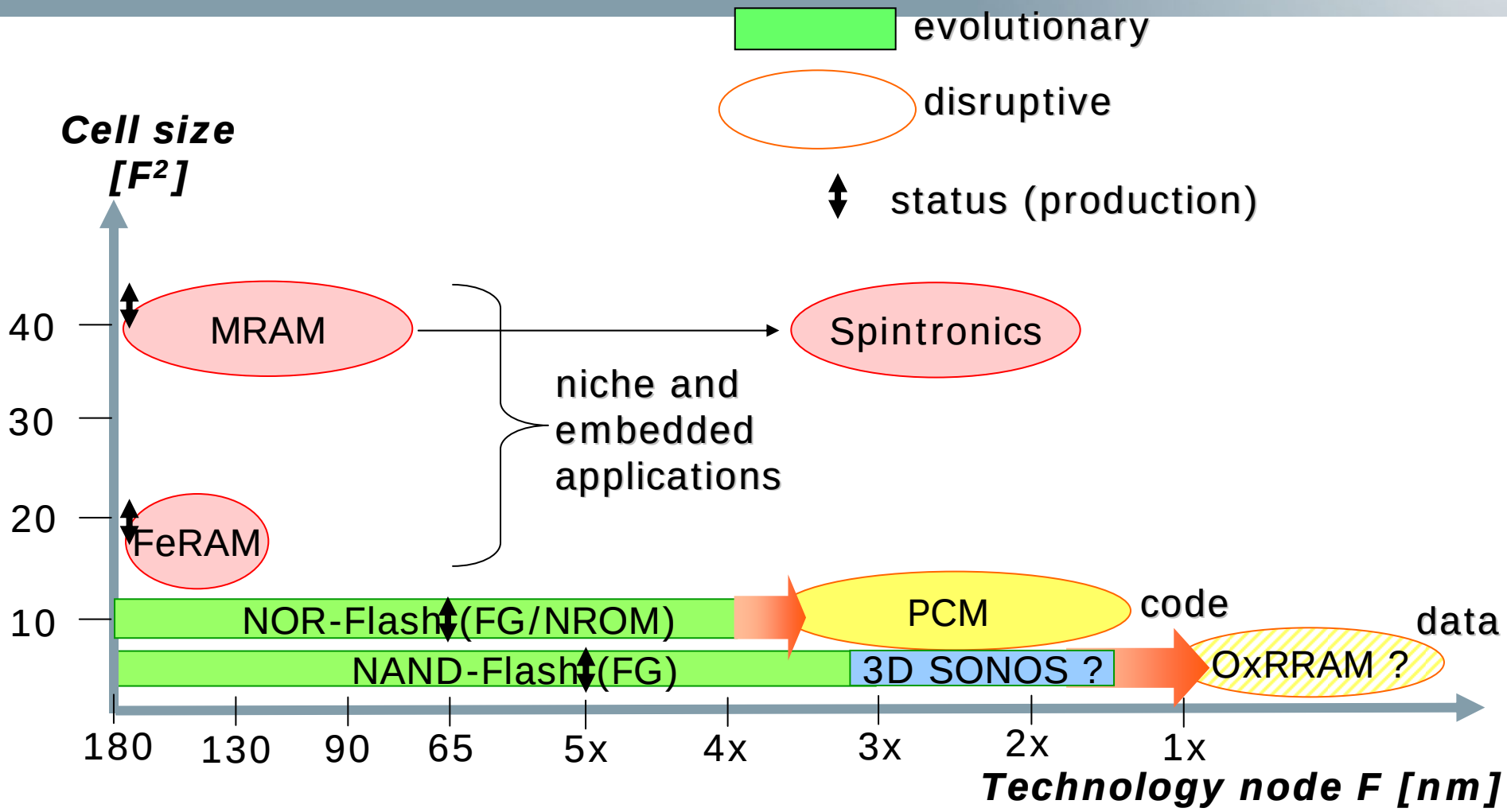
# Outline

- Introduction
- What is a resistive switching device (concept)
  - Focus on unipolar switching RRAM
- Short History of switching in oxide films for memory application
  - Revival of on old idea
- Mechanisms of resistive switching in oxides
  - Unipolar (vs. bipolar) switching in TMO's
- Scaled OxRRAM for FLASH memory replacement?
  - Scaling prospects of RRAM
- Conclusions

# Conclusions

- Unipolar switching in TMO (OxRRAM) is an interesting alternative for scaled NVM
- Models for switching mechanism exist, but need refinement (e.g. to include effects of low-power programming)
- Links with bipolar switching in same material my elucidate switching mechanics (role of vacancies)
- From current extrapolation, scalability is expected to ~10nm node
- Still lack of statistical data, and fundamental scaling limits unclear

# NVM Roadmap




*notes: PCM may be applied in embedded applications as well (65nm)*

# Time for change?

"Nothing is going to change unless something starts to break"
*H.-S. Philip Wong, 2003.11.10, IWFIPT*

***But what needs to breakdown ?***

**Breakdown of Flash scaling**

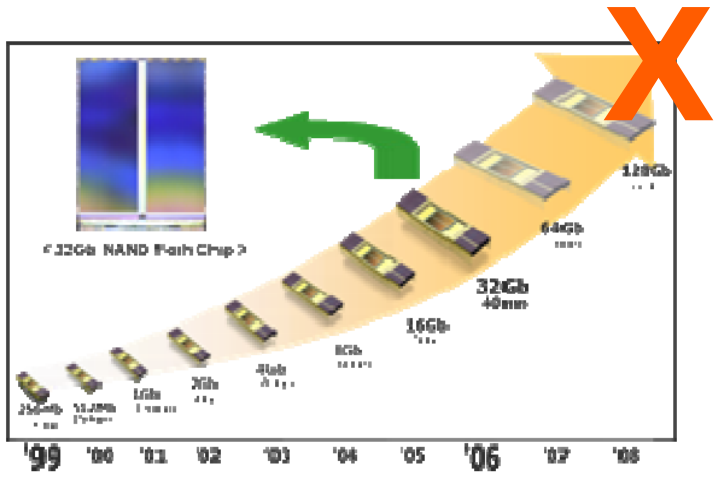



Fig. 2: Doubling phenomena of memory density every 12 months, supporting a new memory-growth model proposed by the author

C-G Hwang, Samsung
IEDM 2006

**Controlled breakdown in OxRRAM**

?

Courtesy of Prof.H.Hwang


# Thank You

Years of Making
Technology Fly