Evolution of Embedded Flash Memory Technology for MCU

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Abstract—**Embedded flash memory technology has undergone tremendous growth of demands with various performance requirements driven by expanded applications of MCU (Micro Controller Unit) products. High temperature operations with highest reliability for auto-motive applications, very low power embedded EEPROM functions for smart-cards, and ultra low-voltage operations for medical applications are driving factors in developing embedded flash technologies. Together with evolving memory cell technology, resolving performance/power trade-offs by developing dedicated design platforms with optimized eFlash technology, memory interface & bus designs, and the whole chip design methodologies, has realized advanced MCU products line-ups by split-gate MONOS flash technology with a wide range of applied products including auto-motive and security applications.**

***Index Terms*—embedded flash memory, split-gate flash memory cell, charge-trapping flash memory cell**

I. INTRODUCTION

Flash-MCU, Micro-Controller Unit with embedded flash memory storage (eFlash), has made a leaping progress in the market acceptance according to the expansion of real-time control applications in 2000's. The programmable code storage by eFlash in place of on-chip mask-ROM has triggered rapid expansion of adaptive control and data stream applications. Together with over-all production and inventory cost reduction, this development has realized an innovation with remarkable cost/value advantage over MCU with fixed ROM or MCU with stand-alone flash memory.

Diversified eFlash technologies for flash-MCU products have challenged new market drivers such as auto- motive, smart-IC card, and medical applications and have expanded the MCU market, while alternately eFlash has become the most successful, largest business in embedded memory technology only second to CMOS-inclusive embedded SRAM. In 1990's Flash-MCU was mainly used in proto-types for debugging systems. With the advancement of Flash-MCU innovation, almost all the MCU market has been focused onto flash-MCU solutions (Fig. 1), where eFlash technology evolution represents the most important factor.

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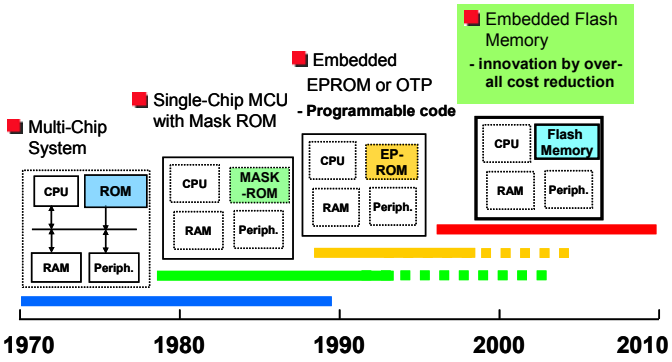

Fig.1. Evolution of MCU products in a memory-centric view.

This paper reviews the past and current status and explore the future directions of eFlash technology for MCU, from the viewpoints of process, circuit, and applications. Innovative factors different from stand-alone flash memory and a future MCU concept in the memory-centric view are also presented.

II. EVOLUTION OF EMBEDDED FLASH TECHNOLOGY

In the flash memory technology tree in Fig. 2, those suitable for embedded uses have been quite selective because of requirements specific to embedded uses. Because high-density flash technologies for stand-alone data memory don't meet the requirements for embedded uses in reliability and performance, eFlash technologies have evolved on its own.

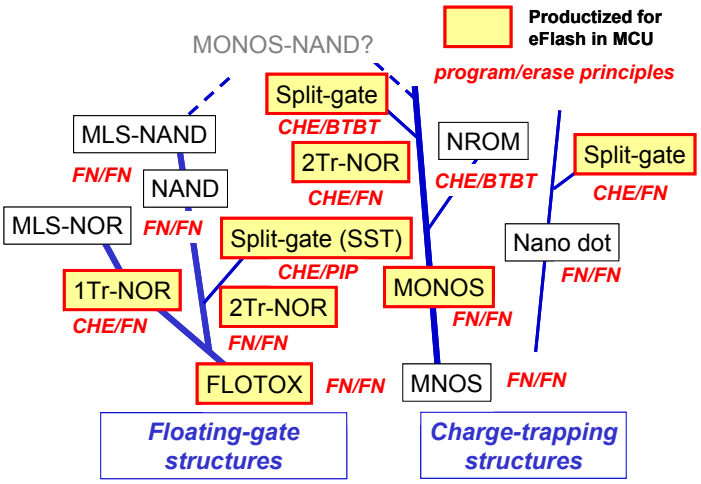

Fig.2. Evolution of Flash and eFlash memory technologies.

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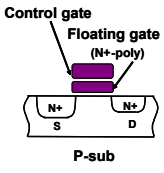
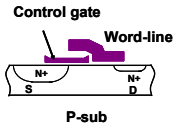
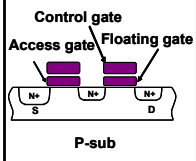
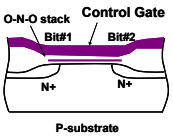
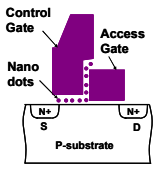
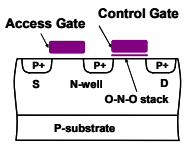
Type	1Tr NOR cell	1.5Tr cell (SuperFlash™)[1]	2Tr cell	1Tr SONOS (NROM™) [2]	1.5Tr Nano-dot [3]	2Tr SONOS (PMOS) [4]
Program	CHE	SSI	FN	CHE	SSI	CHE
Erase	FN (poly-sub)	FN (poly-poly)	FN (poly-sub)	HH	FN	FN
Device structure						
Advantage	High density	Fast program	Low power P/E	2bits/cell	Fast, low-power program	Low power P/E

Fig.3. Embedded flash memory technologies. 1Tr-NOR cells for high density are giving way to 1.5Tr/2Tr cell for performance. Charge-trapping cells are emerging in some applications for reliability.

Two technology transitions specific to eFlash technologies have been remarkable (Fig.3):

(1) 1T cell to 1.5T (split-gate structure) and 2T cells for high-performance/low power, and

(2) Discrete charge-trapping cell technology (MONOS and Nano-dot[5]) for higher reliability.

These trends prove a deviation from the standardized stand-alone flash memory products such as NAND-flash memories. Although the conventional floating- gate NOR structure will survive in some of the high-density embedded uses, pervasive use of split-gate and charge-trapping storage structures are expected according to the requirements by diversified MCU market segments.

Considering the structural compatibility of the split-gate with advanced underlying CMOS logic transistor, Access- Gate first (Control-Gate last), which is only realized by a thin-film charge-trapping storage layer, not by stacked floating gate structure, is preferred. This may indicate that the technological convergence point lies in the split-gate, charge-trapping cell structure in the future. The advantage of this choice has been proved by the implementation in the CMOS logic platforms at 90nm [6],[7].

III. STATE-OF-THE-ART MCU DESIGN

In addition to the over-all cost reduction through design, production and inventory control by programmability in Flash-MCU, the "embedded-ness" is favorably utilized for high performance and data security properties. The advantages and possible drawbacks of embedded flash memory are listed in Table.1. Product design should consider utilizing embedded flash properties with the overall cost and value advantages over- coming drawbacks of higher wafer process cost to incorporate flash memory. In general much diversified MCU product line-ups are efficiently supported only by a unified design platform to employ optimized eFlash macros.

By scaling the device and by circuit developments, a steady scaling trend has been realized in the auto-motive applications of MCUs (Figs.4 and 5), with x20 CPU performance growth by 10 years and x8 ROM capacity growth by 10 years. The techno- logy node development for MCU is not so aggressive as most- advanced SOCs because of the smaller system on the chip and somewhat tailored technology for required higher temperature operations.

Advantages of embedded flash memory:

- **By internal access path,**
  - **(1) Fast, low-power**
  - **(2) High data security**
  - **(3) High-reliability, low EMI, low system cost**
  - **(4) Higher design freedom**
    memory capacity, interface, designed functions, and operating voltage.
- **By low activation rate, act as thermal cooler.**
- **Contributes to optimization of LSI functions and cost.**

Possible drawbacks in embedded flash memory:

- **(1) Higher cost in large and small capacity of memory (owing to low density, higher process cost)**
- **(2) Cost by non-standardization**
- **(3) Single source**
- **(4) Difficult in integrating multiple types of memory.**

Table 1. Advantages and possible drawbacks of embedded flash memory, as compared with stand-alone flash memory.

Example requirements to current state-of-the-art MCU designs are shown in Table.2. Because eFlash in MCU is inherently required a high-speed access to meet the CPU execution speed, performance-oriented design is required in many applications, which is quite different from stand-alone flash memory products. Also data reliability as well as high-temperature and low-leakage product strategy are important factors in most of MCU applications.

Requirements here describe the natures of current MCU market segments as well as eFlash specifications.

(1) Auto-motive applications such as power-train require high-density, high-temperature and highly reliable eFlash designs. A random access as fast as 10ns at 160□(max) in eFlash is achieved by the current state-of-the-art design with

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hierarchical sensing, optimized memory mat division, and highly reliable memory cell technology to fit this application.

(2) Security functions against attacks account for a large portion of the MCU design for smart-IC card applications. Embedded EEPROM for data manipulation functions with quite fast and low-power program/erase operation is essential in non-contact smart-cards, which makes this field of application very selective in the choice of eFlash technologies.

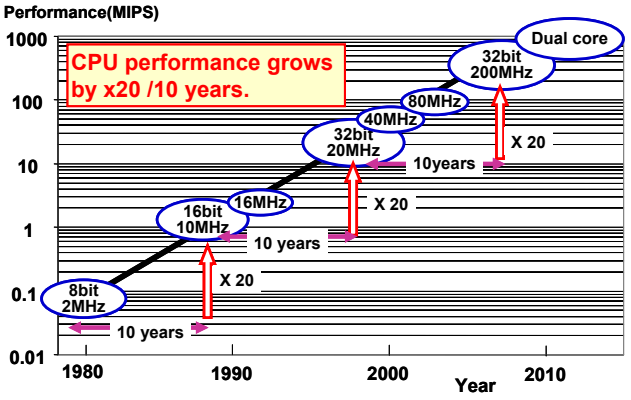

Fig.4. Performance trend in CPU and eFlash for high-end auto-motive market.

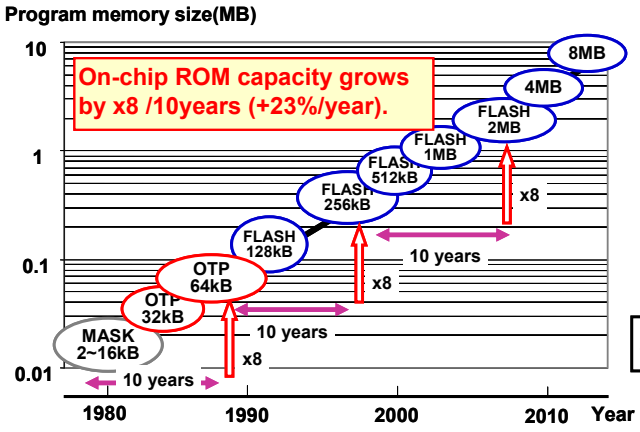

Fig.5. Trend in eFlash capacity for high-end auto-motive market.

		Automotive			Industry	PC/OA	Consumer	Smart-card	Medical
		Power Train	Body	Air-bag					
MCU	Performance (frequency)	~300MHz	150~200MHz	100MHz	~300MHz	25~50MHz	20~100MHz	15~50MHz	1~10MHz
MCU	Power	0.5mA /MHz	0.5mA /MHz	0.25mA /MHz	1mA /MHz	0.5mA /MHz	0.25mA /MHz	0.2mA /MHz	0.1mA /MHz
MCU	Temp.(Ta)	- 40 ~ 125 C			max 85 C	- 20 ~ 85 C			
FLASH	Density	8MB	2MB	2MB	1MB	2MB	1MB	512KB	256KB
FLASH	P/E cycle	Code : 1K-10K cyc. / Data : 100K cyc.(EEPROM)						-500K (EEPROM)	100K (EEPROM)
FLASH	Small Cell	✓							
FLASH	Small Macro			✓		✓	✓	✓	✓
FLASH	Fast Access	✓			✓				

Table.2. Requirements for embedded flash memory in MCU applications.

(3) Very low-voltage/low-power MCU products are required for emerging medical/health-care applications with battery operations. eFlash program/erase is necessary in the future data collection and storage for data streaming operations in the advanced health-care environments.

These sample requirements indicate much diversified MCU product line-ups, suggesting very wide expectations to eFlash performance and functions, much to be explored and exploited in technology/ circuit/system developments.

Fig. 6 depicts key architecture and circuit technologies in eFlash designs. In frequent read operations in the code storage applications, non-boosted word-line utilizing a split-gate cell structure is promising to enhance the random read access speed and for low-power consumptions. Lowe-power design in eFlash is strongly affected by the charge-pumping circuitry in program/ erase operations. Because flash memory technologies have inherent difficulty in scaling down the program/ erase voltage, energy-efficient program/erase algorithms and optimally generated high-voltage waveforms to mitigate excessive power consumption are important in power-aware designs.

Fig. 7 shows a current MCU product line-up employing a split-gate MONOS eFlash technology, with up to 100MHz read access at code storage with 500K program/erase capability in EEPROM on the chip, all under Tj=160□(max). The operating voltage ranges down to 1.62V for battery operations.

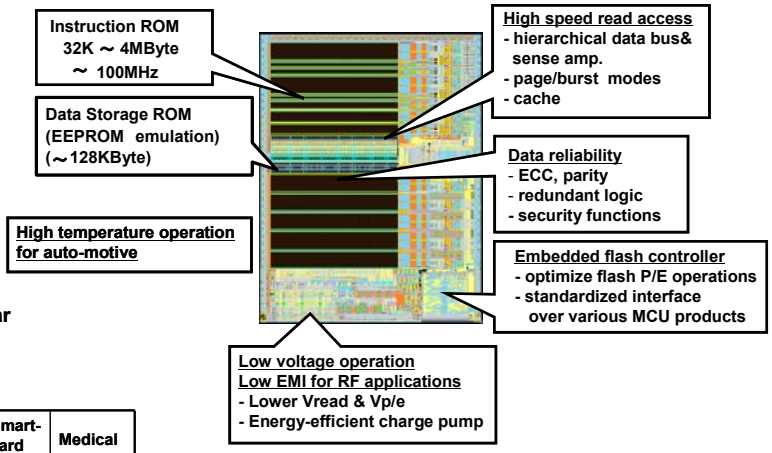

Fig.6. Key considerations in eFlash design [8],[9].

- 90nm CMOS w/i MONOS eFlash
- CPU : 240MHz(max)
- eFlash(split-gate MONOS)
  - Code Flash : 4M Byte(max)
    (freq. =100MHz @ random read)
  - EEPROM : 128K Byte(max)
- RAM:128kB max, A/D:12bit x 37ch etc.
- Applications: auto-motive, industry, consumer, PC/OA, smart-card etc.

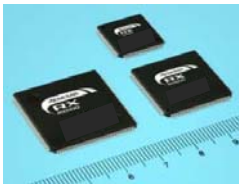

Fig.7. 90nm flash-MCU products.

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IV. IMPACT OF ENERGY-EFFICIENT NV- MEMORY

Energy-efficient system approaches require low-energy frequent re-write performance of non-volatile memories. As the stand-by leakage problem has emerged as a critical factor in the advanced LSI systems, embedded non-volatile memory will play more important roles in reducing the system power by intermittent power switching schemes (Fig. 8), to frequently switch idling states into power-off states. Frequent power On/Off necessitates frequent non-volatile store and retrieval of circuits states and data. Fast and energy-efficient re-write is required for non-volatile memories in this context.

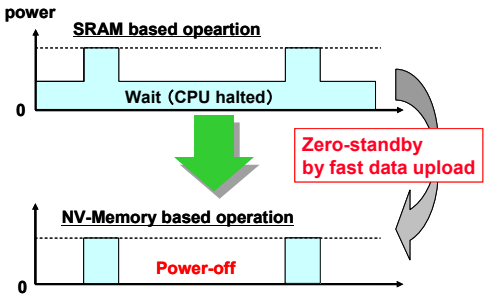

Fig. 8. Intermittent system operations with normally off schemes.

Fig. 9 describes re-write speed and energy in various eFlash technologies compared with Magnetic-RAM. Because system requirements are diverse in power control schemes, all the current eFlash and next-generation NV-memories are good for uses in intermittent power control applications. However, efficient power-down schemes will store and retrieve circuit states instantly, favoring distributed fast non-volatile storage on the chip. One remarkable feature realized by emerging NV memory is orders-of-magnitude lower energy per bit re-write than existing eFlash by fast and low-voltage re-write capabilities (Fig. 10), which can be exploited effectively [10].

Programmability provided on the chip has been an important factor in the design and cost structure of LSI (Table 3). Beginning with the ROM-based logic operated by stored instructions in the CPU, alterable/reconfigurable logic organizations have emerged in the 2nd stage, where the main players are Flash-MCU and re-configurable logic products. The 3-rd stage realized by NV-RAM will see a much broader possibility of innovation by energy-efficient NV memories.

V. CONCLUUSIONS

Flash-MCU has achieved a rapid market penetration attributed to the leap in value/cost for innovation by virtue of evolving eFlash technologies. eFlash cell and circuit technologies will see some convergence points quite different from stand-alone flash memory, according to diversified market requirements. Designs of energy-efficient MCU and of MCU for energy-efficient systems will be the next focus of technology, circuit, and system co-development in emerging applications, where non-volatile memory technologies will play important roles in the scaled LSI environments.

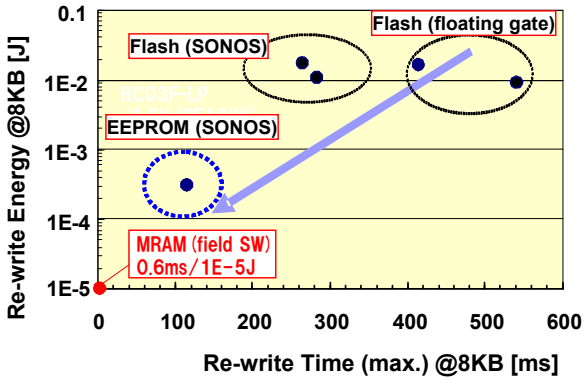

Fig.9. Re-write performance by energy/bit in various eFlash and MRAM. Re-write energy and time by memory cell and periphery circuitry.

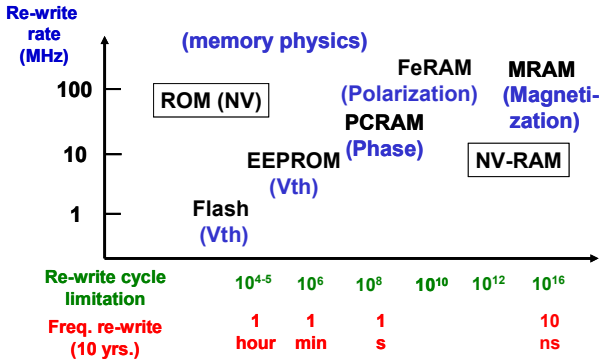

Fig. 10. Re-write performance by non-volatile memories. Re-write frequency requirement ranges over power On/Off schemes in the system.

	Innovation	Main Enabler	Product	Effect
1	Memory-based Logic	ROM Program Register-based comput.	MPU, MCU	Programmable Logic
2	Alterable Logic	SRAM/Flash	Flash-MCU, FPGA	Re-configurable Production, Inventory, Delivery Efficiency
3	Universal Memory	NV-RAM w/i energy-efficient re-write	Unified-Memory/ MCU, SOC	Instant ON Intermittent operation Re-usable logic

Table 3. Evolution of on-chip programmability [9].

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