KATHOLIEKE UNIVERSITEIT LEUVEN

ESAT

Architecture Design

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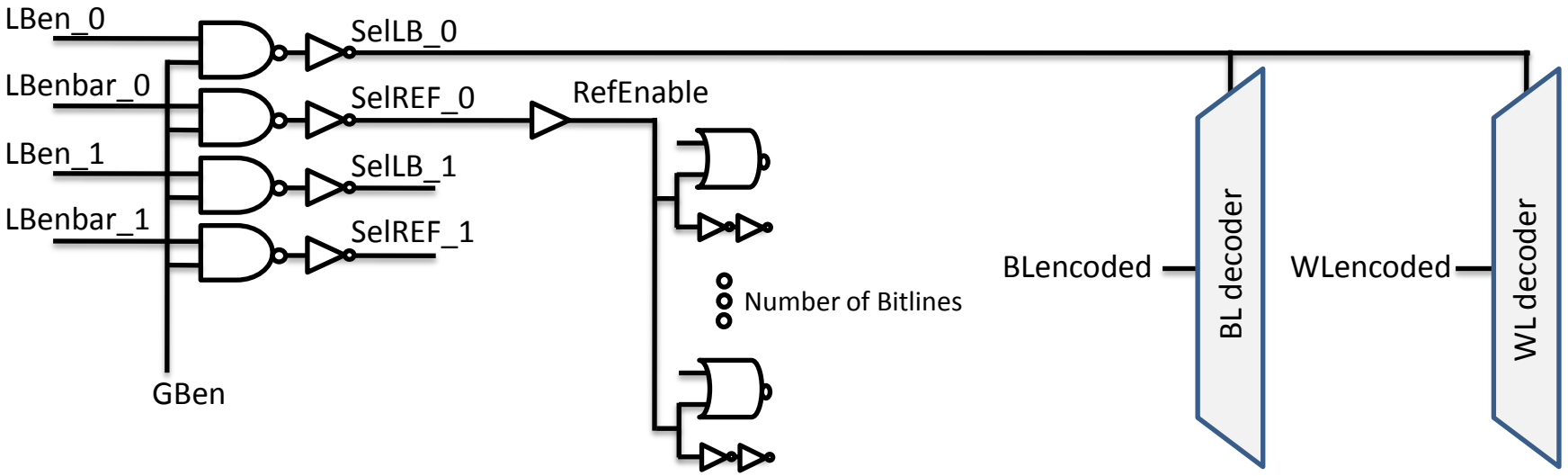
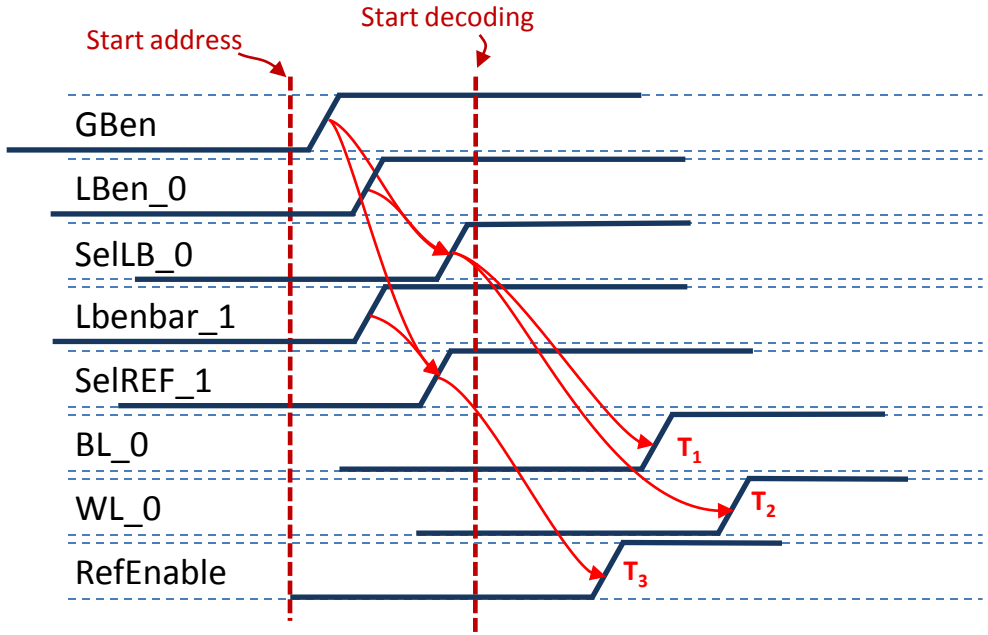
Wouter Diels

OUTLINE

- **ARCHITECTURE AND TIMING**
- **DECODERS**
- **SENSE AMPLIFIERS**
- **LOAD**
- **PLANNING AND CONTENT TABLE**
- **CONCLUSION** : **Conclusion and Future work**

TIMING (I)

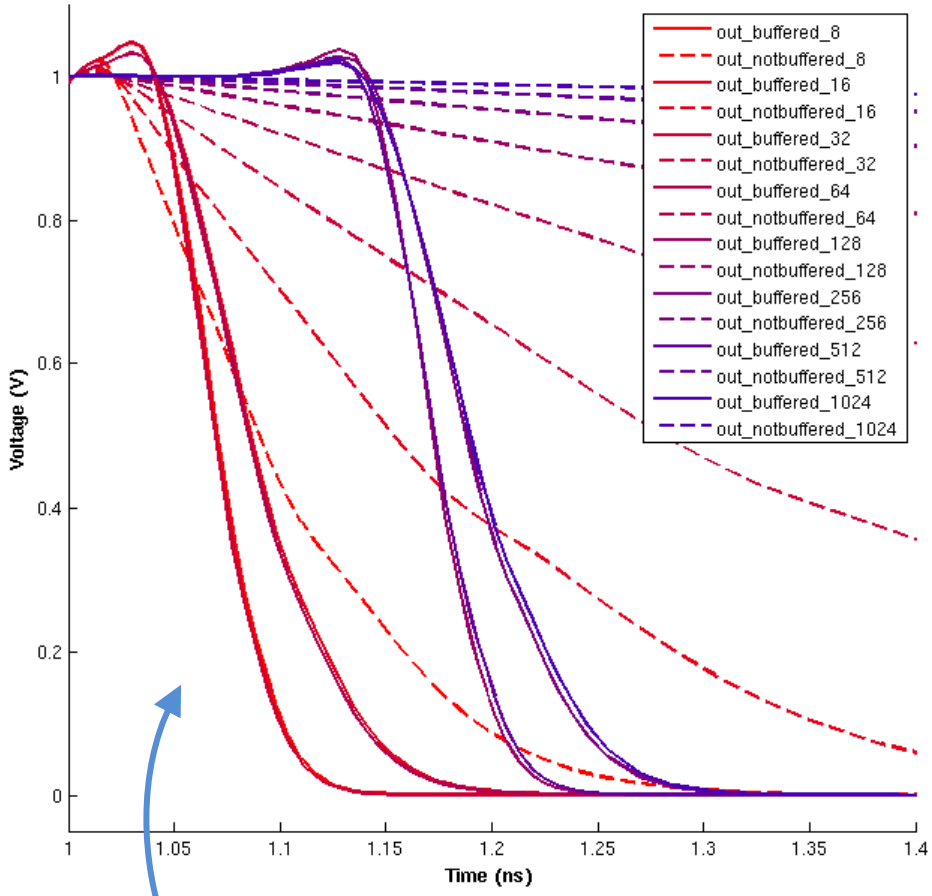


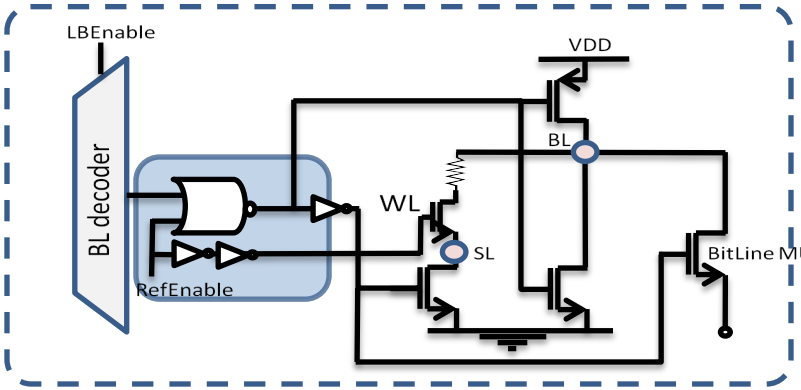


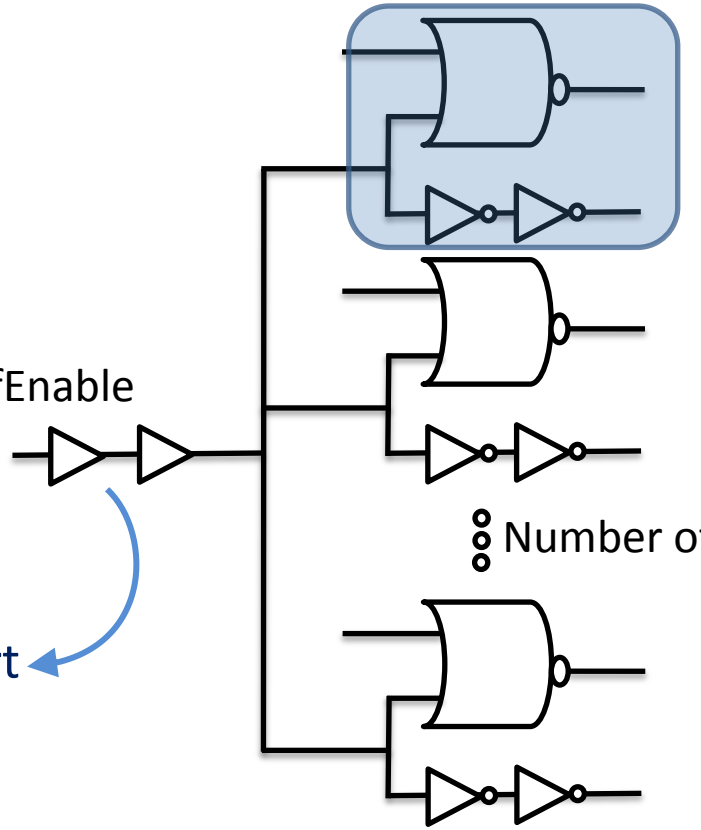
Constraints / Optimization

1. T1 ≈ T2 : cell should be selected when the load is turned on, if not → dead time. (BL and WL decoder same size)
2. T1 ≈ T3 : if T1 > T3 ref is selected before mem → energy waste (Design non optimal ref buffer)

REFERENCE ARRAY: Buffers

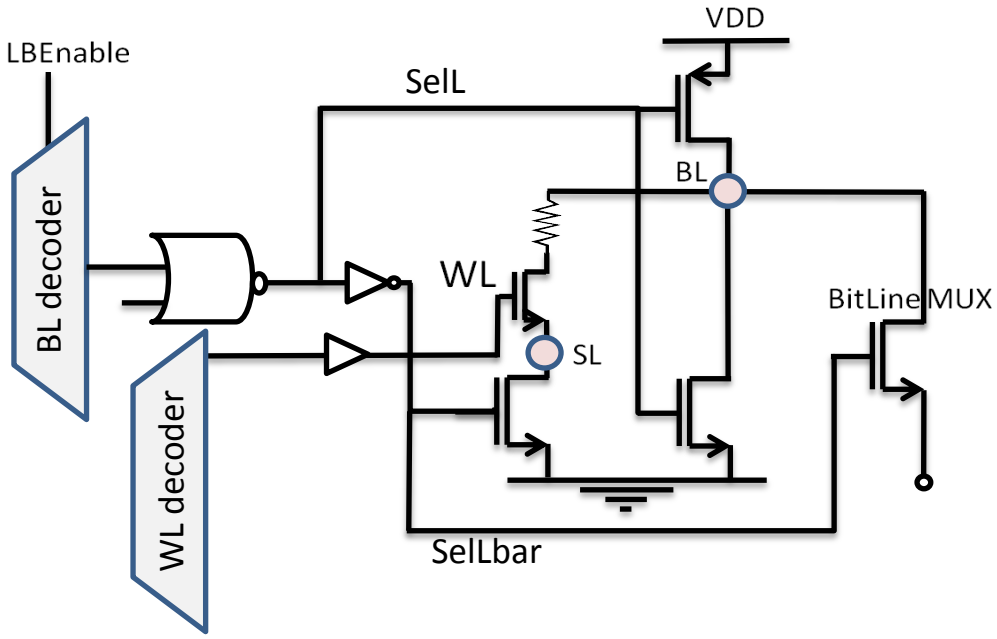


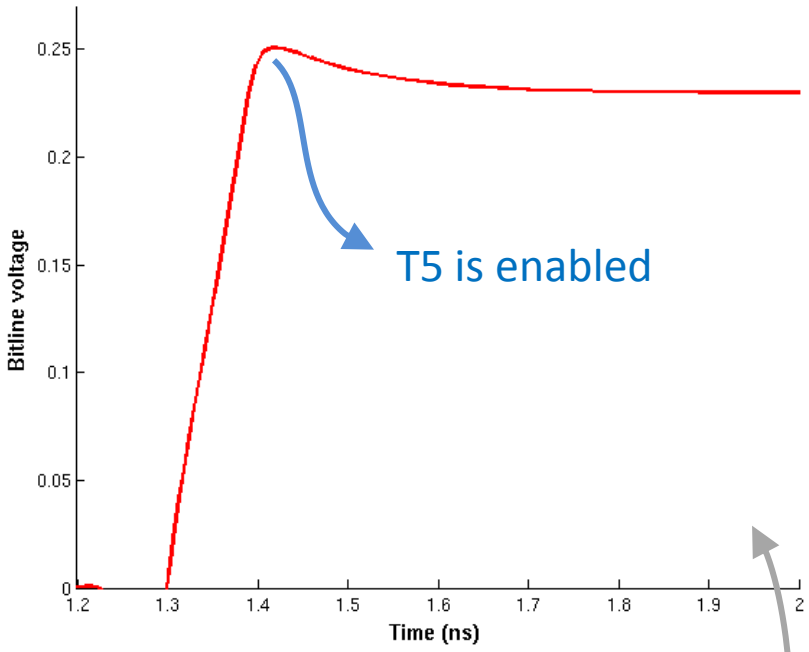


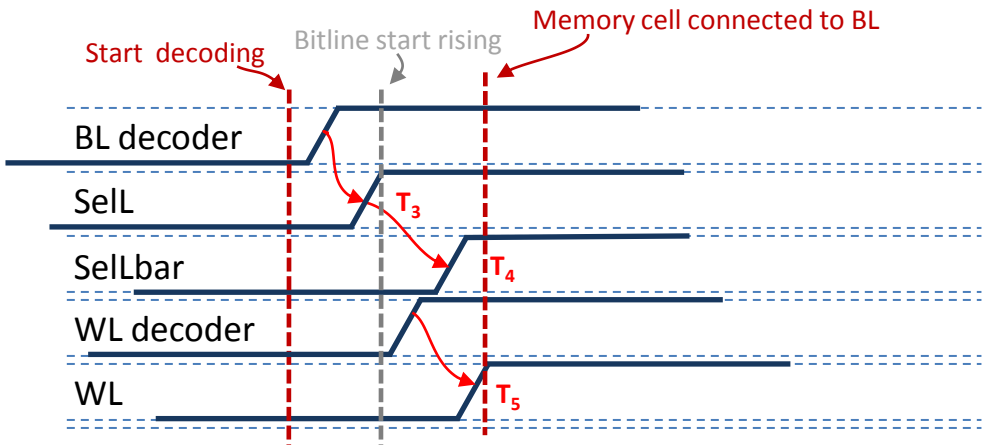


Buffer designed with logical effort
(stage effort = 4)

TIMING (2)



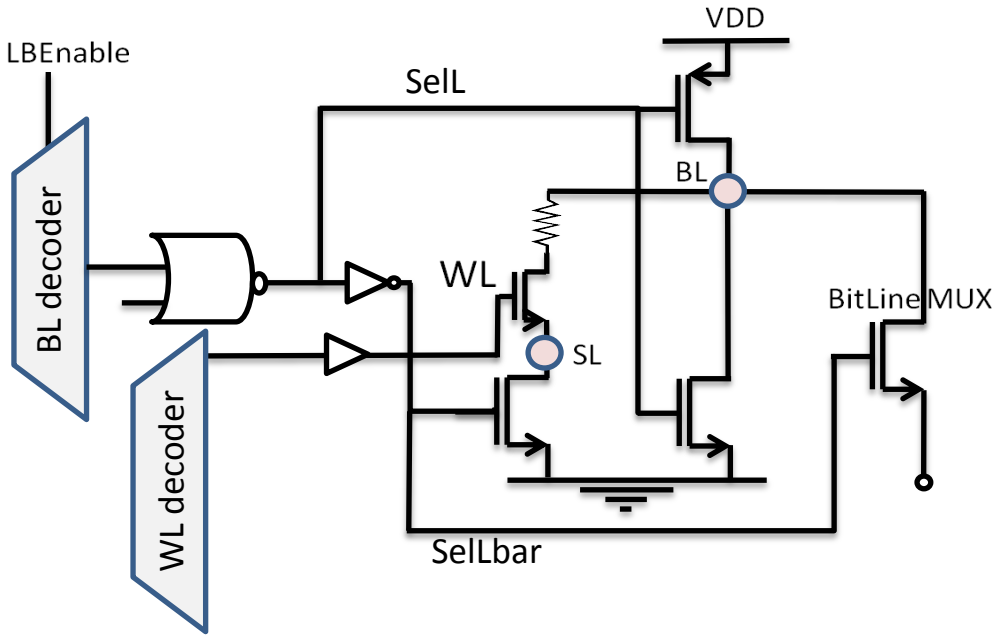


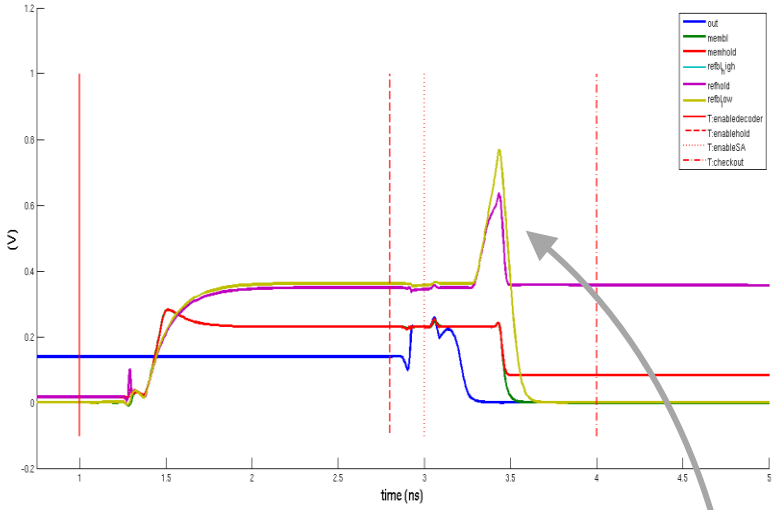


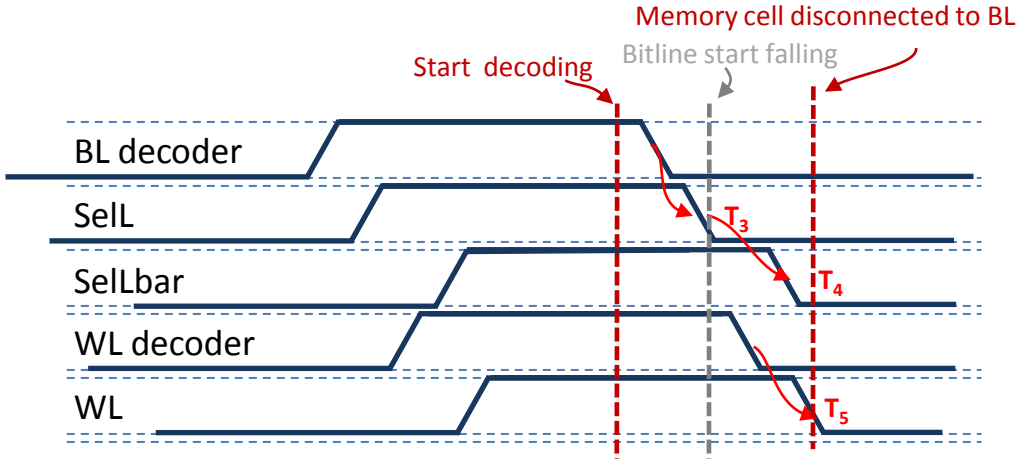
Constraints / Optimization

3. cell should be selected when load is turned on → $T_3 \approx T_4 \approx T_5$. $T_3 < T_4$ because of inverter. T_5 is dependent of size of BL and WL decoders. When $T_3 < T_4, T_5$ the bitline is rising without cell selected

TIMING (3)



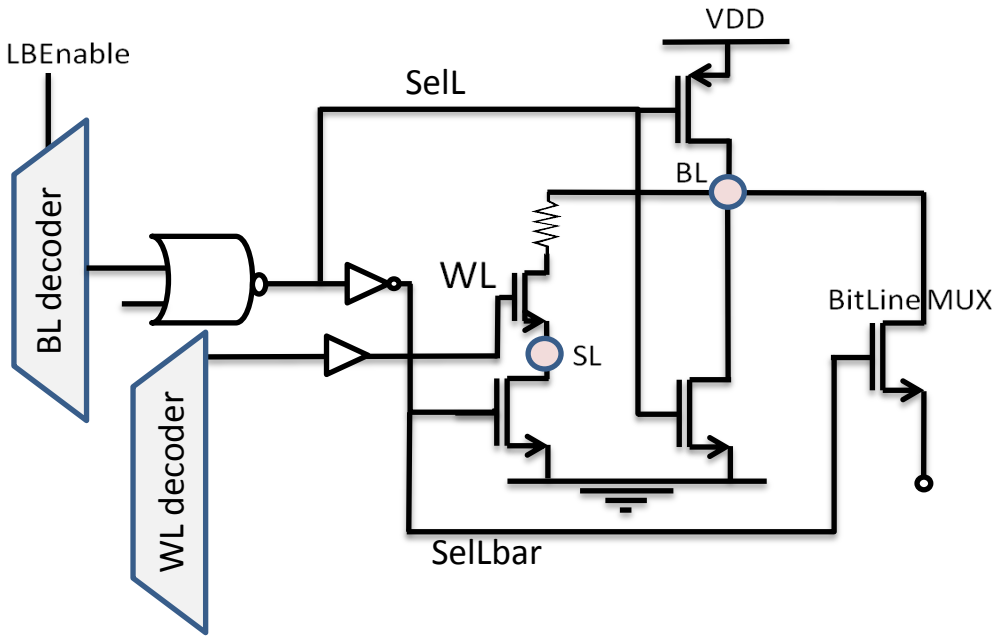


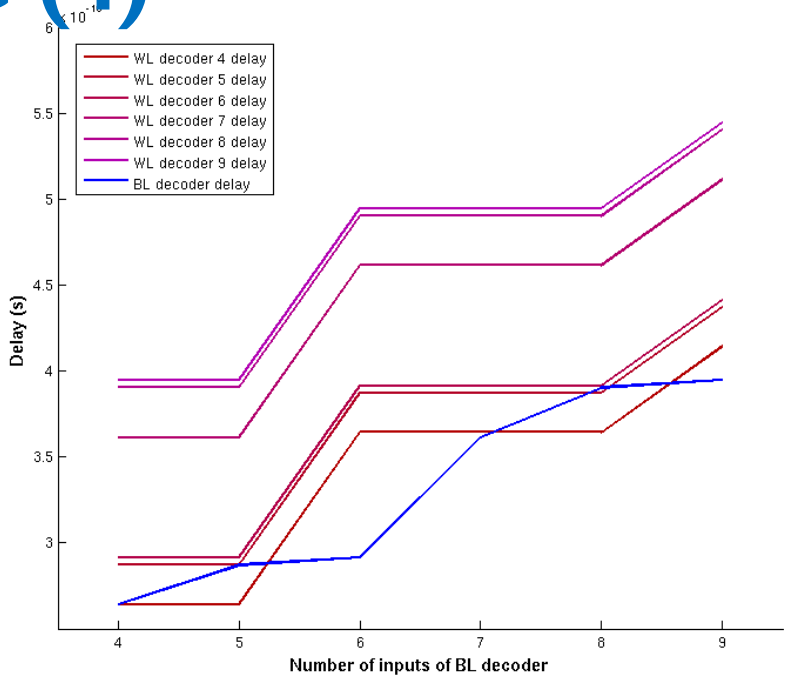


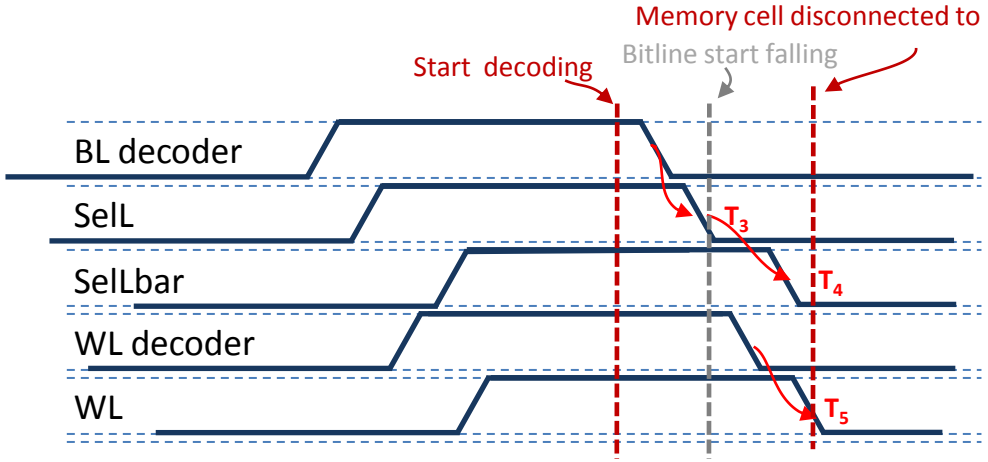
Constraints / Optimization

4. cell should be deselected when load is turned off → $T_3 \approx T_4 \approx T_5$. $T_3 < T_4$ because of inverter. T_5 is dependent of size of BL and WL decoders. When $T_3 > T_5$ the bitline is rising without cell selected

TIMING (4)



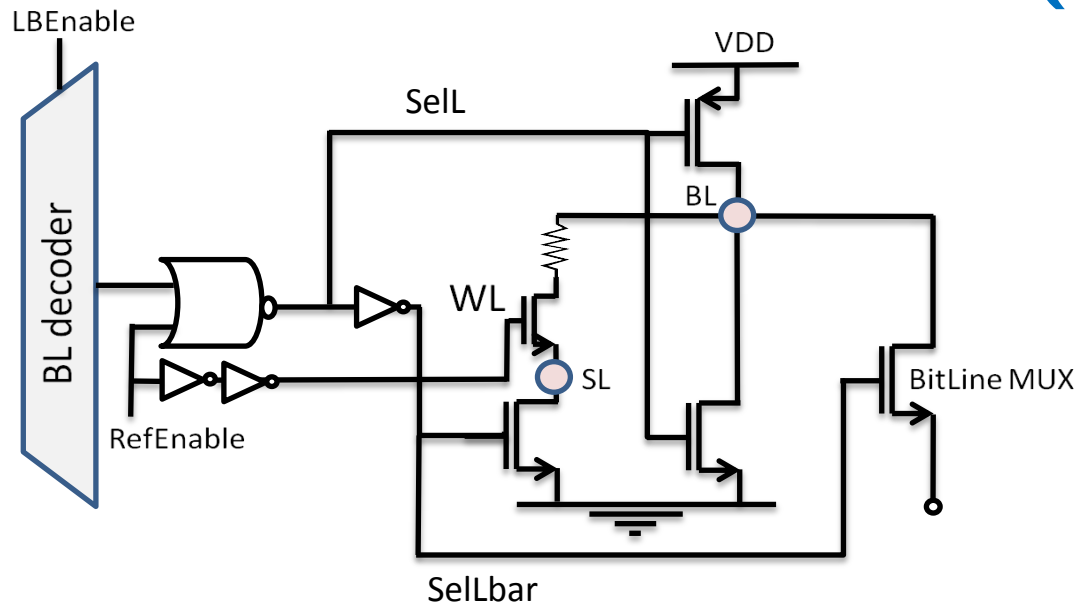


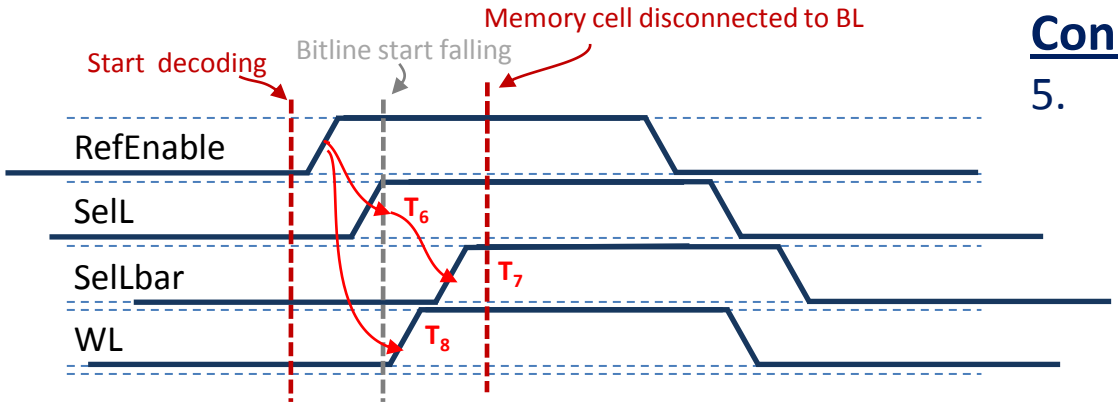


Constraints / Optimization

4. cell should be deselected when load is turned off → $T_3 \approx T_4 \approx T_5$. $T_3 < T_4$ because of inverter. T_5 is dependent of size of BL and WL decoders. When $T_3 > T_5$ the bitline is rising without cell selected

TIMING (5)

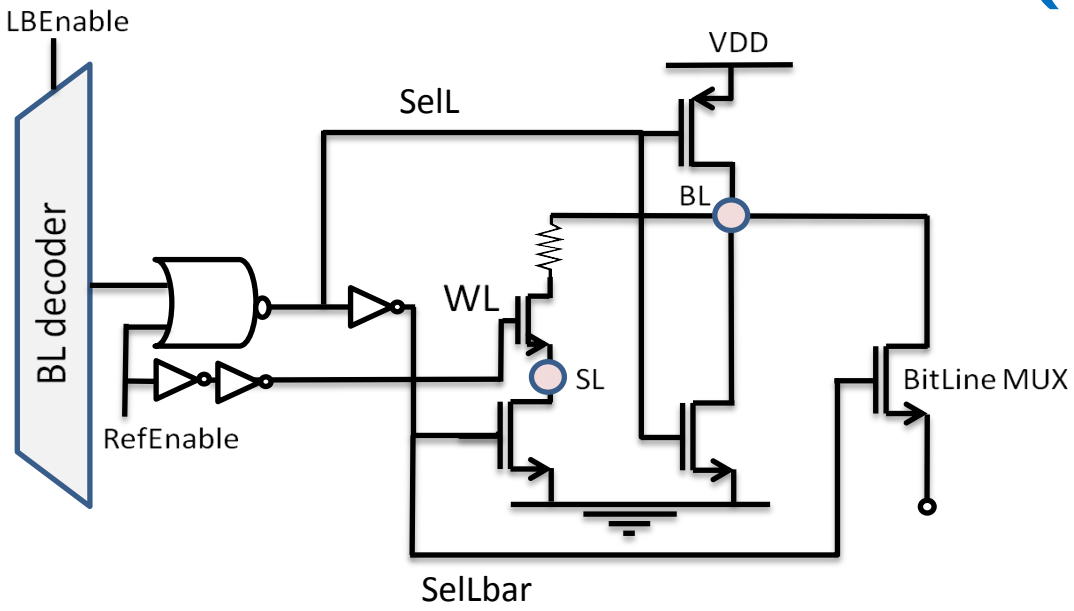


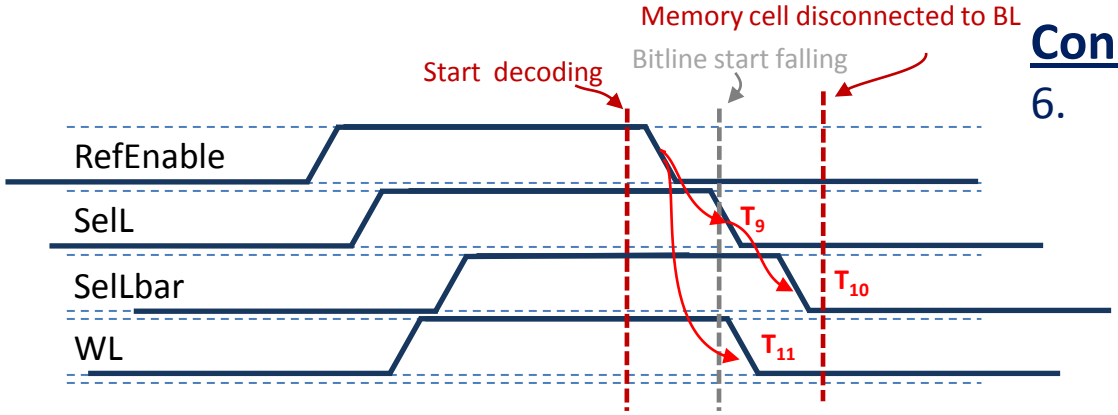


Constraints / Optimization

5. ref should be selected when load is turned on → $T_6 \approx T_7 \approx T_8$. $T_6 < T_7$ because of inverter. T_8 is dependent of delay element (2 inverters)

TIMING (6)





Constraints / Optimization

6. ref should be selected when load is turned off → $T_9 \approx T_{10} \approx T_{11}$. $T_9 < T_{10}$ because of inverter. T_{11} is dependent of 2 inverters

TIMING (7)

	Affects	Implies
(1)	Speed	#WL ≈ #BL
(2)	Energy	/
(3)	Speed	#WL < #BL
(4)	Clean signals	#WL > #BL
(5)	Speed	$T_{delay} < T_{nor +inv}$
(6)	Clean signals	$T_{delay} > T_{nor +inv}$

Could try to extend ref delay to compensate energy wast in bitlines but time is to short
→ Don't connect all the ref cells to bitline

ADDRESSING

Use not fully coded address (number of bits = 24??)

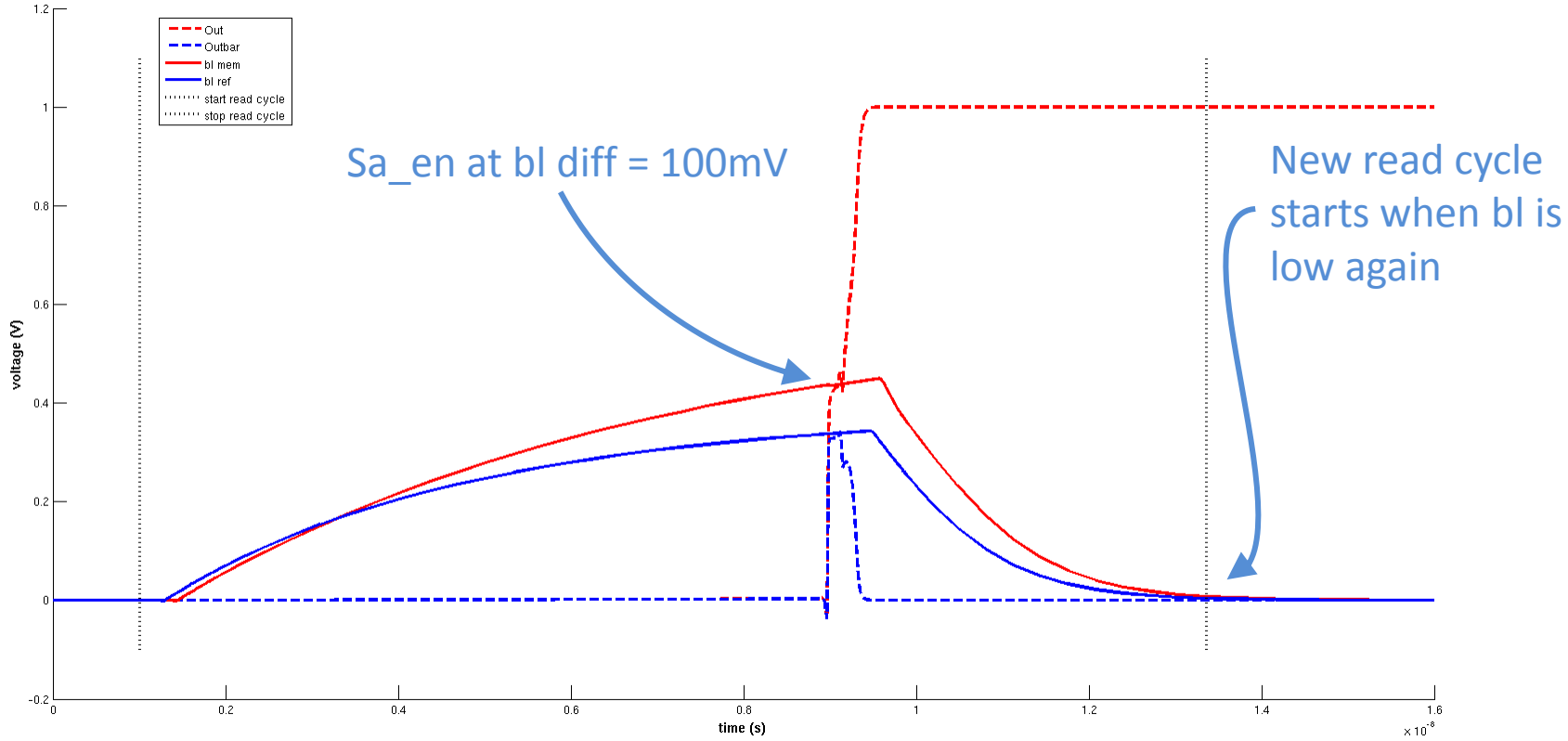
address_GB	select_LB0	select_LB1	address_BL	address_WL

Consider address bit voltage to come from ideal voltage source

ARCHITECTURE (I)

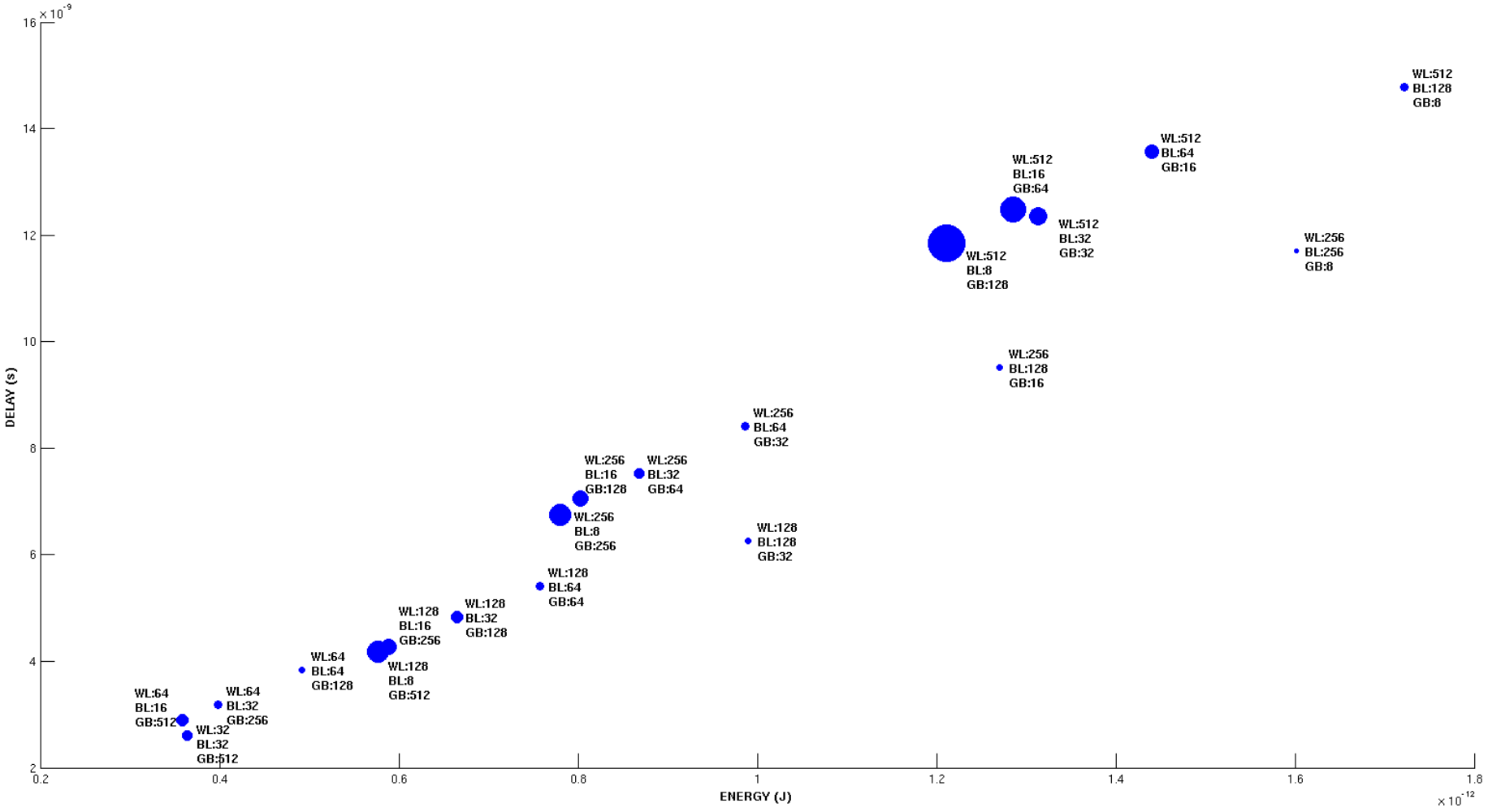
- Find all possible solutions for #WL, #BL, #GB in the range 2^{3-9}
- That comply to the following constraints:
  - # cells = 4194304 (4MB)
  - # BL ≤ #WL
- Simulate as follows:

20 solutions



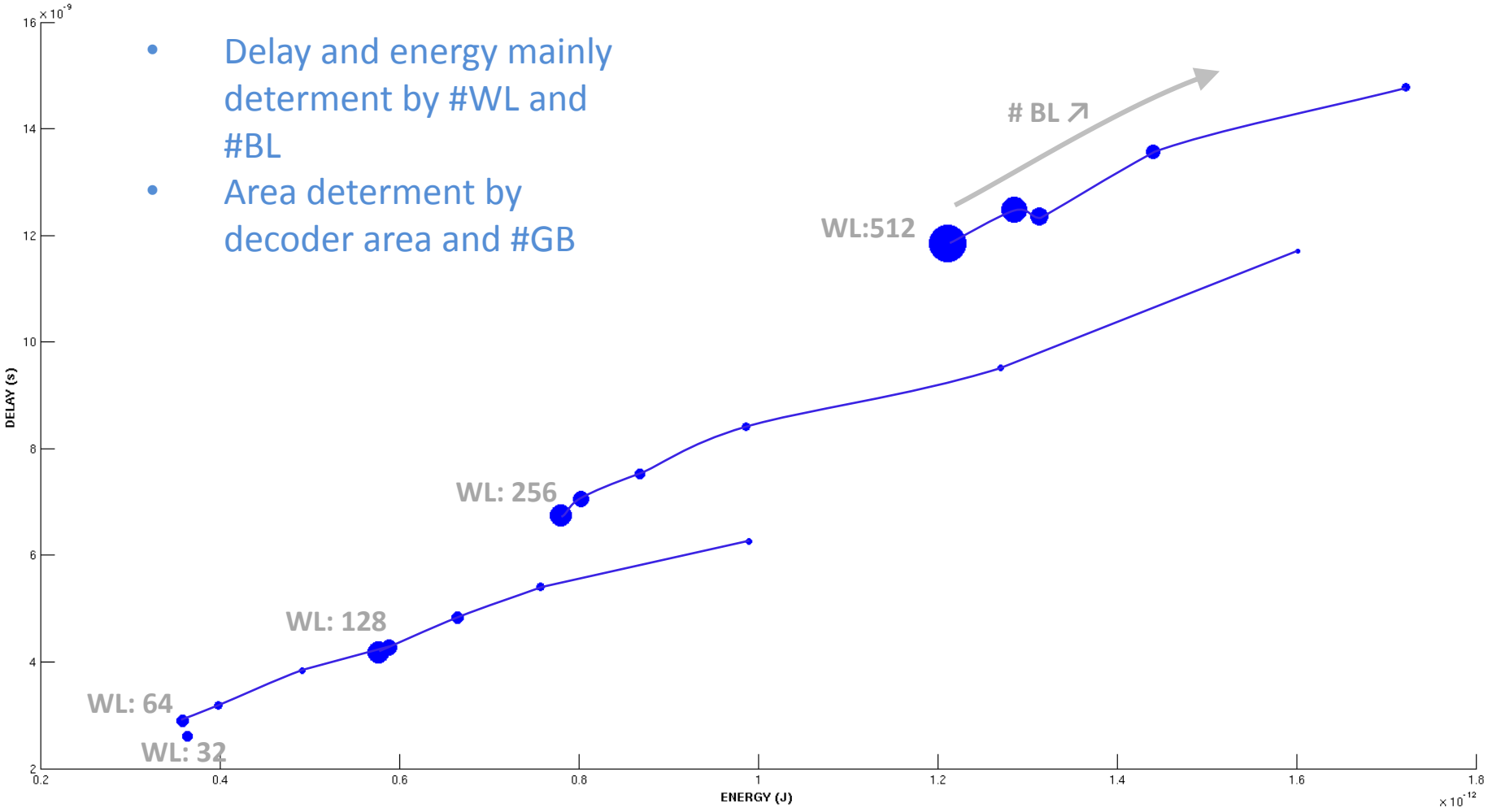
- Add initial conditions to nodes to get a quicker convergence in dc op point

ARCHITECTURE (2)

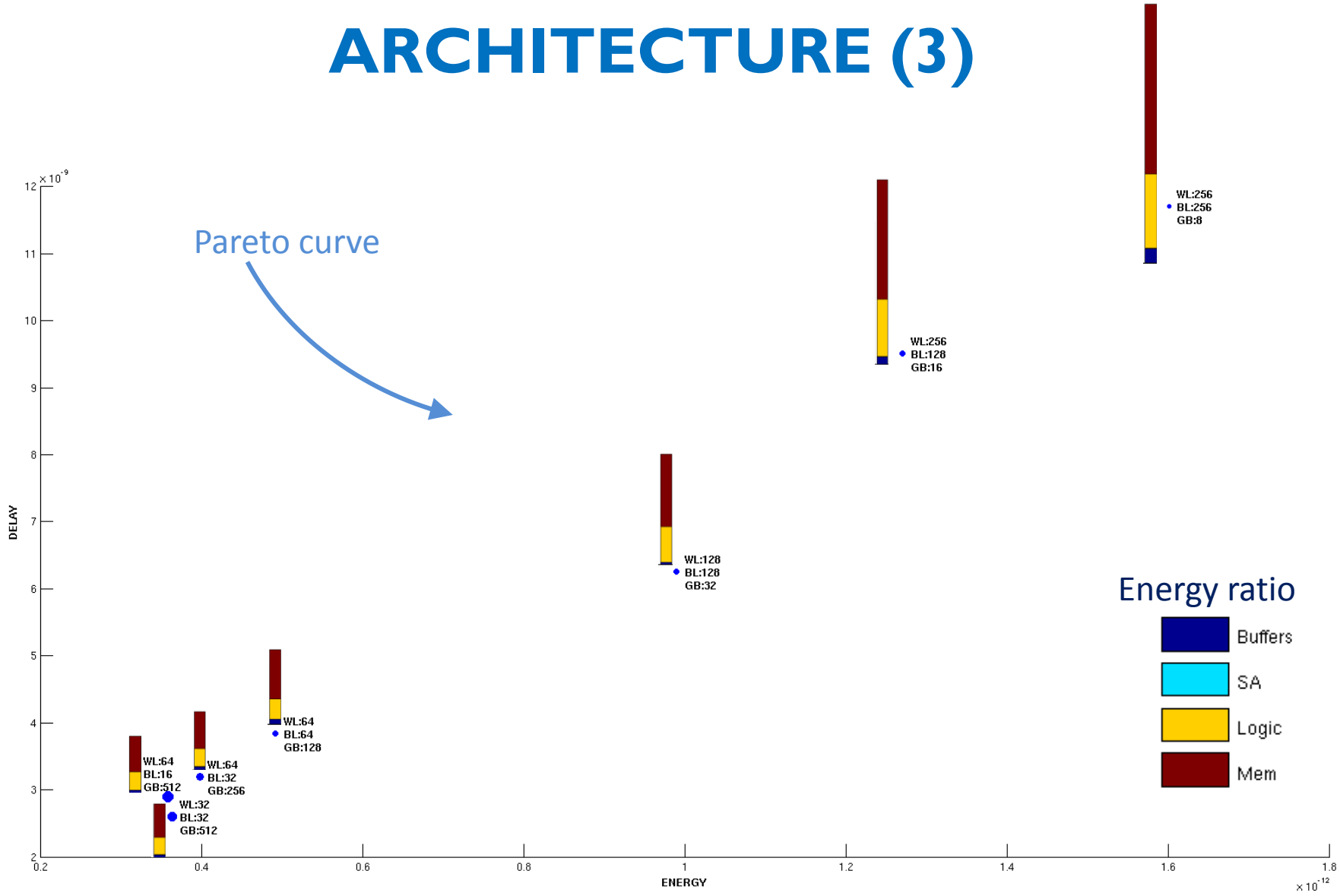


ARCHITECTURE (2)

- Delay and energy mainly determent by #WL and #BL
- Area determent by decoder area and #GB



ARCHITECTURE (3)



Leakage energy is 2 orders of magnitude smaller

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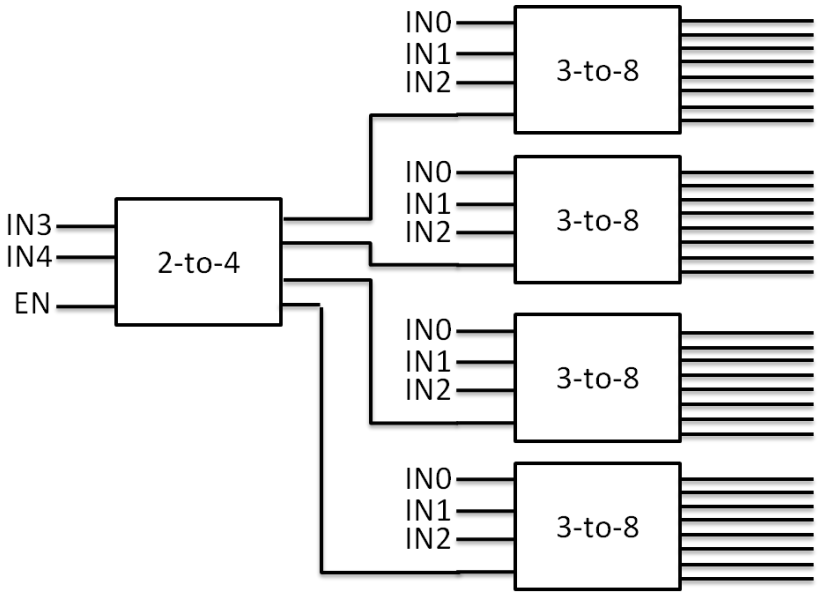
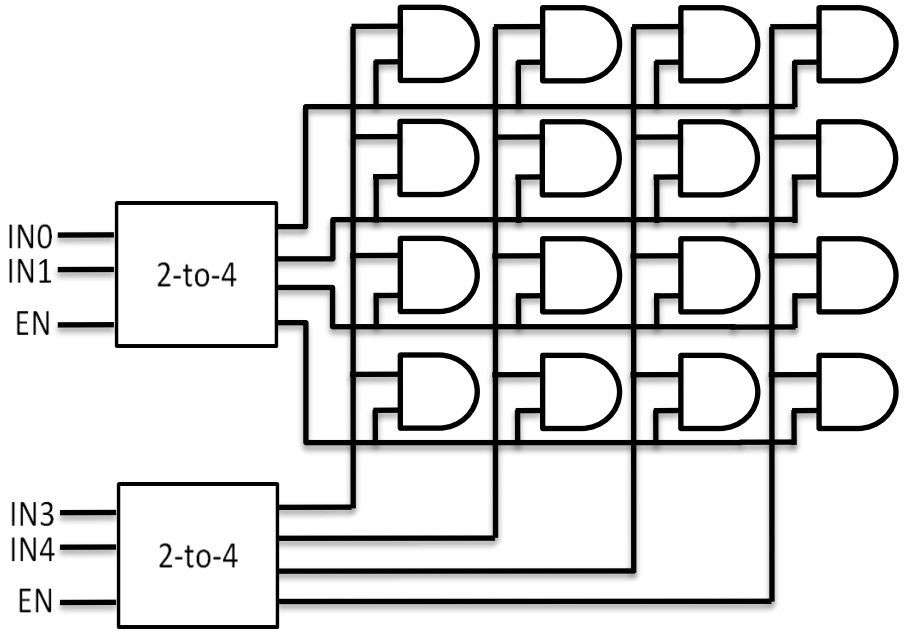
DECODERS (1)

Type 1



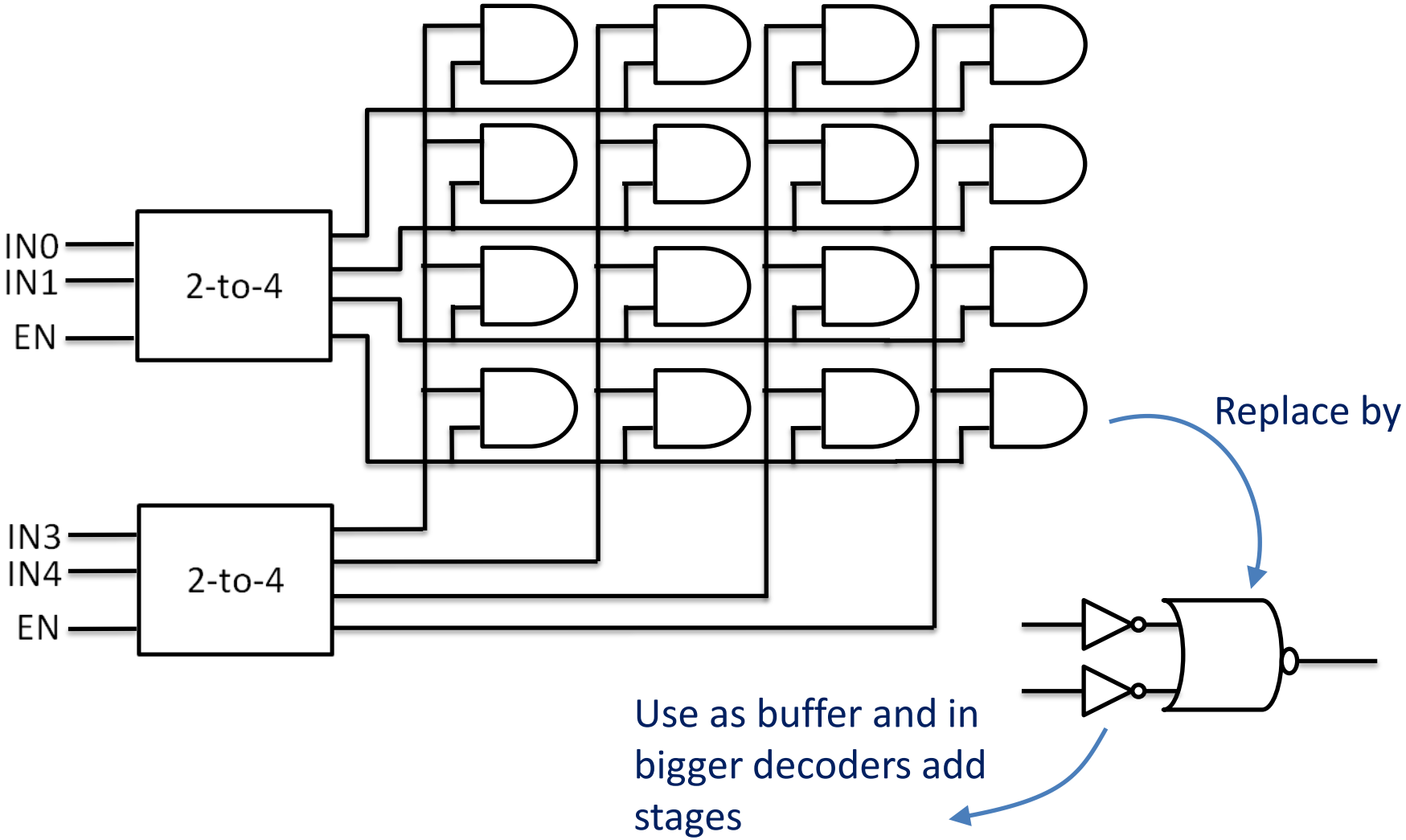
- Delay dependent of previous and current address
- Prone to glitches

Type 2

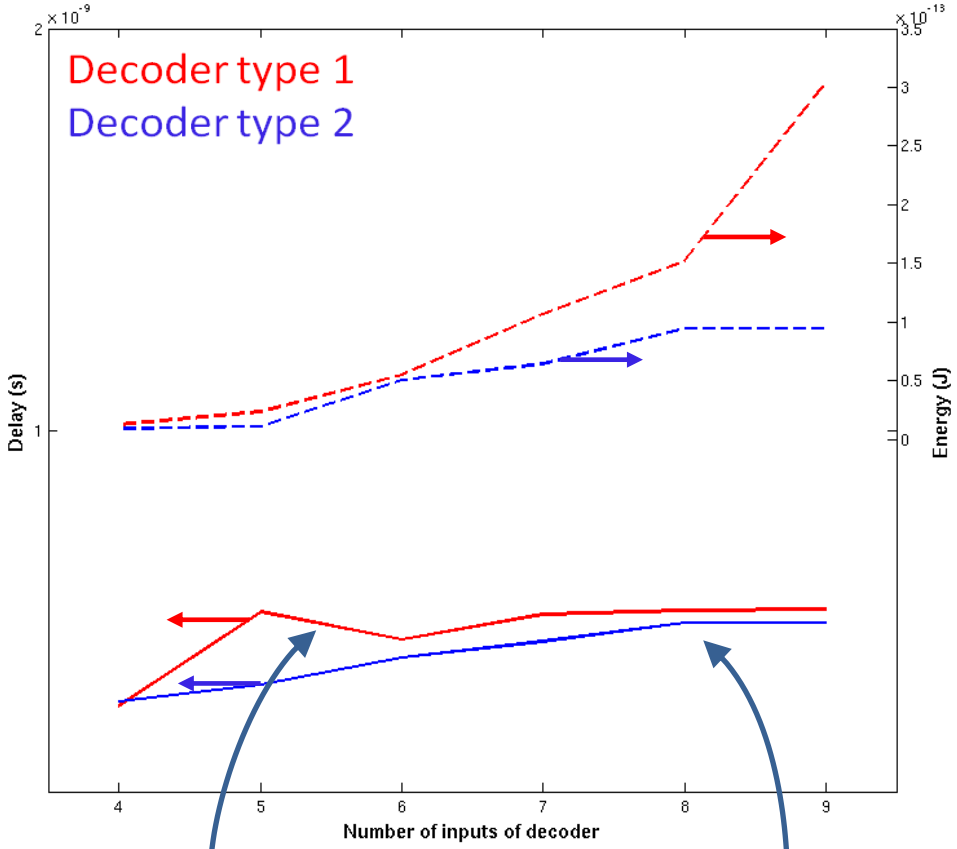


- Delay more or less constant for each address
- Delay and Energy are more robust against mismatch

DECODERS (2)

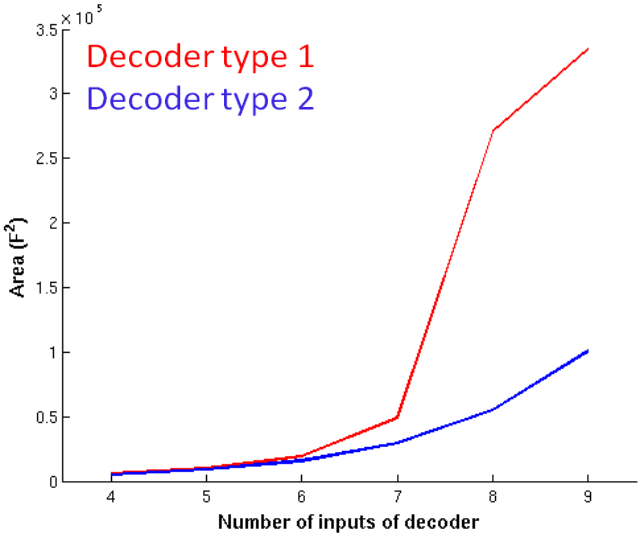

IN0
IN1
EN
2-to-4
IN3
IN4
EN
2-to-4
Replace by
Use as buffer and in bigger decoders add stages

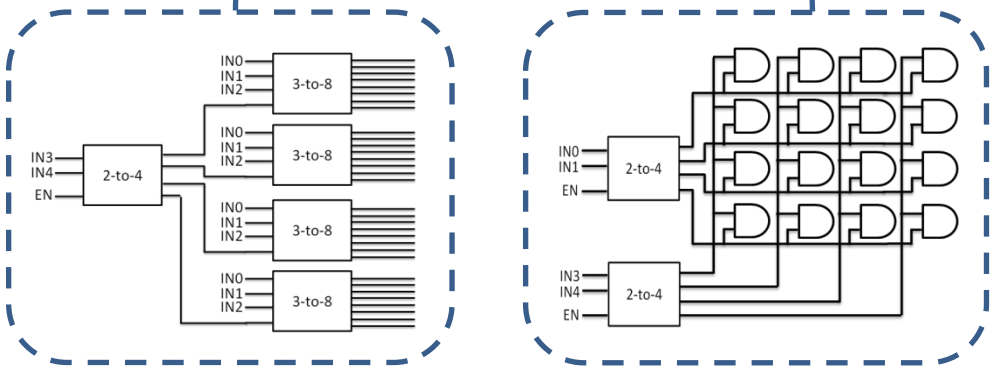
DECODERS (3)



←Worst case delay and energy at worst case delay
(≠ worst case energy !!!)

↓Total area (F^2 = min technology area)





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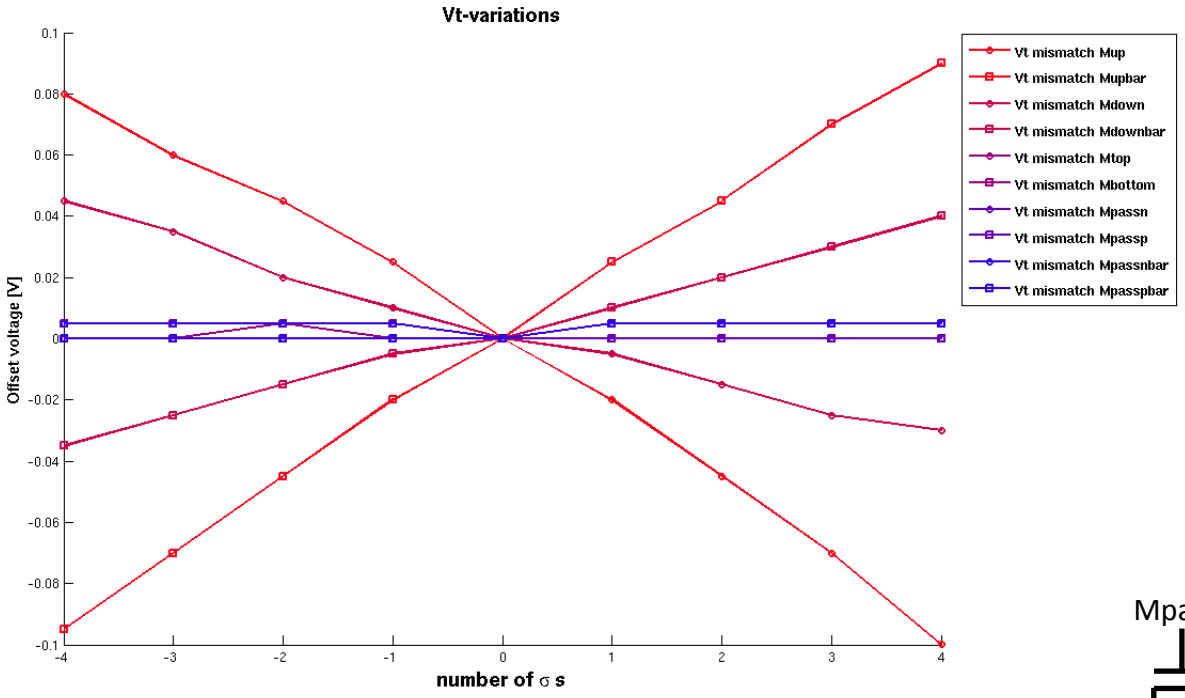
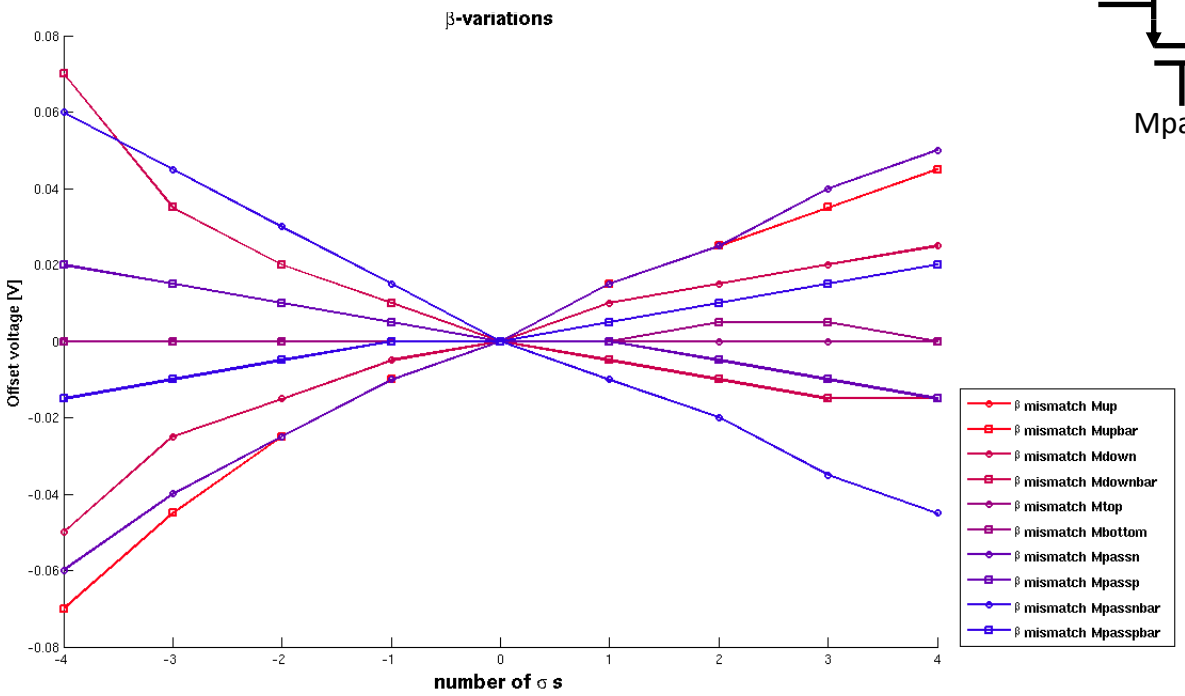
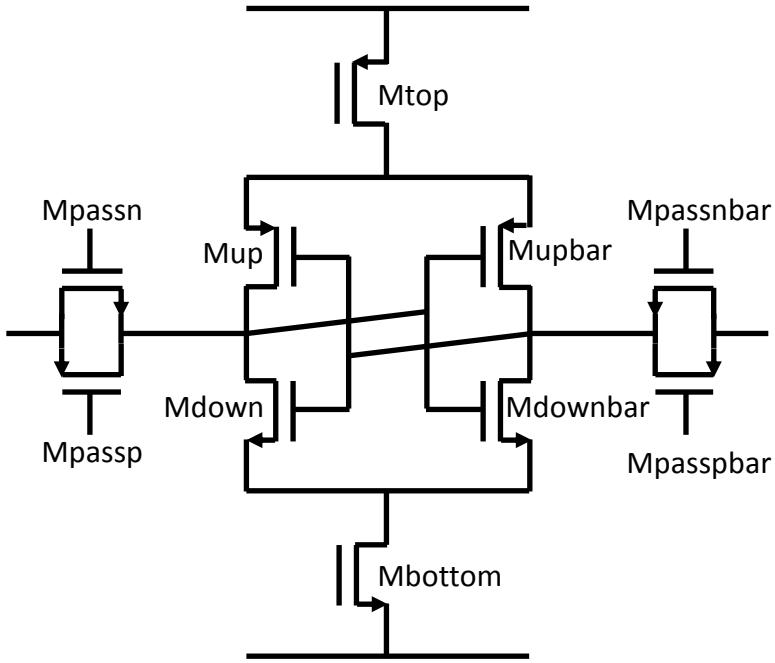
Sense Amplifier

- Sensitivity analysis
- Sweep Vt- & β-mismatch of different transistors independently and manually
- Offset as function of variation instances
- Done for minimal SA, since no idea yet of sizes to be used in our architecture

Sensitivity results

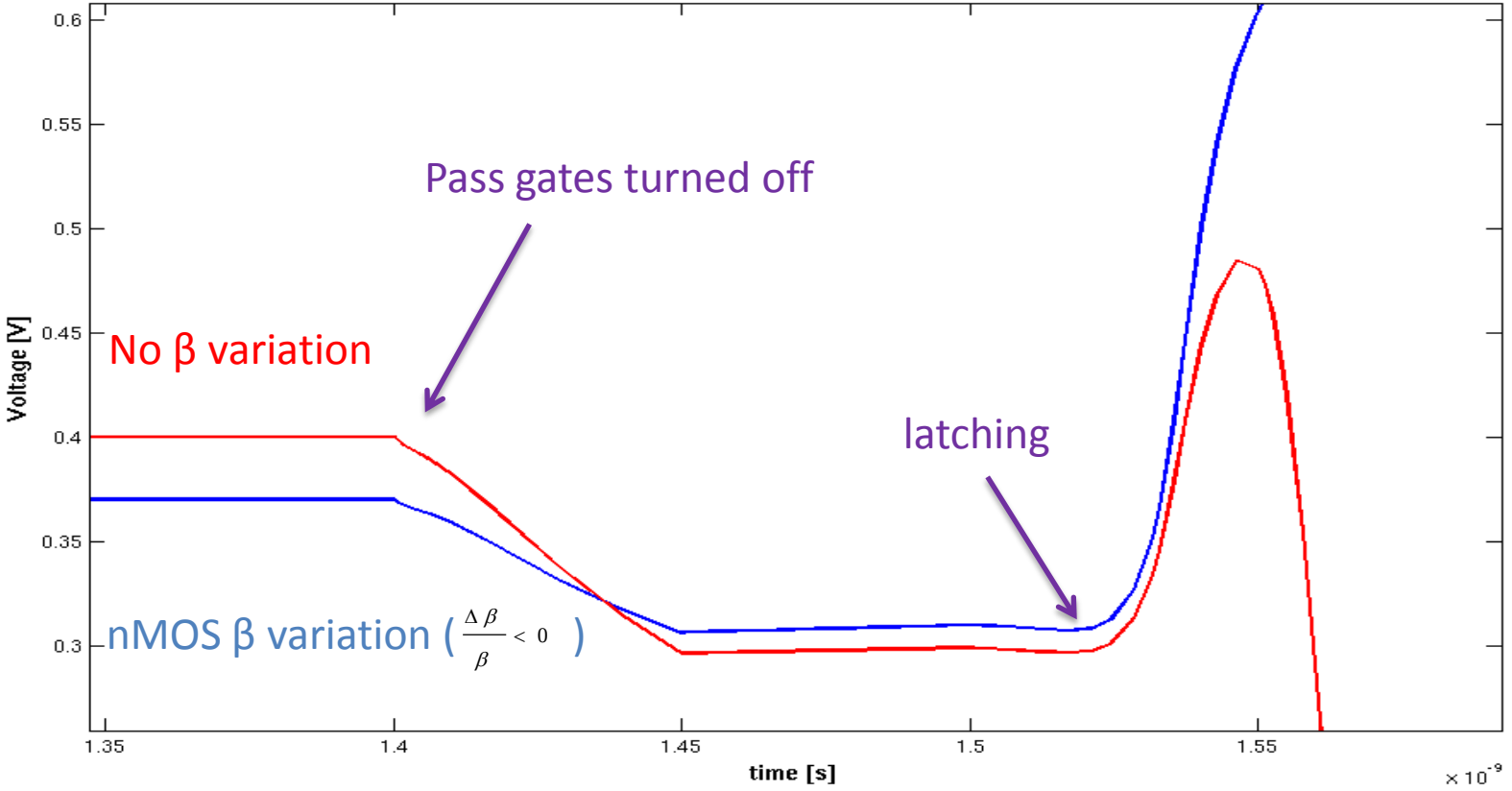






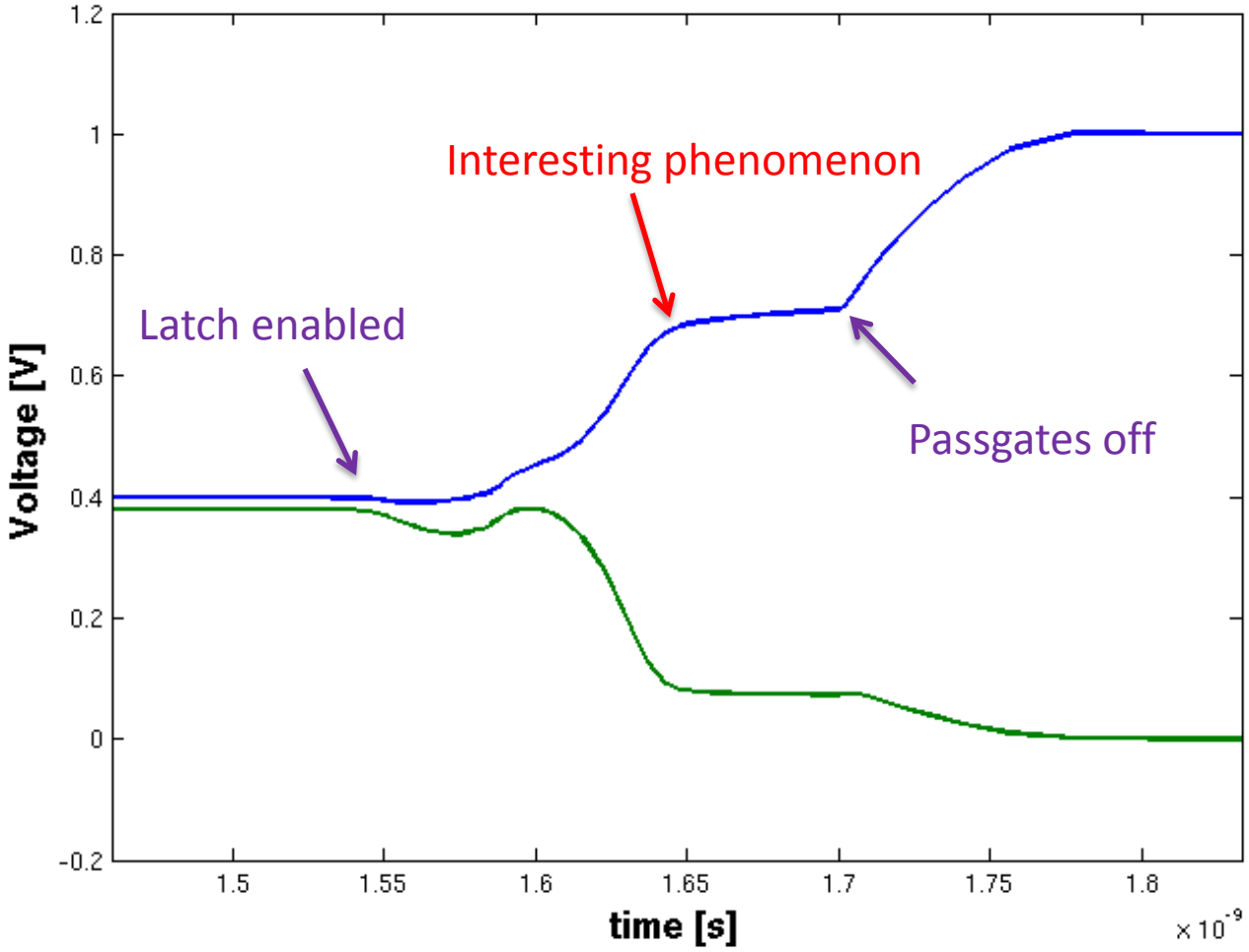
Sensitivity Analysis

- Mainly contributions by differential pair
- Also β-variations pass-gates:
  charge injection not matched anymore



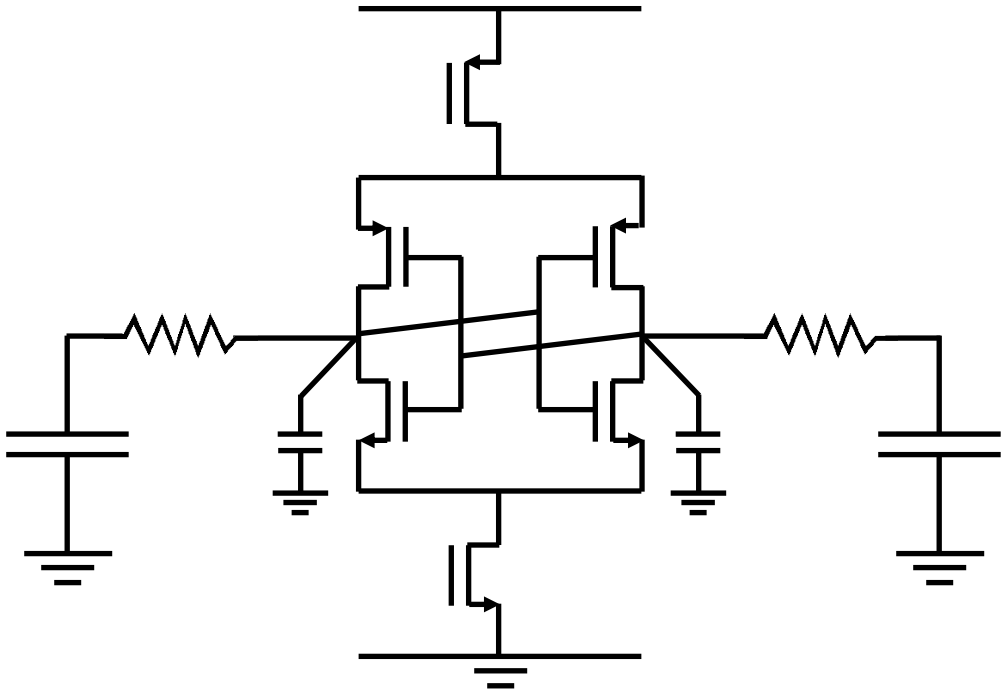
Pass Gate mismatch

- Avoid by allowing (short) overlap PassEnable & LatchEnable



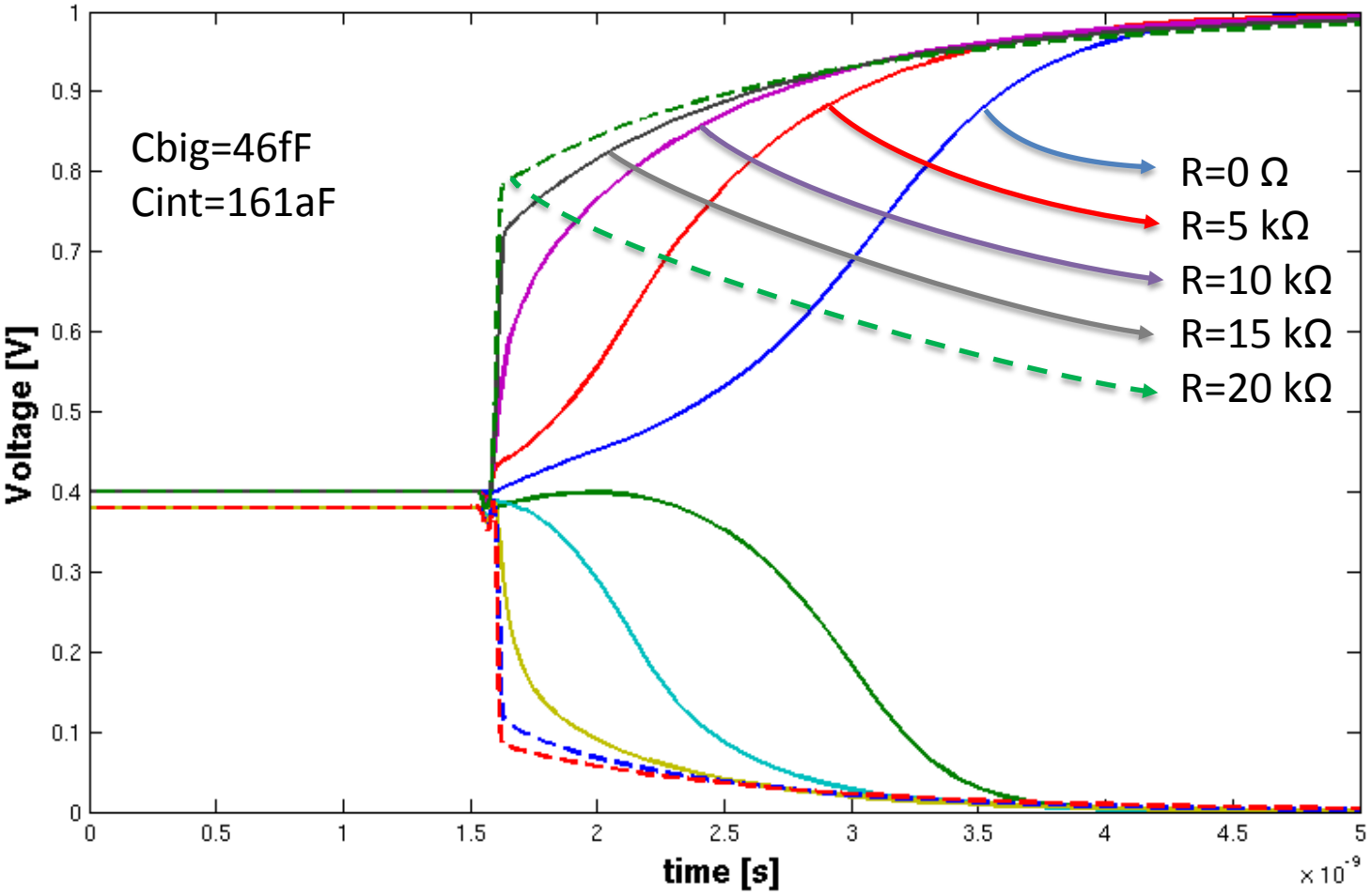
Diels effect ©®

(minimal SA)



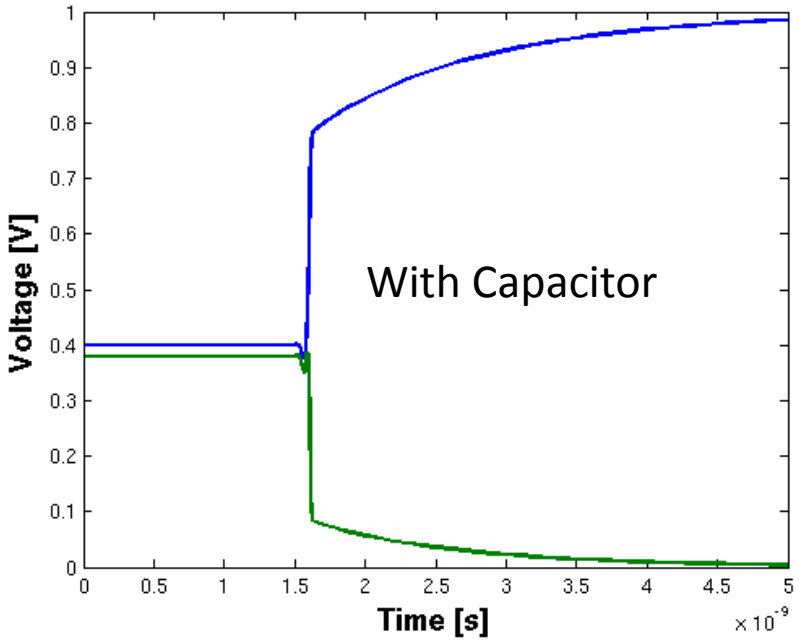
Diels effect ©®

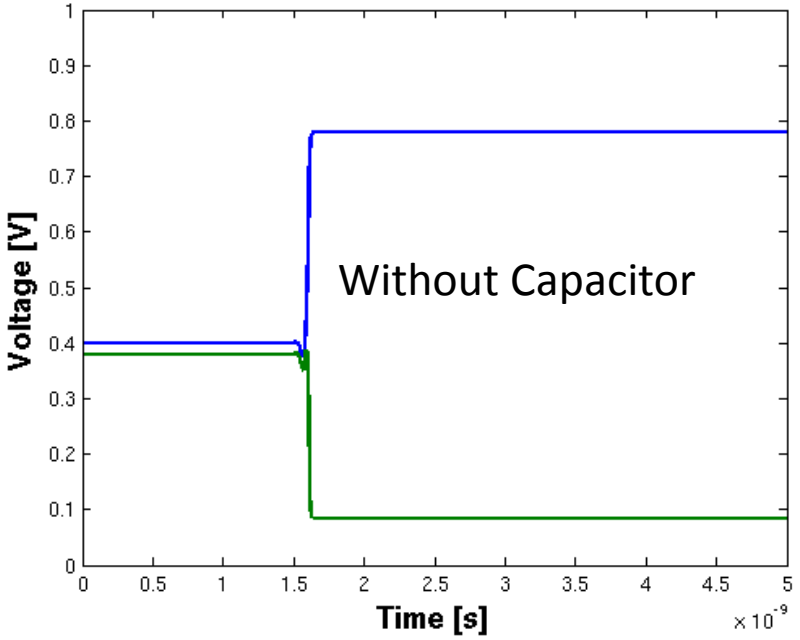
- Depending on resistance value, strange dynamic behaviour.



Diels effect ©®

- Capacitor acts as short in beginning
- Ordinary voltage drop over resistor, output charges normally (high frequencies)
- Afterwards also charging C





Diels effect ©®

- Out(bar) charges almost linearly
- AC voltage over capacitor almost zero
- Latching and RC-charging are separated
- Vc response for linearly charging source

$$v_c(t) = t - RC\ (1 - e^{-\frac{t}{RC}})$$

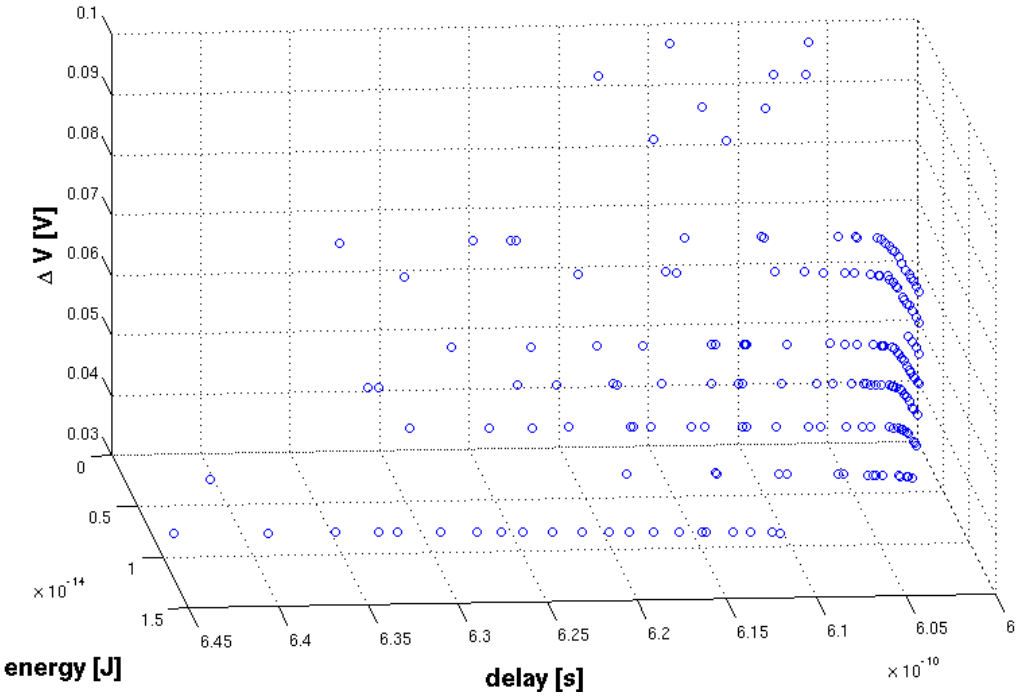
- RC-product must be large enough in order for C-short approximation to hold

Diels effect ©®

- When RC-product is too small:
- Latching and RC-charging no longer separated
- Difficult to mathematically describe

Sense amplifier pareto

- Very large simulation
- Pareto surface delay-energy-ΔV



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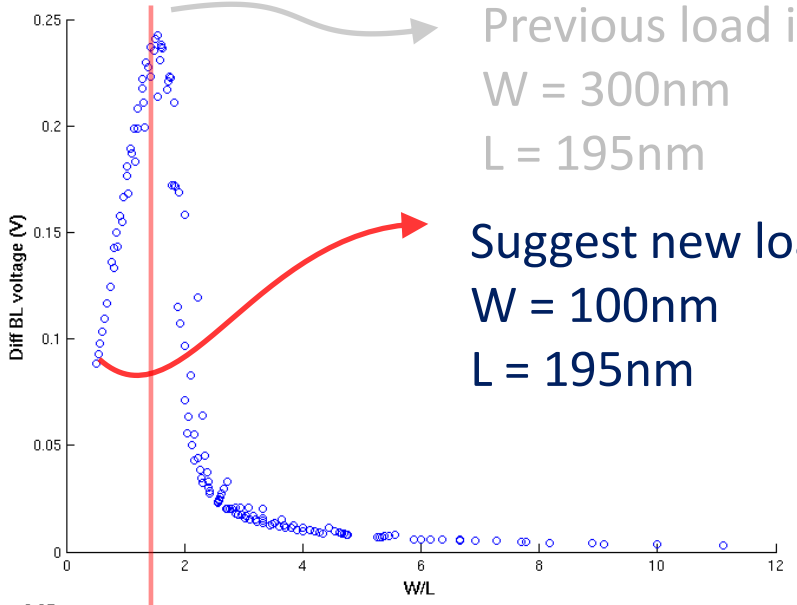
LOAD

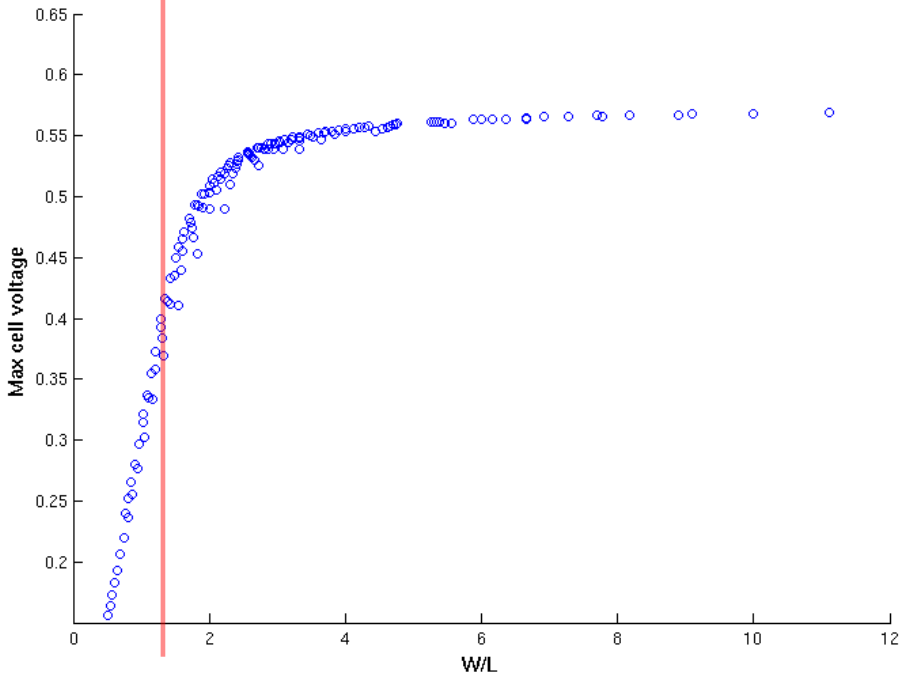


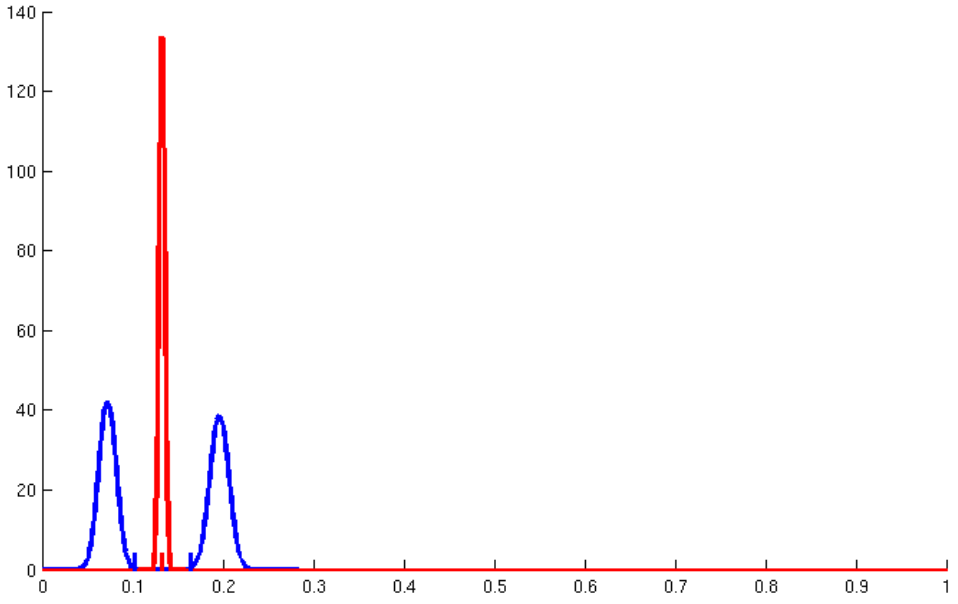
Previous load is here
W = 300nm
L = 195nm

Suggest new load
W = 100nm
L = 195nm

Size x 4 for mismatch
→ $3\sigma_{Vdiff}$ = 29mV
→ Vcell max = 176mV (after mc)

(todo schrijf hoe berekend)





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