KATHOLIEKE UNIVERSITEIT LEUVEN

ESAT

Load Analysis 2

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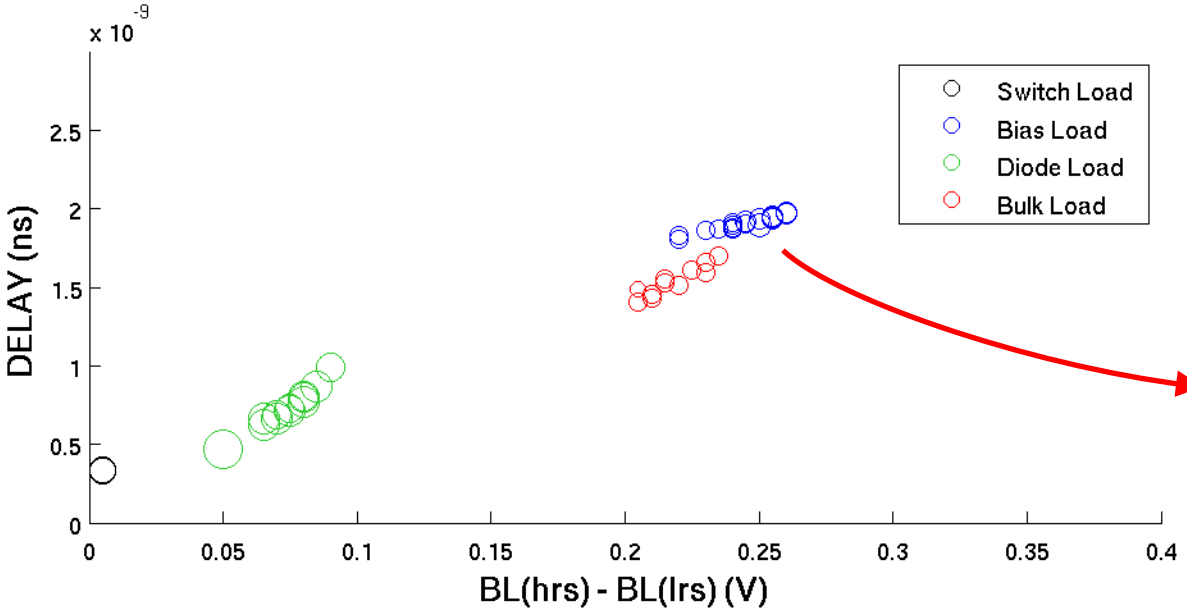
Wouter Diels

OUTLINE

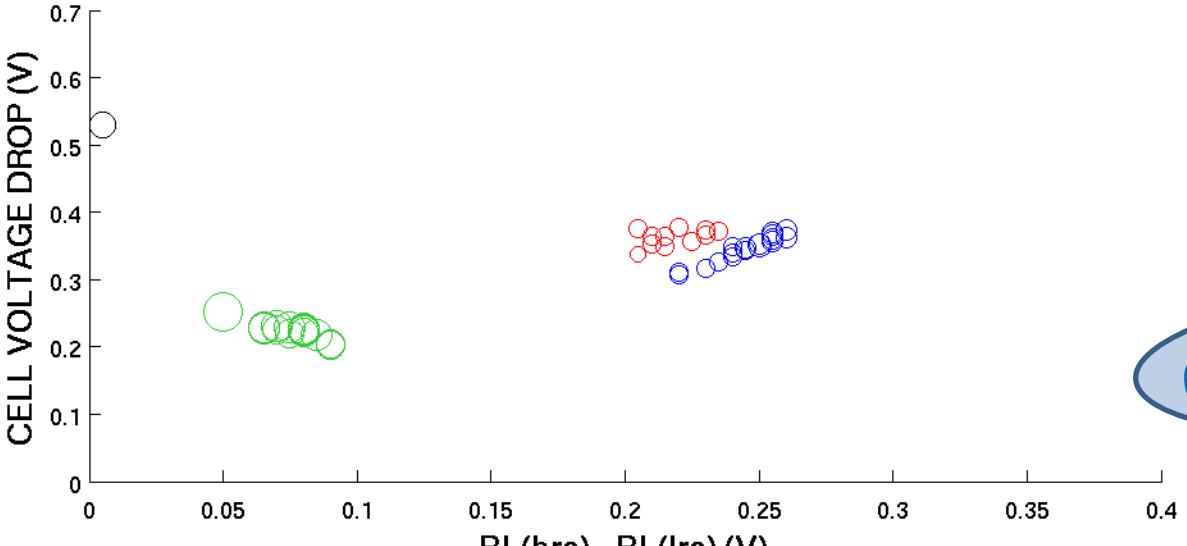
- RECAP LAST MEETING
- TRIPLE LOAD
- SINGLE LOAD
- CONCLUSION

MONTE CARLO: PARETO



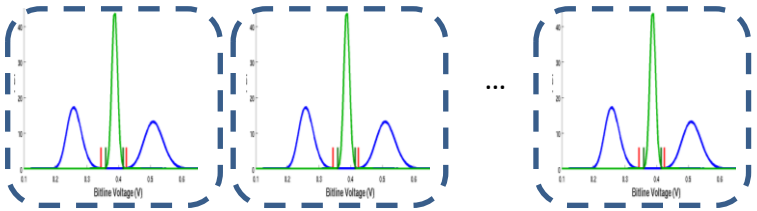
48 SOLUTIONS

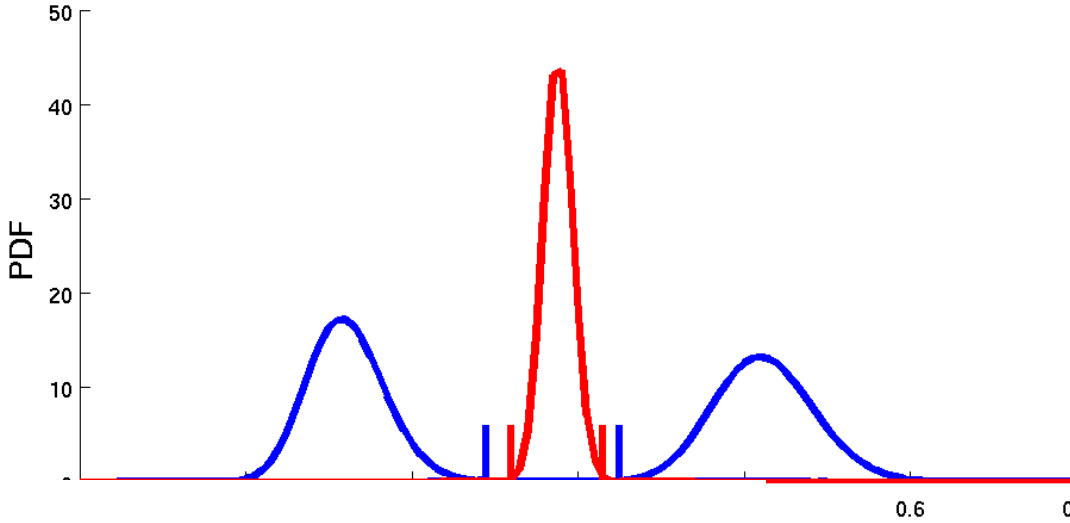
CHOICE FINAL LOAD:
Type = bias
W_switch = 100nm
W_bias = 180nm
V_bias = 0V

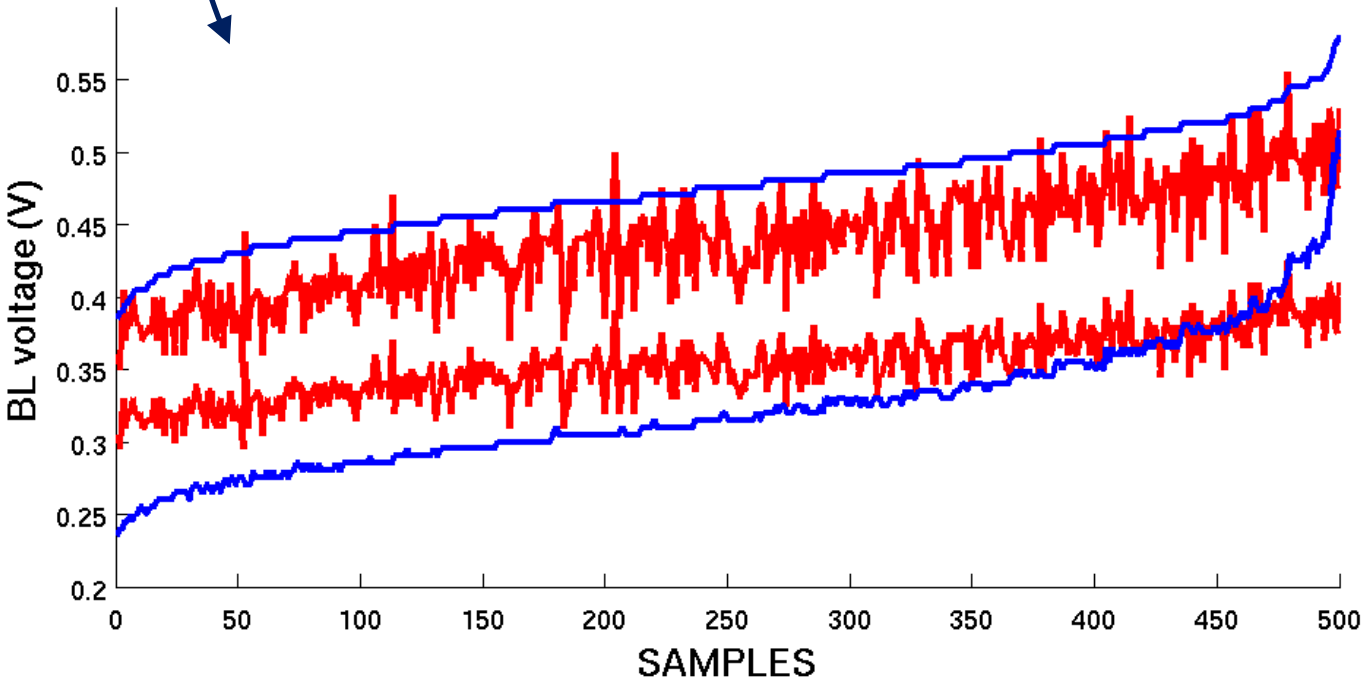


600 mc iterations

BIAS LOAD: BEST CASE SCENARIO

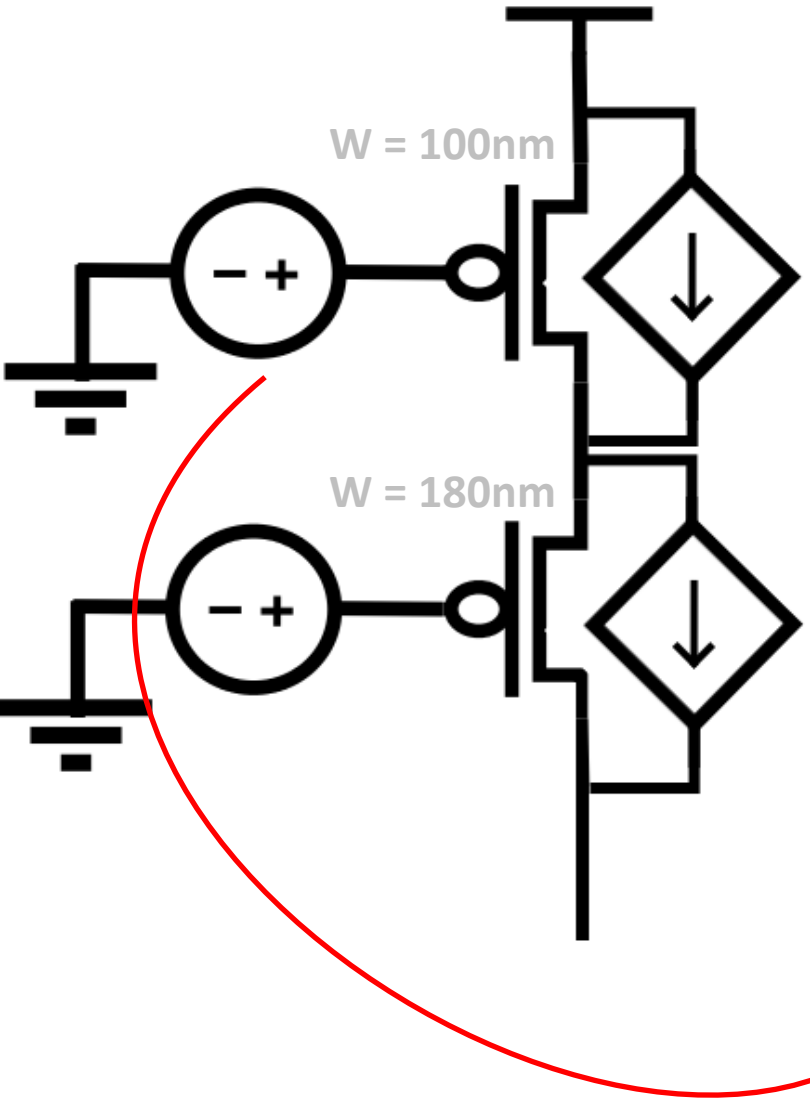


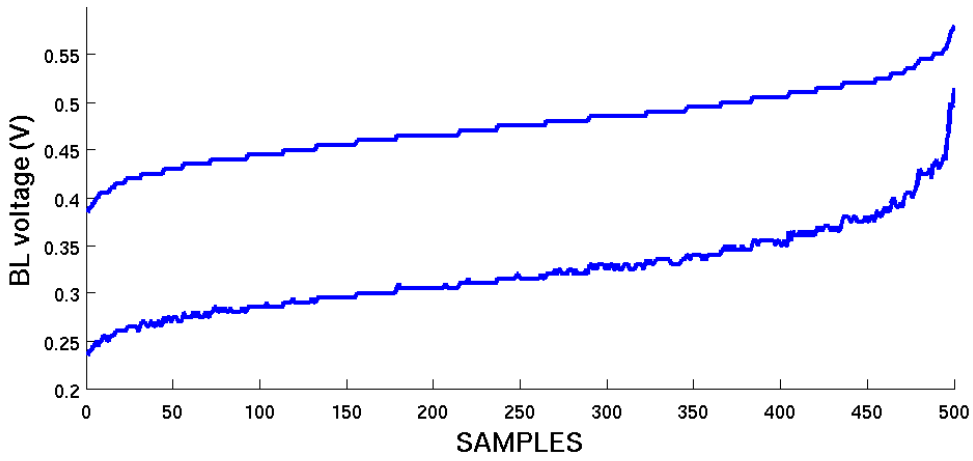


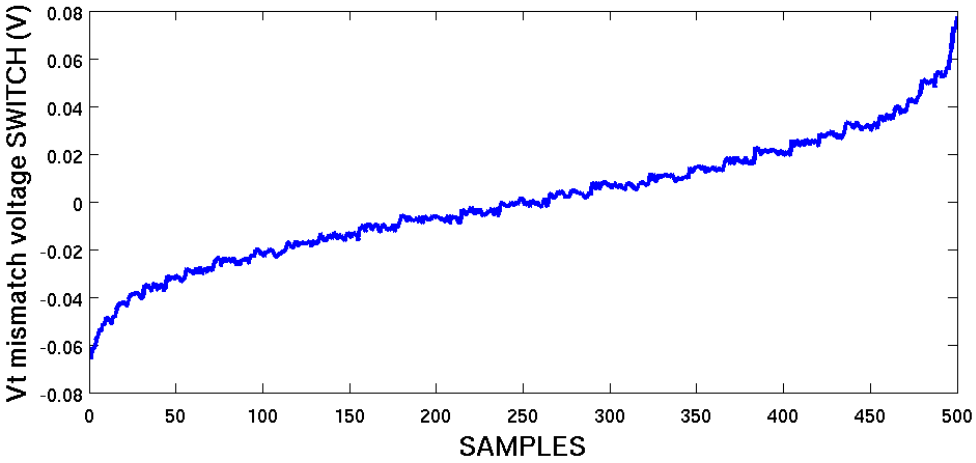


Why do the BL voltages react this way?

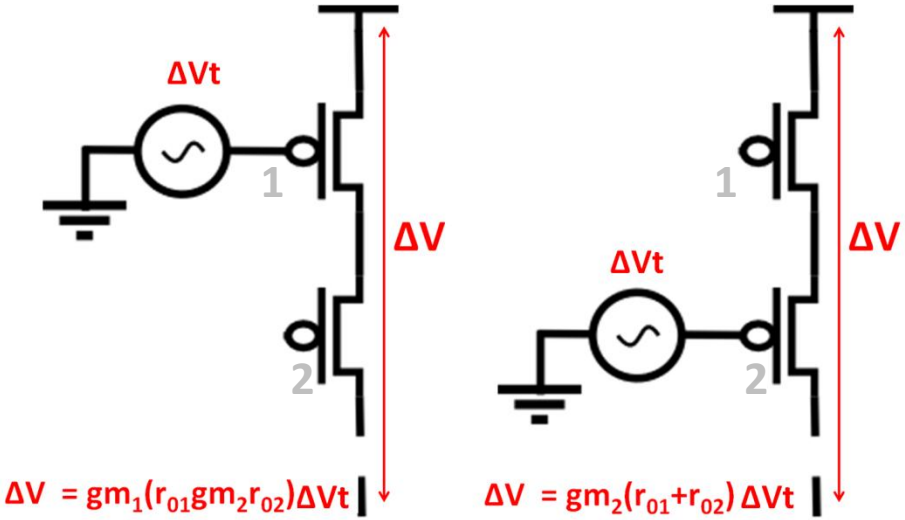
BIAS LOAD: BEST CASE SCENARIO





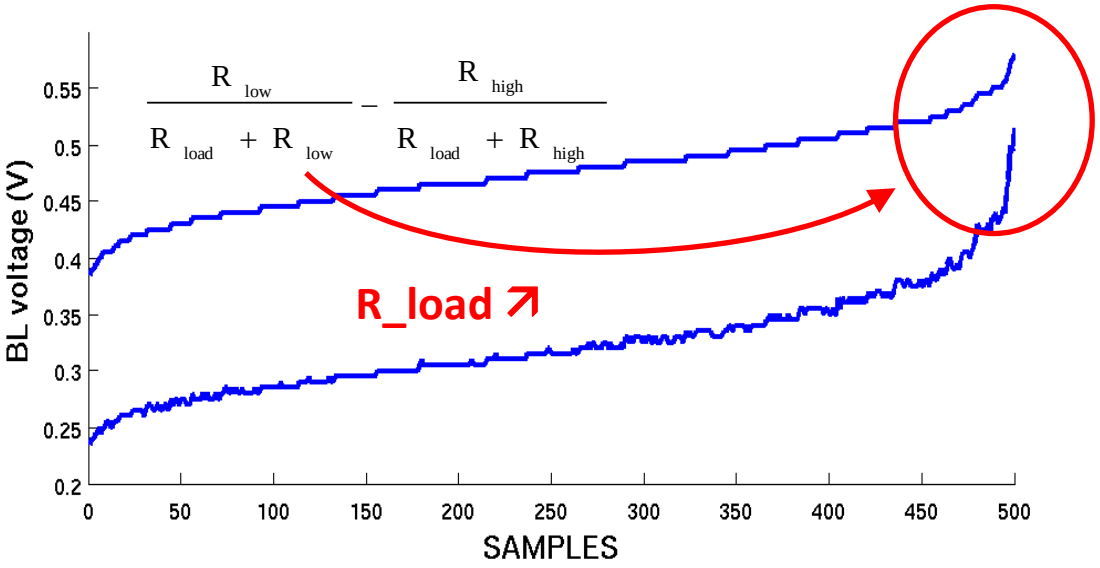


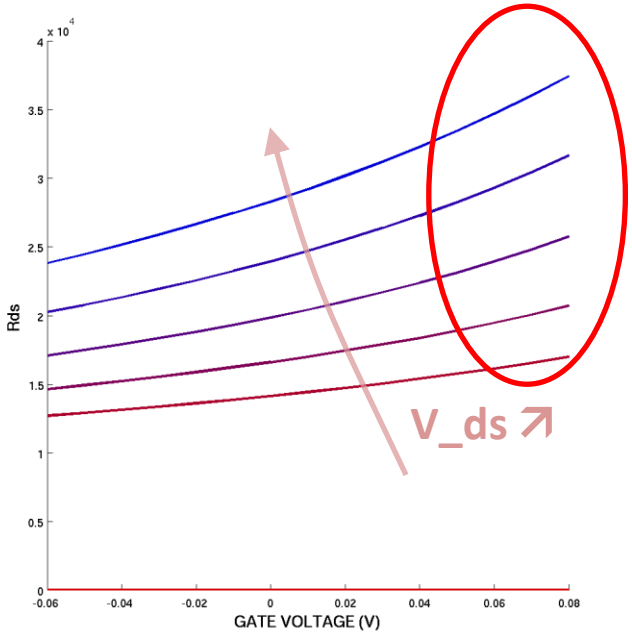
BIAS LOAD: BEST CASE SCENARIO



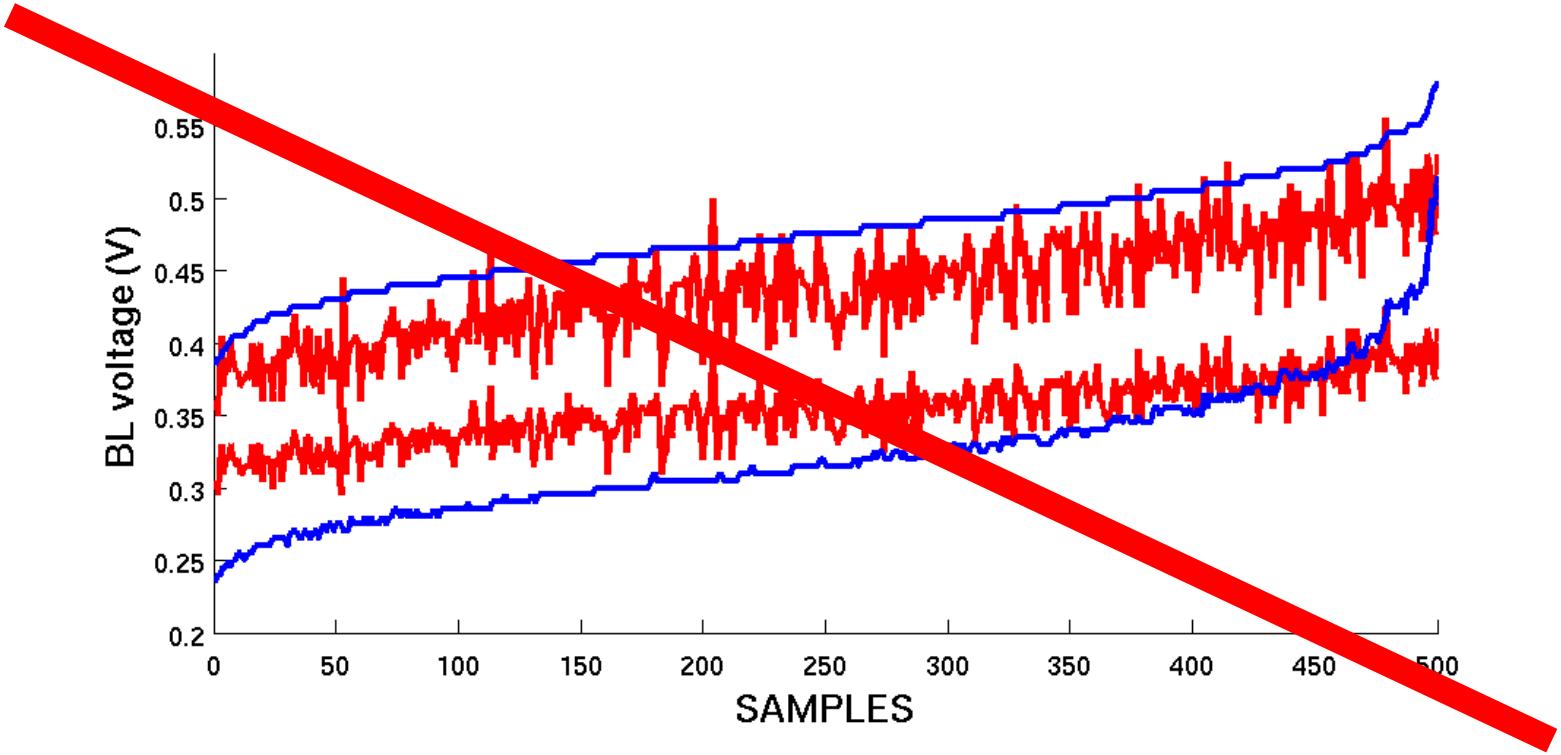
1) Cascode effect : explains why mismatch switch is dominant

2) Increase ds resistance : explains why V_bl(HRS)- V_bl(LRS) becomes smaller at extreme positive values of ΔVt





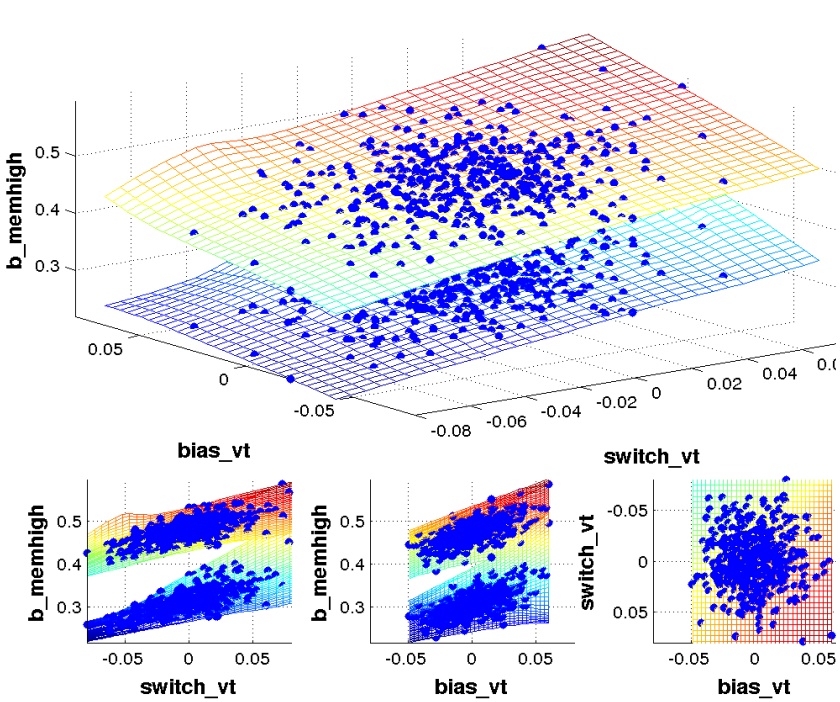
BIAS LOAD: BEST CASE SCENARIO

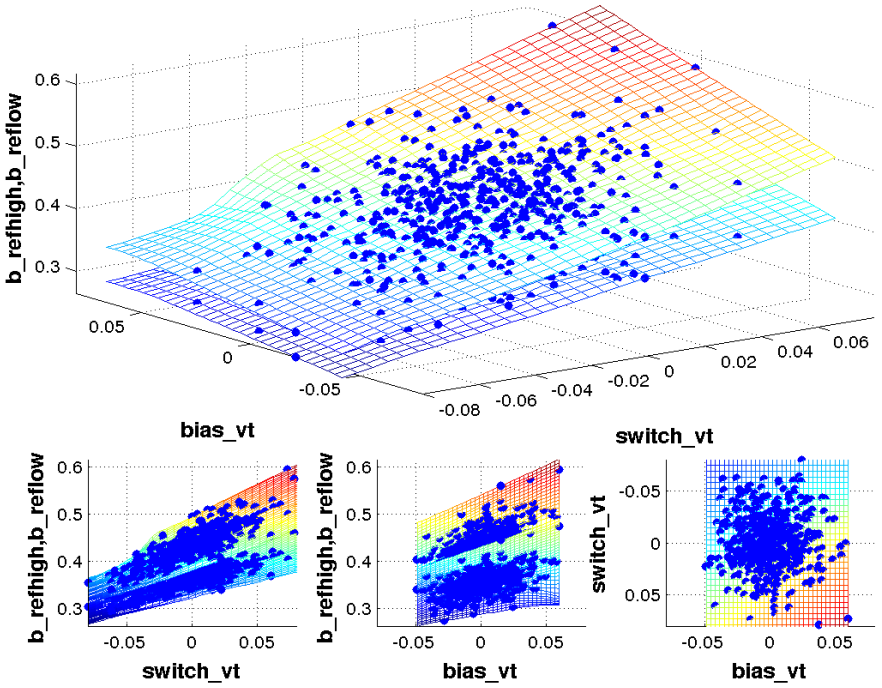


→Typo error

Cascode effect also not really valid because both transistors are in linear region

BIAS LOAD: BEST CASE SCENARIO





Corrected results → Both BL of reference and memory array react the same

→ Both transistor give equal mismatch problems

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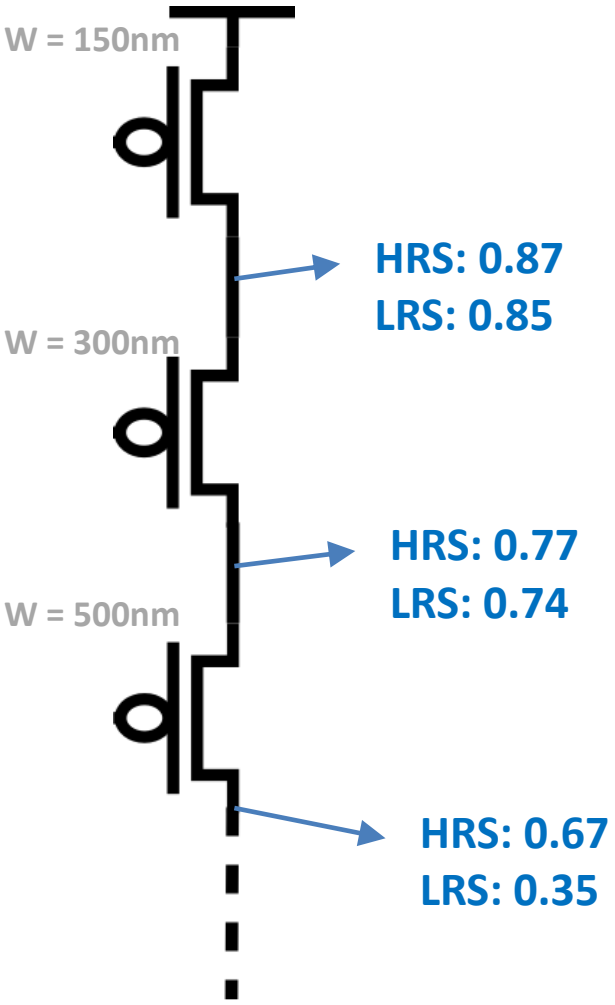
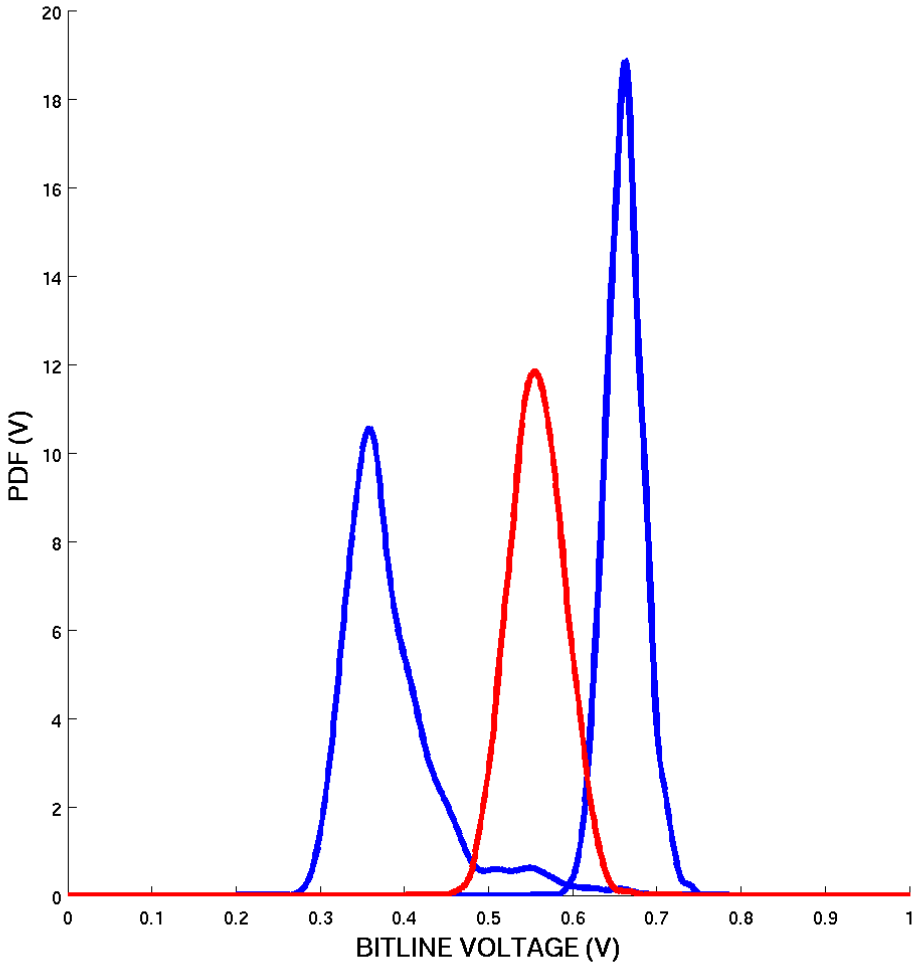
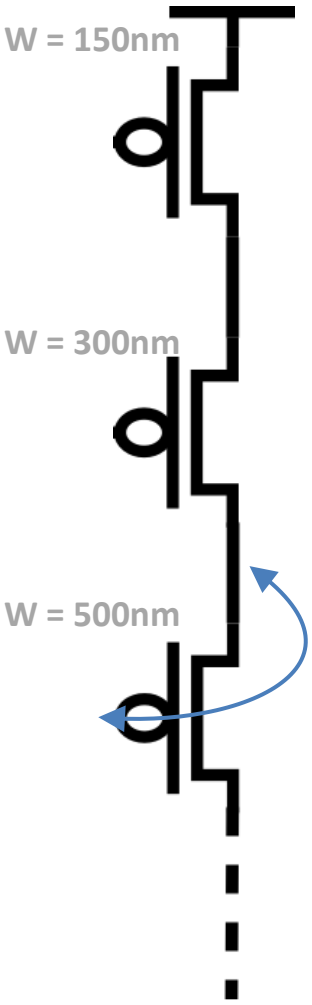
TRIPLE LOAD

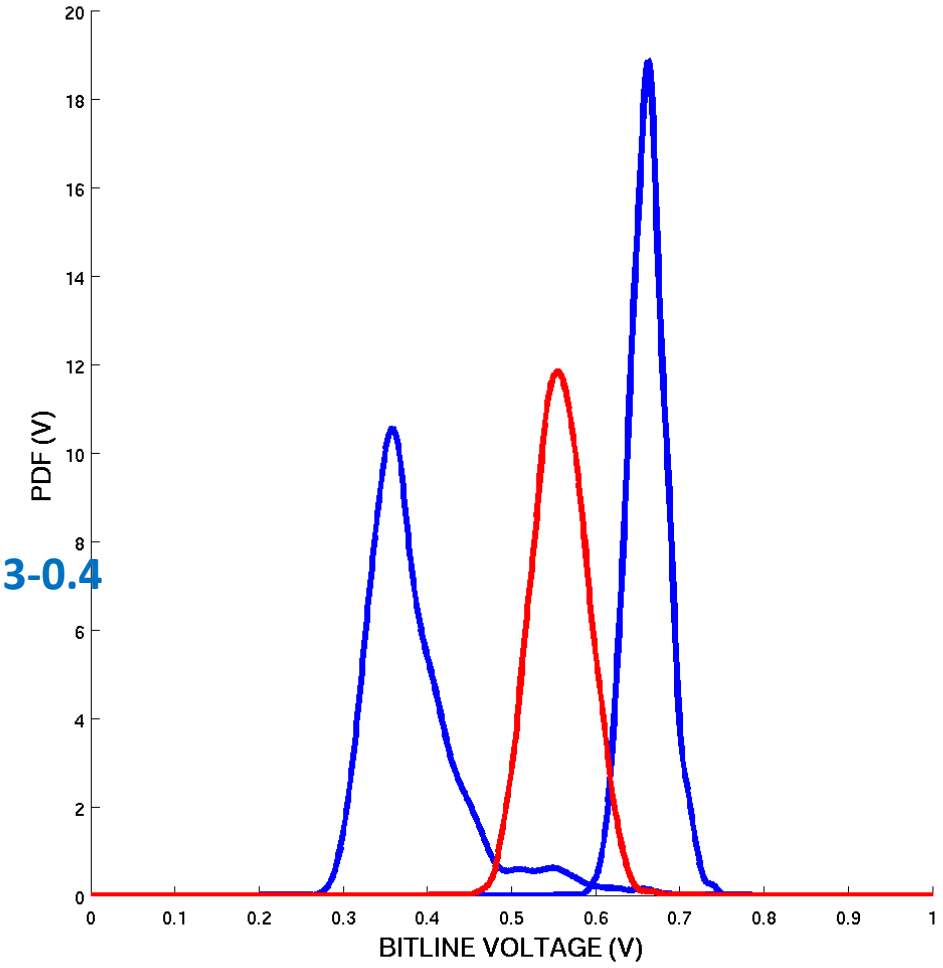

W = 150nm
W = 300nm
W = 500nm
HRS: 0.87
LRS: 0.85
HRS: 0.77
LRS: 0.74
HRS: 0.67
LRS: 0.35


PDF (V)
BITLINE VOLTAGE (V)
0
2
4
6
8
10
12
14
16
18
20
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

TRIPLE LOAD



Vgs ≈ 0.3-0.4 with Vth ≈ 0.3-0.4
→ maybe in subthreshold



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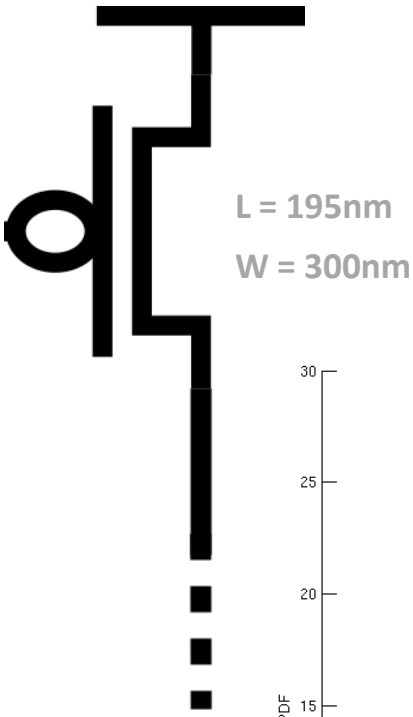
SINGLE LOAD

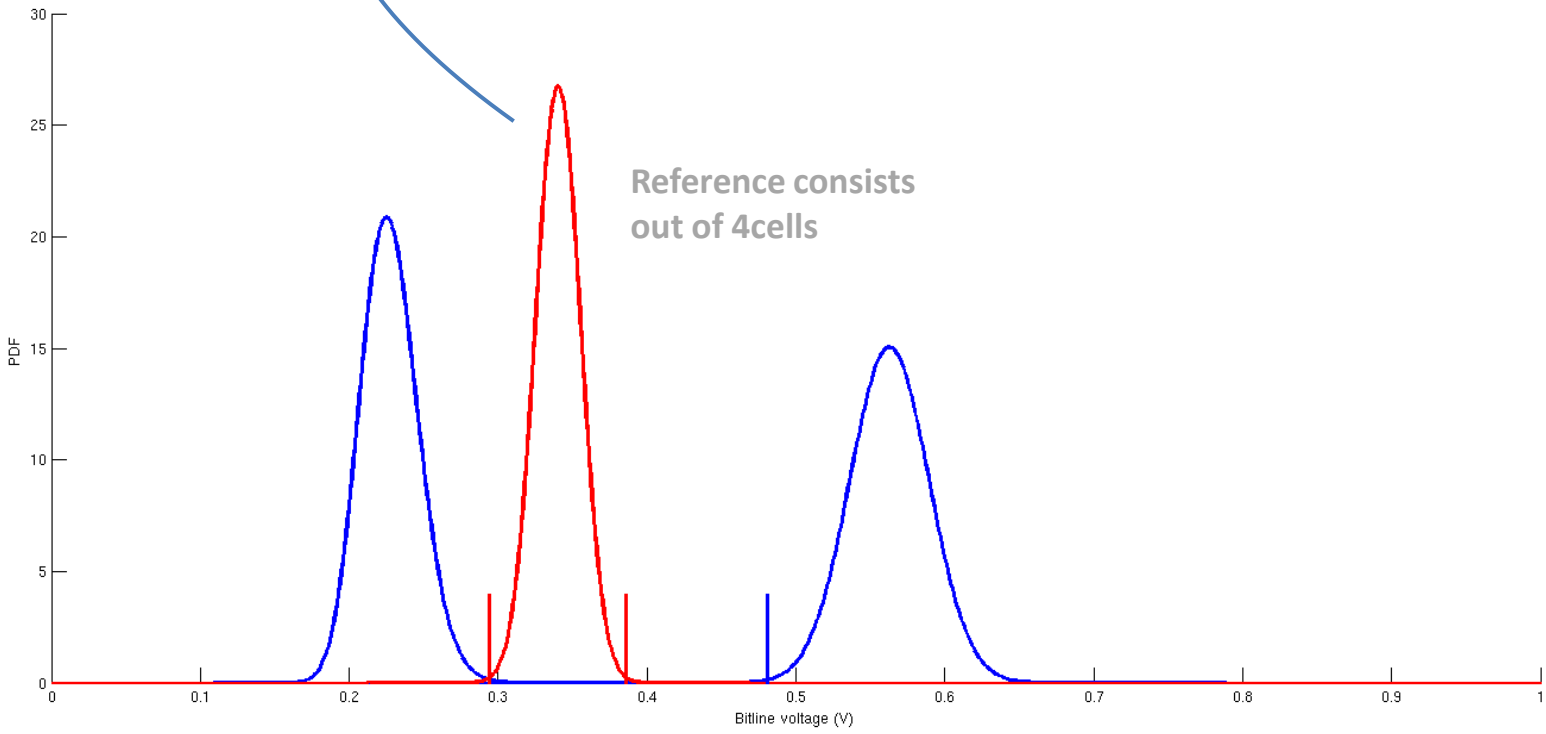


L = 195nm

W = 300nm

About 200mV margin and
Reference can easily be shifted to center

Reference consists
out of 4cells



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