RRAM Crossbar Array With Cell Selection Device: A Device and Circuit Interaction Study

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***Abstract*—The resistive random access memory (RRAM) crossbar array has been extensively studied as one of the most promising candidates for future high-density nonvolatile memory technology. However, some problems caused by circuit and device interaction, such as sneak leakage paths, result in limited array size and large power consumption, which degrade the array performance significantly. Thus, the analysis on circuit and device interaction issue is imperative. In this paper, a simulation method is developed to investigate the critical issues correlated with the interaction between devices and the circuit. The simulations show that a large off/on ratio of resistance states of RRAM is beneficial for large readout margin (i.e., array size). The existence of the selector connected in series with an RRAM device can eliminate the need for high R_{on} resistance, which is critical for the array consisted of only RRAM cells. The readout margin is more sensitive to the variation of R_{on} and is determined by the nonlinearity of the I–V characteristics of RRAM, whereas the nonlinear characteristics of the selector device are beneficial for a larger readout margin. An optimal design scheme for turn-on voltage and conductance of the selector is proposed based on the simulation.**

***Index Terms*—Crossbar, leakage path, memory array, nonlinearity, readout margin, resistive random access memory (RRAM), selection device, selector.**

I. Introduction

With the increasing demand for high-density, low-power, high-speed, and low-cost nonvolatile memory (NVM) technology, alternative memory technologies beyond 20-nm node [1] have been extensively studied. Among the candidates of the next-generation NVM technology [2]–[9], resistive random access memory (RRAM) has become a competitive candidate and has been widely studied in recent years due to excellent scalability, fast switching speed, simple device structure, multibit storage and 3-D architecture potential, and good compatibility with complementary metal–oxide–semiconductor technology [10]–[15].

To realize high-density and low-power storage, an RRAM crossbar structure was introduced for memory circuit application and has been studied in recent years for its simple array architecture and 3-D application potential [16]–[18]. However, with its intrinsic drawbacks of purely passive RRAM crossbar array architecture, such as parasitic leakage paths in unselected cells and series interconnect resistance, the purely passive crossbar array will get a limited signal swing, which means the array size may be reduced and adding a large sensing circuit is necessary. Furthermore, power dissipation and reliability problem may become serious with the increase in the array size. To solve these problems, a selection device connected in series with the memory device, such as a diode (resulting in a 1D1R structure), a transistor (resulting in a 1T1R structure), or a selector (resulting in a 1S1R structure), is introduced, as has been reported in recent years [19]–[22]. Other methods such as complementary resistive switching have been also investigated [23], [24].

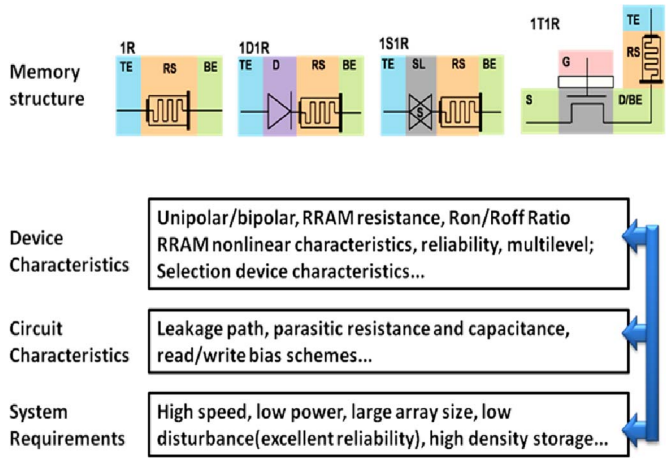

Fig. 1. Device and circuit interaction issues in RRAM crossbar array. Different cell structures, device and circuit characteristics, and their impacts on system performance should be comprehensively investigated.

To understand the RRAM crossbar array thoroughly, different factors including different memory cell structures, device characteristics, circuit characteristics, and the system performance should be comprehensively considered, as shown in Fig. 1. Considering the interaction between the circuit and devices, the device and circuit characteristics can be optimized through design and fabrication process to achieve high system performance.

Many literature works have discussed about RRAM crossbar array, but most of them were from a circuit's point of view [25]–[27]. Only some of them worked on the circuit and device interaction issues [28]–[32]. However, most of them are based on a simplified circuit model and using a linear resistor to represent an RRAM device, which may draw inaccurate

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conclusion due to too much simplicity used in the analysis. A detailed and comprehensive analysis focused on the device and circuit interaction is still lacking, particularly considering the RRAM device and selection device variation and their impacts on circuit performance.

In this paper, the impacts of variation of RRAM device and selection device characteristics on the crossbar array performance based on a circuit simulation are addressed. The device characteristics and correlated analytical models of RRAM and selection devices will be described in Section II. The crossbar array architecture and read/write operation modes will be also discussed in this part. In Section III, we mainly discuss the impacts of selected cell position and the data patterns of the memory cells on the circuit performance. We investigated the worst case scenario of selected cell and data patterns for different read and write operation modes. The simulation setup is also summarized in this part. According to the worst case scenario, the impacts of the device characteristics of RRAM and selector devices on the circuit performance are discussed in Section IV. The variation of high/low resistance and nonlinear characteristics of RRAM and the variation of resistance, turn-on voltage, and nonlinear characteristics of selection device and their impacts on the read operation are investigated.

II. Device and Circuit Structure

A. Device Characteristics and Analytical Device Model

The RRAM device structure is usually a resistive switching layer sandwiched between two electrodes. The resistance of the device can be changed by applying voltage on the electrodes, which induce resistance change of the resistive switching layer between a high-resistance state $R_{\rm off}$ and a low-resistance state $R_{\rm on}$. The transition process from a high-resistance state $R_{\rm off}$ to a low-resistance state $R_{\rm on}$ is called SET process, whereas from $R_{\rm on}$ to $R_{\rm off}$, it is called RESET process. In most RRAM devices, an electrical forming process is necessary to achieve reversible resistive switching between $R_{\rm on}$ and $R_{\rm off}$. The switching modes may be classified into two modes, i.e., unipolar and bipolar modes. Unipolar switching mode means the switching direction depends on the amplitude of the applied voltage but not on the polarity of the applied voltage. Thus, SET/RESET can occur at the same polarity. If unipolar switching can symmetrically occur at both positive and negative voltages, it is also referred as a nonpolar switching mode. Bipolar switching mode means the switching direction depends on the polarity of the applied voltage. Thus, SET can only occur at one polarity and RESET can only occur at the reverse polarity. In this paper, the study mainly focused on the bipolar RRAM due to the superior memory performance to unipolar devices.

In order to accomplish the circuit simulation, the analytical models of RRAM and selector devices are developed. In an RRAM device, $R_{\rm on}$ and $R_{\rm off}$ can be fitted well with the function as follows [30]:

$$\text{For } R_{\rm on}: \qquad I = g_1 \times V \tag{1}$$

$$\text{For } R_{\rm off}: \qquad I = g_2 \times \sinh(\alpha \times V). \tag{2}$$

In the equation, g_1 and g_2 represent the conductance of $R_{\rm on}$ and $R_{\rm off}$, and α is the nonlinear factor in the high-resistance state, which can represent the nonlinear characteristics of RRAM I–V curves. With a larger nonlinear factor α, the I–V curves may be more similar to the exponential function and become steeper. It should be noted that the model predictions can be fitted well with the measured I–V curves of the high- and low-resistance states of both bipolar and unipolar RRAM devices [30].

When we consider the selection device, a diode, a selector, and a transistor may be used for the RRAM crossbar array. However, due to the intrinsic drawback of more than $8F^2$ cell size, the 1T1R structure cannot be scaled down to an ideal size compared with other structures [20]. Thus, we mainly discuss the more promising 1S1R and 1D1R structures in this paper. The 1D1R structure is used for unipolar RRAM, whereas the 1S1R structure is used for bipolar RRAM. The selector is actually a device with bidirectional diode I–V characteristics and has been extensively studied in recent years [20], [35]–[37].

Considering that the selector is actually a bidirectional diode and the similar I–V characteristics of high- and low-resistance states of bipolar and unipolar RRAM devices, we can mainly discuss the 1S1R structure because the I–V curves of the 1D1R structure can be obtained simply by using only one polarity of the 1S1R structure and the discussion may be similar.

For a selector, we can use the function to fit the I–V curves as follows:

$$\text{For selector}: \qquad I = g \times \exp\left((V - V_{\rm on}) \times \beta\right). \tag{3}$$

In the equation, g represents the conductance of the selector, $V_{\rm on}$ is the turn-on voltage of the selector, and β is the nonlinear factor of the selector.

According to the measured data [20], I–V curves can be fitted using the analytical model of RRAM and selector devices, as shown in Fig. 2(a) and (b). The simulated I–V curves using the analytical device model can fit the experimental data well. Then, the I–V curves of a 1S1R memory cell can be simulated, as shown in Fig. 2(c). The current of low-resistance state is strongly constrained by the selector when the applied voltage is lower than the turn-on voltage in the 1S1R structure, as compared with the structure without the selector.

B. RRAM Crossbar Array Architecture

The crossbar array is composed of bit lines and word lines, and the memory cell is positioned at the cross points of bit lines and word lines, as shown in Fig. 3(a). The inset shows the memory cell structure, the selection device is in series with the RRAM device, and the memory resistance is the total resistance of the two devices.

Due to the leakage paths in the crossbar array, some problems such as output signal degradation, programming failure, and crosstalk problem may happen in the array, as shown in Fig. 3(b). During read operation, the leakage paths in the unselected cell will degrade the output signal and make it hard to distinguish the resistance states of the memory cells. Therefore, the selection device is used to annihilate this problem.

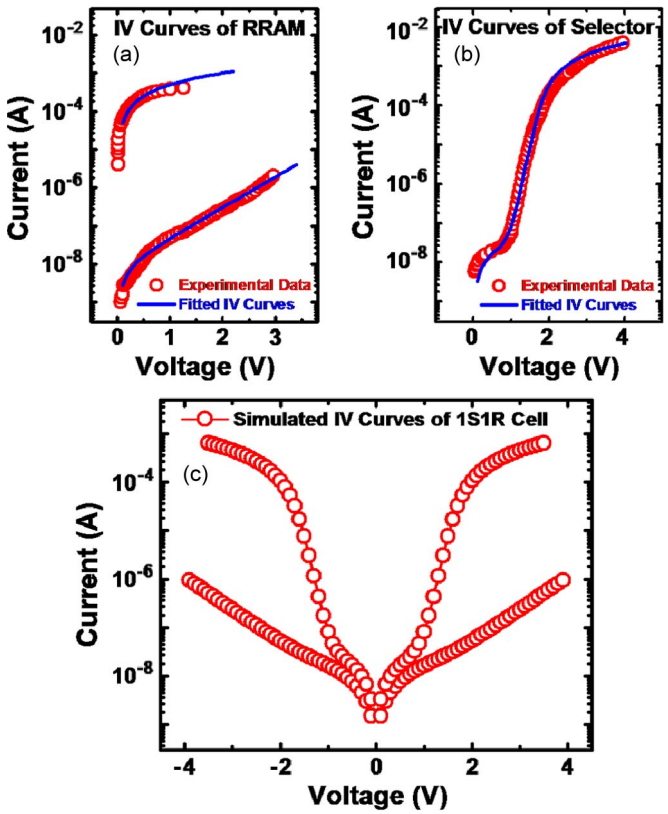

Fig. 2. Fitted I–V curves and experimental data from [20] of (a) RRAM and (b) selector based on the analytical device model. The simulated I–V curves can fit the data well. (c) Simulated I–V curves of a 1S1R memory cell. The current of low-resistance state is strongly constrained by the selector device in the 1S1R cell compared with the case without the selector.

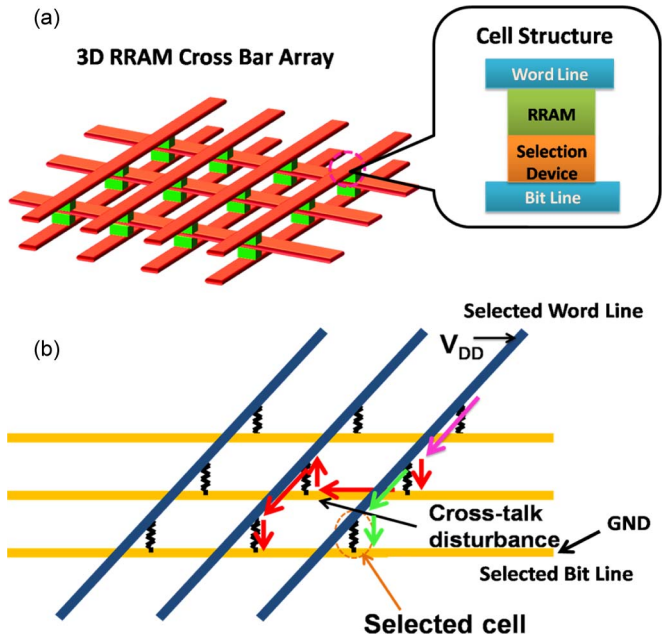

Fig. 3. (a) Schematic of the RRAM crossbar array. (Inset) Cell structure at each cross point of bit lines and word lines. The memory cell is composed of RRAM and a selection device. (b) Schematic of the leakage paths in the crossbar array. The current from (pink arrow) the voltage source may flow into (green arrows) the selected cell and (red arrows) the unselected cells. The current flowing into the unselected cells may cause output signal degradation and crosstalk problem.

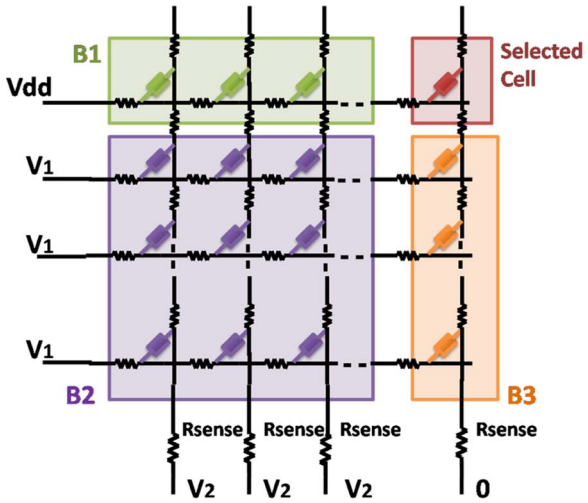

Fig. 4. Schematic of the crossbar array circuit. The memory cell, interconnect resistance, and R_{sense} are shown in the figure. V_1 and V_2 represent the voltage applied on the unselected word lines and bit lines. The unselected cells can be divided into three groups as B1, B2, and B3. The memory cells in the same group share the same resistance state, whereas in different groups, they can be different.

During the write operation, the voltage drop on the interconnect caused by the leakage path may cause the voltage drop on the selected cell insufficient to write successfully. Moreover, the crosstalk disturbance may cause some reliability problems such as misprogramming and electric stress-induced retention failure. All these problems will degrade the performance of the crossbar array and have to be investigated in detail.

In order to understand these device and circuit interaction issues in the RRAM crossbar array, a circuit simulation is used in this paper. The analytical model is put into the circuit using Verilog-A, whereas the SPICE simulation is used to study the performance of the array.

C. Read and Write Operations

The crossbar memory array is schematically shown in Fig. 4. In the circuit, V_{dd} represents the voltage source that is applied on the selected word line. The selected bit line is grounded. All the unselected word lines and bit lines are set to be V_1 and V_2, respectively, as shown in Fig. 4. Different bias methods can be used to read or write the selected memory cell in the array, such as 0 (for read operation only), floating, 1/2 V, and 1/3 V methods [34], which corresponds to different bias modes applied on unselected word lines V_1 and bit lines V_2. In 0, floating, and 1/2 V methods, all the unselected word lines and bit lines are set to be grounded, floating, and half of the voltage value of the selected word line, respectively. All the unselected word lines and bit lines are set to be 1/3 and 2/3 of the voltage value of the selected word line in the 1/3 V method.

To guarantee a successful write operation, the voltage drop on the RRAM of the selected cell must be larger than the switching voltage, whereas the voltage drop on the unselected cell should be lower than the switching voltage to avoid misprogramming.

During the read operation, to make sure that the reading process is nondestructive, the voltage drop on all the RRAM

devices should be lower than the switching voltage. Current difference ΔI, which is obtained by reading $R_{\rm on}$ and $R_{\rm off}$, is then sensed by connecting all the bit lines to sense amplifiers (SAs), which act as current-to-voltage converters, and thus, the resistance states can be detected this way. An example of an SA is a simple current mirror or an operational amplifier with a feedback resistor to sense the current. (The design of SAs is not part of this paper, and the peripheral sensing circuits are not included in the simulation.) Due to the existence of parasitic leakage current paths distorting the real signal and the additional degradation caused by the parasitic interconnect resistance, the voltage difference (ΔV or readout margin) diminishes, and thus, the signal-to-noise ratio is degraded. The degradation will become much more serious when the array size increases, and then the array size may be constrained by the degradation of the readout margin. Therefore, in a certain array with a limited size, a larger readout margin means a potential for a larger array size under certain device and circuit characteristics. To maintain the readout margin when the array size increases (or to enlarge the readout margin in a certain array size), device and circuit characteristics need to be optimized, which will be discussed later in this paper.

Moreover, the input resistance (i.e., $R_{\rm sense}$, as shown in Fig. 4) of the SAs should be considered. We assume that the input resistance $R_{\rm sense}$ of the SAs is the same for all conditions, and the readout voltage is detected from $R_{\rm sense}$. The transresistance $R_{\rm tran}$ of the SAs has to be considered. However, in practice, $R_{\rm tran}$ must be within a certain range for the speed, area, and power considerations, and the maximum array size is also directly related to the properties of SAs. All these problems will make the discussion too complicated; hence, in this paper, we only detect the voltage difference (ΔV or readout margin) on $R_{\rm sense}$. The $R_{\rm sense}$ in the following simulation is set to be 2 kΩ. The interconnect resistance between two adjacent junctions is 2.8215 Ω for a $4F^2$ crossbar structure according to the International Technology Roadmap for Semiconductors for 22-nm technology node [33].

III. Worst Case Discussion

A. Worst Case Selected Cell

The location of the selected cell will strongly influence the write and read operations. Readout margin and access voltage dropped on the selected cell can be different with different locations of the selected cells during read and write operations, respectively. We find that the worst case scenario of the selected cell during read and write operations is the one that is located at the farthest corner from the word- and bit-line sources, as shown in Fig. 4. In this case, the voltage dropped on the selected cell is the smallest during write operation and the readout margin is the smallest during read operation. All the following discussions are based on this worst case scenario.

B. Worst Case Data Pattern

Different data patterns of the unselected cells strongly influence the write and read operation performance. In order to investigate this issue, we divide the unselected cells into three groups, as shown in Fig. 5. All the cells in the same group share the same resistance state, but the resistance state of the cells in different groups can be different.

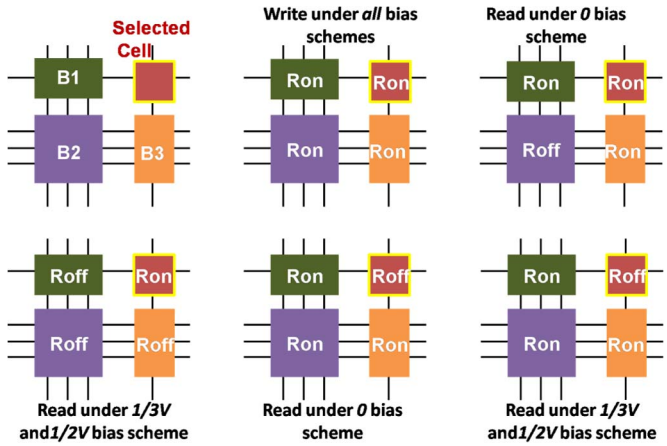

Fig. 5. Schematics of the worst case data pattern during read and write operations. The worst case for different resistance states of the selected cell may be different. In the write operation, the worst case is when all the cells are in $R_{\rm on}$, whereas in the read operation, the worst case is different under different bias modes.

During the write operation, the worst case data pattern is the case that all the cells are in low-resistance state, as shown in Fig. 5. In this case, the leakage current may be the largest, resulting in the largest degradation of the access voltage on the selected cell.

During the read operation, the worst case scenario is the case in which the readout margin is the smallest. In our simulation, it means that the voltage drop on $R_{\rm sense}$ is the largest when the selected cell is in high-resistance state and is the smallest when the selected cell is in low-resistance state. The worst case data patterns are different under different bias methods, as shown in Fig. 5. Although this three-group division method is a simplification method, the extreme condition can be outlined. More detailed analysis on data pattern can be found in [32].

Based on the worst case scenario, the performance of different bias modes is obtained. For different bias modes, we can find that the 1/3 V method gets a better performance at maintaining the readout margin as the array size increases using circuit simulation. In the following part of this paper, all the simulation work is based on the 1/3 V bias method and the data patterns are set to be the worst case discussed above. The array size is set to be 128 $\times$ 128, and the memory cell is 1S1R structure. All the voltage shown in the figures represents the voltage applied on the selected word line during read operation and is set to be 2 V, if it is not stated in advance. All the simulation parameters are listed in Table I.

IV. Device Characteristics Variation

A. RRAM Device Characteristics Variation

Based on the analytical model we described earlier, the variation of the RRAM I–V characteristics can be simulated. As shown in Fig. 6, the RRAM I–V curves vary with the increase in the conductance of $R_{\rm on}$ (g_1) and $R_{\rm off}$ (g_2) and the

TABLE I
SIMULATION PARAMETERS USED IN THIS PAPER

Parameters	Values
Array size	128×128
Conductance of R_{on} of the RRAM (g_1)	5.0×10^{-4}
Conductance of R_{off} of the RRAM (g_2)	1.5×10^{-8}
Nonlinear factor of the RRAM (α)	1.85
Conductance of the selector (g)	4×10^{-7}
Turn-on voltage of the selector (V_{on})	1.2V
Nonlinear factor of the selector (β)	10.5263
Interconnect resistance (R_{wire})	2.8215Ω
Input resistance of amplifier (R_{sense})	2kΩ
Voltage at selected word line (V_{dd})	2V
Voltage at selected bit line	0

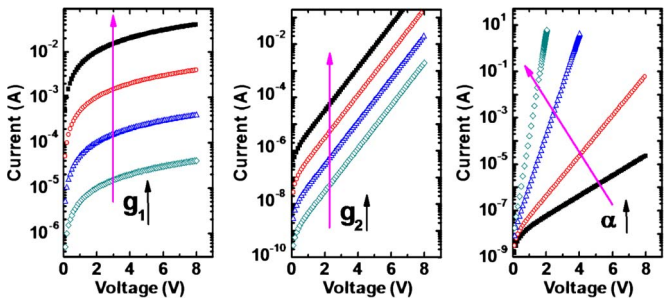

Fig. 6. Variation of the RRAM I–V curves as the variation of the $R_{\rm on}$ and $R_{\rm off}$ characteristics in the analytical model. The impact of the increase in the conductance of $R_{\rm on}$ (g_1) and $R_{\rm off}$ (g_2) and the nonlinear factor α of $R_{\rm off}$ is simulated. The increase in the conductance of different resistance states results in a larger current at a constant voltage, whereas the I–V curves become steeper with a larger nonlinear factor α.

nonlinear factor α of $R_{\rm off}$, which can represent the main I–V characteristics of RRAM.

First, we focus on the impact of conductance variation on the read operation. We change the conductance of $R_{\rm on}$ (g_1) and $R_{\rm off}$ (g_2), and the corresponding variation of the readout margin ΔV is shown in Fig. 7. The variation range of the conductance of $R_{\rm on}$ and $R_{\rm off}$ is considered based on the fitted experiment data as aforementioned. The red region means a larger readout margin, and the white region (also part of the dark blue region in the upper figure, which is hard to distinguish, hence we make it white in the lower figure) means that the readout margin in this region is 0 or below zero. This is because the worst case for the $R_{\rm on}$ or $R_{\rm off}$ of the selected cell is different. Under a common condition, the detected voltage of $R_{\rm on}$ may be larger than that of $R_{\rm off}$, which results in a positive readout margin. However, when the resistance of $R_{\rm on}$ increases, the readout margin may become zero or even below zero due to the different worst case for $R_{\rm on}$ and $R_{\rm off}$ of the selected cell. Thus, a too large resistance of $R_{\rm on}$ may be unacceptable for read operation. According to [30], a large resistance of $R_{\rm on}$ may be beneficial for low leakage current and low power consumption in the purely passive array. However, the selection devices in the crossbar array strongly constrain the leakage current; hence, the impact of resistance of $R_{\rm on}$ on constraining leakage current is weak. Thus, a lower resistance of $R_{\rm on}$ is preferred when the selection device is used in the circuit. Furthermore, the results show that a lower $R_{\rm on}$ resistance and a higher $R_{\rm off}$ resistance are beneficial for a large readout margin, which reflects the need for a large resistance

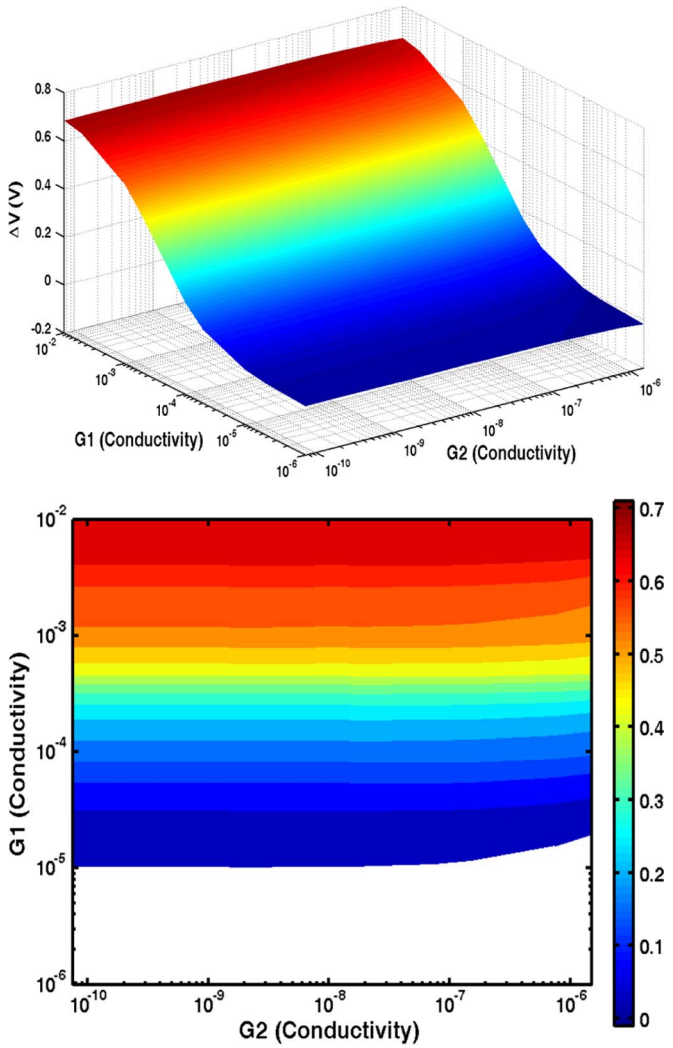

Fig. 7. Readout margin as a function of the conductance of $R_{\rm on}$ (g_1) and $R_{\rm off}$ (g_2). The red region means a larger readout margin, and the white region means a zero or below zero readout margin. It shows that a higher $R_{\rm off}$ and a lower $R_{\rm on}$ are needed for a larger readout margin. In a circuit with the selection device, a lower $R_{\rm on}$ is preferred, whereas a higher $R_{\rm on}$ is preferred in a circuit without the selection device [30]. Furthermore, the optimization of $R_{\rm on}$ is more efficient as the impact of variation of $R_{\rm on}$ is much stronger than that of $R_{\rm off}$.

ratio of $R_{\rm off}$ and $R_{\rm on}$. As shown in Fig. 7, the impact of variation of the conductance of $R_{\rm on}$ is much stronger than that of $R_{\rm off}$. Therefore, it is more efficient to optimize the resistance of $R_{\rm on}$ than that of $R_{\rm off}$ to get a larger readout margin in this condition.

The nonlinear characteristics of RRAM I–V curves may be beneficial for read operation according to [31]. However, in an array with a selection device, the effect of nonlinear characteristics should be discussed in detail. As shown in Fig. 8, the normalized readout margin gets smaller when the nonlinear factor α of $R_{\rm off}$ increases. The nonlinear characteristics may be beneficial for leakage current constraining, but the increase of it may result in a lower $R_{\rm off}$ and $R_{\rm on}$ ratio and the effect is more obvious at a higher reading voltage, as shown in Fig. 8. This is because the I–V curve of $R_{\rm on}$ is constant and the increase in nonlinear factor α causes the I–V curve of $R_{\rm off}$ to be steeper; hence, the resistance ratio of $R_{\rm off}$ and $R_{\rm on}$ becomes smaller. Therefore, the nonlinear characteristics of $R_{\rm off}$ are detrimental

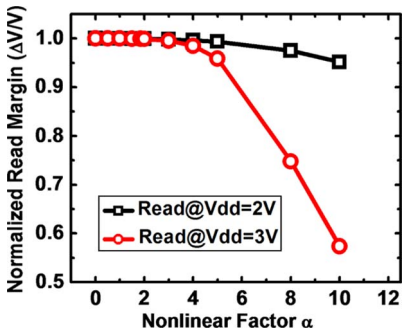

Fig. 8. Normalized readout margin as a function of the nonlinear factor α of $R_{\rm off}$. A larger nonlinear factor α may get a smaller readout margin, and the effect is more obvious when a larger read voltage is applied. The nonlinear characteristics of $R_{\rm off}$ may be detrimental to the readout margin.

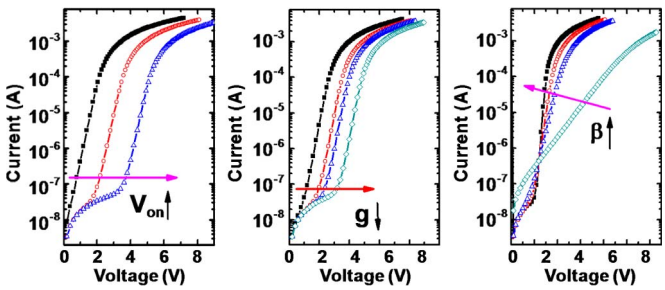

Fig. 9. Variation of the turn-on voltage $V_{\rm on}$, conductance g, and nonlinear factor β of the selector device and its impact on the I–V curves using the analytical model described earlier. The variation of turn-on voltage $V_{\rm on}$ and conductance g shares the similar variation trend of I–V curves, whereas the increase in nonlinear factor β results in steeper I–V curves.

to the readout margin in this condition. However, due to the analytical model we used, the nonlinear characteristics of $R_{\rm on}$ are not discussed here. Because of the metallic conduction mechanism in low-resistance state, the I–V curves of $R_{\rm on}$ are linear in many cases. Therefore, the discussion here may be useful for the understanding of the general cases.

B. Selection Device Characteristics Variation

The characteristics of the selection device have strong impact on the performance of the crossbar array. In this part, we will discuss the variation of the characteristics of the selector and its impact on the read operation.

As shown in Fig. 9, the variation of the I–V characteristics of the selector is obtained using the analytical model aforementioned. The variation of turn-on voltage $V_{\rm on}$, conductance g, and nonlinear factor β results in a different variation trend of I–V curves.

The impact of the variation of the selector characteristics on the readout margin is shown in Fig. 10. The impact of the variation of turn-on voltage $V_{\rm on}$ and nonlinear factor β on the readout margin is shown in the figure. For the turn-on voltage, an optimal point can be obtained, which means that an optimized value of the turn-on voltage of the selector can be found under certain device and circuit characteristics. When the turn-on voltage is too high, the voltage drop on the selected cell may be reduced, and thus, the $R_{\rm off}$ and $R_{\rm on}$ ratio of RRAM at that voltage may be too small, resulting in a small readout margin. When the turn-on voltage is too low, the

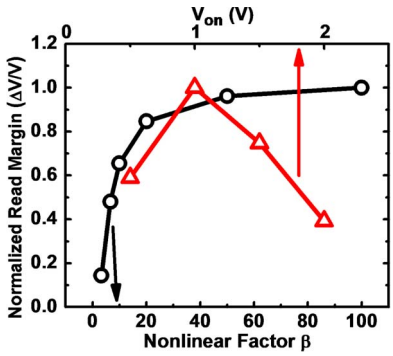

Fig. 10. Readout margin as a function of the turn-on voltage $V_{\rm on}$ and nonlinear factor β of the selector. An optimal point can be obtained for turn-on voltage $V_{\rm on}$, whereas a larger nonlinear factor β may result in a larger readout margin.

leakage current cannot be efficiently constrained, also resulting in a small readout margin. For the conductance of the selector, a similar variation trend of I–V curves to the turn-on voltage is shown in Fig. 9; hence, an optimal point may be also obtained (not shown here). The explanation of the phenomenon is also the same as the analysis of turn-on voltage.

For the nonlinear characteristics, a larger nonlinear factor β may result in a larger readout margin, as shown in Fig. 10. This may be attributed to the larger on/off ratios of the selector as nonlinear factor β increases, as shown in Fig. 9. Therefore, an optimized turn-on voltage $V_{\rm on}$ and conductance g and a higher nonlinear factor β are beneficial for a larger readout margin (i.e., array size).

Based on the method aforementioned, different experiment data of different RRAM devices and selectors can be fitted by the analytical model and the circuit performance can be obtained using the simulation method. Then, the optimization of the device and circuit characteristics can be accomplished based on the simulation results.

However, the discussion about device characteristics here is only based on the readout margin (i.e., array size). The performance of the circuit, such as speed, power consumption, and reliability issues, should be considered comprehensively, which is our ongoing work.

V. Conclusion

An analysis of device and circuit interaction in an RRAM crossbar array considering the variation of RRAM/selector I–V characteristics and their impacts on readout margin (i.e., array size) has been conducted using the developed circuit simulation method. The existence of the selector eliminates the need for high $R_{\rm on}$ resistance, whereas a large $R_{\rm off}$ and $R_{\rm on}$ ratio is still needed for a large readout margin. The readout margin is more sensitive to the variation of $R_{\rm on}$. An optimal value can be obtained for the turn-on voltage and conductance of the selector to get a larger array size. The nonlinearity of the RRAM may be detrimental to a large readout margin, whereas the nonlinearity of the I–V curves of the selector is beneficial for a large readout margin. This paper may provide a simulation method and a guideline for device and circuit design and optimization of an RRAM crossbar array from a circuit and device interaction point of view.

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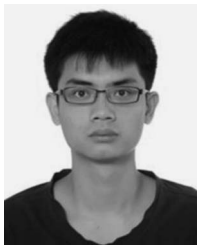

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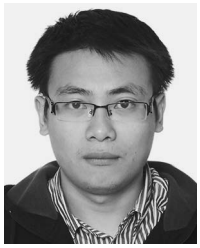

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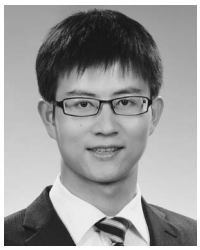

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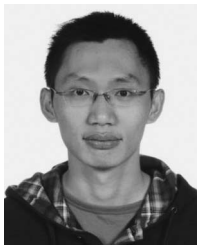

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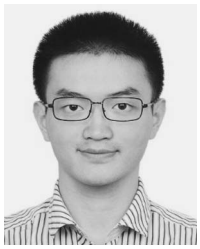

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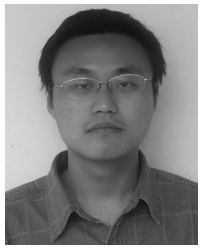

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