A 0.13μm 8Mb Logic Based Cu_xSi_yO Resistive Memory with Self-Adaptive Yield Enhancement and Operation Power Reduction

X. Y. Xue, W. X. Jian, J. G. Yang, F. J. Xiao, G. Chen, X. L. Xu, Y. F. Xie, and Y. Y. Lin*
ASIC and System State Key Laboratory, Fudan University, Shanghai, 200433, China
R. Huang, Q. T. Zhou, and J. G. Wu
SOC Technology Development Center, Semiconductor Manufacturing International Corp., Shanghai, 201203, China
*Email: yylin@fudan.edu.cn

Abstract

A 0.13μm 8Mb Cu_xSi_yO resistive memory test macro with $20F^2$ cell size is developed based on logic process for the first time. Smart and adaptive assist write and read circuit are proposed and verified in order to fix yield and power consumption issues from large write speed and high temperature resistance variation. SAWM (self-adaptive write mode) helps to enlarge R_{off}/R_{on} window from 8X to 24X at room temperature. The reset bit yield is improved from 61.5% to 100% and large power consumption is eliminated after set success. SARM (Self-adaptive read mode) improves read bit yield from 98% to 100% at 125℃. The typical access time of on-pitch voltage sensing SA(sense amplifier) is 21ns and high bandwidth throughput is supported.

Keywords: RRAM, SAWM, SARM, on-pitch SA, yield

Introduction

Several resistive memory (RRAM) test chips have been reported with high bandwidth or quick access time circuits based on CBRAM or metal oxide.[1-3] However, some yield and power consumption issues caused by large write speed and high temperature resistance variation are not addressed yet. In this work, we demonstrate a 0.13μm 8Mb Cu_xSi_yO RRAM macro based on logic process with smart and adaptive circuit assisted yield enhancement and power consumption reduction.

Adaptive Dynamic Write Mode

The set power consumption and reset yield issues are described in Fig.1. The set and reset algorithms are SVP (a single voltage pulse) mode and RPS (a ramped-pulse series) mode respectively, as same with our previous work [4]. The measurement results show large set/reset speed variation. In order to meet set yield requirement or decrease reset ramped pulse number, the set and reset pulse duration are usually longer than fastest speed. Hence, large set power consumption is caused because high current will flow through the low resistance after set success for those fast speed cells. Besides, write disturbance leads to reset fail because fast speed cells are set to low resistance again after reset succeed. This also causes wide R_{off} distribution and decrease R_{off}/R_{on} margin.

SAWM (self-adaptive write mode) for both set and reset is proposed to fix above-mentioned issue. Fig. 2 shows the schematic and simulation results. The write drive (WD) circuit consists of a SAWM module, a verdict module, a Vref generator, a polarity selector etc. The SAWM module detects the write current IWRITE through the cell and generates a marking signal FB for the verdict module to control the Vref generator. During reset operation, IWRITE will decease instantly after reset success and the SAWM module will change FB from high to low. Then, the verdict module will change its output COMP from high to low to turn off the Vref generator. Consequently, the reset stimulus pulse is cut from the written cell to avoid write disturbance after reset success. During set operation, IWRITE will increase instantly after set success, and the SAWM module will change FB from low to high. Then the verdict module will switch COMP from high to low to turn off the Vref generator. The set stimulus pulse is cut off and then the large set power consumption after set success is eliminated. The response time of SAWM for reset and set are as fast as 1.9ns and 1.8ns respectively.

Adaptive Dynamic Read Mode

RRAM resistance has large variation at high temperature, especially, R_{off} distribution extends to low resistance direction more seriously than R_{on} does [5]. R_{off}/R_{on} window degradation leads to read fail issue at high temperature. SARM (self-adaptive read mode) is proposed to fix the issue. Different from ref. array independent of main memory [2], two dummy rows divides one block in half and share the same decoder and WD with the main array, which ensures low peripheral overburden and tracking high resistance variation of main array more accurately. Voltage sensing sense amplifier (SA) is embedded on-pitch to get high array efficiency and support high bandwidth. A read operation activates a row in one half and enables corresponding dummy row in the other half. The BL/BLBs of selected dummy row are shorted by activating the corresponding equalization signal (EQ0 for left/EQ1 for right). Thus the averaging of dummy cells makes sensing reference. The dummy row is configured here as one R_{on} every 7 R_{off} according to the resistance distribution in Fig. 5 measurement at room temperature. This can make reference locate in the middle of HRS and LRS. Hence large sensing margin is acquired for both 1 and 0. The reference can adaptively track the resistance PVT variation and move dynamically to low resistance direction at high temperature, as shown in Fig.4, which can ensure enough sensing margin at high temperature. There is no read disturbance issue in positive voltage direction, as shown in Fig. 1. This advantage is taken to increase read voltage as high as 0.6V in order to ensure large sense margin.

Measurement Results

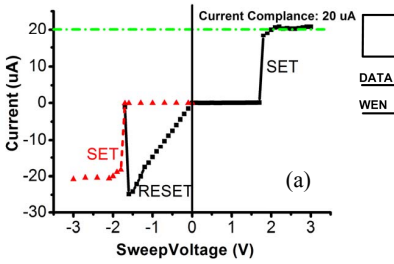
An 8Mb Cu_xSi_yO RRAM test chip is fabricated base on 0.13μm logic process as our previous work.[5] SAWM helps to concentrate HRS distribution significantly and R_{off}/R_{on} ratio is enlarged from 8X to 24X, as shown in Fig.5. SAWM improves reset bit yield from 61.5% to 100%, while SARM improves read bit yield from 98% to 100%, as shown in Fig.6. Fig. 7 shows the measured typical access time of 21ns. Fig. 8 shows the cell layout of $20F^2$, die micrograph and key parameters.

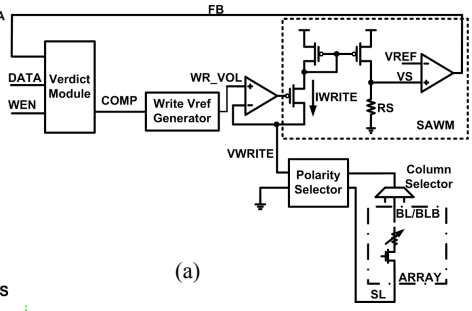
Conclusion

Self adaptive assisted write and read circuits of SAWM and SARM are proposed to fix yield and power consumption issues, which is verified in a 0.13um 8Mb Cu_xSi_yO RRAM test macro.

References

[1] W. Otsuka et al., ISSCC, pp. 210-212, 2011; [2] S.S. Sheu et al., ISSCC, pp. 200-202, 2011; [3] P. Schrogmeier et al., Symp. on VLSI Circ., pp. 186-187, 2007; [4] M. Yin et al., EDL, pp. 681-683, 2008; [5] M. Wang et al., Symp. on VLSI Tech., pp. 89-90, 2010.





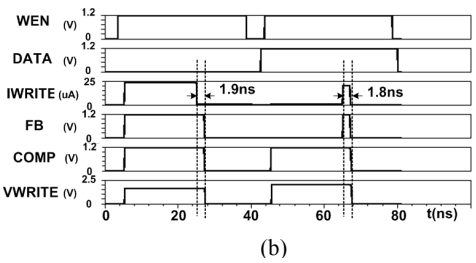
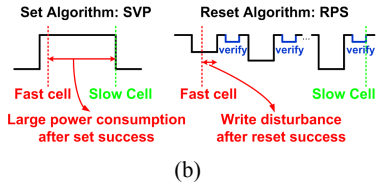


Fig.2 (a) Write driver with self-adaptive write mode (SAWM) (in dotted box) for both set and reset. (b) Simulation waveforms. The response time of SAWM for reset and set are 1.9ns and 1.8ns respectively.



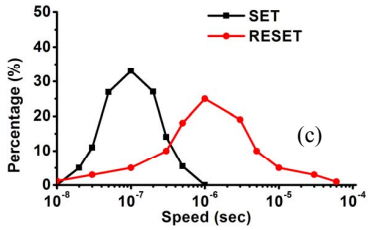


Fig.1 (a) Cu_xSi_yO RRAM I-V curve. Positive voltage can realize set, however, negative voltage can realize both set and reset. (b) SVP and RPS algorithm for set and reset respectively. (c) Set speed based on SVP distributes from 10 to 100ns. Reset speed based on RPS distributes from 10ns to 60µs. Fixed set and reset pulse at slowest case will lead to large set power and reset fail.

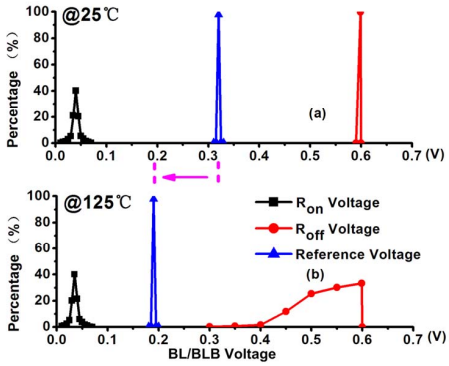


Fig.4 Monte Carlo simulation for SARM based on 1000 samples (a) @25℃ and (b) @125℃. The dummy row is configured as one R_{on} every 7 R_{off} to make reference locate in the middle between HRS and LRS in order to get large sensing margin for both R_{off} and R_{on}. The reference adaptively dynamically moves towards low resistance direction to ensure enough sense margin at 125℃. There is no read disturbance issue in positive voltage direction, as shown in Fig. 1. This advantage is taken to increase read voltage as high as 0.6V in order to ensure large sense margin.

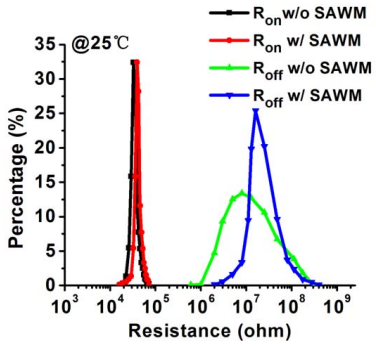


Fig.5 SAWM for reset with RPS together significantly concentrates R_{off} distribution. Hence R_{off}/R_{on} ratio is enlarged from 8X to 24X.

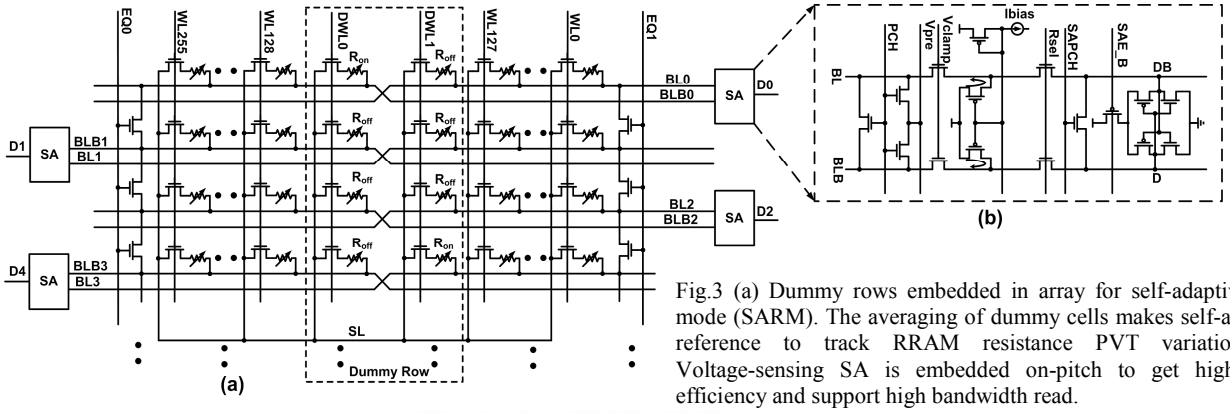
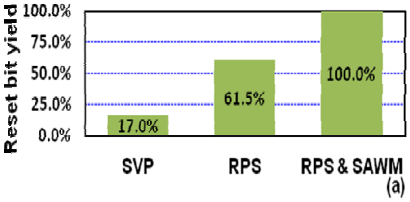


Fig.3 (a) Dummy rows embedded in array for self-adaptive read mode (SARM). The averaging of dummy cells makes self-adaptive reference to track RRAM resistance PVT variation; (b) Voltage-sensing SA is embedded on-pitch to get high array efficiency and support high bandwidth read.



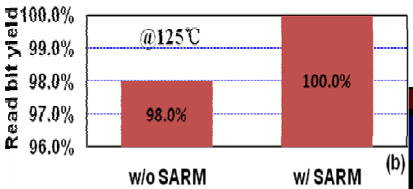


Fig.6 (a) SAWM with RPS together fixes reset bit yield issue; (b) SARM fixes read bit yield issue at 125℃.

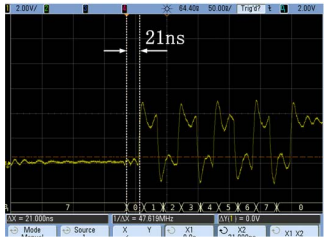
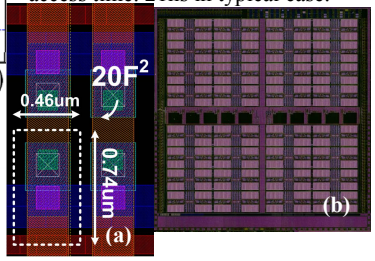


Fig.7 Measurement results of access time: 21ns in typical case.



process	0.13µm Logic based
storage media	Cu_xSi_yO
capacity	8Mb
cell size	0.46*0.74µm^2 (20F^2)
organization	256 row * 256 column * 8 block * 16 plane , dummy rows for SARM embedded in block array
supply power	1.2V / 3.3V
read access time	21ns typically
Reset yield enhancement feature	SAWM, reset bit yield improves from 61.5% to 100%
Set power reduction feature	SAWM for set
Read yield enhancement feature	SARM, read bit yield improves from 98% to 100% at 125℃.

Fig.8 (a) cell layout with cell size of 20F^2, (b) die micrograph and key parameters