Analysis of the Effect of Cell Parameters on the Maximum RRAM Array Size Considering Both Read and Write

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***Abstract*— A numerical framework is developed to analyze the requirements of Self-Rectifying Resistive RAM cells for using in cross-point arrays. This paper analyzes the relation between maximum array size and cell characteristics, such as non-linearity, absolute current level and on/off ratio. Furthermore, optimal bias conditions are determined, and the advantage compared to a standard ½ voltage bias scheme is discussed.**

I. INTRODUCTION

Resistive RAM (RRAM) cross-point arrays are a very promising option for future storage memories, as they are expected to scale beyond the limits of flash technology due to their smallest cell footprint ($4F^2$) and simple fabrication structure. However, single 1R memory structure has its intrinsic drawbacks. The leakage current through the unselected cells degrades the accessibility to a specific device in the array. This reduces the output signal swing for distinguishing the different states of a selected cell and increases the power consumption of the application. To overcome these problems, concepts like using separate selectors (e.g. diode or transistor in series with a resistive element, 1S1R) or Self-Rectifying (selectorless) Cells have been proposed [1, 2]. Although they are conceptually effective, to what extent they improve the circuit performance remains questionable.

Several papers have studied the impact of cell behavior on the cross-point array performance using analytical approaches [3-5]. However, errors remain due to inexact assumptions (e.g. over-simplified device characteristics, over-look parasitics, etc.). Analysis based on circuit simulations will be useful but still not available at present. This work presents a comprehensive Matlab-level DC analysis that determines the required cell characteristics (e.g. non-linearity, current levels, on/off ratio) as a function of desired array size under the worst read and write scenarios.

The remainder of this paper is outlined as follows. The implemented constraints in the simulation are discussed in section II. In section III, the simplified cross-point memory architecture and simulation setup are described. The device characteristic requirements using the optimized bias scheme are analyzed and the results are compared to a standard ½ voltage bias scheme in Section IV. Finally, in Section V the conclusions are presented.

II. IMPLEMENTED CONSTRAINTS

The maximum matrix size that can be constructed with a given cell is limited by several factors. This section details the constraints that are considered in this work.

A. Limitation from a System Perspective

The lowest energy values reported for single-level cell NAND flash products are 42pJ/bit for read, 410pJ/bit for program [6] (data from different products, values include the energy consumption of the peripheral circuits). As compared to NAND flash, Resistive RAM seems to be very promising for the purpose of energy saving since most of the energy consumption of NAND flash is due to the high voltages involved, requiring the use of charge pumps. Resistive RAM operates at much lower voltages. However, as the selectivity of the cells in two-terminal resistive memory cross-point arrays tends to be rather poor, the partially biased cells have fairly large leakage currents, and hence the leakage power is more pronounced in these cross-point arrays.

B. Limitation from the Techonology

Beyond 10nm technology node, the resistivity of Cu increases significantly due to the 'size effect' of Cu wire [7], which leads to a large voltage drop over the wire (Word-Line and Bit-Line). This effect degrades the accessibility to a specific cell in the array since the cell sees a smaller access voltage while cell disturbance may happen at the beginning of the line. Moreover, the current density in Cu wires increases as well. Once the current density reaches the Electro-Migration (EM) threshold, it may cause serious reliability problems. These two factors limit the maximum program current of a resistive memory as well as the acceptable leakage current on the selected WLs and BLs.

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C. Limitation from the Device

Cell disturbance voltage ($V_{disturb}$) is another important limitation in cross-point resistive memory array. Disturbance determines the maximum voltage that can be applied over the unselected cells in the write operation. Otherwise the state of the cell could be changed. Similarly, the read voltage cannot be larger than $V_{distrub}$ either to avoid destructive read.

III. RRAM CELL 'DEVICE' TEMPLATE AND SIMULATION SETUP

A. Array Configuration

To simulate large arrays, we are interested in the behavior of the RRAM cell under the worst case scenario. In our analysis, the wire resistances are not explicitly taken into account. Rather, we account for these resistances by imposing a maximum current through the wires. This way, all cells in the matrix can be categorized into four groups. Fig.1 shows the simplified array configuration. It is clear that the voltage over the selected cell is equal to the sum of the voltages over the WLHS cells, the NS cells and the BLHS cells. Notice that the NS cells are reverse biased compared to the other cells. One bit per matrix is assumed to be selected. Therefore, only one selected cell can be written or read. In our analysis, we optimize the biasing conditions of both the selected and unselected WLs and BLs.

B. RRAM Cell Device Template

Any cell element (i.e., combining selector and RRAM element as in a 1S1R cell, or using a Self-Rectifying Cell) I-V curves can be put into the framework. However, to investigate the requirements for a cell element, the I-V characteristics (i.e. in both on and off state) of the RRAM cell are abstracted into a device template. Fig.2(a) shows the device template as used in our simulations. The non-linearity in the region [0, $V_{disturb}$] is the most important because the unselected cells are biased in this range in any operation conditions. The cell non-linearity parameter S is defined as the ratio of the current read at $V_{disturb}$ and ½ $V_{disturb}$. We assume symmetrical I-V behavior with $|V_{set}|=|V_{reset}|=V_{write}$. (i.e. bipolar-switching). This template is more flexible and better suited to describe actual cell characteristics than previously used templates, such as a parabolic shape [5]: $I(V)=aV+bV^2$, Fig 2.(b) compares the template with an actual cell [1].

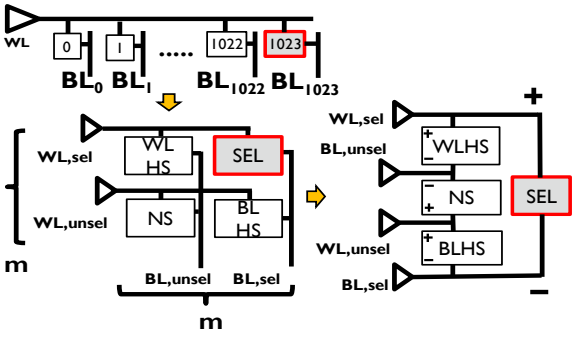

Fig 1. Simplified m x m (square) array. The four main elements are the selected cell (SEL, the cell farthest from the voltage source under the worst case operation condition), the Bit-Line Half Selected (BLHS) Cells, the Word-Line Half Selected (WLHS) Cells and the Non-Selected (NS).

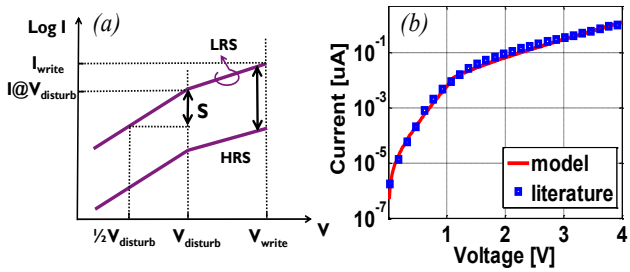

Fig 2. (a) Device template. V_{write}: program voltage, I_{write}: program current, $V_{disturb}$: disturbance voltage, $I@V_{disturb}$: current read at $V_{disturb}$, S: Non-linearity factor. Note that $V_{disturb}$ is also the maximum read voltage. (b)Template fit of an actual cell behavior (e.g. LRS I-V) [1].

To limit the complexity of the generated conclusions, we further simplify the template by fixing some of the parameters.

1) V_{write} is fixed at 1V.
2) I_{write} is set at 1uA, which is close to the max. current that can be supported for a 1024x1024 array in 10nm technology node due to the voltage drops across the wire[8] and EM limitation [9] (constraint II.B).
3) $V_{disturb}$ =1/2V_{write} =max. read voltage (constraint II.C).
4) As for HRS (off-state) current of this cell, all the current are scaled according to the cell on/off ratio.

C. Worst Case Patterns

Write operation: The worst case array pattern for the write operation is that all memory cells are in the LRS (on-state). This results in the highest leakage currents. On the selected word-line and bit-line, this results in the largest voltage drop. For the NS cells, this leads to the highest power consumption.

Read operation: The current on the selected BL is the sum of the read current of the selected cell and the current of the BLHS cells. Define 'read window' as the worst case current ratio between read of an LRS cell (with all the BLHS cells in HRS) and read of an HRS cell (with all the BLHS in LRS).

D. Write Operation Analysis

From Fig.1, an easy way to check whether a combination of cell properties and matrix size allows a functional write operation or not is to determine the max. voltage over each group of cells while taking into account all the constraints. Then, sum the values, and compare this to the cell program voltage. Fig.3 shows the applied constraints and the basic principle of determining the maximum voltage over each cell.

E. Read Operation Analysis

We optimize the read window, including optimization of the bias on the selected and the non-selected BLs and WLs while meeting the input constraints (i.e. maximum voltage can be applied across the WLHS, BLHS and NS cells). A successful read operation requires sufficient signal for the sense amplifier under the worst case conditions. To ensure this, we impose a minimum required read current (e.g. 10nA). After the read window optimization, we check whether a sufficient read window is achieved.

All constraints used in simulation are listed in Table.I.

TABLE I. Constraints Value Used in the Simulation

	$V_{disturb}$	$I_{constraint}$	Energy/bit	Access time	R_{wire}/sq[8]
Write	0.5V	≤1uA	50pJ/bit	1us	20ohm
Read	0.5V	≥10nA	25pJ/bit	1us	20ohm

Compared to NAND flash: $E_{program}$=410pJ/bit ,E_{read}=42pJ/bit ,$t_{program}$=100us,t_{read}=1us [6]
$I_{constraint}$:max. write current and min. read current
$V_{distirub}$=1/2 V_{write}

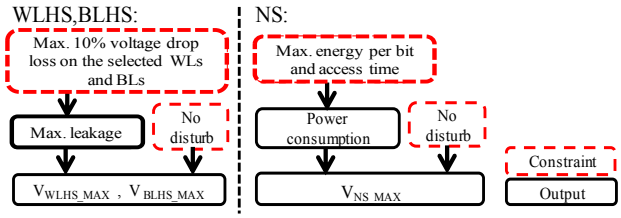

Fig 3. For both write and read, maximum voltage over the HS cells is determined by the voltage drop (constraint II.B) and disturbance (constraint II.C). Power consumption (constraint II.A) and disturbance (constraint II.C) determines maximum voltage over the NS cells.

IV. Results and Discussion

A. Write Operation

1) Influence of Non-linearity S

Fix $I@V_{disturb}$ =0.5uA in our template and sweep the non-linearity parameter S to check the influence of non-linearity on the write performance. Fig.4(a) shows the calculated max. voltage over the selected cell as a function of array size. A larger array size can be achieved with larger values of S, as a higher non-linearity allows to apply a larger voltage over the NS and HS cells without exceeding the leakage constraints.

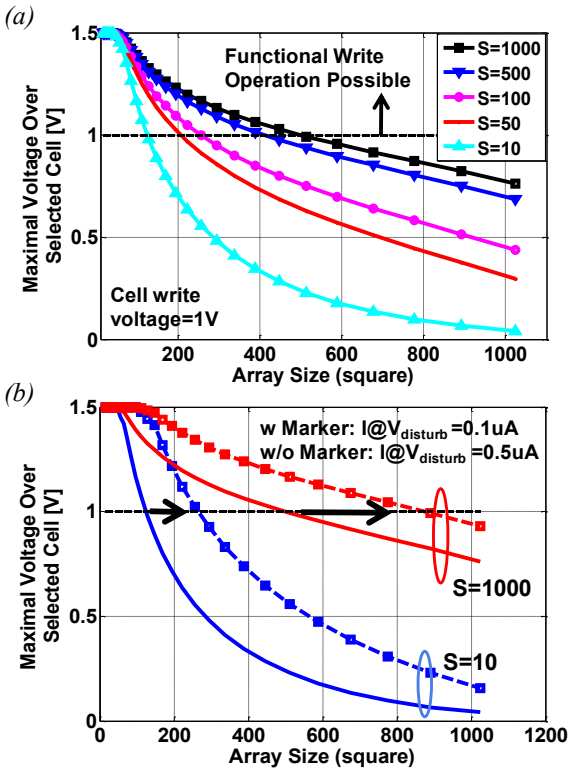

Fig 4. (a) Max. voltage over the selected cell vs. array size for cell with different non-linearity S, curves intersect the required program voltage for our template device (i.e.1V), the cross-points indicate the maximal array size can be achieved (b) Lower $I@V_{disturb}$ also allows larger array size.

2) Influence of $I@V_{disturb}$

Fix the S parameter while changing the $I@V_{distrub}$, Fig.4(b) shows that larger array sizes can also be accomodated by decreasing $I@V_{disturb}$.

B. Read Operation

1) Influence of Non-linearity S

Fix $I@V_{disturb}$ =0.5uA, cell on/off ratio at 10 and sweep the S parameter. Assume that the minimum read window required to distinguish different states of the cell is two. Fig.5 (a) shows that increasing the non-linearity factor S also improves read performance. However, the benefit of increasing S is limited by the read window staircase behavior due to the leakage current constraints. Initially, optimized max. read window smoothly decreases as the array size increases. In this region, the read voltage is optimized at $V_{disturb}$ to allow maximum read current. The reduction of read window is entirely due to the increasing contribution of bit-line leakage current (more cells more leakage paths). Once the leakage current increases up to the applied constraints, the only way to increase further array size is to lower the voltage over the unselected cells, which means the read voltage applied to the selected cell has to be reduced as well.

2) Influence of $I@V_{disturb}$

Lowering $I@V_{disturb}$ directly improves the read window. Fig.5 (b) shows that the cells with larger $I@V_{disturb}$ require a

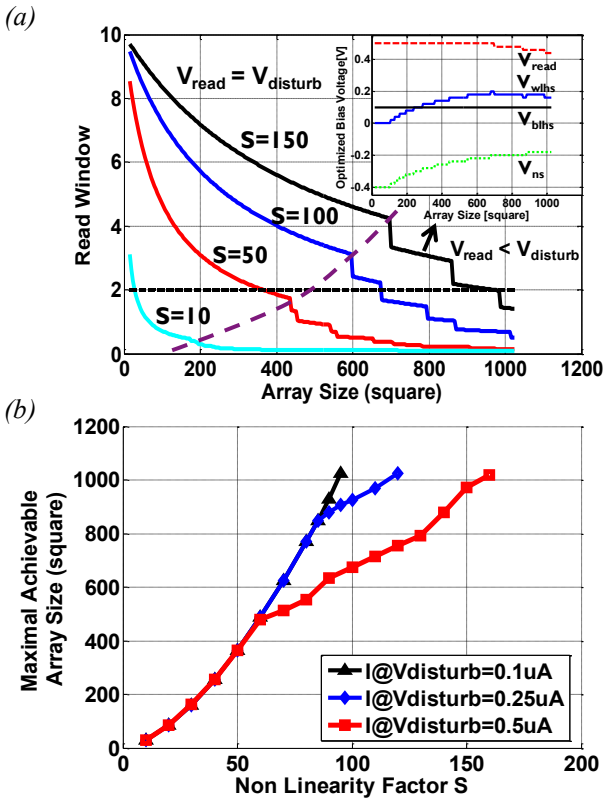

Fig 5. (a) Optimized read window vs. array size for cells with different non-linearity. Inset: example of optimized bias voltage vs. array size for cell with non-linearity S=150. Read window staircase behavior due to the discrete optimization step for the bias voltages. For sufficient sense amplifier signal: Vblhs≥100mV is required in the simulation (b) Cells with larger $I@V_{disturb}$ require a larger non-linearity to accomodate the same array size.

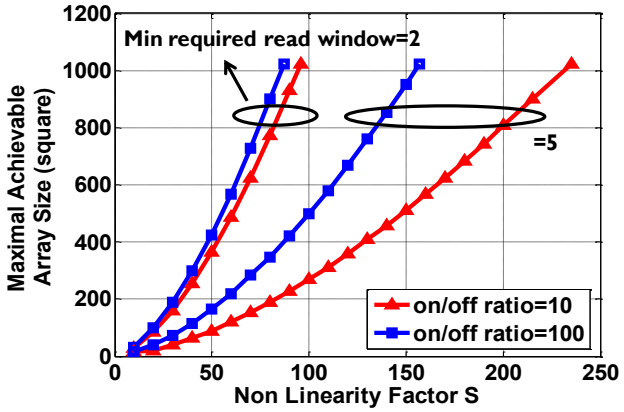

Fig 6. Influence of cell on/off ratio on maximal achievable array size for different minimal required read window (Fix *I@Idisturb*=0.1uA).

larger non-linearity to accomodate the same array size due to the high leakage currents. This indicates that it is more important to reduce the leakage currents than to achieve high read current.

3) Influence of Cell on/off Ratio

Fig.6 shows that, if we impose a minimum required read window of two, improving on/off ratio from 10 to 100 hardly improves the maximum array size. However, a higher ratio does help if we impose a higher required read window, e.g. five. This indicates that for single level cells, an on/off of 10 is good enough, while for multi-level cells, a larger on/off is desirable.

C. Optimized Bias Scheme vs. ½ Voltage Bias Scheme

In both read and write conditions, the above simulations determine the optimal voltages on the selected BL, WL, the non-selected BLs and WLs. However, most prior work relies on a fixed partial bias scheme (e.g. ½ voltage bias scheme), where half of the voltage is applied over WLHS cells and half of the voltage is applied over the BLHS cells. Fig. 7 shows that the max. achievable array size can be much larger for the optimized bias scheme, especially using cells with higher non-linearity. The reason is, that for more non-linear cells, we can allow a higher voltage over the NS cells while still meeting the current constraints. The benefit of increasing cell non-linearity vanishes using the ½ voltage bias scheme, because in our template, non-linearity only works in $V_{disturb}$ region. Moreover, the result indicates that I@$V_{disturb}$ should be around 10nA to achieve a 400x400 array if using the standard bias scheme. Cells with such low current may cause problems in the read operation (i.e. low read speed and small S/N ratio).

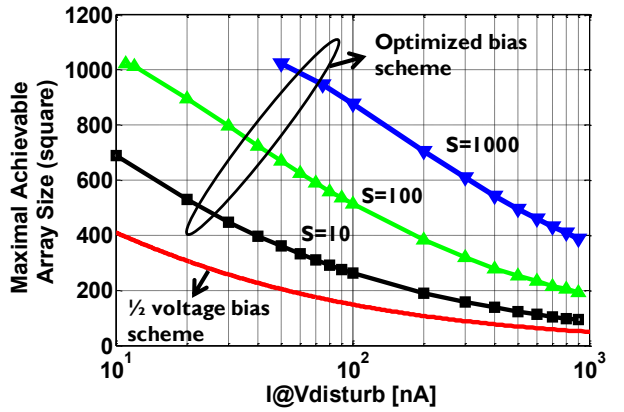

Fig 7. Non-zero bias on the non-selected cells using optimized bias scheme allows larger maximal achievable array size than using ½ voltage bias scheme in the write operation.

V. Conclusion

Cross-point memory arrays have been analyzed considering both read and write operations. A template-based exploration shows that larger non-linearity and low current level are important as they allow larger array size. LRS/HRS current ratio is not very critical when a small read window is required, such as for single-level cells, but it is important when a larger read window is required, e.g. for multi-level cells. Biasing the unselected bit-lines and word-lines to optimally distribute the voltage over the BLHS, WLHS and NS cells allows for much larger array size than a fixed ½ voltage bias scheme.

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