Simulation Study of dimensional effect on Bipolar Resistive Random Access Memory (RRAM)

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Abstract

The dependency of the RRAM device electrical parameters such as set voltage, reset current and resistance on the RRAM cell dimensional scalability is investigated with Monte Carlo simulation to optimize the power consumption of bipolar RRAM. It is found in the simulation that the switching process in bipolar RRAM is related to the cell dimension in the sub-nm region in terms of its horizontal length. The suppressing effect of existing conducting filament is also discussed. With optimal cell size sufficient initial resistance and a low forming voltage will be achieved, accelerating the feasibility of the high-density low-power RRAM.

Keywords: RRAM, power consumption, electric parameter and computational simulation

Introduction

To replace conventional flash memory, various new memory devices have been proposed. Among them, resistive switching random access memory (RRAM) devices are one of the possible candidates due to its simple structure, fast switching speed and high scalability [1]. The RRAM device can be fabricated with various materials such as binary oxides or perovskite oxides [2]. However, the current switching uniformity and reliability of current RRAM devices are not sufficient for high density memory applications. In addition, a detailed clarification on the switching mechanism has not yet been fully developed [3].

In many literatures of RRAM, the researcher studied resistive switching behavior of large area devices, which might not be applicable for future nano-scale high density memory application. So far, very limited researchers have focused on the scaling effect of RRAM devices. In this paper, we investigated the scaling issues of RRAM device with computational simulation. Our Monte Carlo simulation results show that the charged ions can be reasonably described as charged point particles which play an important role in the switching process of RRAM device. The present approach also provides a new way to probe the inner process of dielectric breakdown.

Computational Methods for RRAM Structure Simulation

We employ the kinetic Monte Carlo (KMC) method by considering the ion dynamics in a simplified way. It is assumed that the oxidation, transportation and reduction of electrode atoms in switching layers are simulated in a two-dimensional matrix. The electrochemical transitions, switching time and final state of the device are determined by the random-test method. The hopping rate P between jumps is obtained from the following Boltzmann relationship:

$$P = \nu\, e^{(-E_a/kT)} \qquad (1)$$

where ν, k and T are attempting frequency of atoms, Boltzmann constant and local temperature, respectively. E_a is the migration barrier along the jump direction. The magnitude of E_a and its variation in different situation are based on our previous work [4], where more detailed simulation descriptions were also provided.

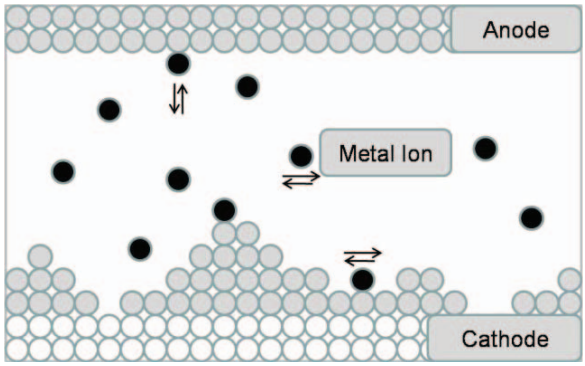

Fig.1 Schematic diagram of simulation box in KMC simulation for RRAM cell

Simulation box of different length in x dimensional are studied in the modeling process and periodic boundary conditions are also used. The intrinsic defect is introduced and randomly generated when initializing simulation, the concentration of which is assumed to be around 1% in the simulation box. In the KMC simulation process we adopt a simple residence-time algorithm. For the sake of simplicity, we consider only the movement to the nearest neighbor positions, and the interaction between charged ions is not considered.

Results and Discussion

A. Dimensional scaling effect I :Degradation of the electric characteristics

Previous studies have revealed that the switching mechanism of RRAM stack structure was attributed to conductive filament formation/rupture by oxygen vacancy or

metal ions [5]. Although RRAM device with oxygen vacancy (VOs) conducting path and metal conducting bridge have different switching mechanism, similar conducting filaments (CFs) dynamic behavior was observed [6]. In our research the simulation model is mainly based on metallic conducting bridge RRAM (also called CBRAM) device, but it should be pointed out that the simulation results also apply VO based RRAM.

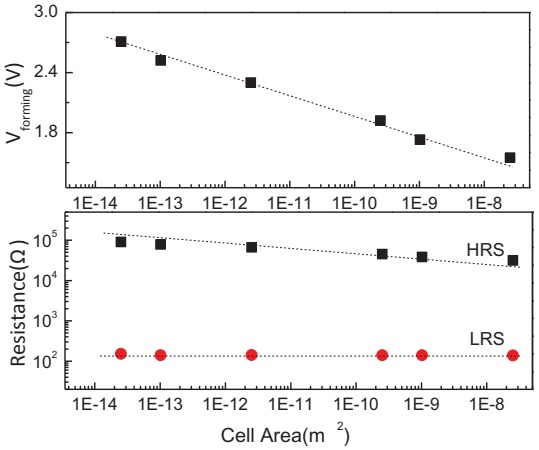

Fig. 2 Resistance and forming voltage as a function of cell area

As shown in Fig. 2, $V_{forming}$ and R_{HRS} of the device are strongly related to active device area. With device area scaling down, $V_{forming}$ and R_{HRS} increase. The increase in voltage with scaling area can be attributed to the reduced number of defects. Generally, the formation of a conducting filament can be induced by connection of defects in the active memory area, where metal ions could be more easily accumulated. In large area device, a relatively small voltage is sufficient to induce the formation of a conducting filament in the dielectric layer. Because of reduction in the defects, a higher voltage is required for filament formation in nano devices. Forming voltage also increase with cell area scaling due to defect reduction in nano device.

In the low resistance state (LRS) case, however, same resistances were observed regardless of the device area. In this situation, the resistance is mainly affected by the formed conducting filaments. According to the suppressing effect of existing conducting filament to its neighboring area, the CFs dynamics don't show much difference with device area scaling down.

B. *Dimensional scaling effect //: Uniformity improvement*

By simulating the forming operation of a large number of devices, it is possible to extract the statistical distribution of the forming voltage. Fig. 3 shows the statistical charts of the resistive switching parameters for different devices with linearly scaled active memory area. 100 randomly initialized simulation boxes are selected to evaluate the switching uniformity of devices. Compared with large area devices, the nano devices show more uniform and sharp distribution of switching voltage.

These improvements can be attributed to the difference in the amount of uncontrollable defects in the active memory areas of the devices. It is well known that vacancies and grain boundaries are major causes of intrinsic defects in metal oxide dielectric films. These intrinsic defects may be responsible for the formation of filaments comprising metallic atoms during resistive switching, thus leading to instable resistive switching. If the deviation from the defects in the nano-scale device can be minimized with device area shrinking, resistive switching uniformity can be improved.

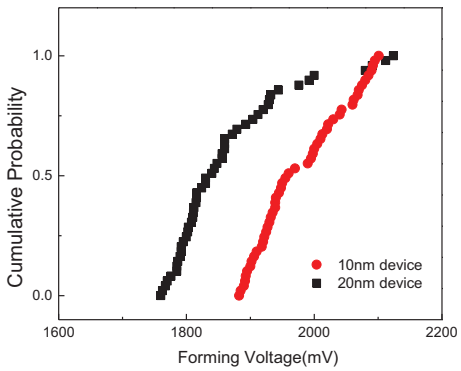

Fig.3 Distribution of switching voltages for different nano- scale RRAM devices

C. *Dimensional scaling effect ///: Local heat effect*

We also investigated the effect of area scaling on the local heating of filament. It is well known that charged ion movement is closely related to local temperature. To confirm the temperature effect on the resistive switching, we simulated the response time under different background temperature.

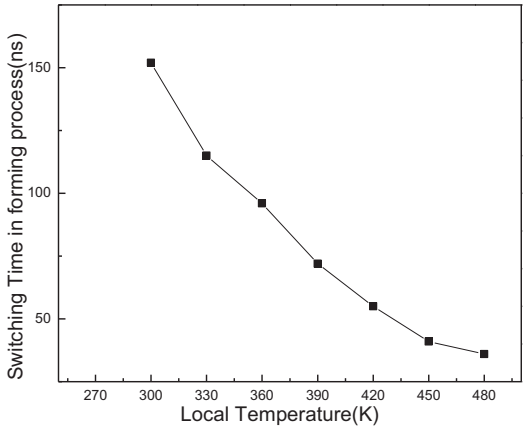

Fig.4 Trend of switching time as a function of local temperature

As shown in Fig. 4, with increasing temperature, the response speed of the device increases significantly, this confirmed the acceleration of metal ions movement during switching. In other words, if additional heat is generated in active area of the device during switching, significant speed improvement is possible to be obtained. Compared with large

area device, current density of small area device increases significantly in the switching process, which induced the high temperature under same bias, thus the enhanced switching speed which can be explained by local heat effect.

Based on empirical estimates from literature, we expect the effective temperature of nano devices to be approximately 100^{o}C higher than that of large area device. However, in order to obtain more precise simulation results, further study for thermal barrier calculation is required, and other simulation method should be introduced into the calculation process.

Conclusions

This paper has clarified some properties of RRAM devices resulting from area scaling down for clarification of the switching mechanism. When adopting device area scaling, three phenomena can be confirmed: 1) variation of electric characteristics; 2) improvement of uniformity; 3) local heating effect. It is shown that the process of formation of conducting filaments is greatly affected by the scaling of device area. The present work can provide a feasible way for simulating RRAM operations and obtaining reliable and uniform device for future high-density memory application.

Acknowledgments

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