KATHOLIEKE UNIVERSITEIT LEUVEN

ESAT

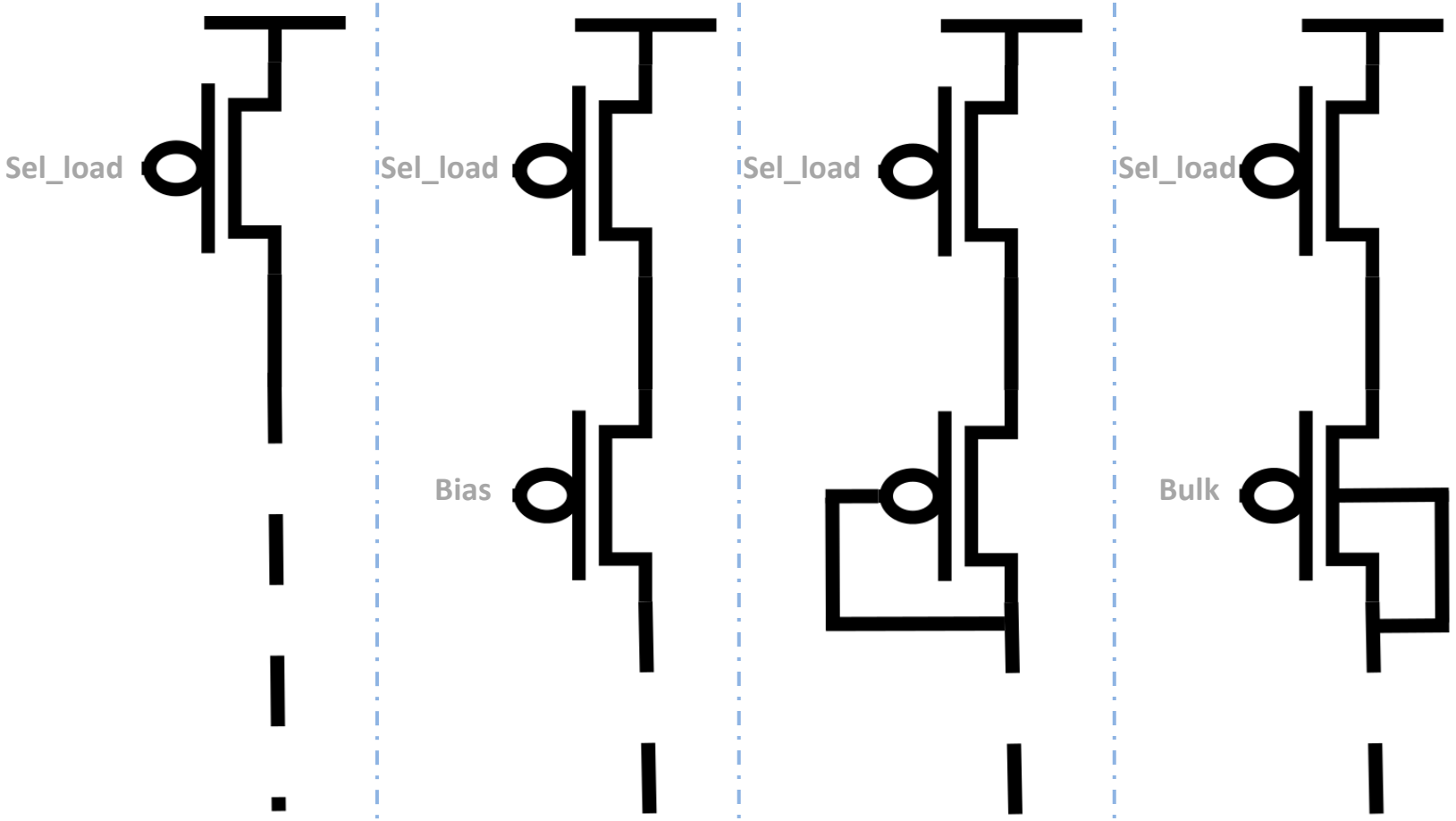
Load Analysis

Alexander Standaert
Wouter Diels

OUTLINE

- **INPUTS** : Load types, Design parameters and Simulation set up
- **OBJECTIVES** : Linear sweep and Monte carlo
- **RESULTS LINEAR SWEEP**
- **RESULTS MONTE CARLO**
- **FINAL LOAD**
- **CONCLUSION** : Conclusion and Future work

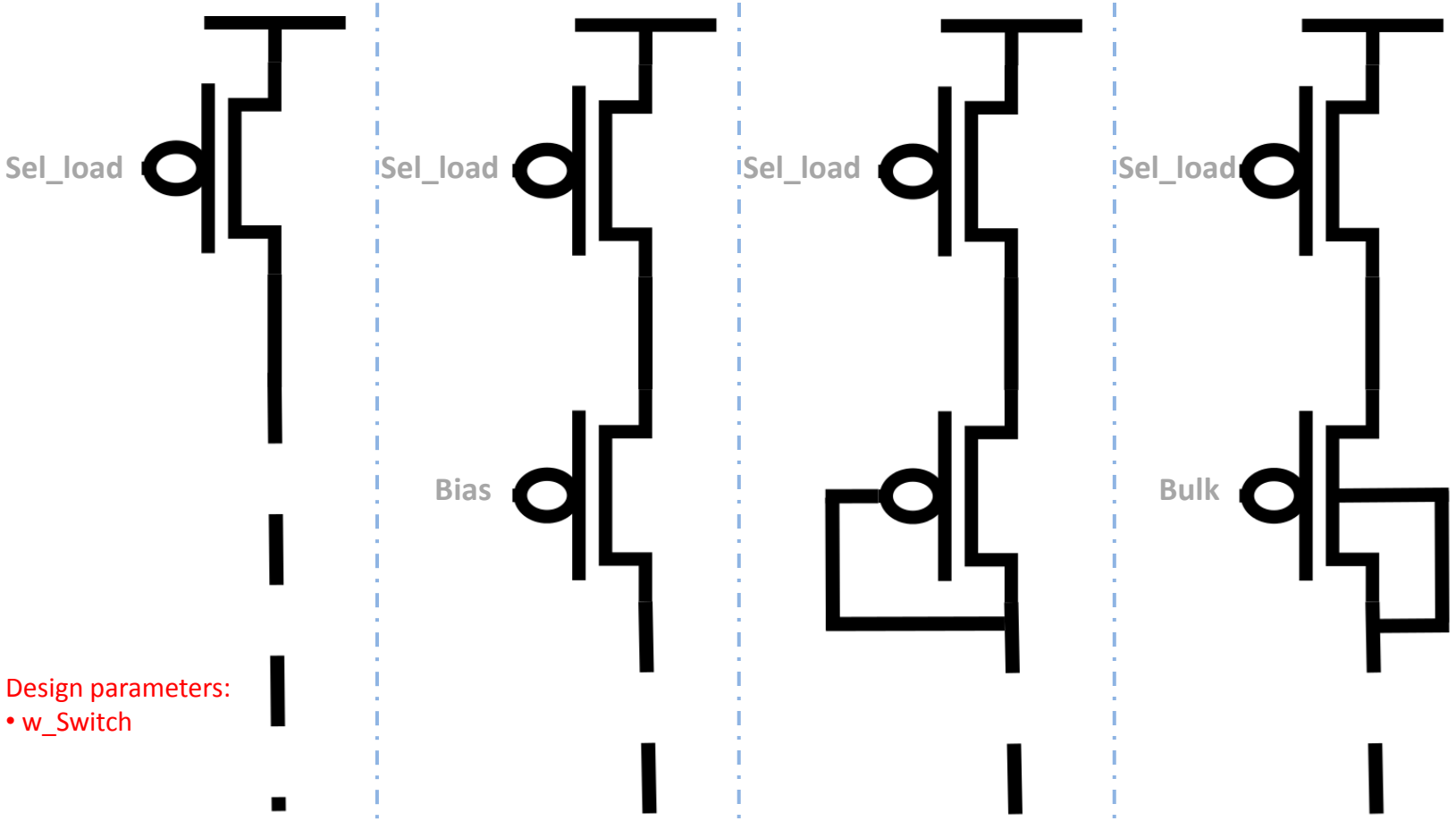
LOAD TYPES



Switch Load **Bias Load** **Diode Load** **Bulk Load***

*(Ren et al., "A body-voltage-sensing-based short pulse reading circuit for spin-torque transfer RAMs (STT-RAMs) ", 2012)

LOAD TYPES



Design parameters:
- w_Switch

Switch Load | **Bias Load** | **Diode Load** | **Bulk Load***

*(Ren et al., "A body-voltage-sensing-based short pulse reading circuit for spin-torque transfer RAMs (STT-RAMs) ", 2012)

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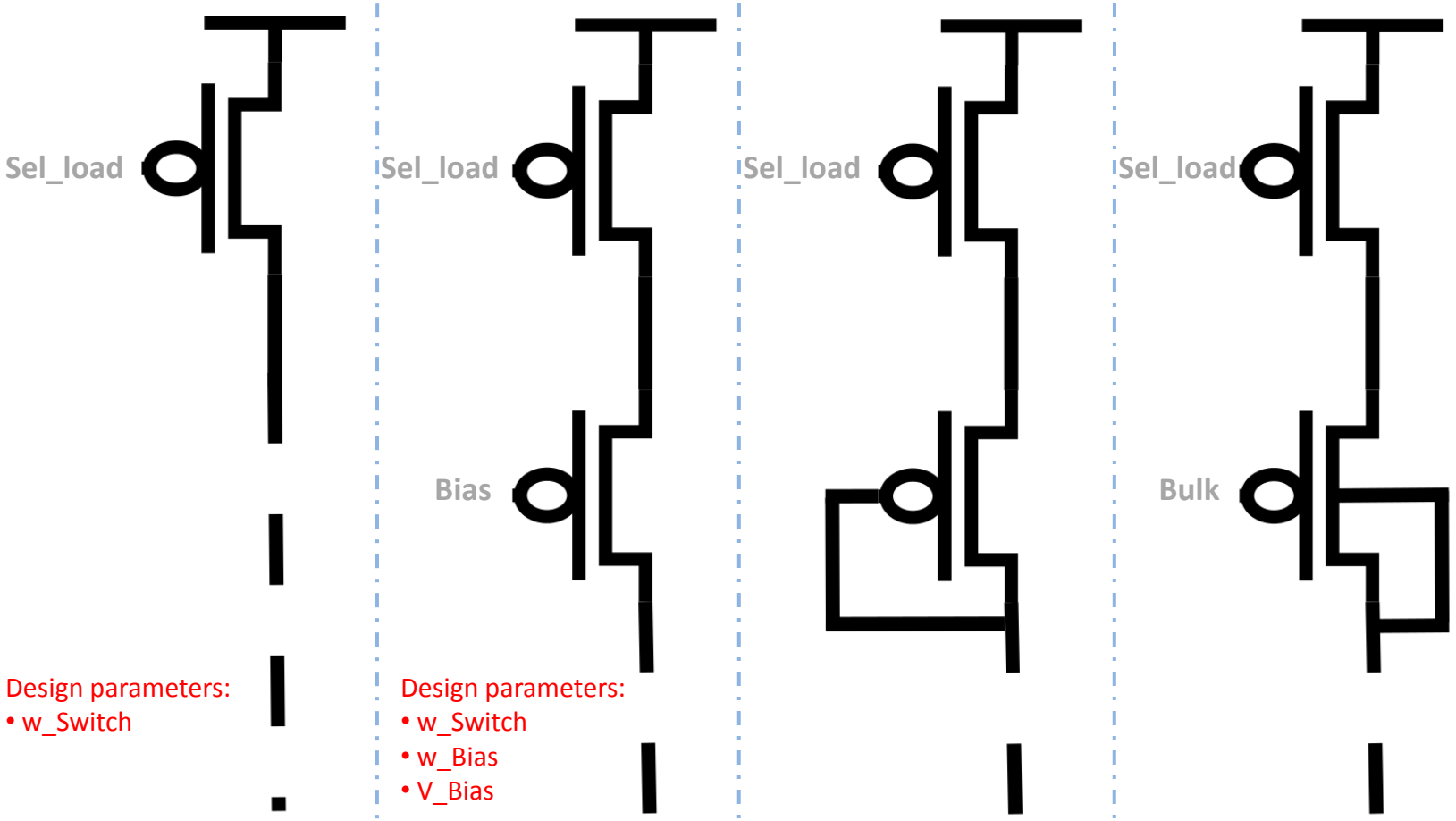

Design parameters:
- w_Switch

Design parameters:
- w_Switch
- w_Bias
- V_Bias

Switch Load

Bias Load

Diode Load

Bulk Load*

*(Ren et al., "A body-voltage-sensing-based short pulse reading circuit for spin-torque transfer RAMs (STT-RAMs) ", 2012)

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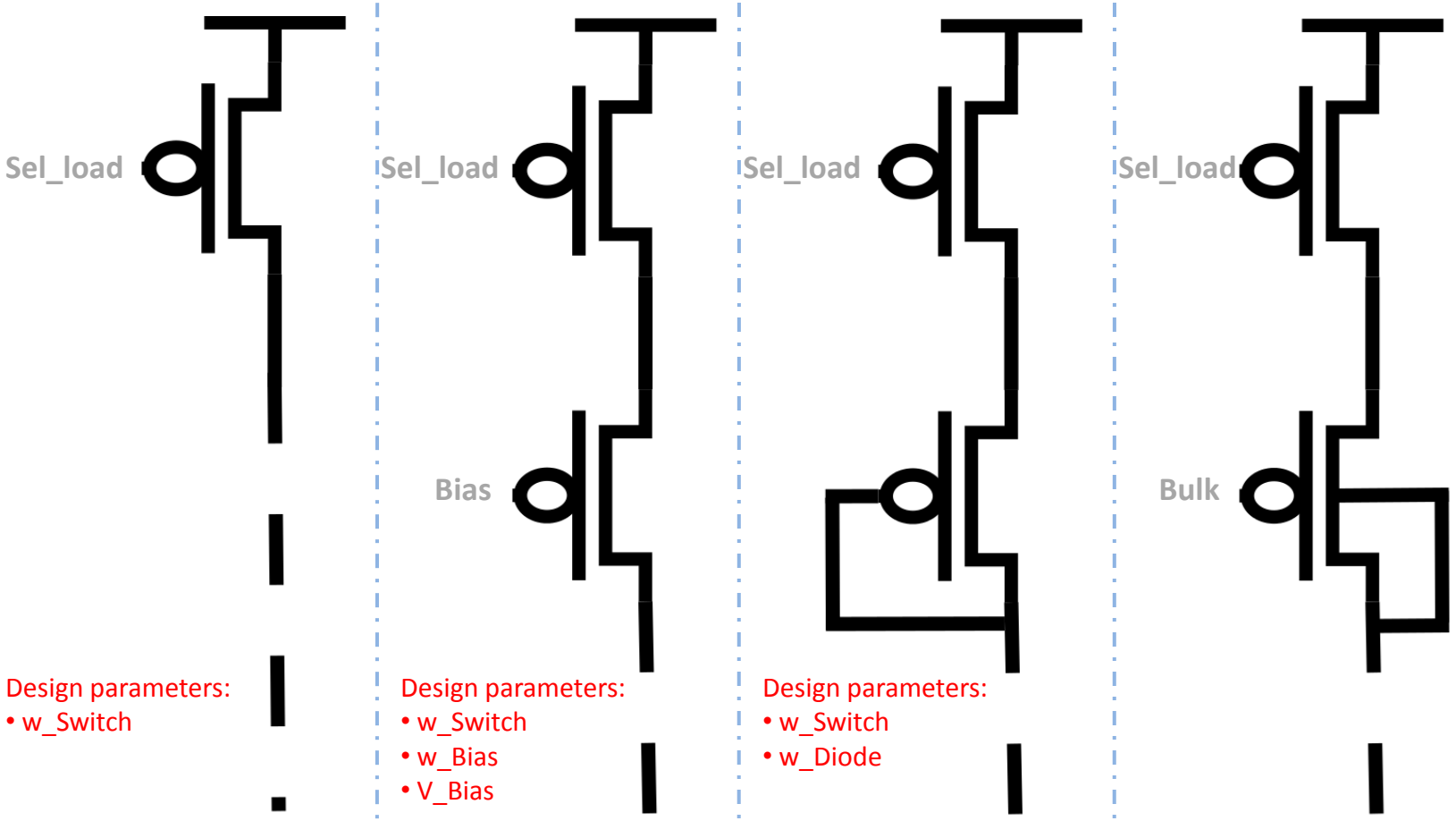

Design parameters:
- w_Switch

Design parameters:
- w_Switch
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- V_Bias

Design parameters:
- w_Switch
- w_Diode

Switch Load

Bias Load

Diode Load

Bulk Load*

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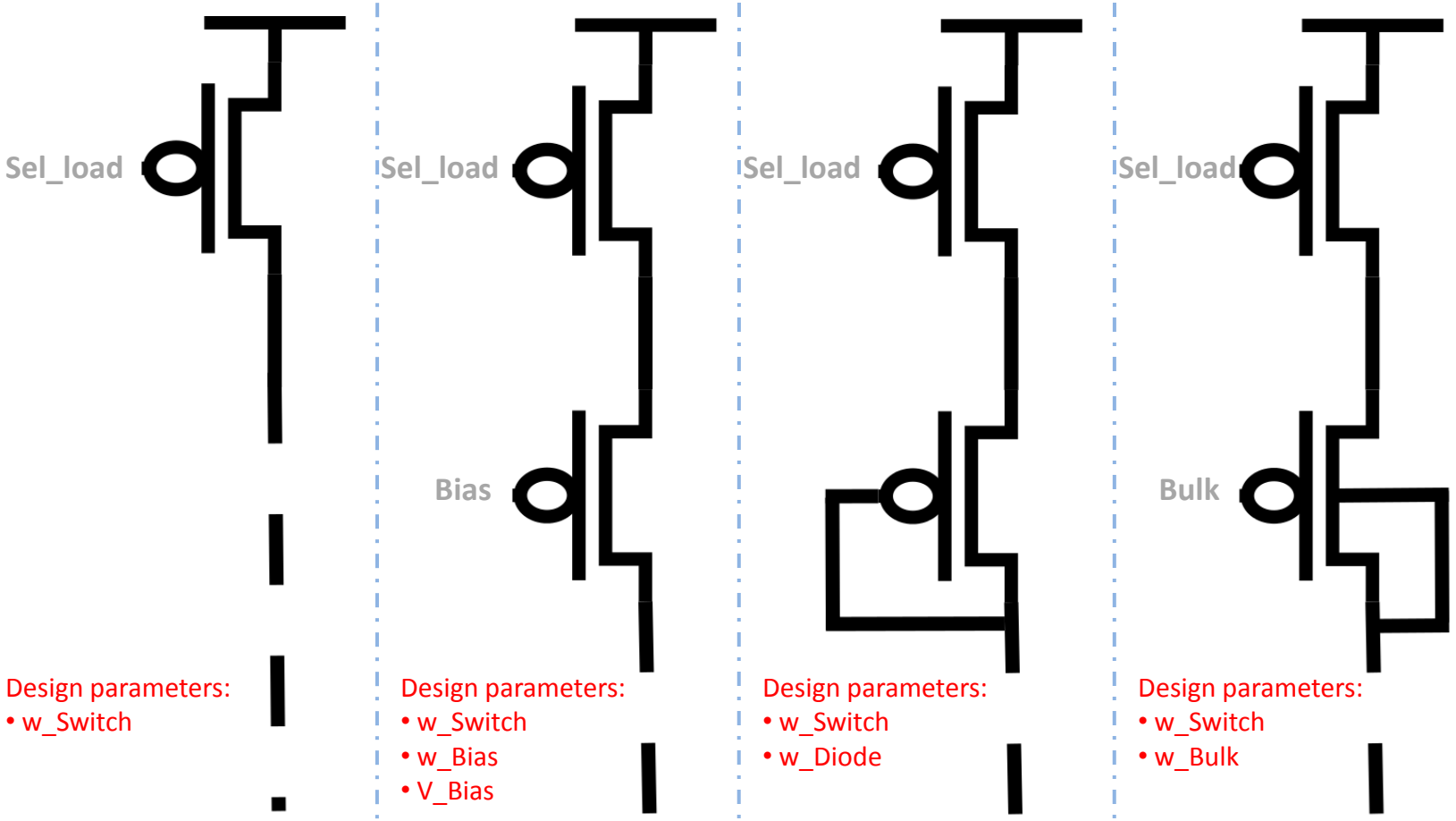
LOAD TYPES



Design parameters:
- w_Switch

Switch Load

Design parameters:
- w_Switch
- w_Bias
- V_Bias

Bias Load

Design parameters:
- w_Switch
- w_Diode

Diode Load

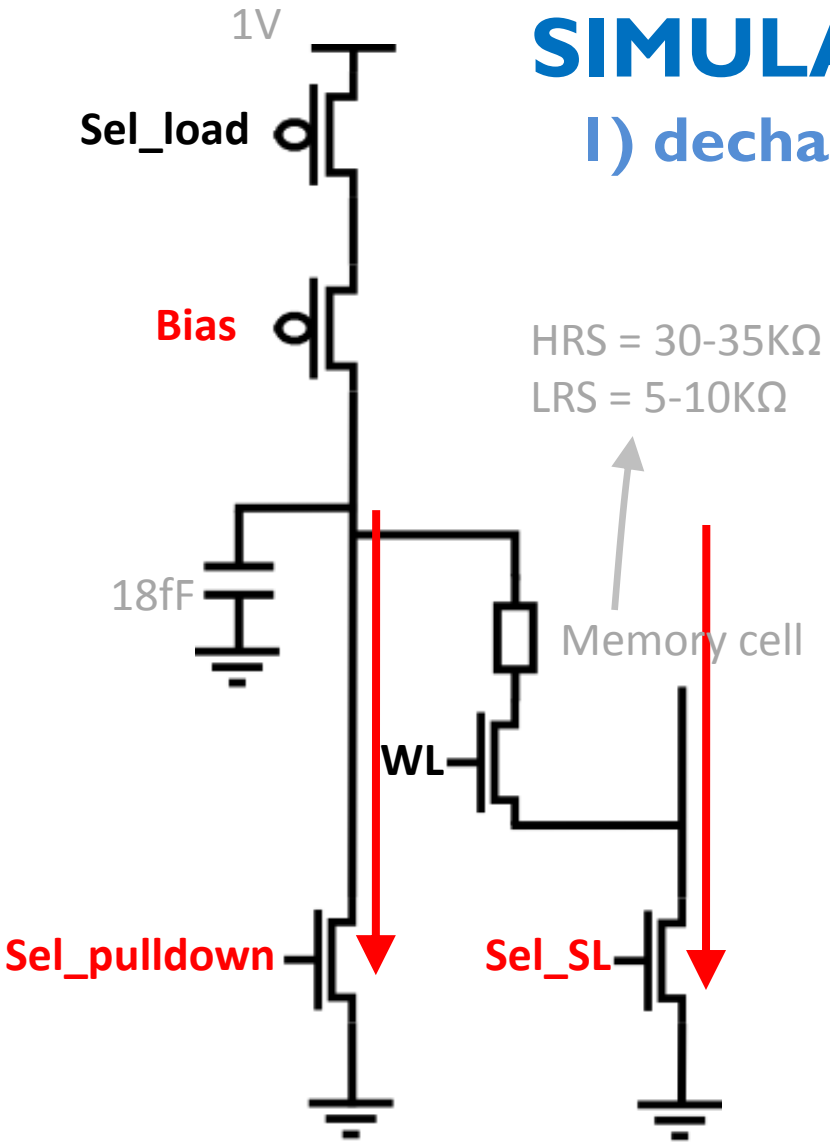
Design parameters:
- w_Switch
- w_Bulk

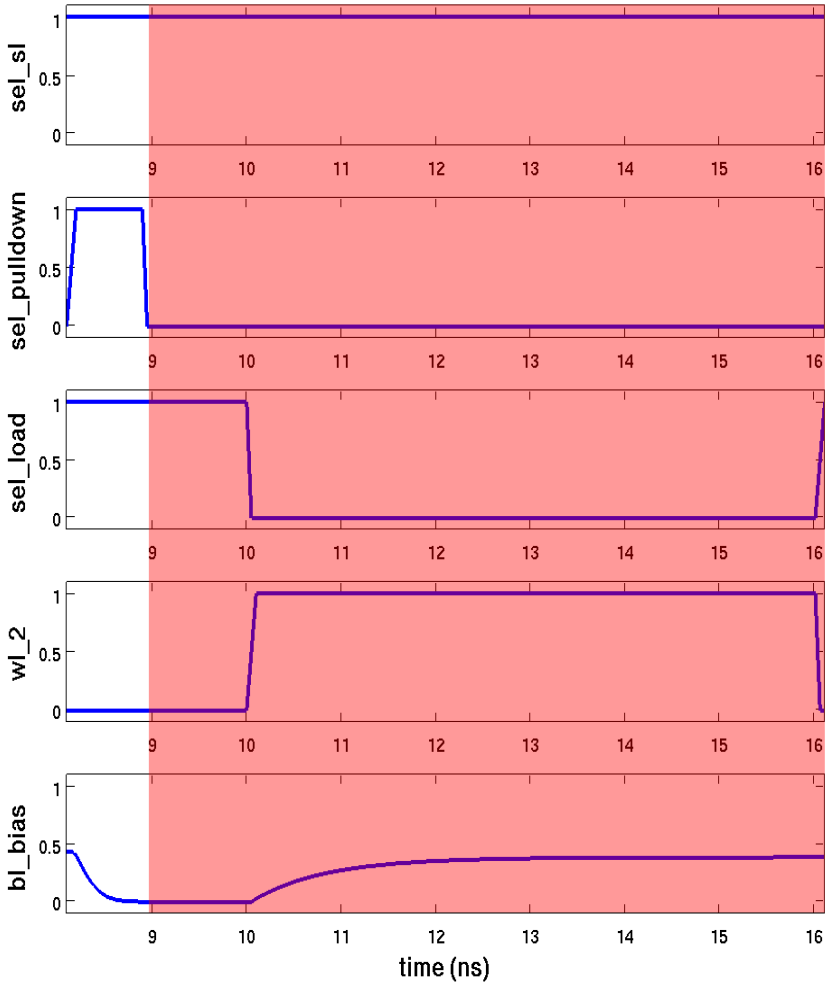
Bulk Load*

*(Ren et al., "A body-voltage-sensing-based short pulse reading circuit for spin-torque transfer RAMs (STT-RAMs) ", 2012)

SIMULATION SETUP

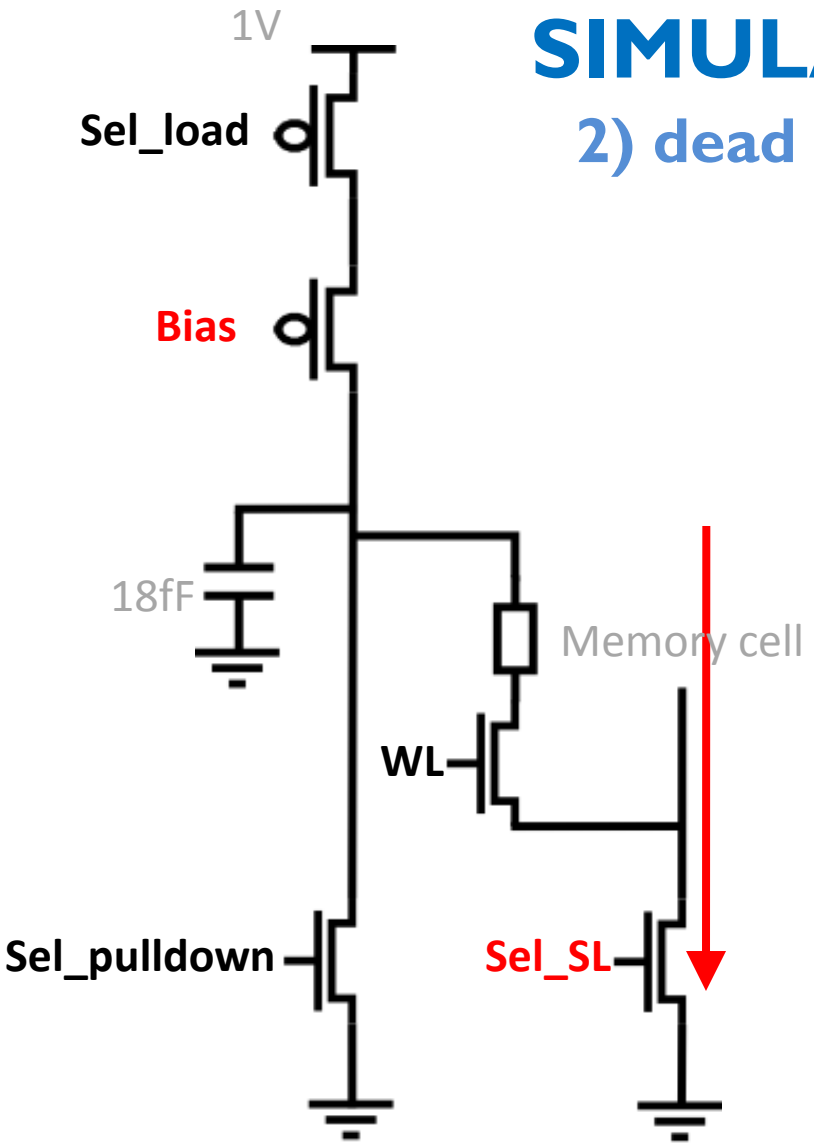
I) decharge

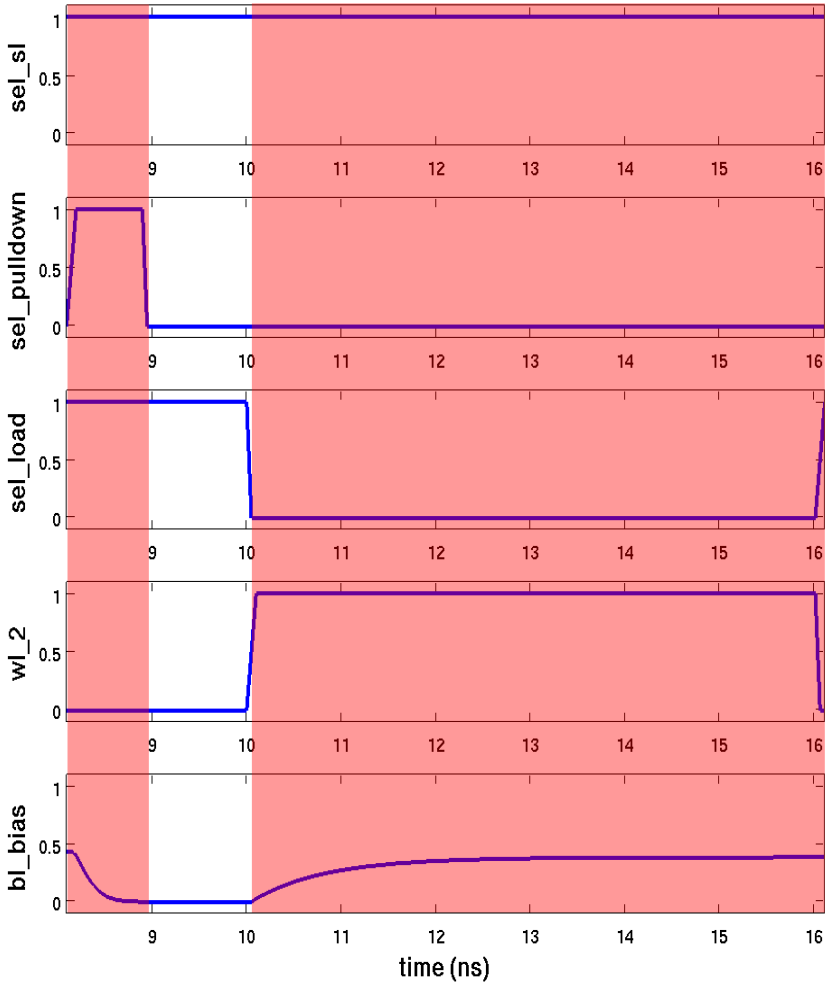




SIMULATION SETUP

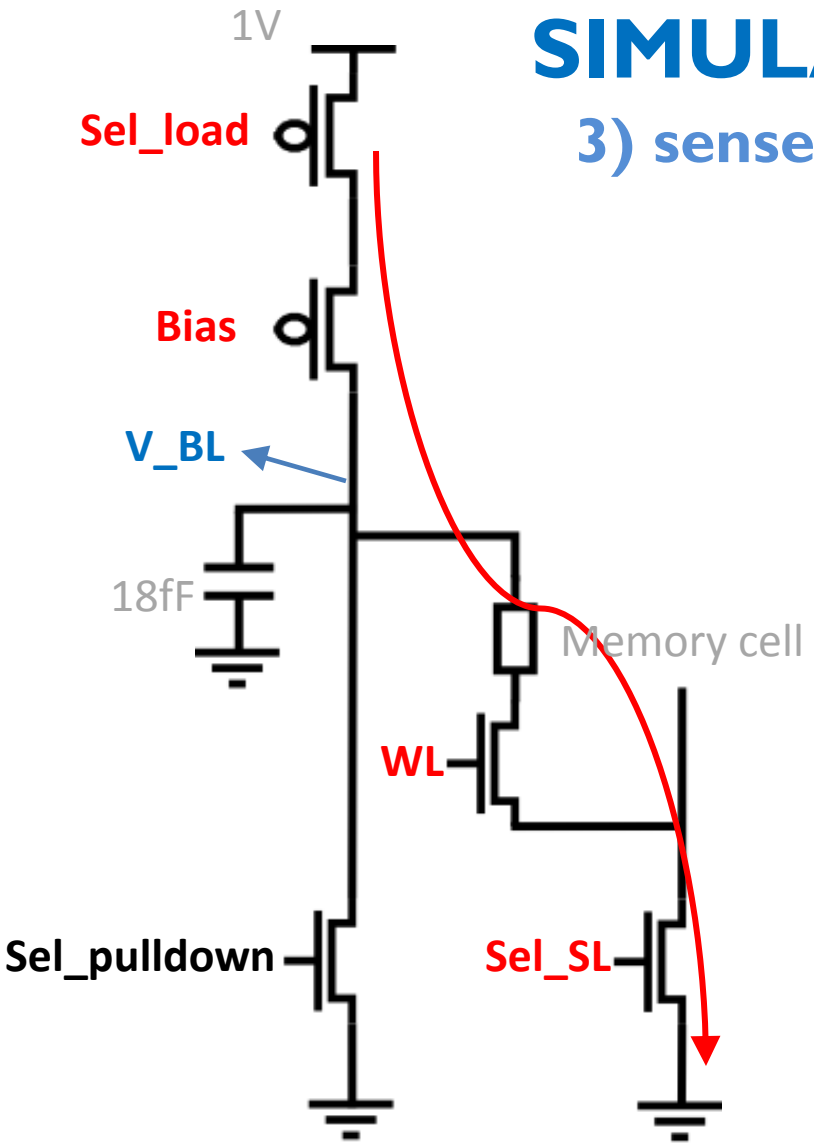
2) dead time

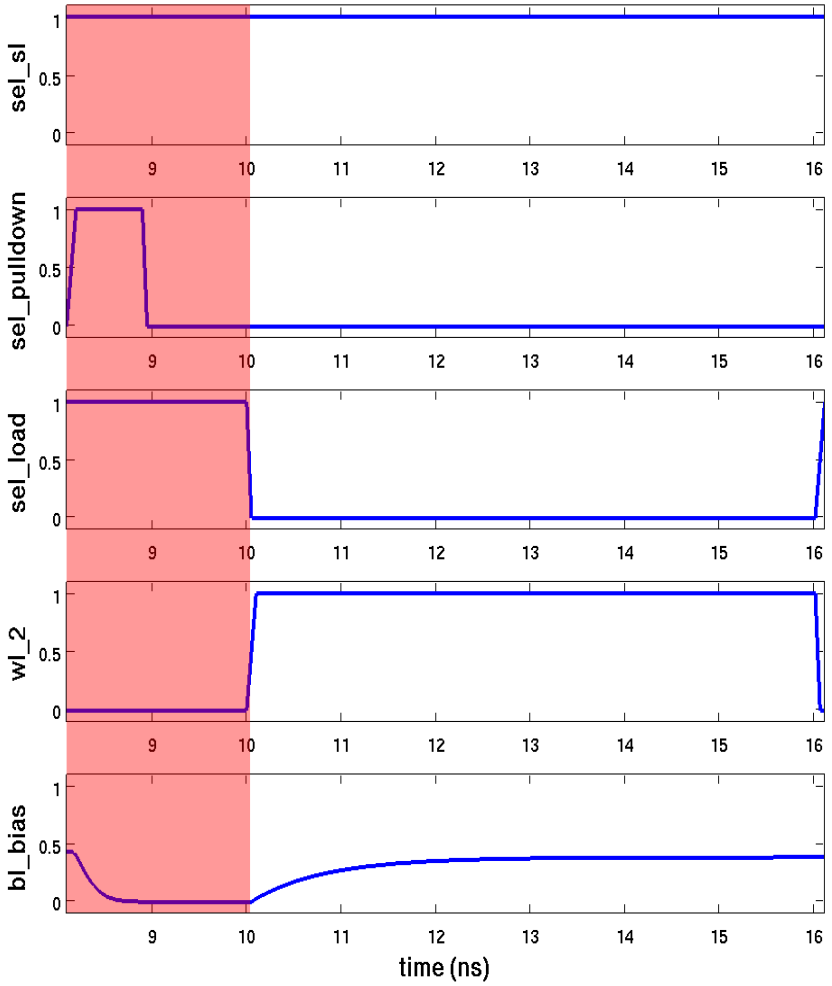




SIMULATION SETUP

3) sense





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OBJECTIVES

- Bitline voltage difference: V_BL(HRS) – V_BL(LRS)
- Bitline delay
- Area
- Voltage drop memory cell

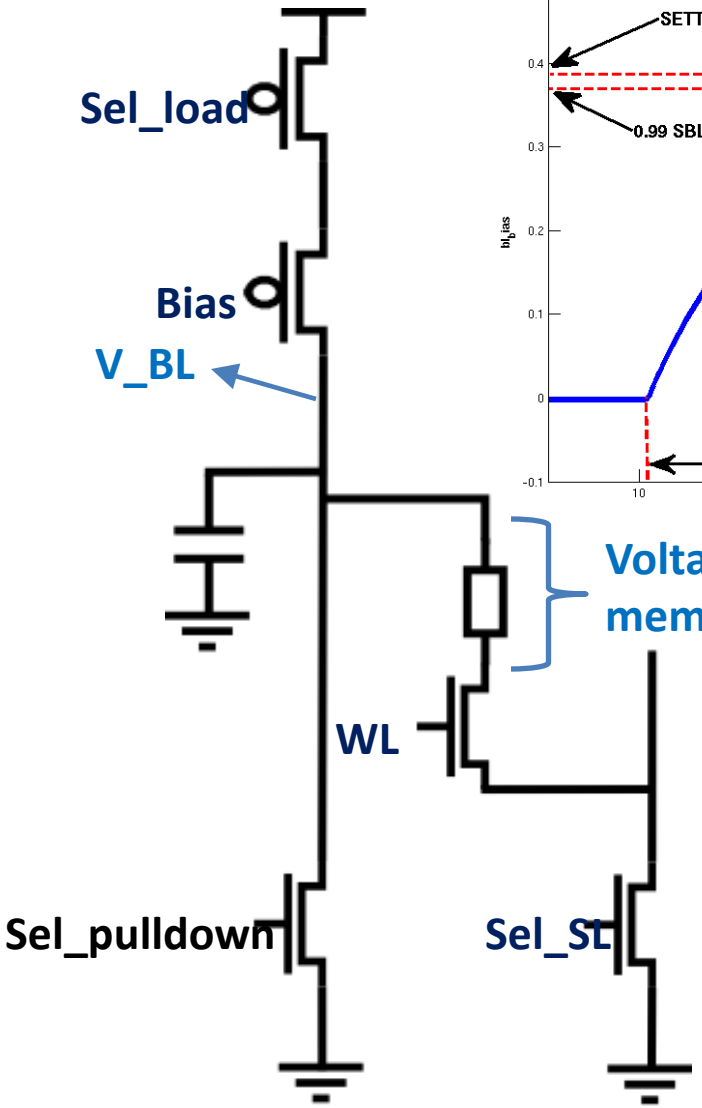
LINEAR SWEEP

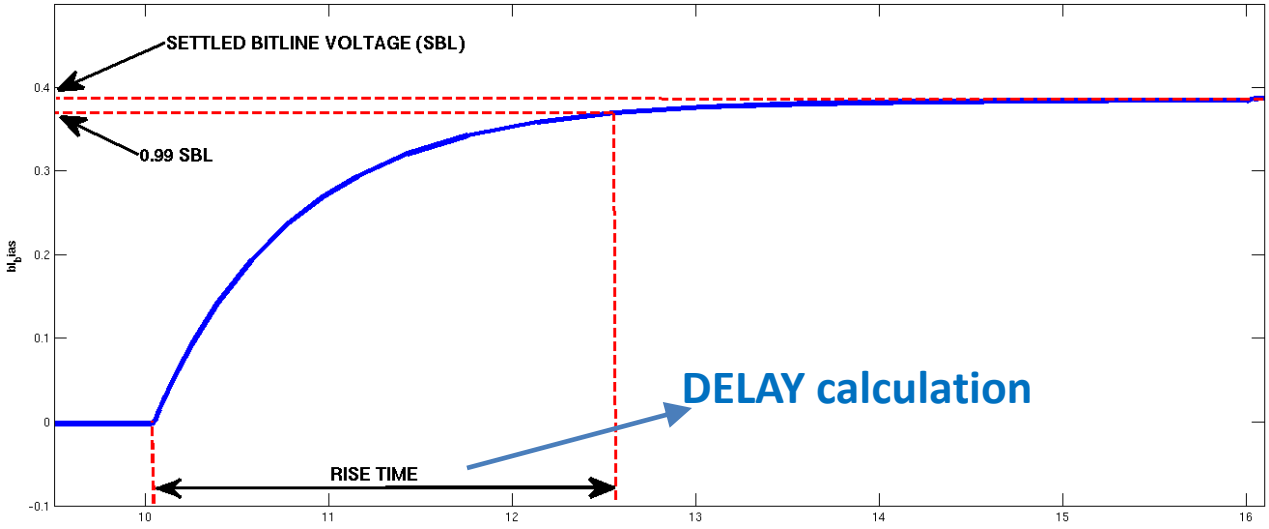
- Minimal Bitline voltage difference
- Minimal Standard deviation Bitline voltage
- Maximal Bitline delay

MONTE CARLO

- Robustness Temperature, Vss, ... variations

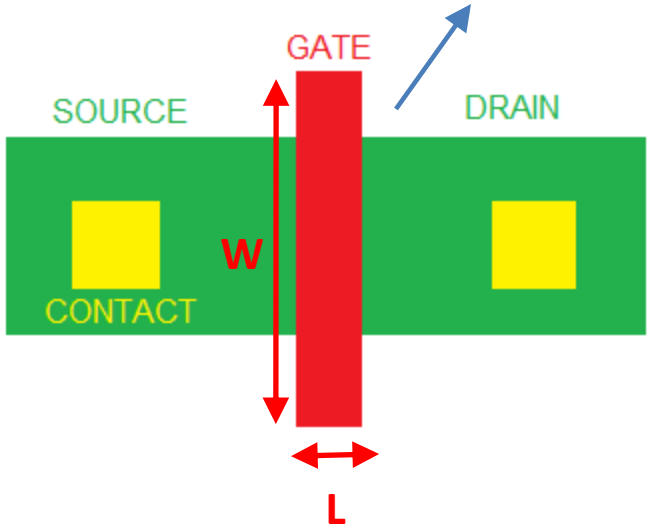
OBJECTIVES LINEAR SWEEP



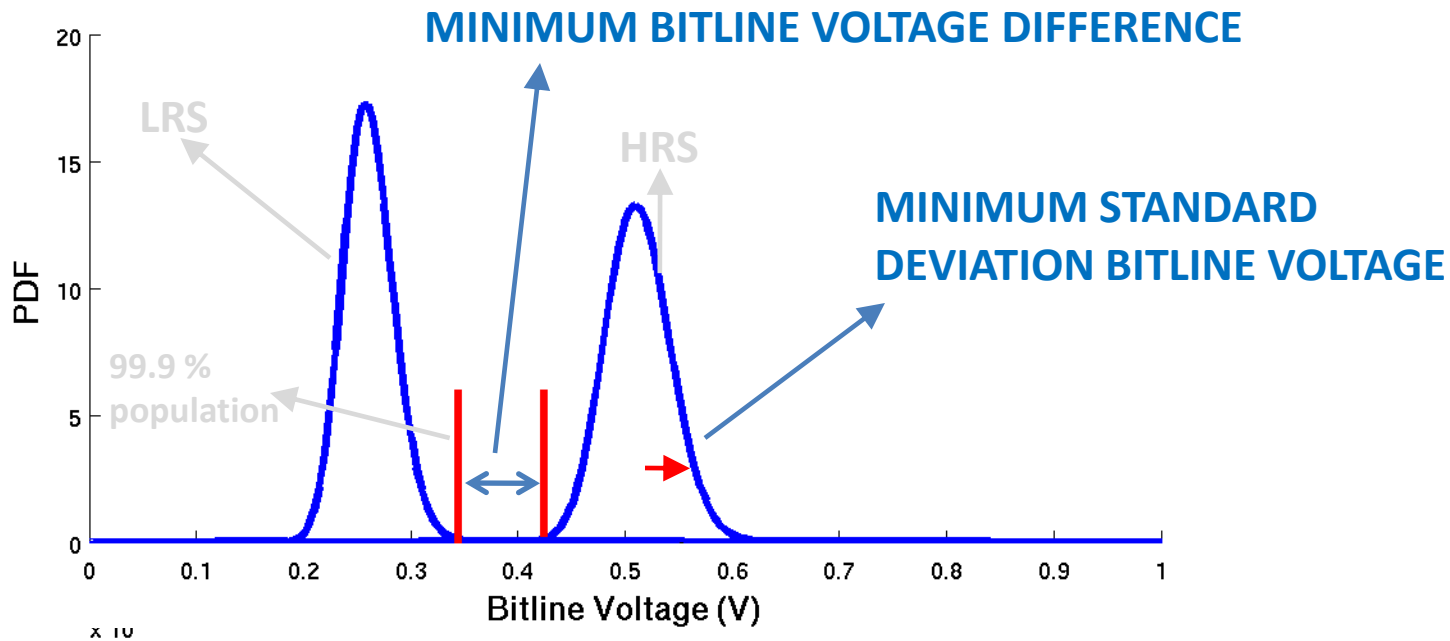


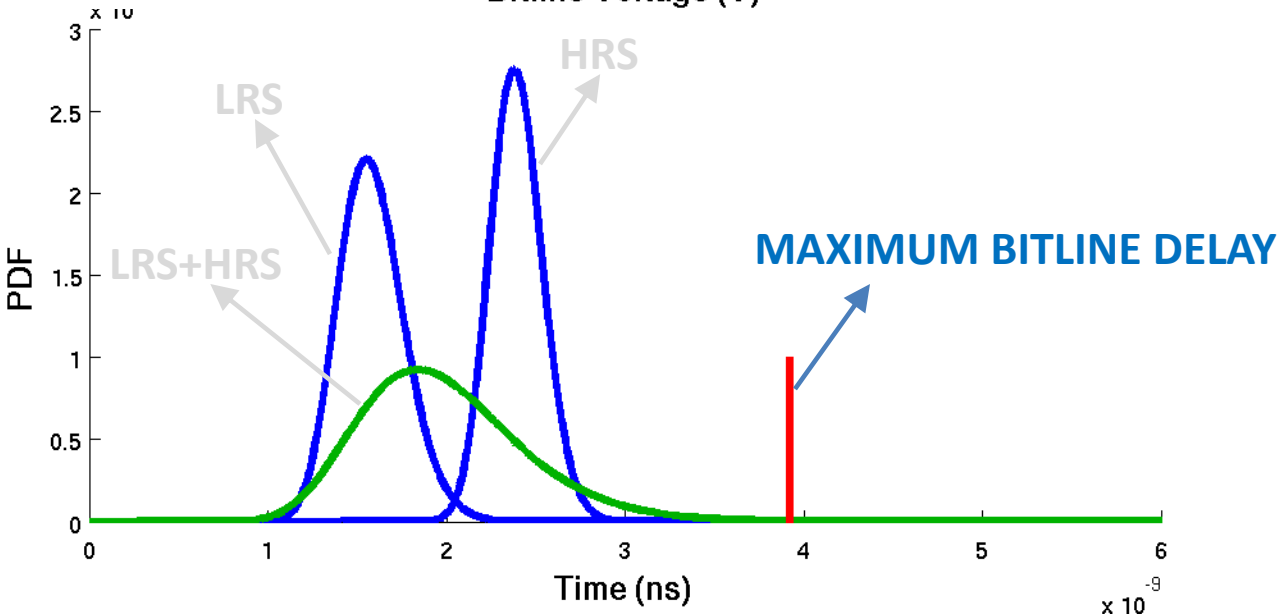
Voltage drop memory cell

AREA calculation



OBJECTIVES MONTE CARLO





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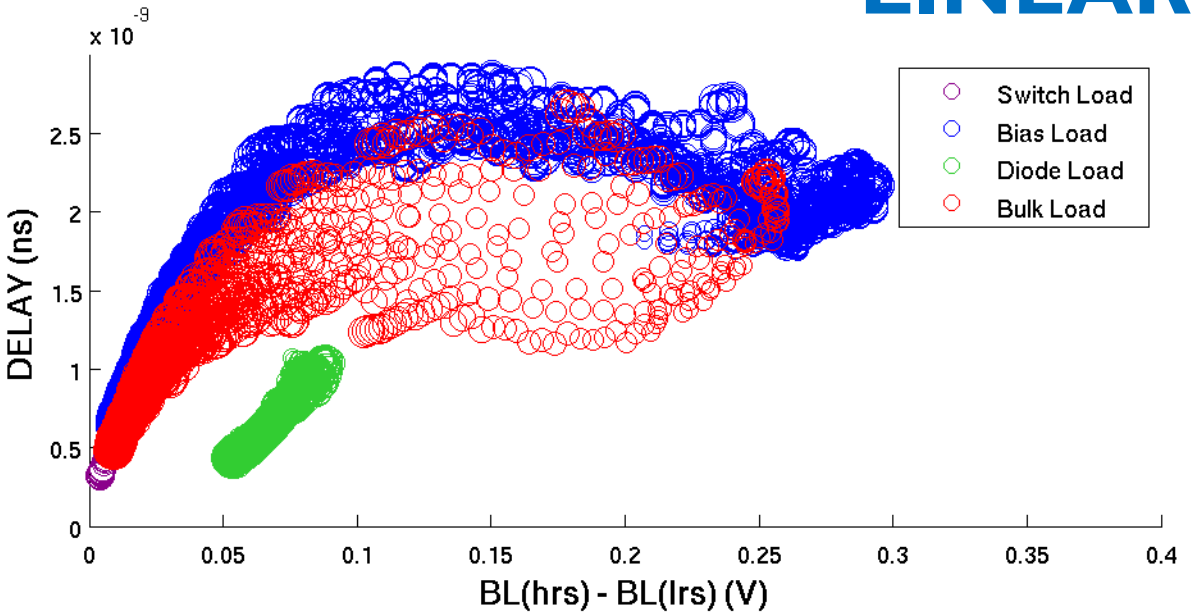
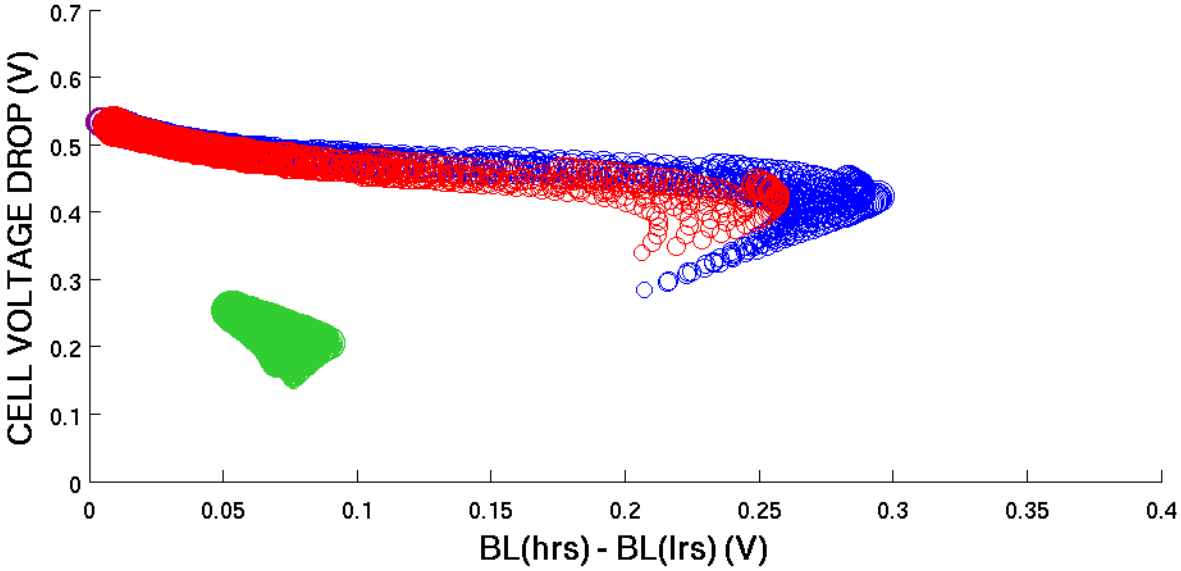
LINEAR SWEEP

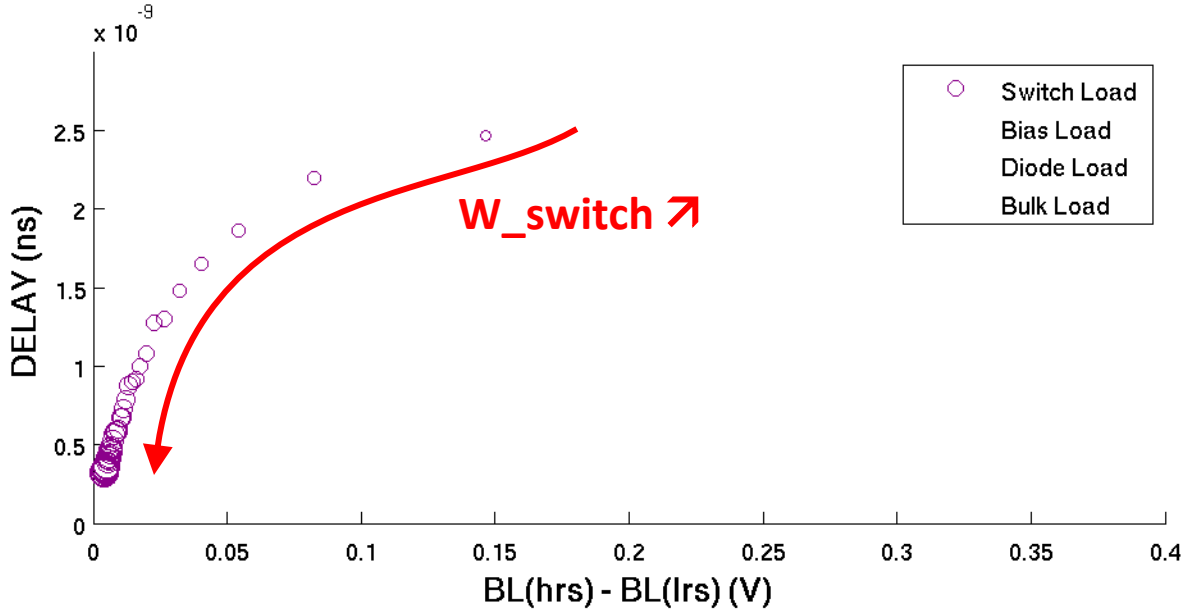


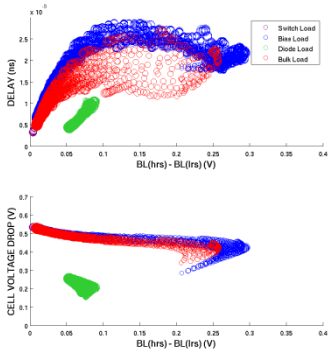
21894 SOLUTIONS

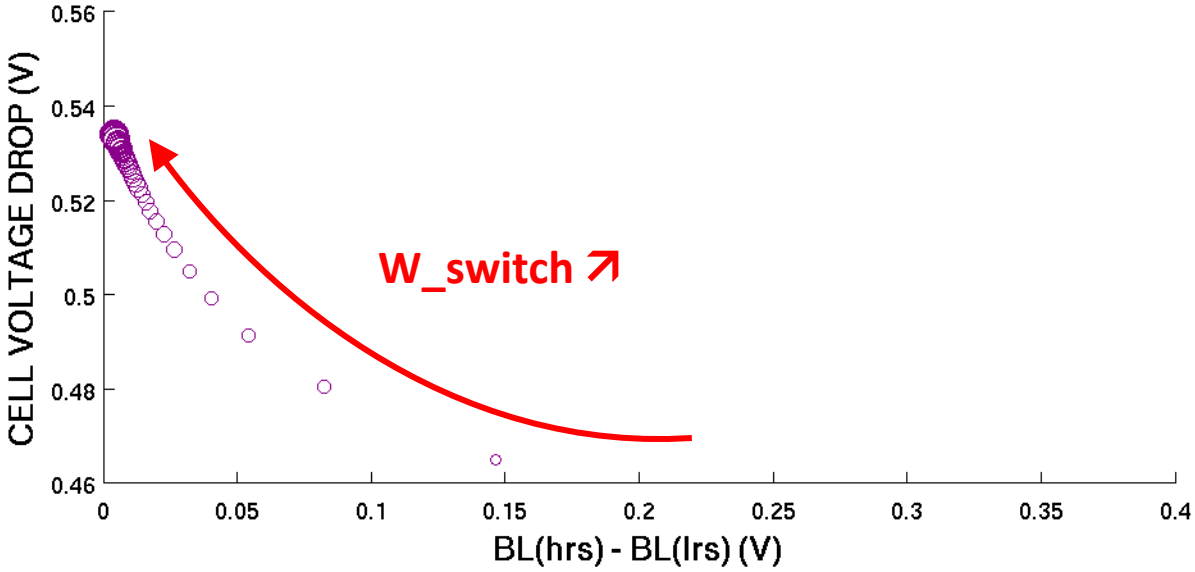


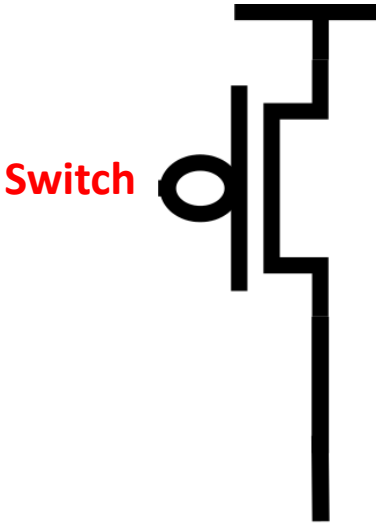
SWEEP RANGE:
W_switch = 100-500nm
W_load = 100-500nm
V_bias = 0-0.4V

LINEAR SWEEP: SWITCH LOAD

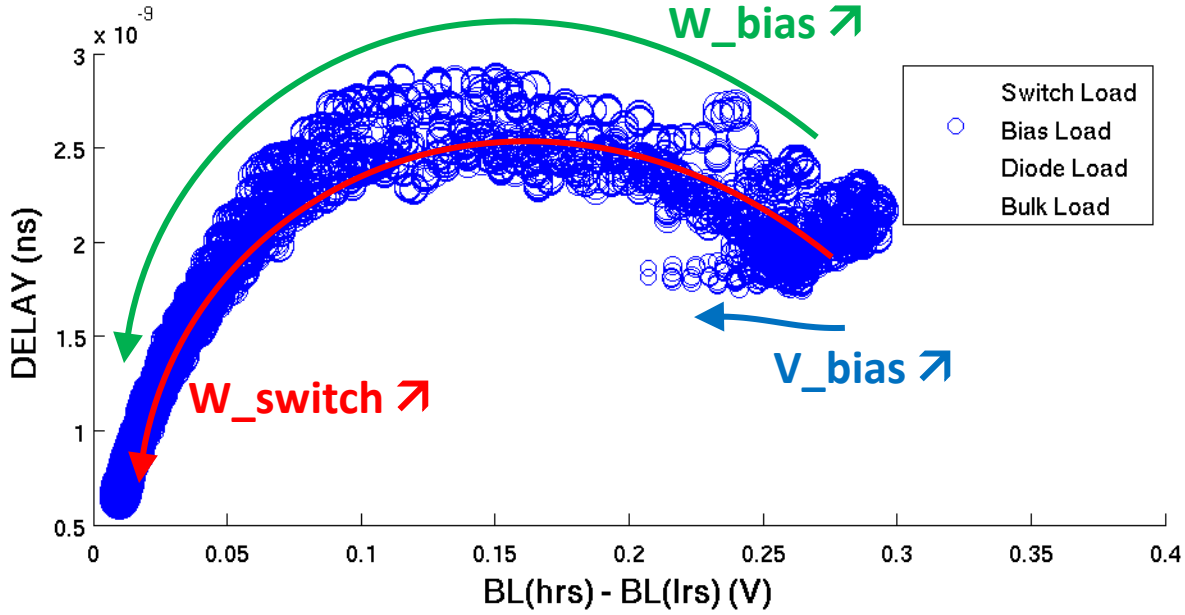


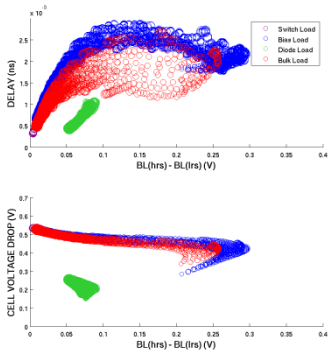


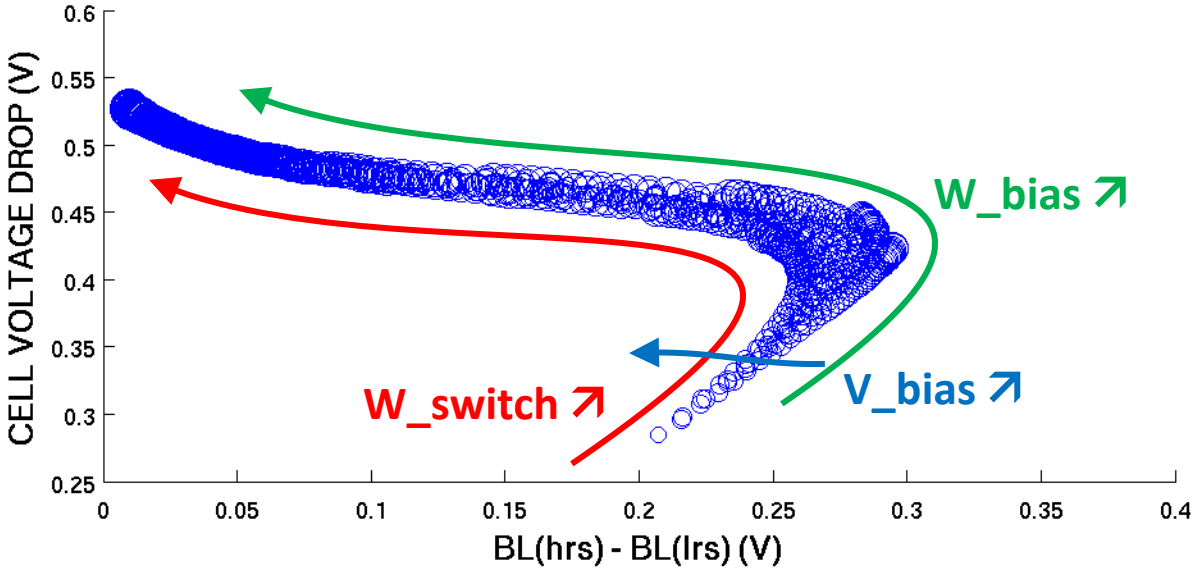


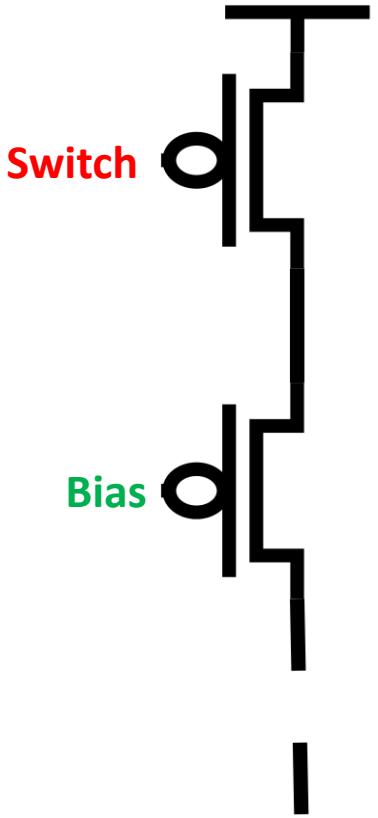


LINEAR SWEEP: BIAS LOAD

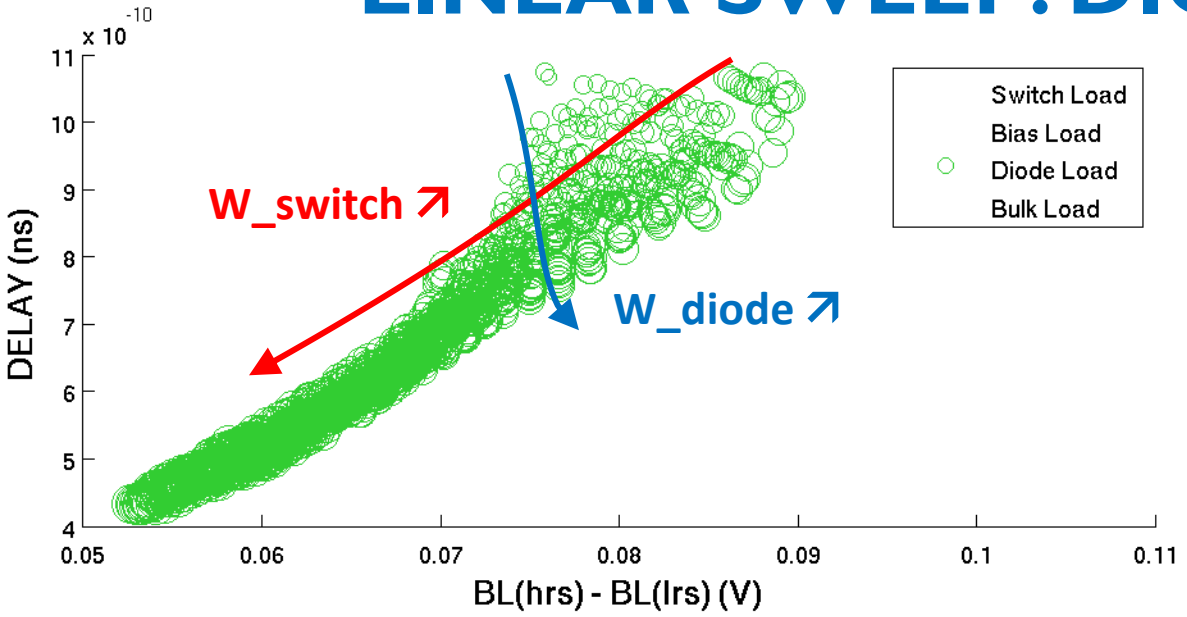


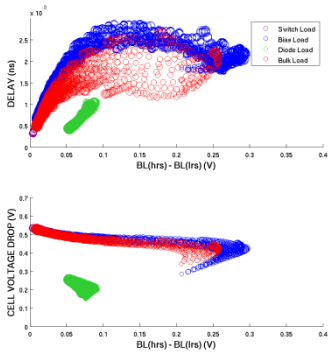


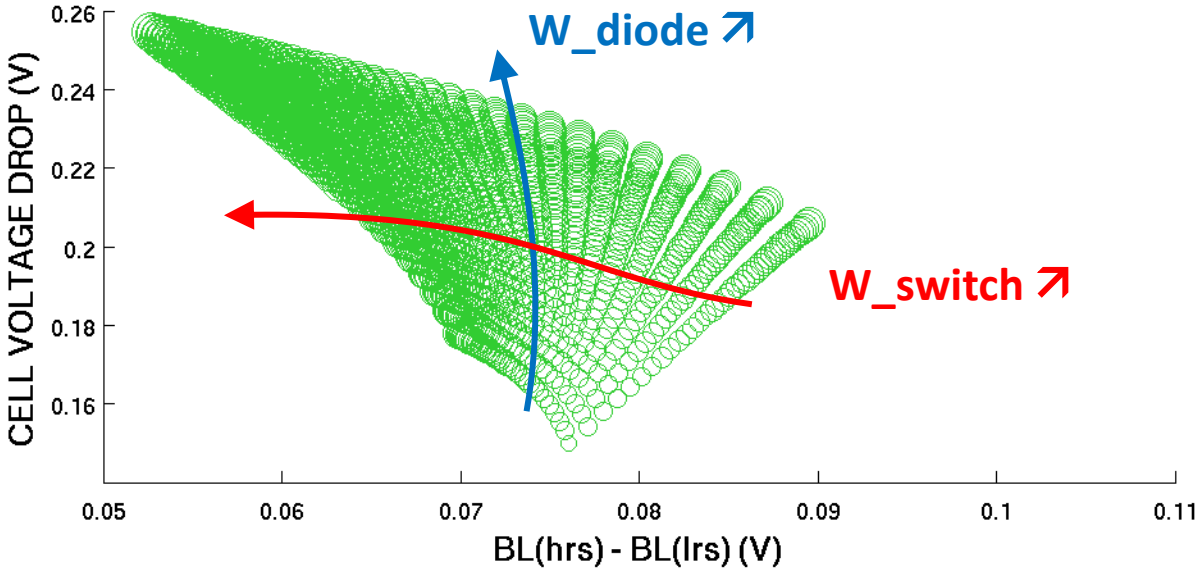


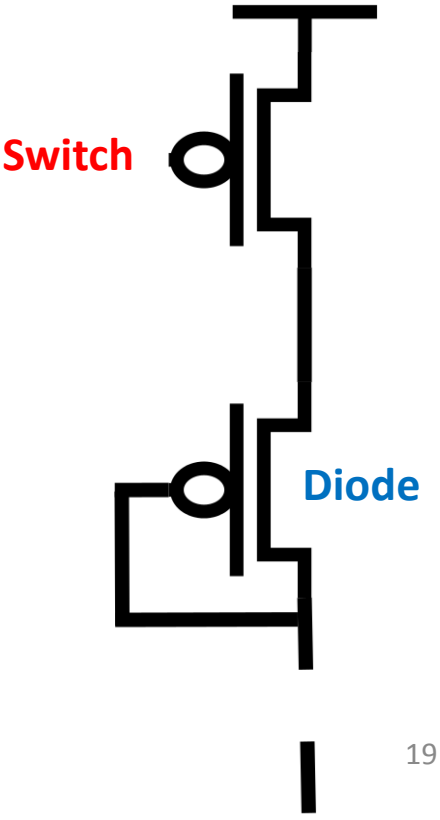


LINEAR SWEEP: DIODE LOAD

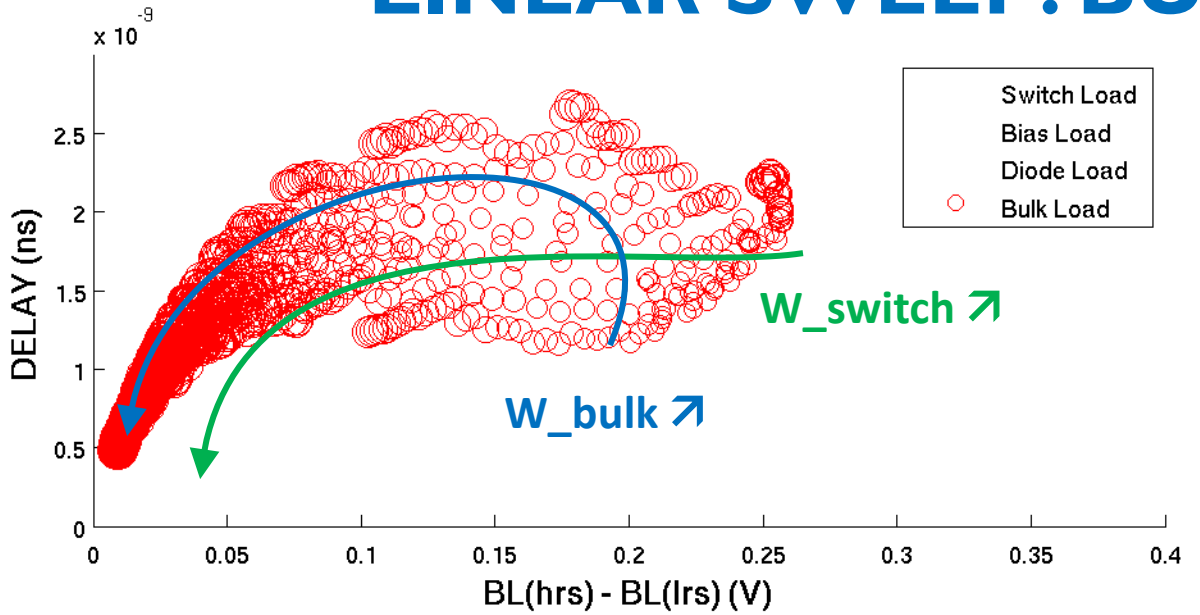


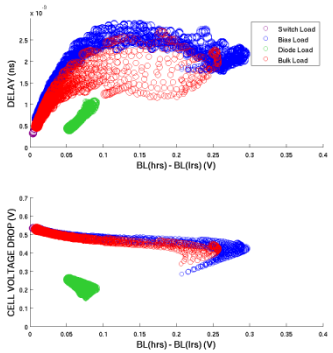


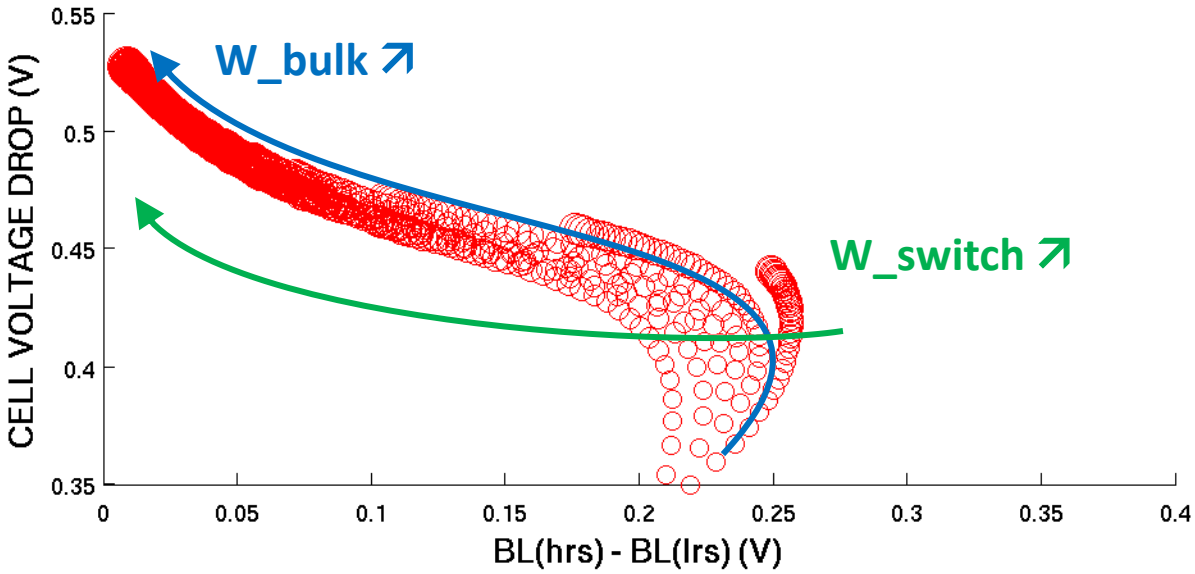


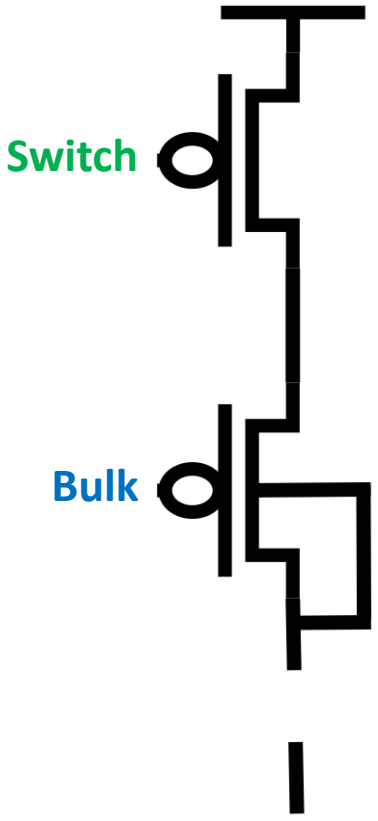


LINEAR SWEEP: BULK LOAD

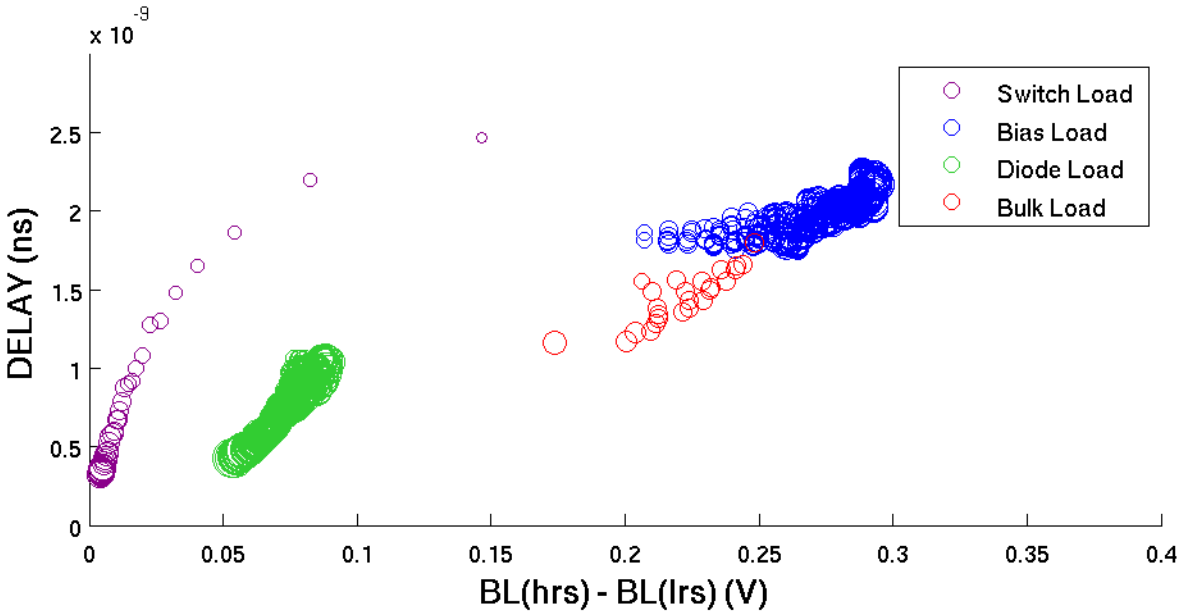


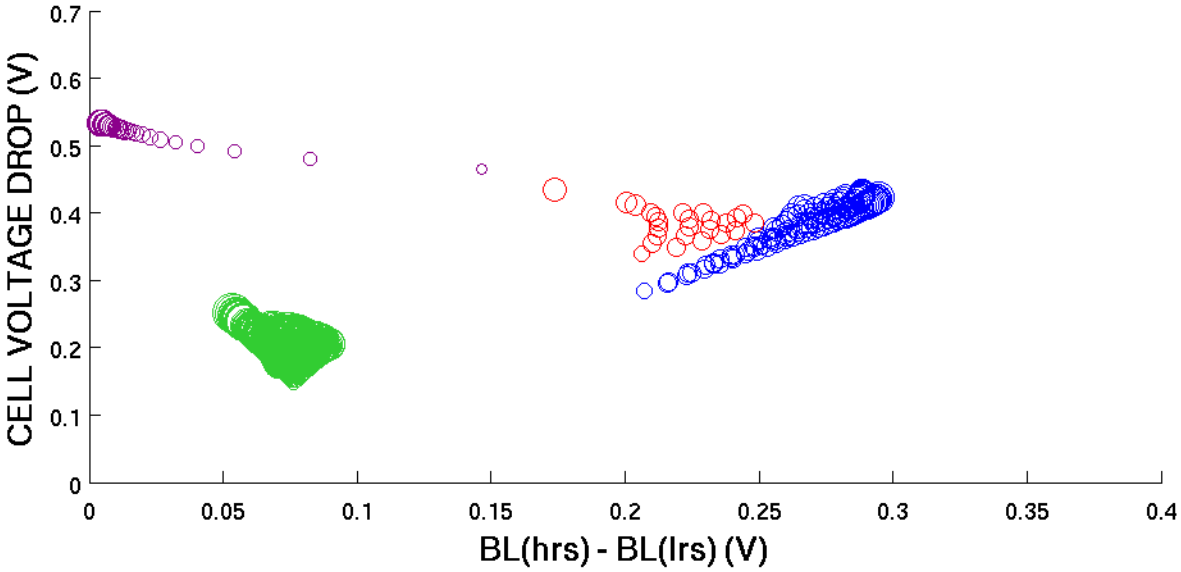






LINEAR SWEEP: PARETO





1681 SOLUTIONS

PARETO OBJECTIVES:

- Area
- Diff BL voltage
- Settle Time
- Voltage drop memory cell

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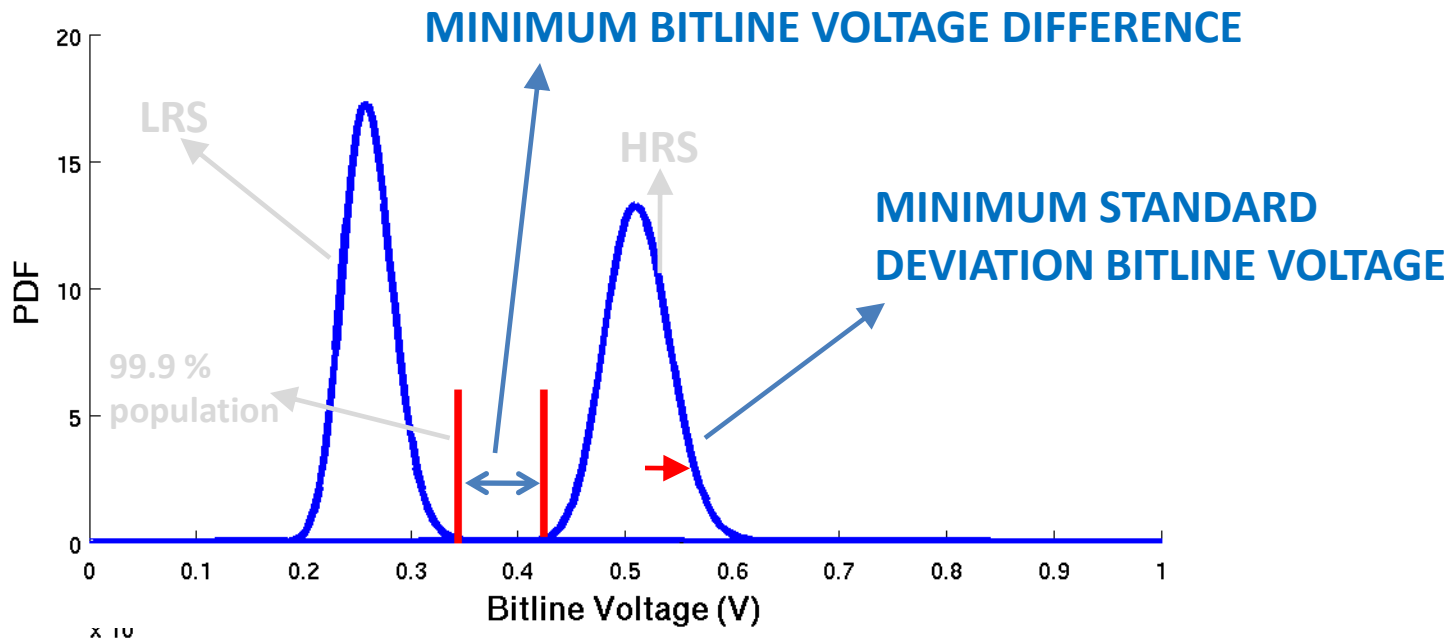
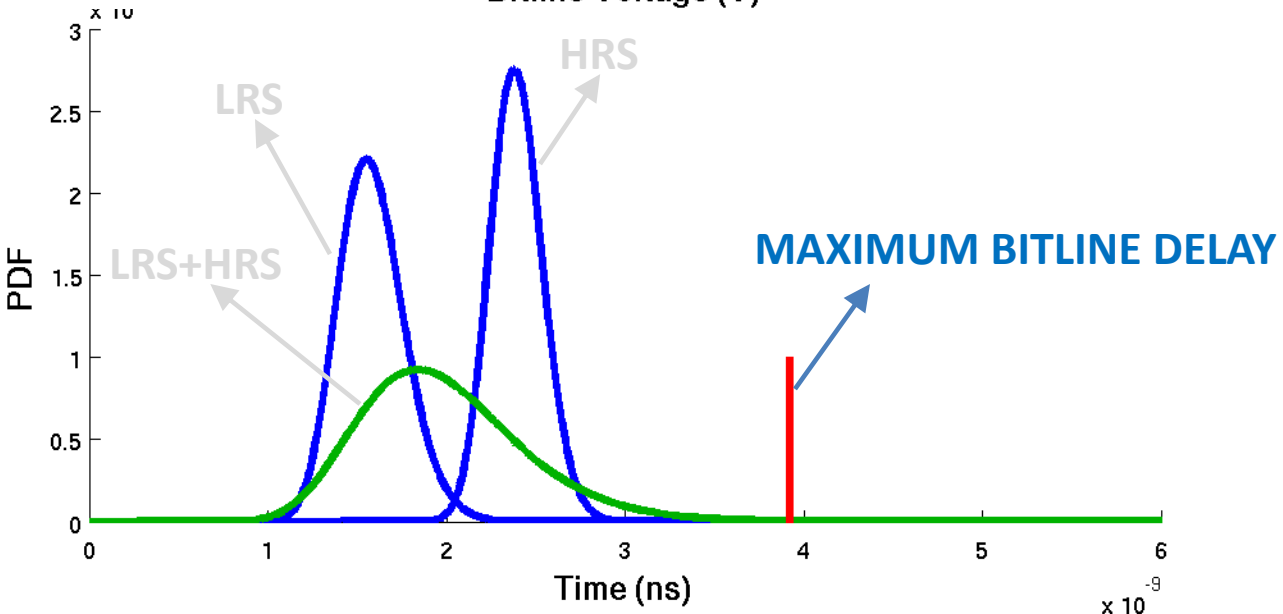
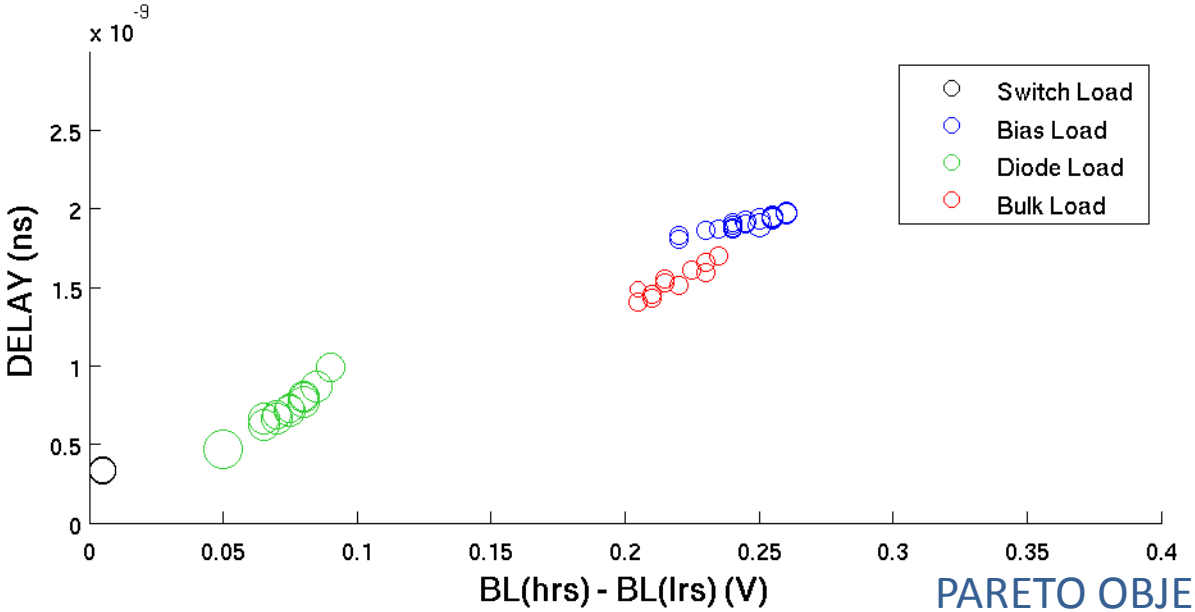
OBJECTIVES MONTE CARLO





MONTE CARLO: PARETO

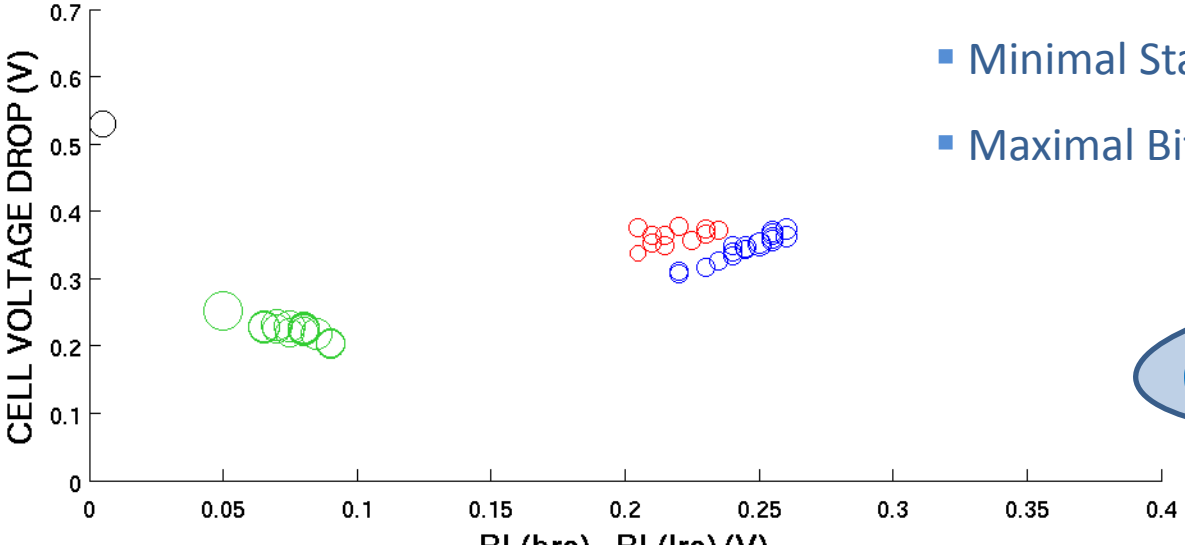


48 SOLUTIONS

A_Vt = 2.5 mV*um
A_I0 = 1.2

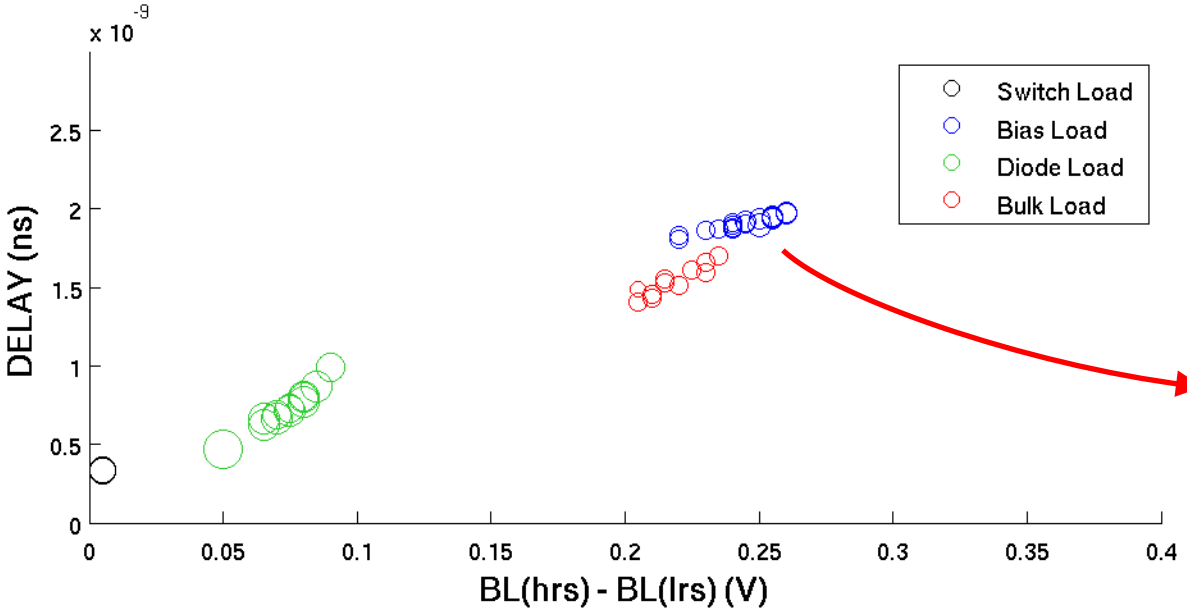
PARETO OBJECTIVES:

- Minimal Bitline voltage difference
- Minimal Standard deviation Bitline voltage
- Maximal Bitline delay



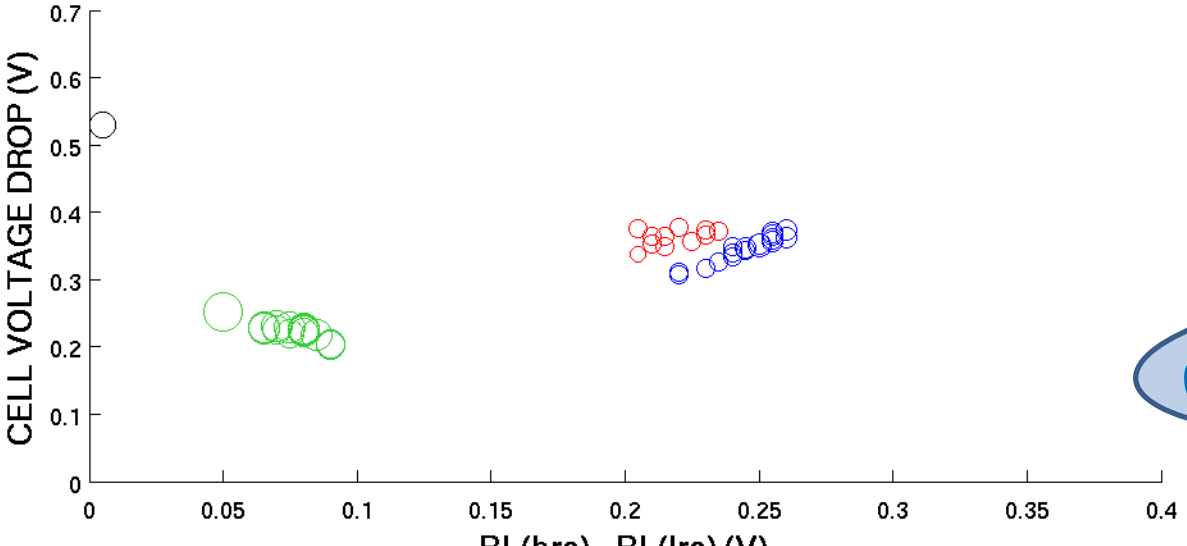
600 mc iterations

MONTE CARLO: PARETO



48 SOLUTIONS

CHOICE FINAL LOAD:
Type = bias
W_switch = 100nm
W_bias = 180nm
V_bias = 0V



600 mc iterations

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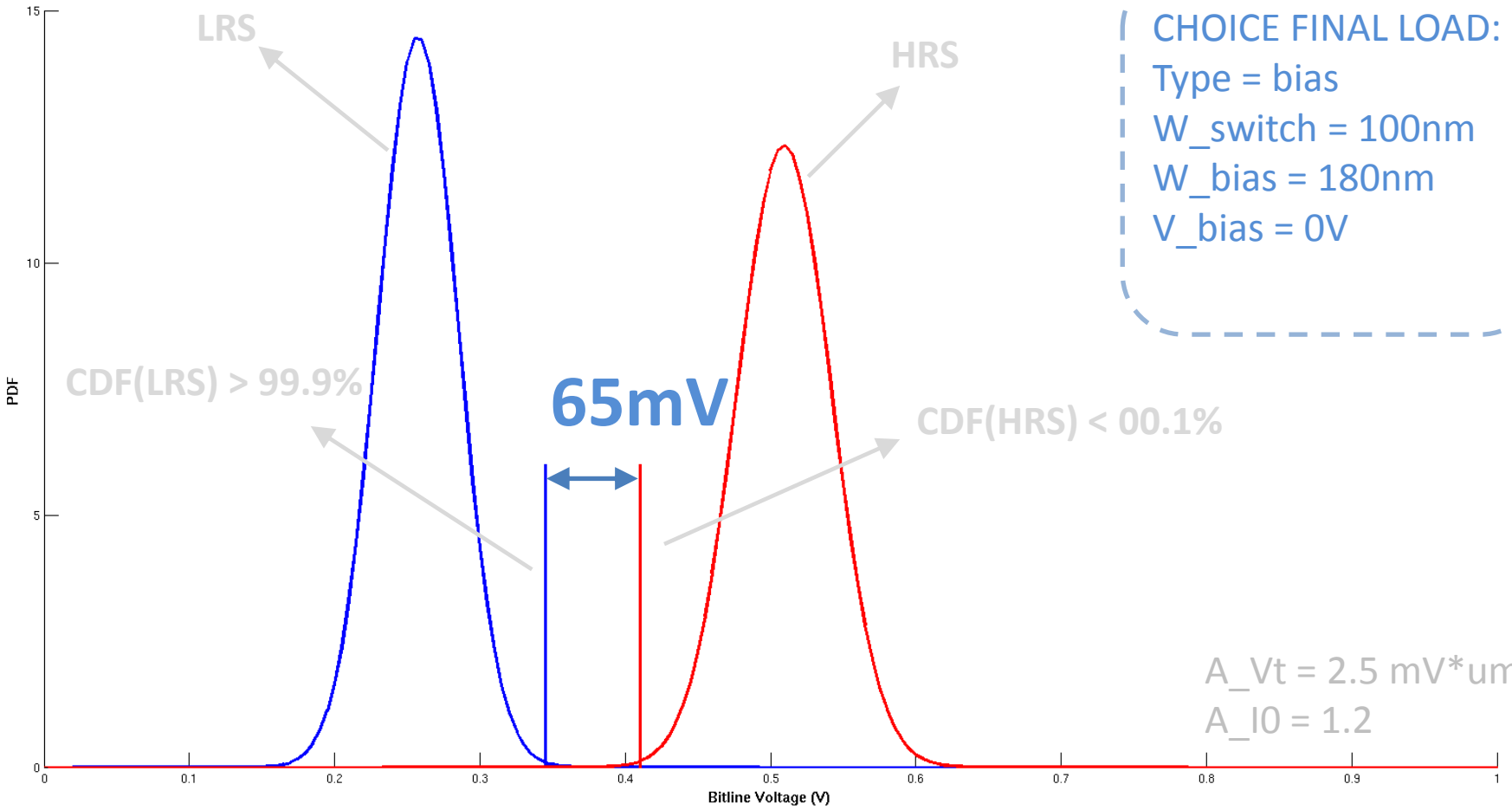
FINAL LOAD: WORST CASE SCENARIO

Everything has mismatch



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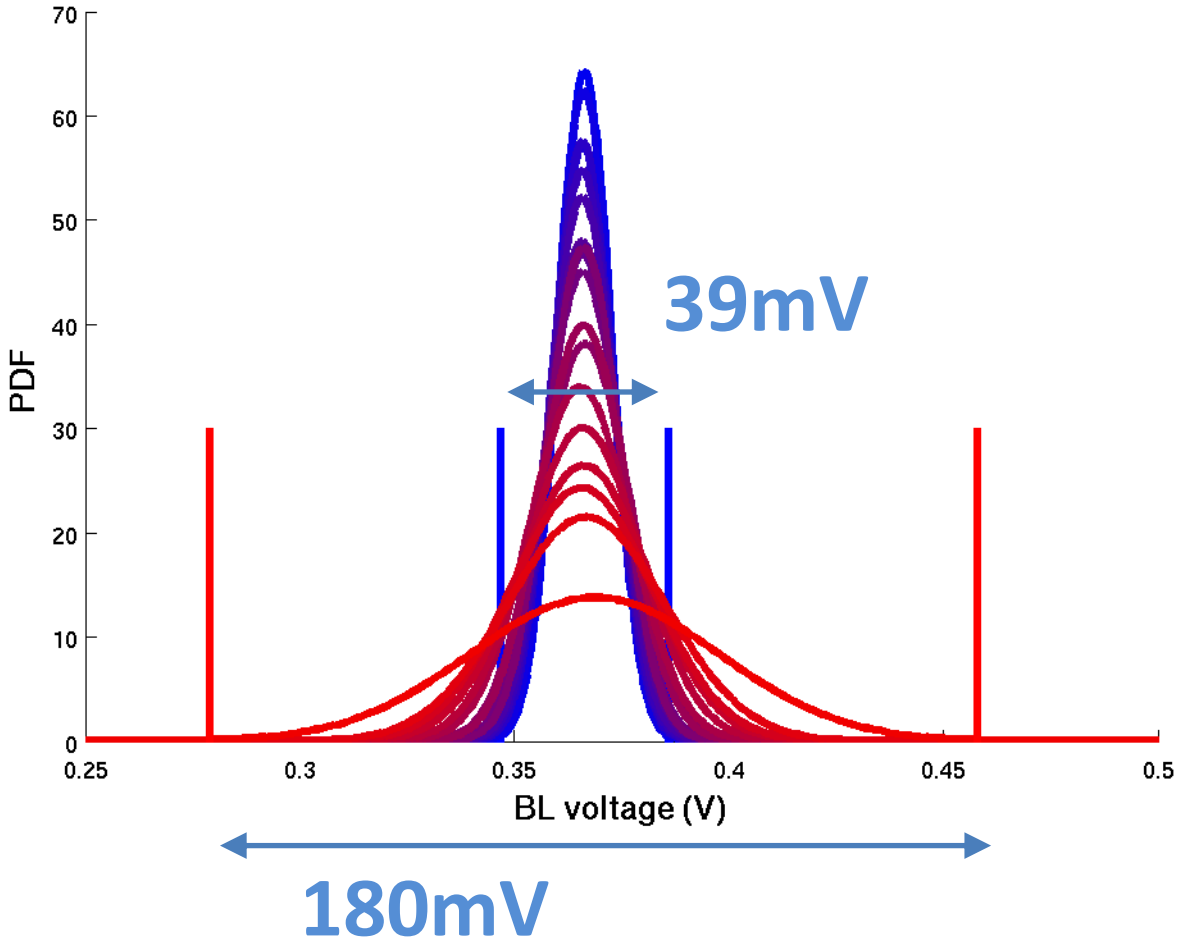
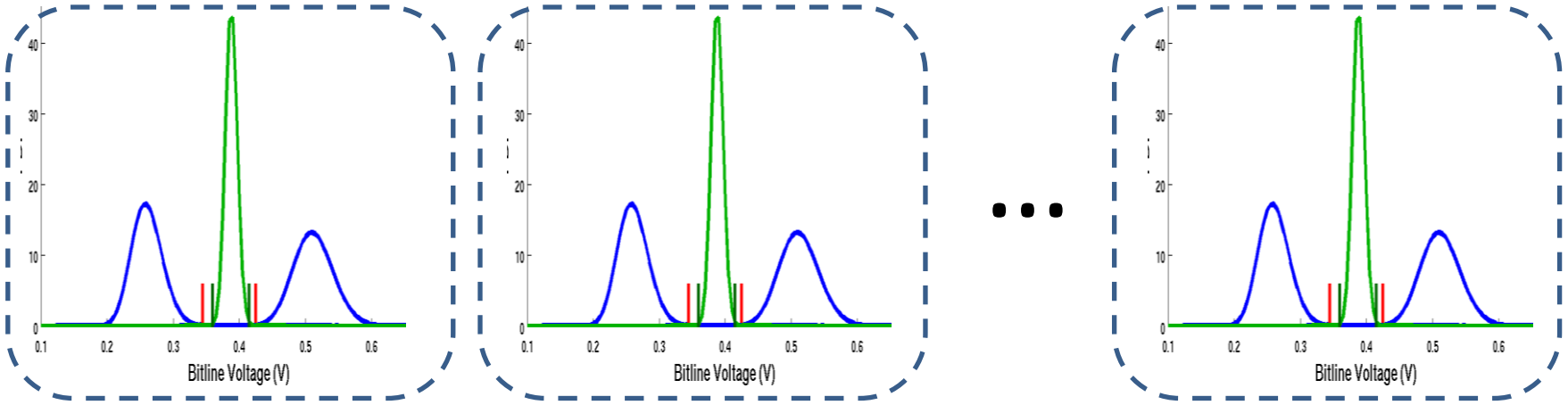


FINAL LOAD: BEST CASE SCENARIO

Load of memory BL and reference BL are matched → Both loads have a mismatch but their mismatch is the same

FINAL LOAD: BEST CASE SCENARIO

Load of memory BL and reference BL are matched → Both loads have a mismatch but their mismatch is the same = 100% correlation

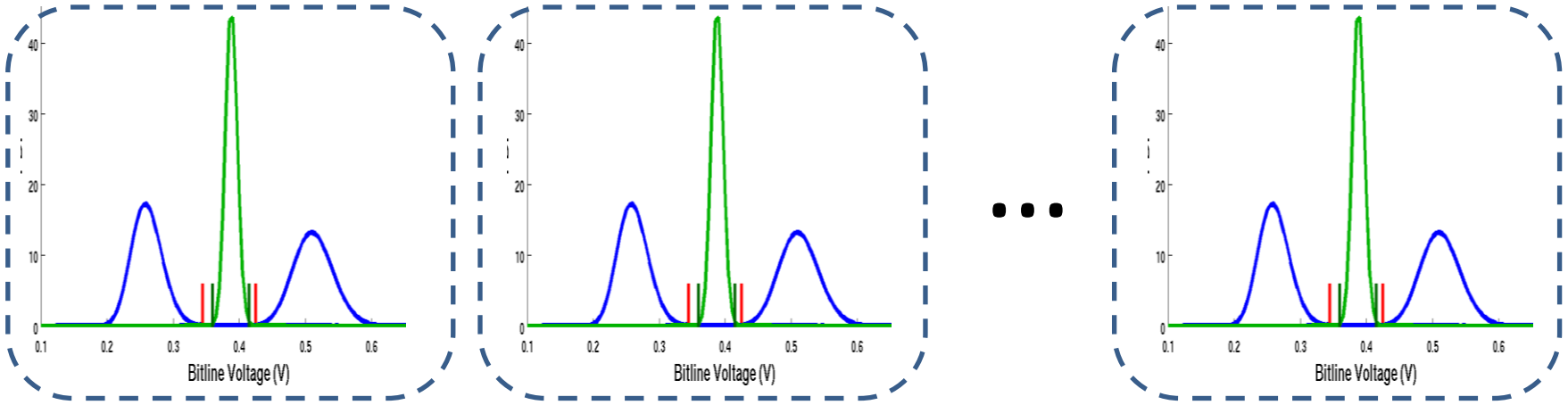


PDF of BL voltage at mismatch instance 1 of loads

PDF of BL voltage at mismatch instance i of loads

FINAL LOAD: BEST CASE SCENARIO

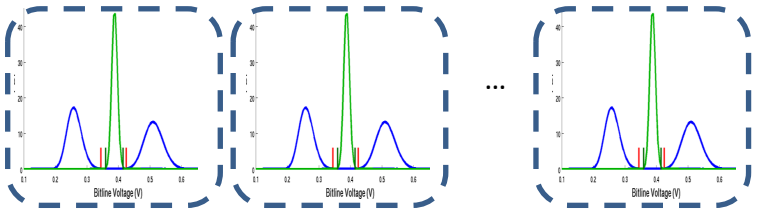
Load of memory BL and reference BL are matched → Both loads have a mismatch but their mismatch is the same

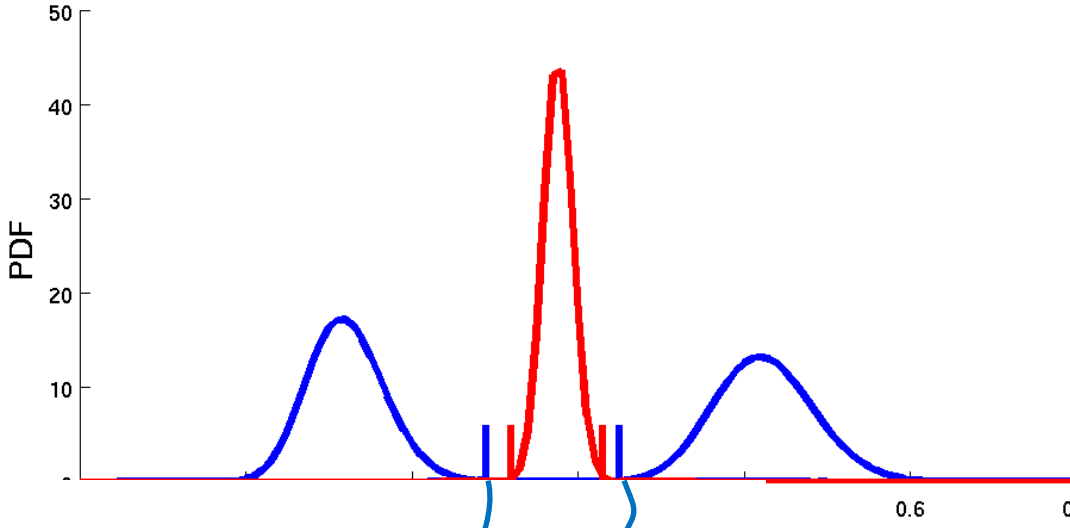


Measure

- CDF(BL_voltage HRS) < 0.1%
- CDF(BL_voltage LRS) < 99.9%
- CDF(BL_voltage REFERENCE) < 0.1%
- CDF(BL_voltage REFERENCE) < 99.9%

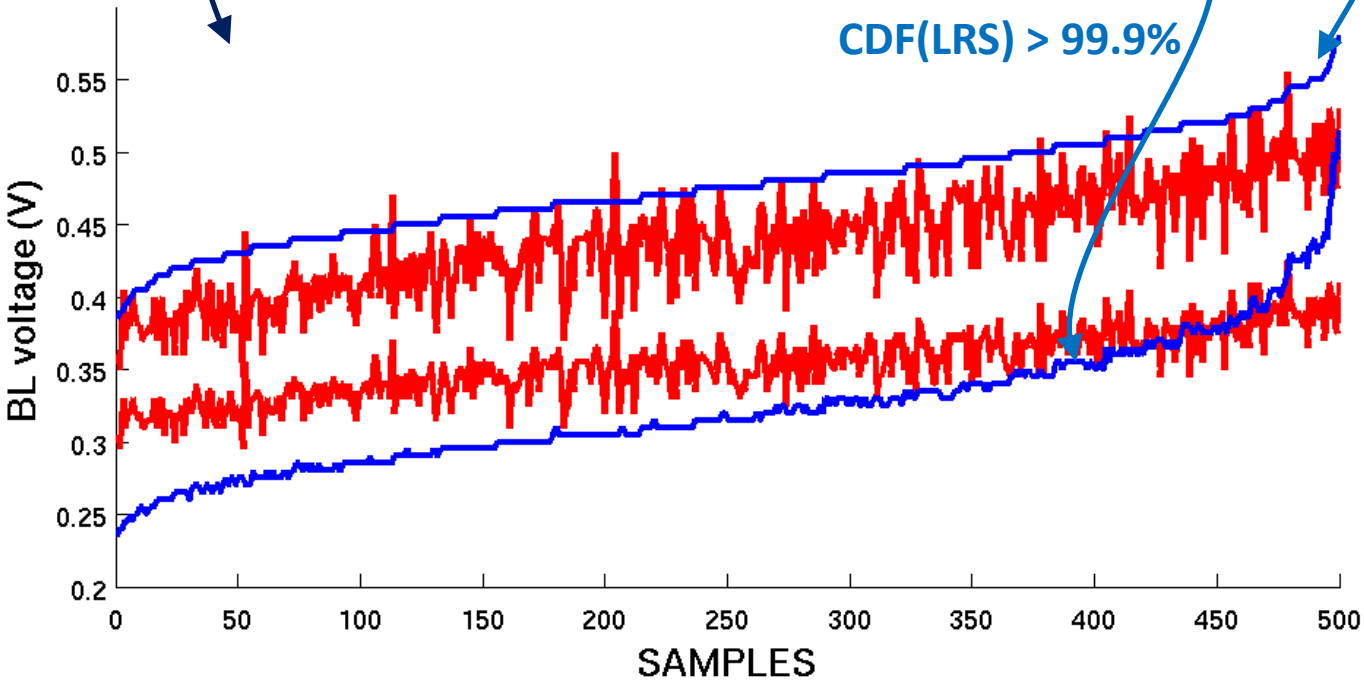
FINAL LOAD: BEST CASE SCENARIO



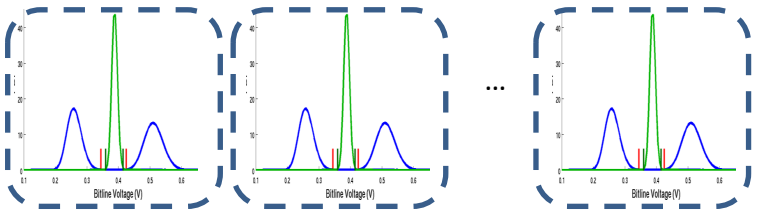


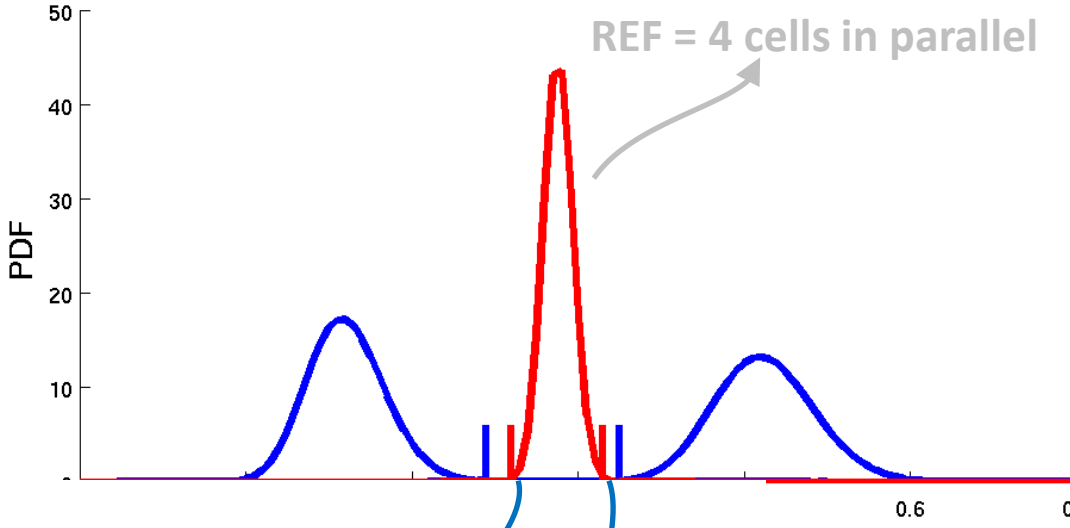
CDF(LRS) > 99.9%

CDF(HRS) < 00.1%



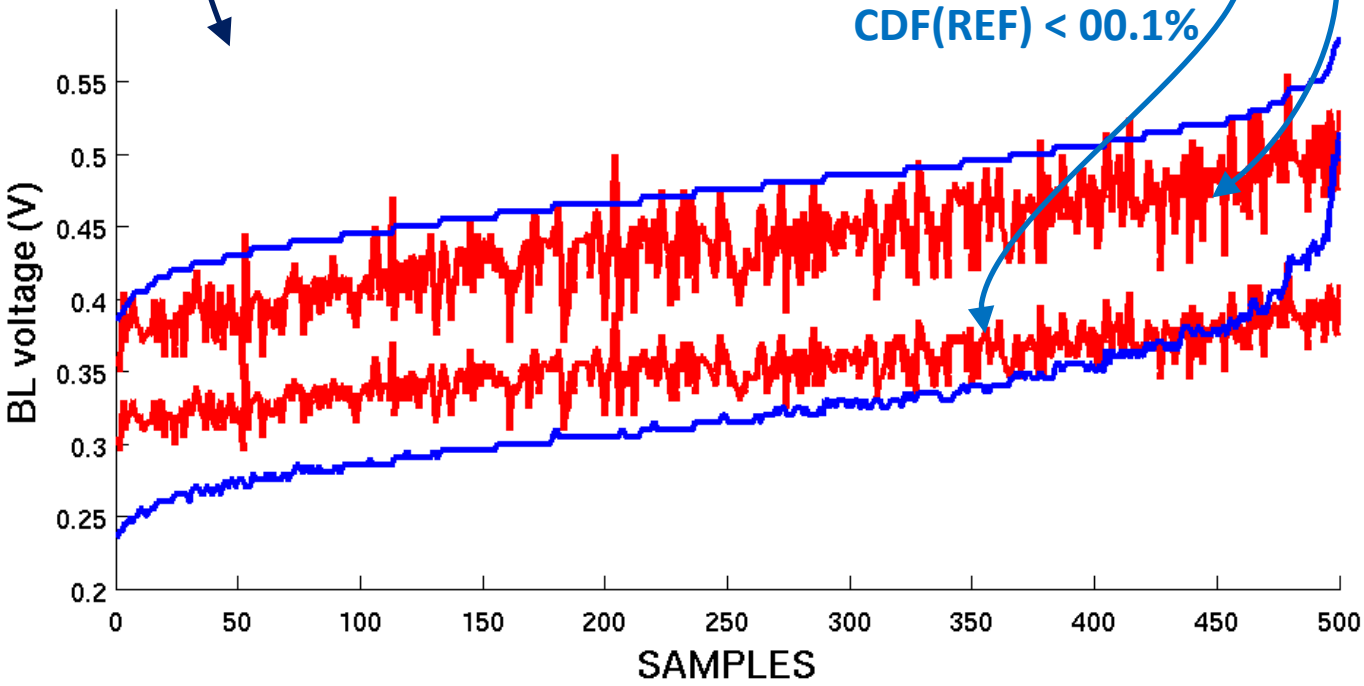
FINAL LOAD: BEST CASE SCENARIO



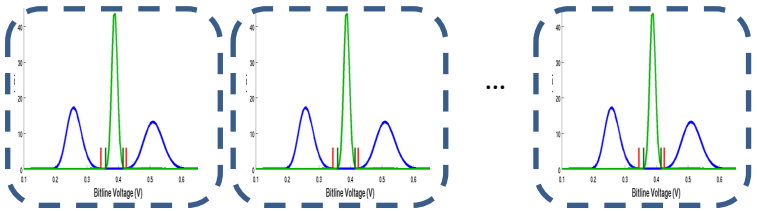


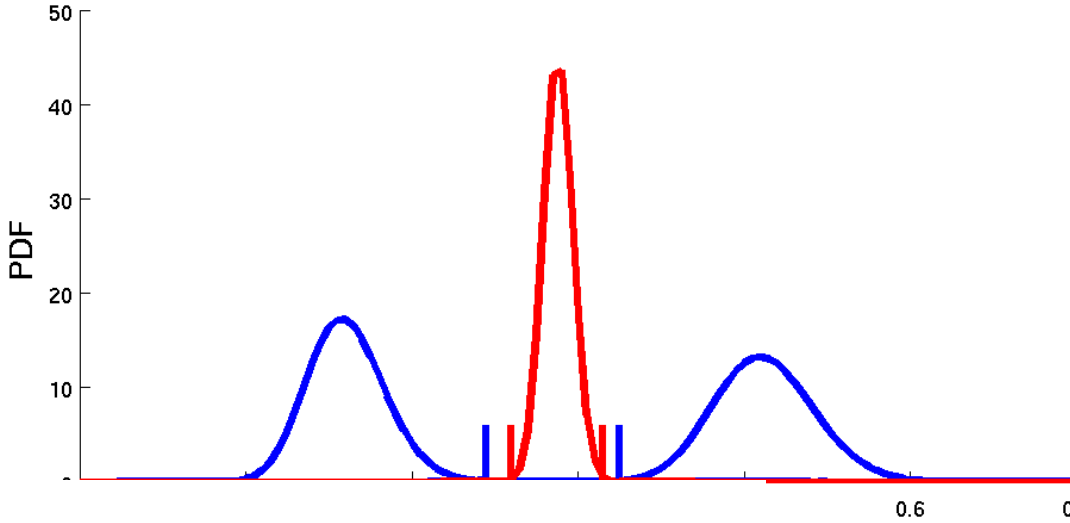
CDF(REF) < 00.1%

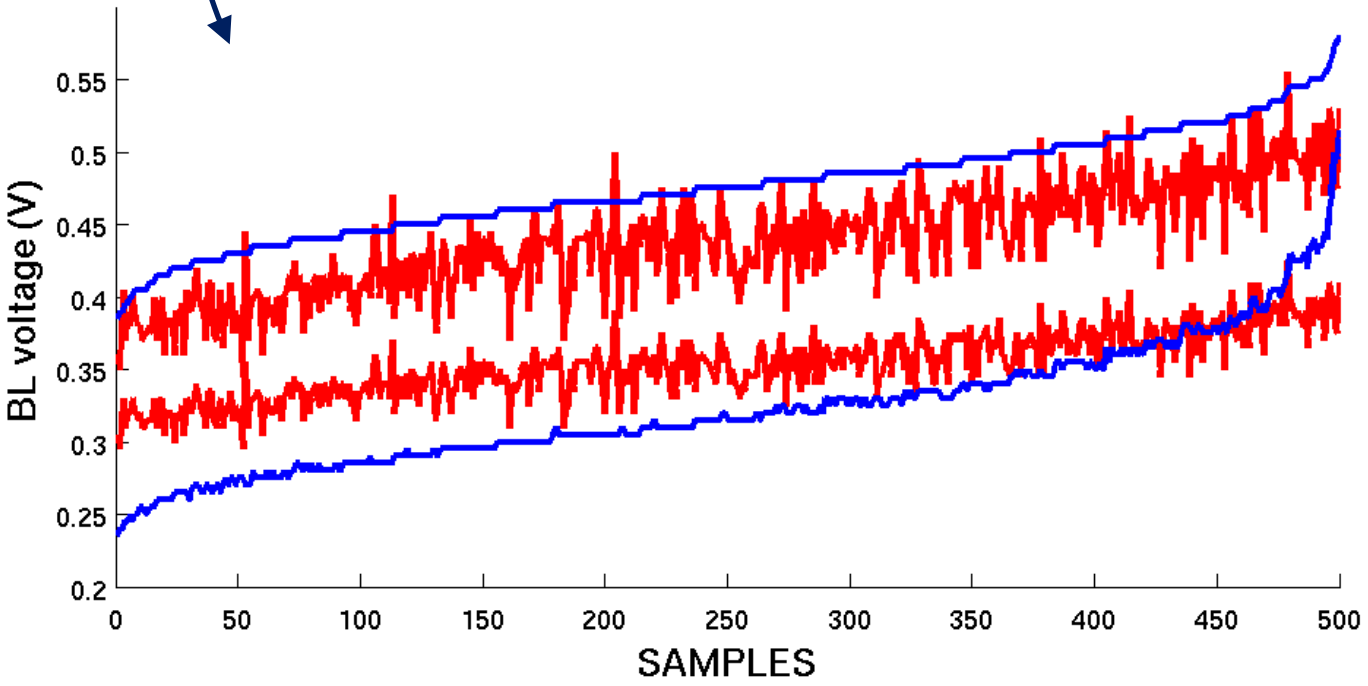
CDF(REF) > 99.9%



FINAL LOAD: BEST CASE SCENARIO

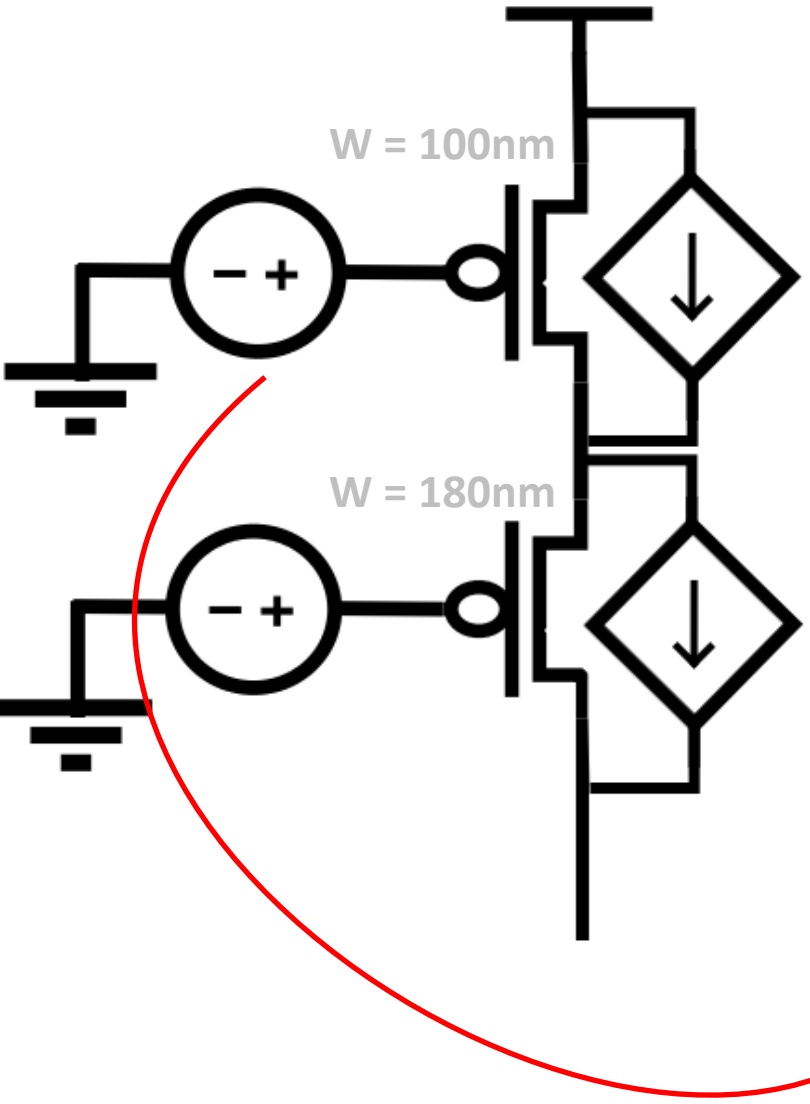


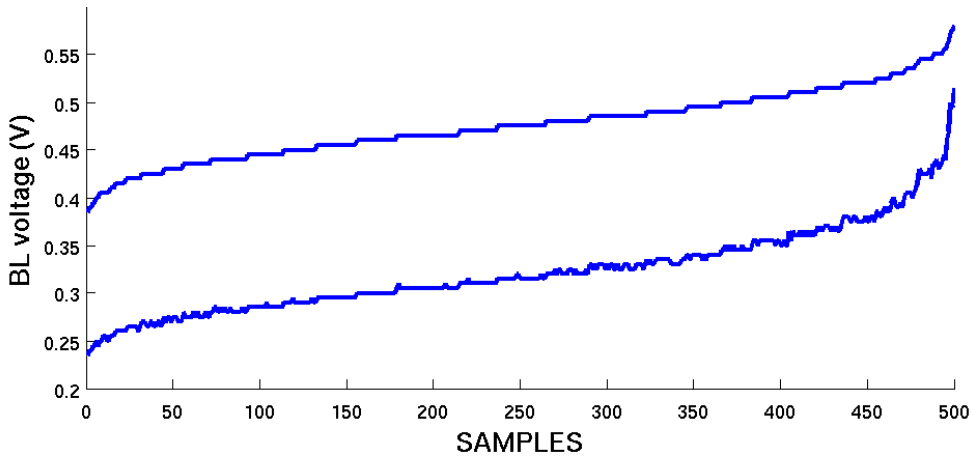


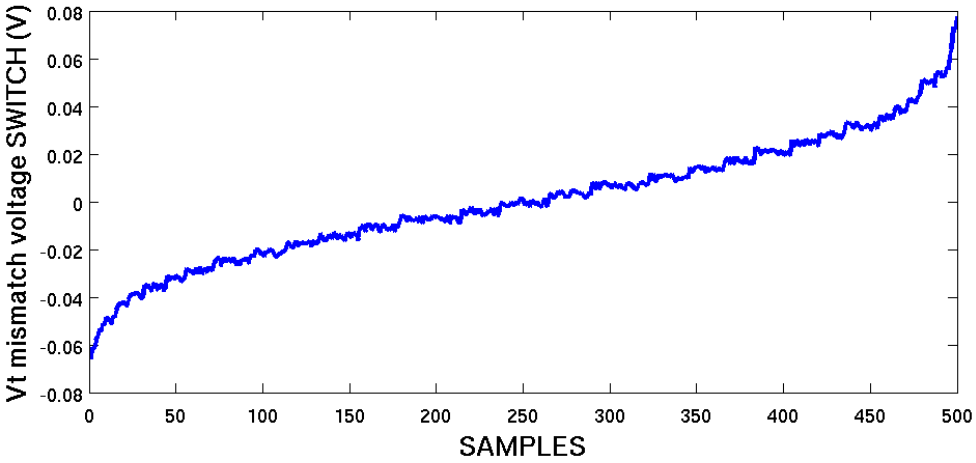


Why do the BL voltages react this way?

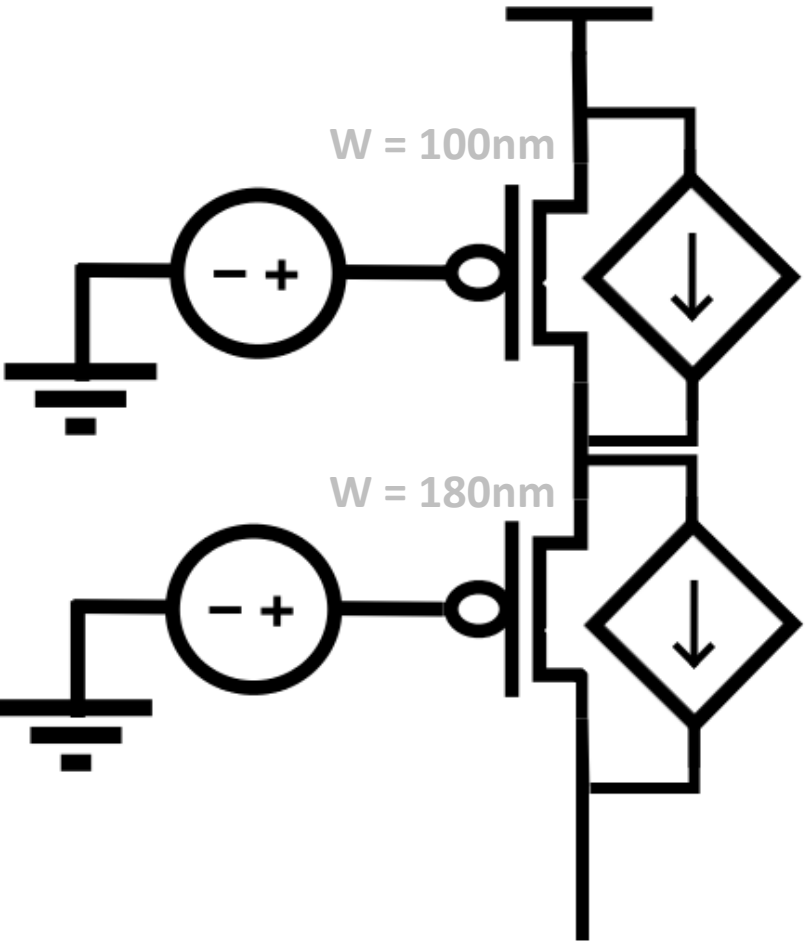
FINAL LOAD: BEST CASE SCENARIO

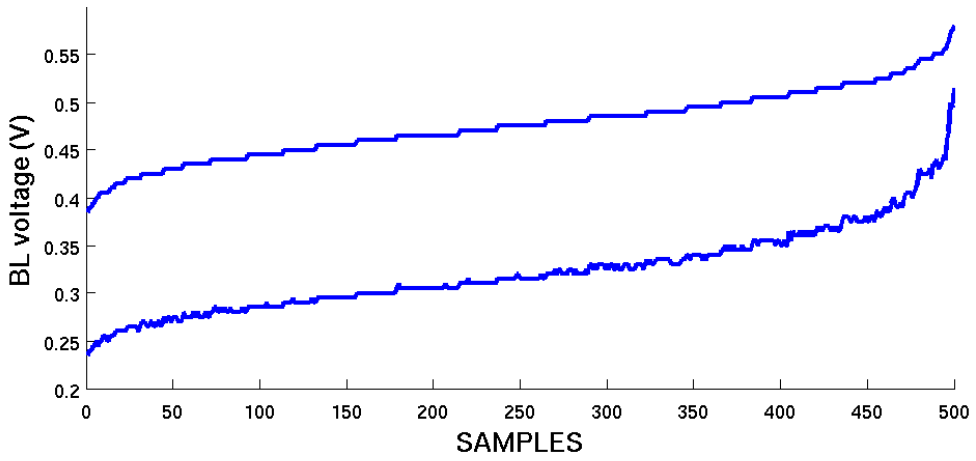


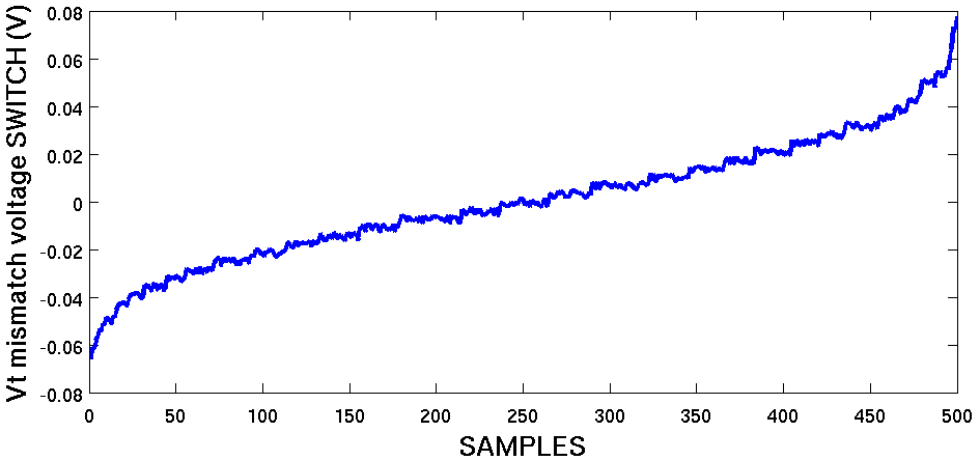




FINAL LOAD: BEST CASE SCENARIO

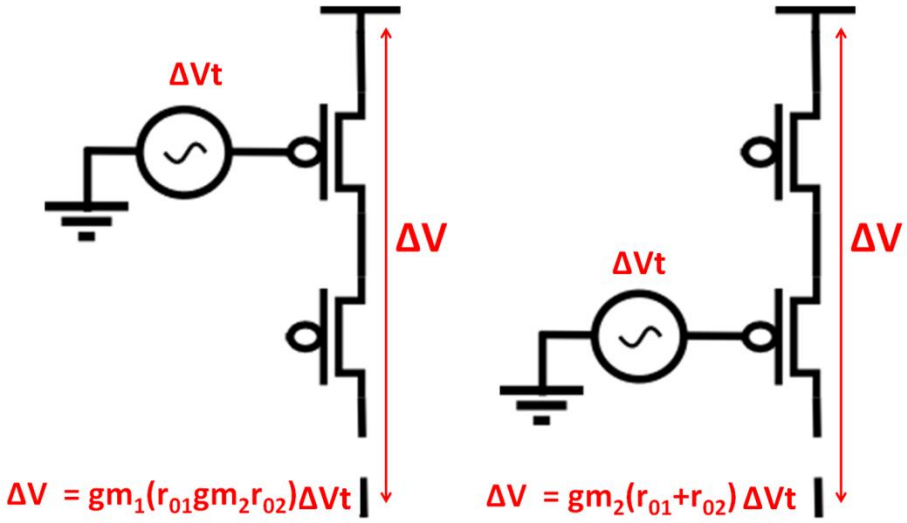






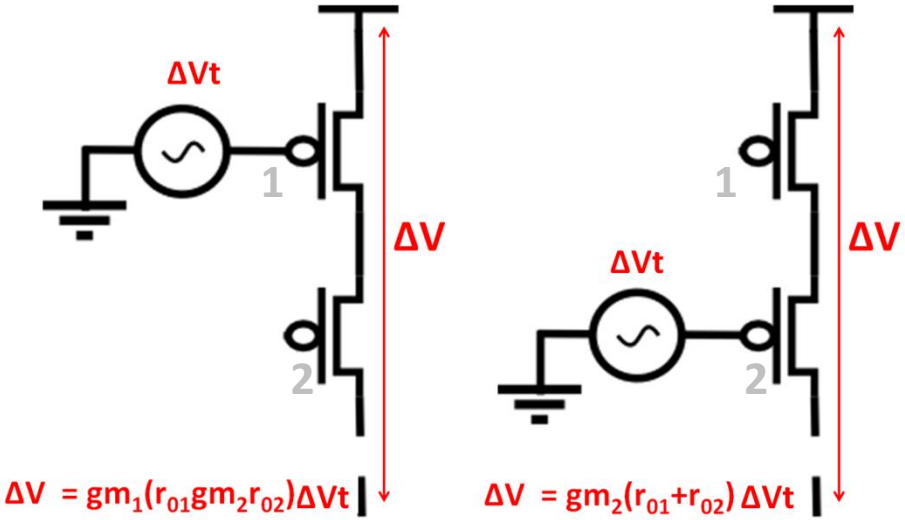
Why Dominant ?

FINAL LOAD: BEST CASE SCENARIO



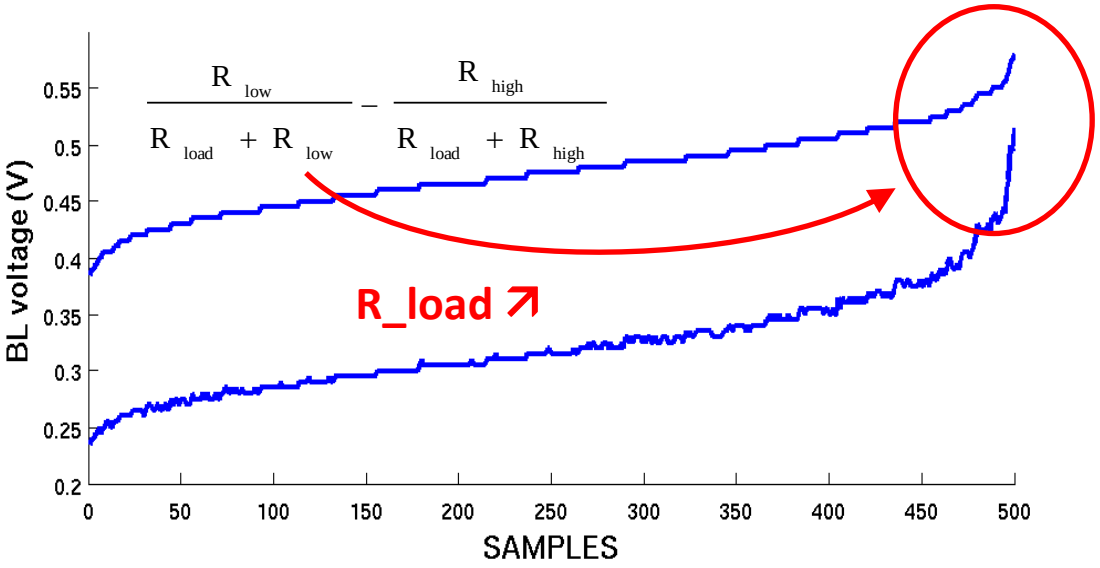
1) Cascode effect : explains why mismatch switch is dominant

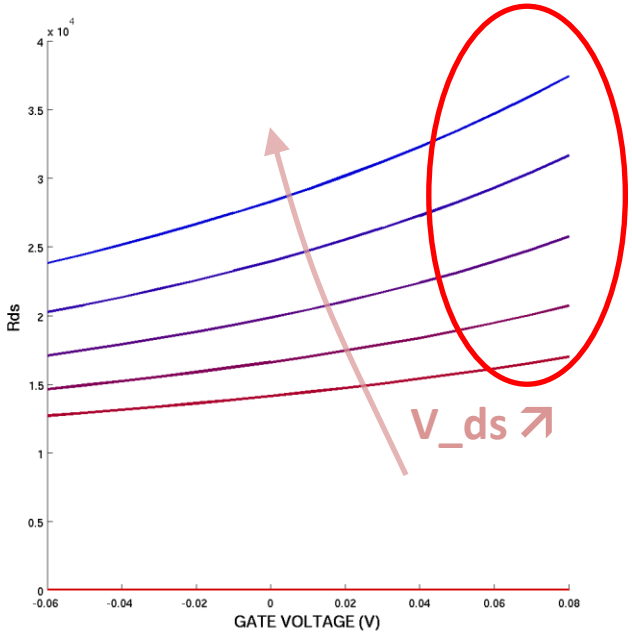
FINAL LOAD: BEST CASE SCENARIO



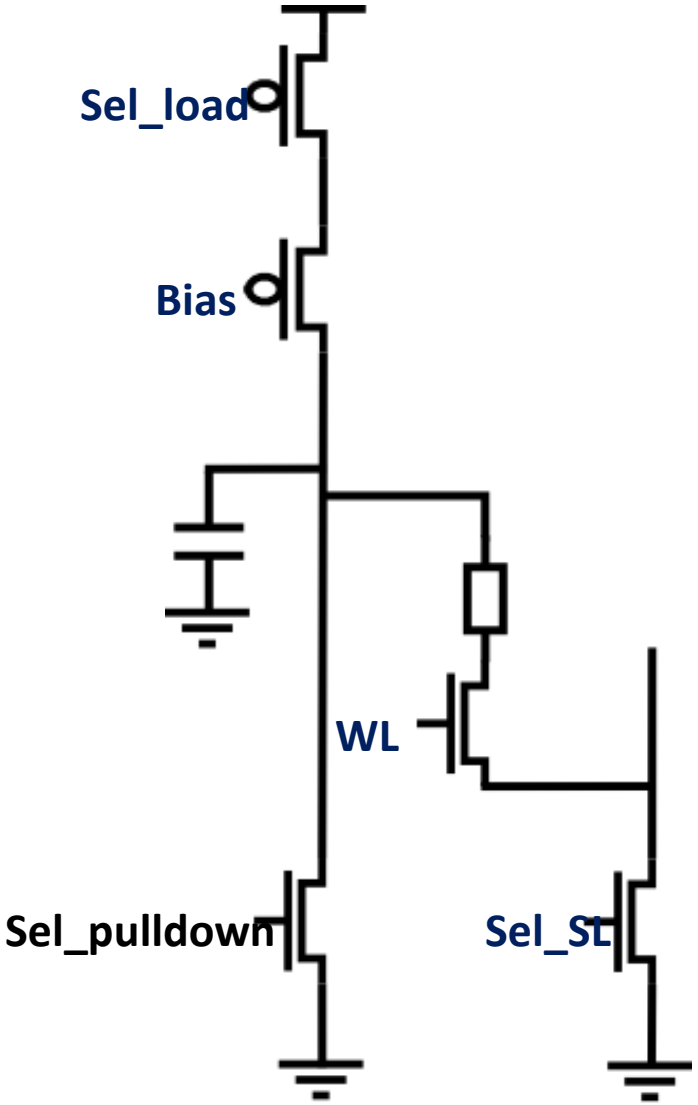
1) Cascode effect : explains why mismatch switch is dominant

2) Increase ds resistance : explains why V_bl(HRS)- V_bl(LRS) becomes smaller at extreme positive values of ΔVt





INTERMEZZO



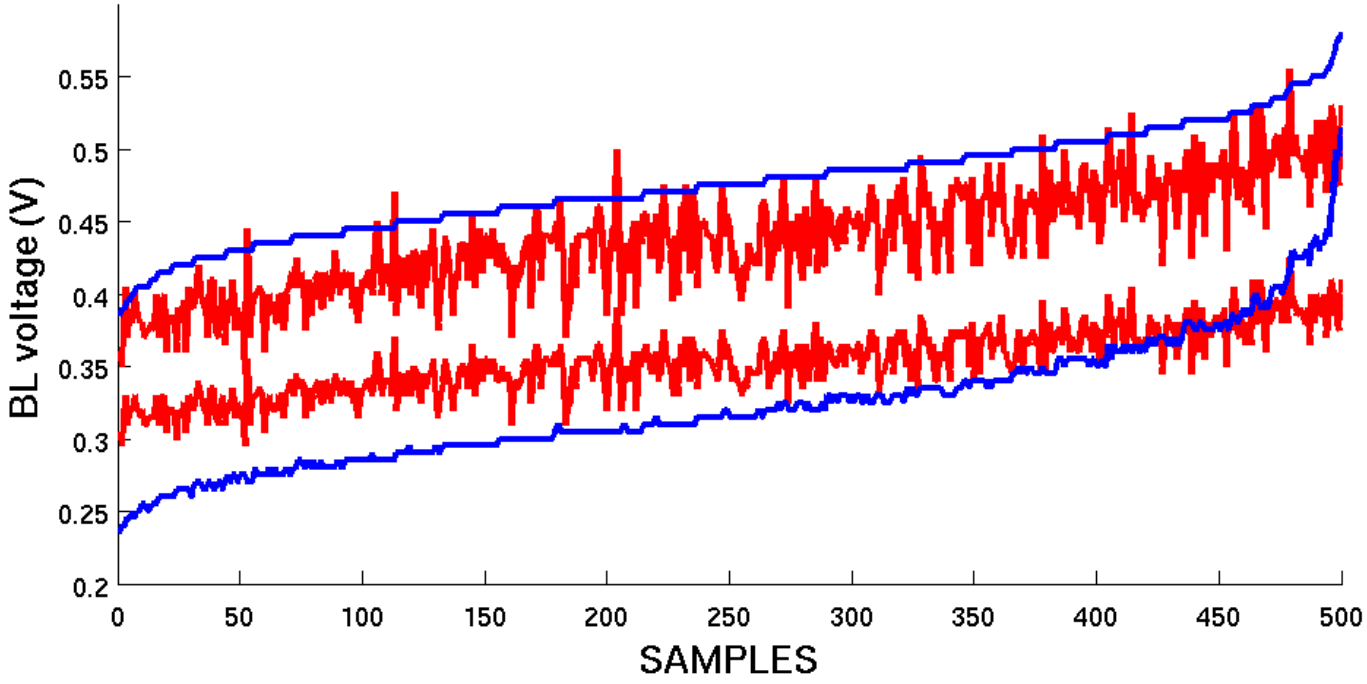
Why no cascode effect with WL and Sel_SL transistors?

$\Delta V = gm_1(r_{01}gm_2r_{02})\Delta Vt$

OUTLINE

- **INPUTS** : Load types, Design parameters and Simulation set up
- **OBJECTIVES** : Linear sweep and Monte carlo
- **RESULTS LINEAR SWEEP**
- **RESULTS MONTE CARLO**
- **FINAL LOAD**
- **CONCLUSION** : Conclusion and Future work

FUTURE WORK


BL voltage (V)
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0
50
100
150
200
250
300
350
400
450
500
SAMPLES