A 5ns Fast Write Multi-Level Non-Volatile 1 K bits RRAM Memory with Advance Write Scheme

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Abstract

A 1-Kb HfO_2 based RRAM for high speed nonvolatile memory application is proposed. With this chip, a high speed write characteristic in the RRAM cell can be achieved. The present circuit design includes a 1T1R RRAM (1 transistor/1 resistive memory) cell and a voltage write circuit, which limit the current through the memory cell. The random write time at VDD = 3.3V is as fast as 5 ns in the RRAM, which were fabricated with a 0.18 μm TSMC process.

Introduction

High performance memory is required for program execution and data storage in computer and consumer electric products [1] [2]. RRAM is a high performance non-volatile memory with fast write characteristic and shorter random access time. The write circuit includes voltage control and current restrict method to switch the resistance state in the memory cell. We propose a read and write scheme of the HfO_2 RRAM in this paper.

Device characteristic

Figure 1 shows the morphology of cross-sectional TEM for HfO_2 staked layers. TiN was used as electrode, and a thin Ti film was inserted between top electrode and the insulator, such a memory cell show excellent memory characteristics [3]. This typical I-V curve is shown in Fig. 2. By the exanimation of the endurance and cycling test, the HfO_2 RRAM can reach 10^8 cycles and both of resistance states are stable. Fig. 3 shows the results of endurance and cycling test.

Chip Organization

The cell schematic diagram is presented in Fig. 4. Fig. 5 shows the array organization of the 8 I/O RRAM 1 Kb chip. Each I/O has 128 bit cells and dummy cell array are located at the left side of 1st I/O and right side of 8th I/O, respectively. Each I/O will select on bit line by SEL circuit. The SET and RESET MUX control the direction of the current in the memory cell. A WL circuit provides a voltage to turn on the select cell and limit the current during the set operation.

Operation Scheme

Figure 6 is a simplified schematic diagram of the write operation. The cell is applied with 1.8 V at positive bias via the bus line and the source line of 0 V is adopted to execute the set operation. Source line is 1.6 V at negative bias in cell and the bus line is 0 V during the reset operation. It needs a maximum limited current of 500 μA to finish the SET operation. So the WL voltage needs provides 2 V to turn on the cell transistor and limit the current. Fig. 7 is a simplified schematic diagram of the read circuit. The power supply of read circuit is 1.8 V. The RRAM reference cell generates a 40 μA as a reference current, and a read current (I_{read}) of 1/4 of the reference current in cell guarantees the sense margin while the sense amplifier reads out the set state in the memory cell. The read enable signal triggers a high but short EQ pulse when the read process is activated. The RBL terminal will generate reference voltage with 4 times I_{read} to compare the DBL cell terminal voltage.

Multi level operation

For multi-level operation of the memory cell, the limited current of the cell needs to be modified. This write circuit is shown in Fig. 8. By restricting the cell current through the cell transistor gate voltage, the resistance state in the memory can be divided into 4 levels. The resistance of memory cell depends on different WL voltage, which induced by the different limited current. The WL maximum voltage only needs 3.3V in multi-level operation without the charge pumping circuit.

Measurement Results of 1Kb RRAM chip

Figure 9 shows the photograph of 1 Kb chip RRAM in this work. Fig.10 shows the resistance distribution result of the 1 Kb chip RRAM. Fig. 11also shows the resistance distribution of 4-level in the array. Fig. 12 shows the successive write and read of memory cells from address 02AH to 02EH. When the WE is high, the reset operation is executed. Then RE is high and WE is Low. The voltage of sense amplifier cell is 0.5 V. When the set operation is finished, the voltage of cell changed to 0.05V. The 5-ns pulse width of WE can switch the LRS or HRS in the memory cell. Fig 13 shows the multi-level read circuit results of the 1Kb chip RRAM.

Conclusion

The 1K bits of 1T1R multi-level RRAM of 0.3 μm^2 cell size with HfO2 as storage material have been fabricated successfully on a 0.18 μm technology. The R-ratio is over 1000 and the endurance of the memory cell exceeds over 10^8. A 5 ns random access write speed is achieved at a power supply of 3.3 V VDD. This chip also shows multi-level operation characteristic. It is very attractive for next generation memory.

Reference

[1] M. Kund et al.,IEDM, Tech. Dig., pp. 7736, 2005
[2] P. Schrögmeier et al., VLSI Circuits Symposium, pp.186, 2007.
[3] H.Y.Lee et al., IEDM, Tech. Dig., pp. 297, 2008.

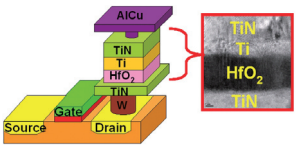


Fig. 1 Schematic of HfO_2 based RRAM in 1T1R configuration and TEM image of 1R cell.

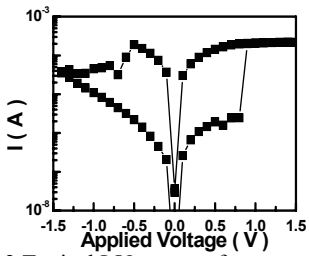


Fig. 2 Typical I-V curves of memory device.

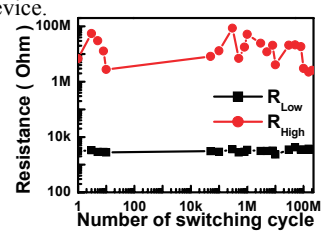


Fig. 3 Switching endurance of memory cell under high speed (20ns) SET and RESET process.

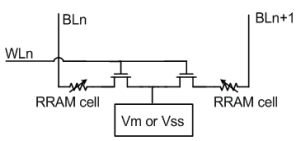


Fig.4 Cell schematic of 1T1R RRAM.

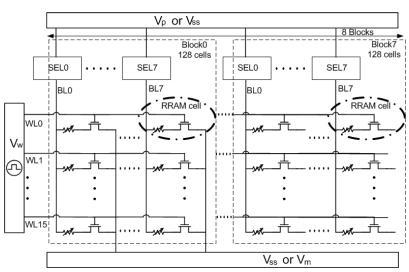


Fig.5 The array organization of 1kb chip.

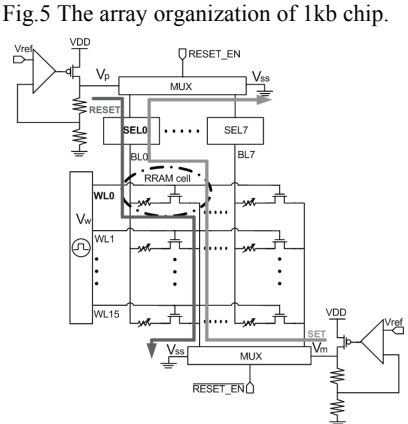
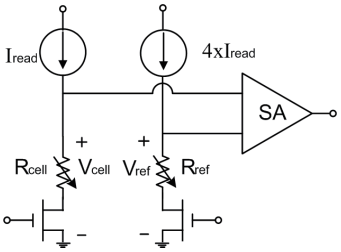
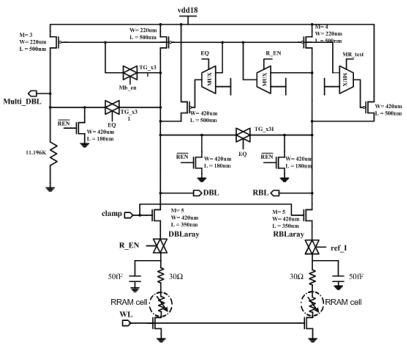


Fig.6 The write circuit of 1kb chip.





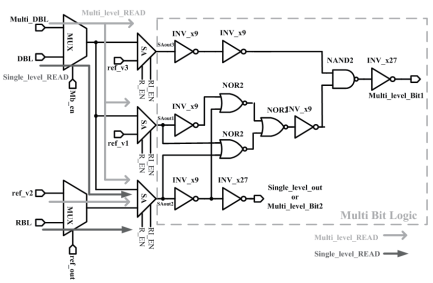


Fig.7 The read circuit of RRAM 1kb chip with multi-level read scheme.

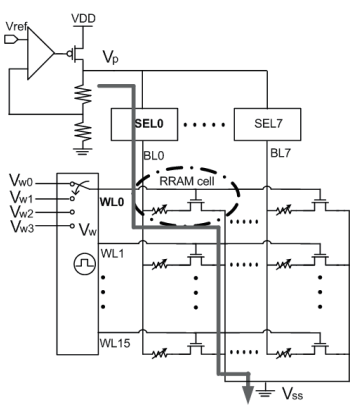


Fig.8 Write circuit for multi-level operation.

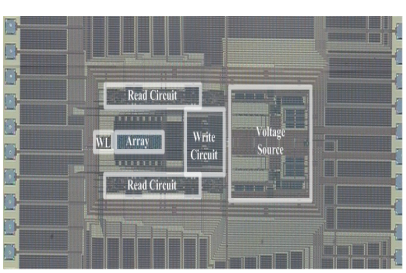


Fig.9 Micro photograph of 1kb chip.

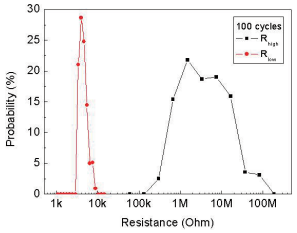


Fig.10 The resistance distribution of 1kb chip.

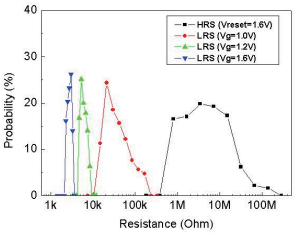


Fig.11The resistance distribution of multi-level operation.

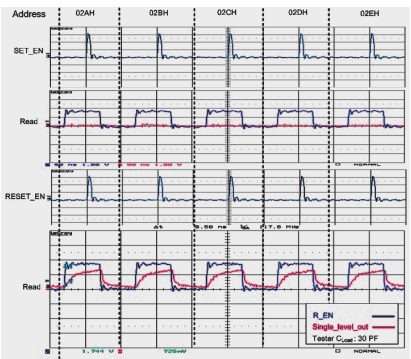


Fig.12 The R/W measurement result of RRAM 1kb chip.

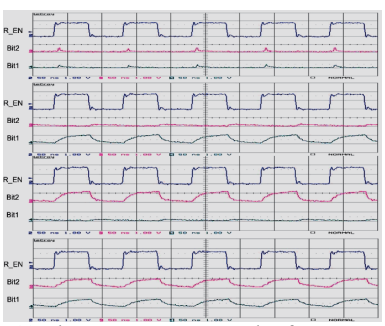


Fig.13 The measurement result of multi-level read circuit.

Table.1 1Kb 4-level RRAM features

Technology node	TSMC 0.18um 1P4M process and RRAM BEOL at ITRI
Organization	128 X 8
Chip Size	7.84 mm^2
Maximum Power	3.96 mW
SET/RESET time	5 ns/5 ns
SET/RESET voltage	1.8 V/-1.6 V
Read time	8.5 ns
Memory Cell size	0.3 um^2
Storage material	HfO_2
Endurance	> 10^8