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**PROTOKOLL**zur Laborübung

***PLL / F-Synthese***



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| --- | --- | --- |
| Gruppe / Klasse | Protokollführer | Unterschrift |
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| BOCH |  |  |
| Note | Mitarbeiter | Unterschrift |
|  |  |  |
| ***PLL / F-Synthese*** | | |
| **Verwendete Geräte**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | Nr. | Gerätebezeichnung | Hersteller | Typ | Platznummer | |  | Oszilloscope | Tektronix | TDS2012B | Oszilloscope | |  | Function Generator | HP Packard | 33120A | Function Generator | |  | Power supply | TTi | EL301 | Power supply | | | |

ÜBUNGS-/ABGABE-DATUM

Klasse /Gruppe

NOTE

LEHRER

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# Task

The job was to build up a PLL and a Counter and to measure each part of it separately. After measuring each part the counter should be connected to the PLL and frequency synthesizer should be built.

# Setup

The pictures below show the complete cuircuit for a PLL with a counter which should be used to make an variable frequency synthesizer. The counter was a programmable hef4059bp ic. By changing the levels at the J1 to j4 pins the counting state could be changed. Ka and Kb was set low and Kc was set high, so a prescaler of 10 was defined. By changing the levels of the pins j1 to j3 the counting state could be changed from 4 to 8.

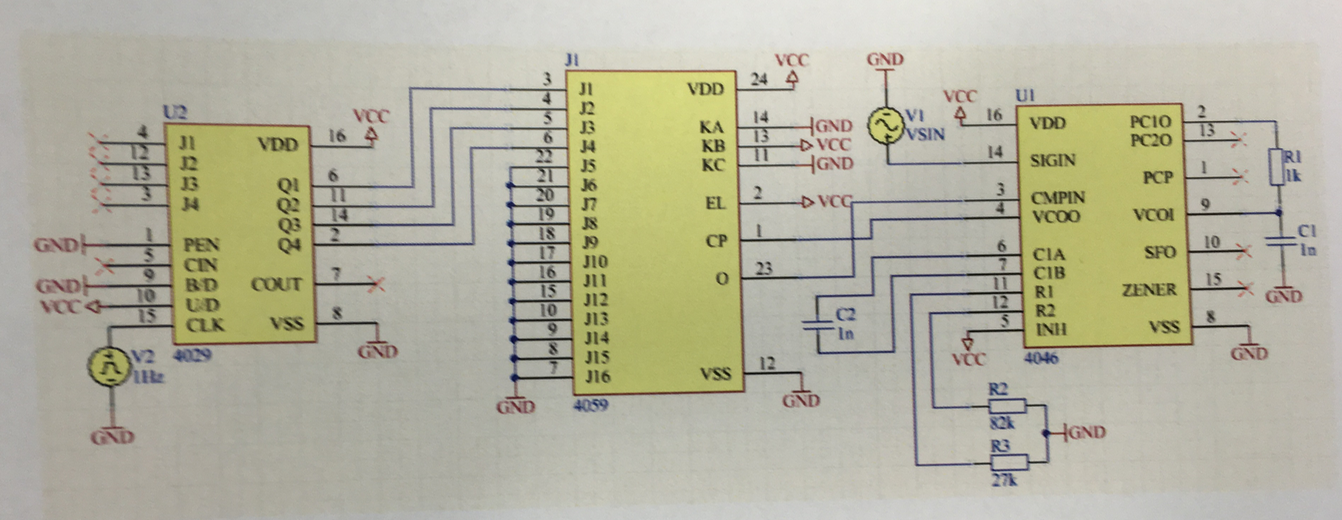


Figure 1 - Complete Circuit (4029 / 4059 / 4046)

# EF4059B

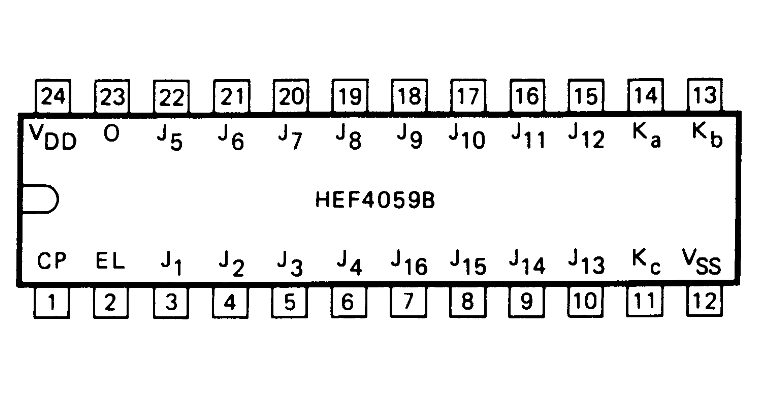


Figure 2 - Pin content from the HEF4059-module

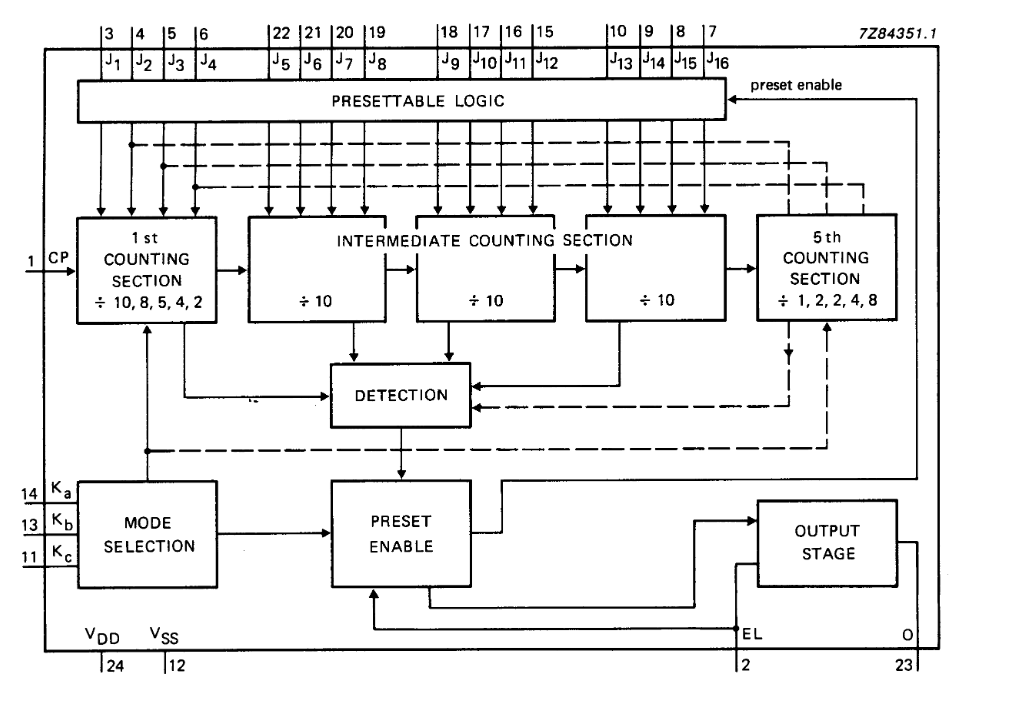


Figure 3 - Functional-Block-Diagram from the divide-by-n Counter

# MC14029B

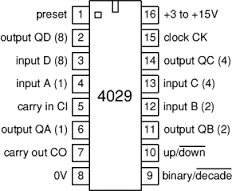


Figure 4 - Pin content form the Up/Down-Counter

# Calculation

The calculation is to find out which pin was set to which state to divide by 10. For this calculation you have to take the table from the Datasheet and the following formula.

N=Mode\*(1000\* decade 5 Preset + 100\* decade 4 Preset + 10\* decade 3 preset + 1\* decade 2 Preset) + decade 1 Preset

N= 10\*(1000\*0 + 100\*0 + 10\*0 + 1\*0) + (J1...J4)

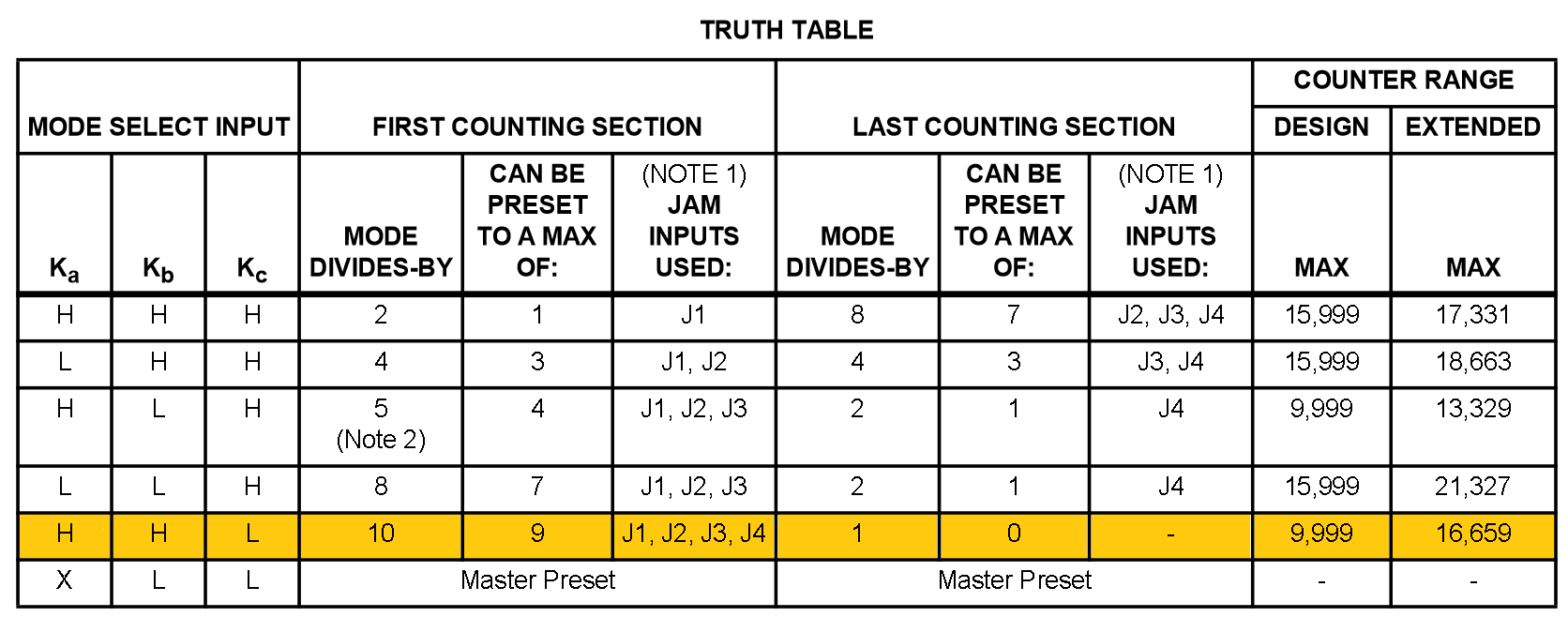


Figure 5 Truth table of the Counter

# Measurements

After setup a truth table for the jam inputs (j1…j4) was made. After this truth table the counter was setup.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| j1 | j2 | j3 | j4 | Divider |
| 0 | 0 | 0 | 1 | 8 |
| 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 1 | 6 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 7 |

Figure 6 - Measure truth table of the divider jam inputs (j1 - j4)

Connected with the PLL, the PLL locked at about 360 kHz mid frequenzy.

Min. frequency: 150 kHz

Max. frequency: 572 kHz

Mid. Frequency: 361 kHz

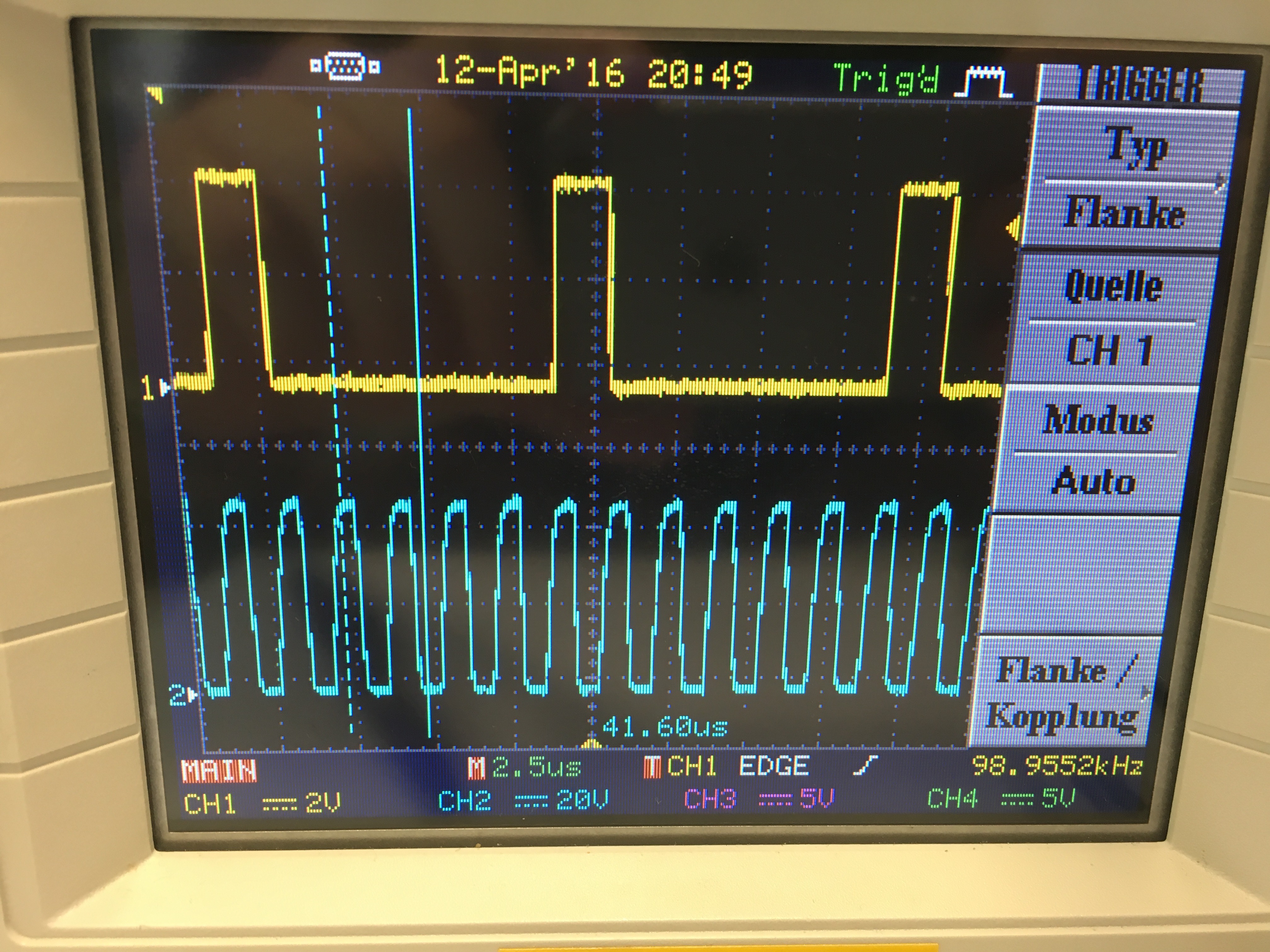


Figure 7 Measurements on the divider IC (4059)

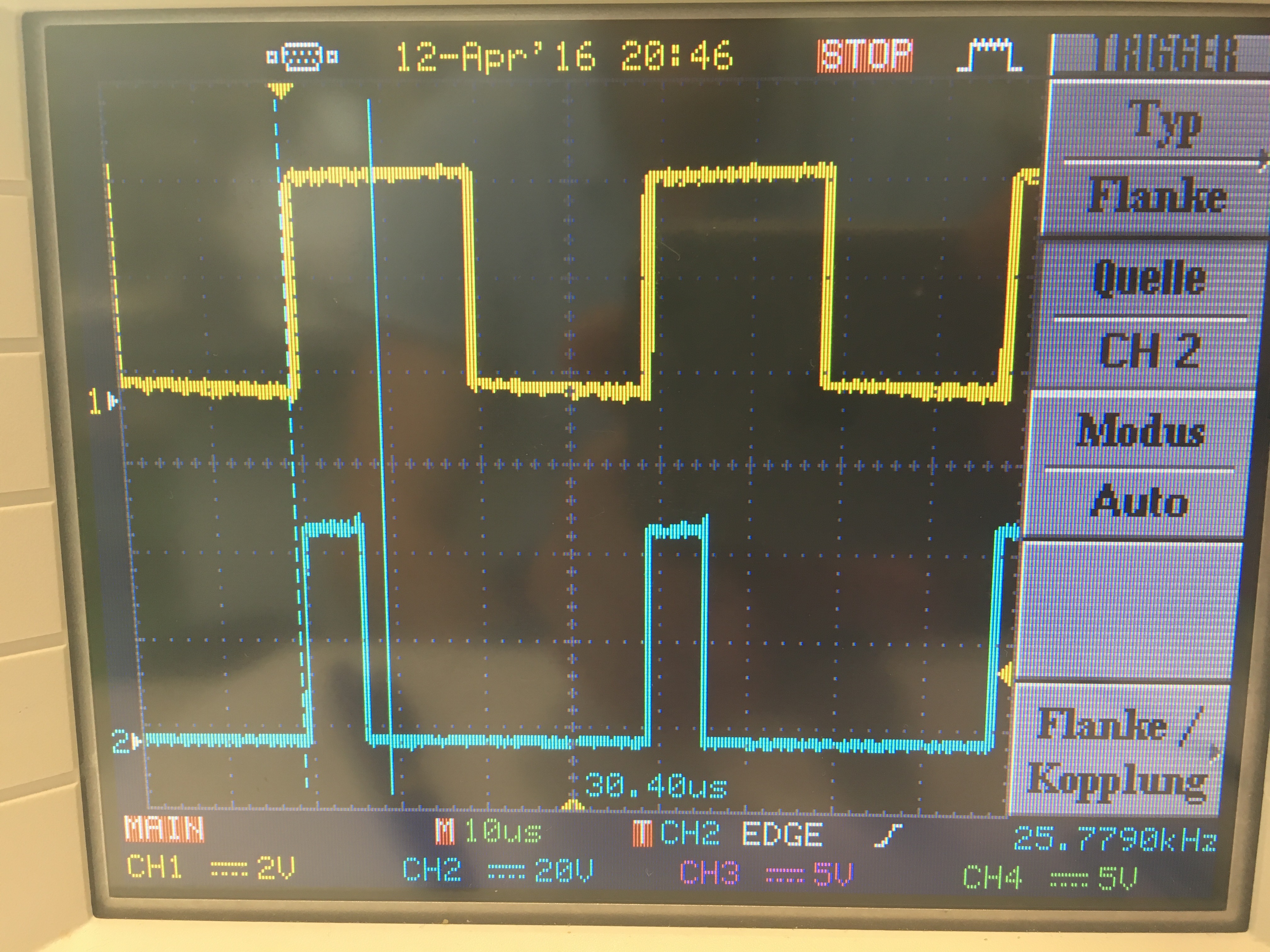


Figure 8 – Locked State of the PLL (Synced)

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