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Low-power 2D gate-all-around logics via epitaxial monolithic 3D integration

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Innovations in device architectures and materials promote transistor miniaturization for improved performance, energy efficiency and integration density. At foreseeable ångström nodes, a gate-all-around (GAA) field-effect transistor based on two-dimensional (2D) semiconductors would provide excellent electrostatic gate controllability to achieve ultimate power scaling and performance delivering. However, a major roadblock lies in the scalable integration of 2D GAA heterostructures with atomically smooth and conformal interfaces. Here we report a wafer-scale multi-layer-stacked single-crystalline 2D GAA configuration achieved with low-temperature monolithic three-dimensional integration, in which high-mobility 2D semiconductor Bi_2O_2Se was epitaxially integrated by high-κ layered native-oxide dielectric Bi_2SeO_5 with an atomically smooth interface, enabling a high electron mobility of 280 $cm^2 V^{-1} s^{-1}$ and a near-ideal subthreshold swing of 62 mV dec^{-1}. The scaled 2D GAA field-effect transistor with 30 nm gate length exhibits an ultralow operation voltage of 0.5 V, a high on-state current exceeding 1 mA μm^{-1}, an ultralow intrinsic delay of 1.9 ps and an energy-delay product of 1.84×10^{-27} Js μm^{-1}. This work demonstrates a wafer-scale 2D-material-based GAA system with valid performance and power merits, holding promising prospects for beyond-silicon monolithic three-dimensional circuits.

Silicon-based metal-oxide-semiconductor field-effect transistors (FETs) dominate the development of modern integrated circuits (ICs) from past decades to the upcoming ångström era, but they are approaching their performance and energy-efficiency limits[1,2]. Although the latest silicon-based gate-all-around (GAA) nanosheet FETs with four-sided gate-drive structures are anticipated to further extend the downscaling of transistors, the semiconductor industry is still struggling to overcome the ground-rule scaling limitations that the transistor supply voltage (V_{DD}) and gate length would not decrease to less than 0.6 V and 12 nm, respectively[3–6]. The challenges are rooted in the material itself, particularly in the increased scattering of the silicon nanosheet channel from the covalent dangling-bond interface as feature sizes shrink below 5 nm (refs. 7,8). High-mobility two-dimensional (2D) semiconductors provide a promising solution owing to their dangling-bond-free nature, better gate controllability and monolithic three-dimensional (M3D) integration prospects[9–14]. Given that the future metal-oxide-semiconductor FETs are less likely to reverse to a planar structure, 2D-based transistors necessarily adapt

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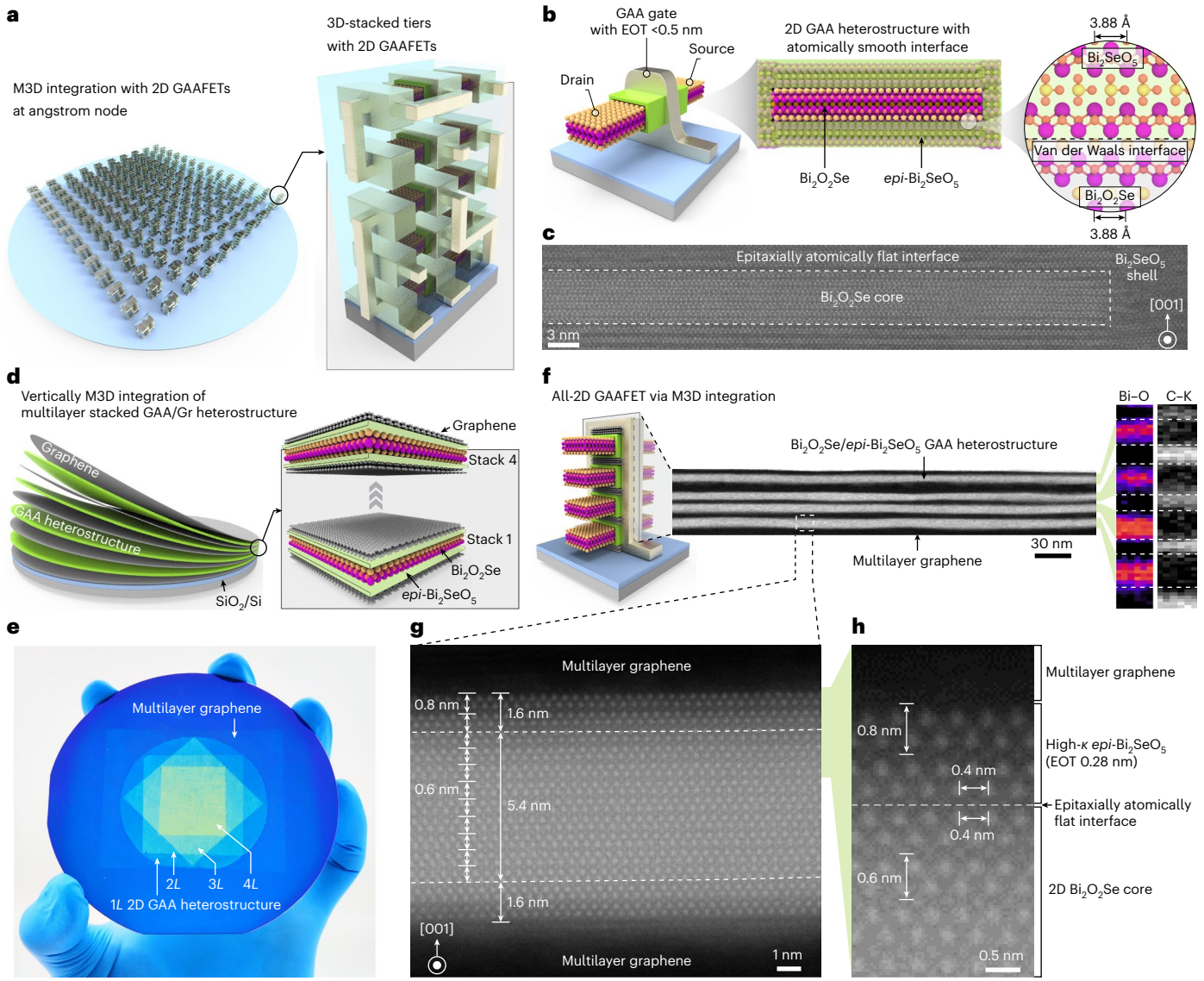

Fig. 1 | Epitaxial M3D integration of 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructures. **a**, Left: a schematic illustration for future M3D integration based on 2D GAAFET at the ångström technology node. Right: vertical 3D-stacked tiers with 2D GAA components. **b**, Schematics of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs with conformal native high-κ dielectric Bi_2SeO_5 at sub-0.5 nm EOT. Two-dimensional Bi_2O_2Se shares the Bi–O layer with Bi_2SeO_5 to ensure an atomically flat interface. **c**, A high-resolution cross-sectional STEM image of the side edge of a 2D Bi_2O_2Se/Bi_2SeO_5 heterostructure, in which Bi_2SeO_5 is entirely wrapped around a Bi_2O_2Se nanosheet to form a core–shell GAA structure with an atomically flat interface. **d**, Schematic of a vertically stacked multi-layer Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure ready for M3D integration, in which the wafer-scale Bi_2O_2Se/Bi_2SeO_5 and multi-layer graphene were integrated via layer-by-layer assembly to prepare the all-2D GAA architecture. **e**, A photograph of the M3D integrated 2D GAA system depicted in **d**, in which the 2-inch Bi_2O_2Se/Bi_2SeO_5 heterostructure and graphene electrode was subsequently integrated onto 4-inch Si/SiO_2 substrate. Note that the 2D GAA heterostructure was clipped to clearly show the multi-layer configuration. *L*, layer. **f**, Left: schematic and cross-sectional STEM image of Bi_2O_2Se/Bi_2SeO_5 2D GAAFET with the M3D integrated all-2D structure demonstrated in **e**, showing the highly ordered van der Waals heterostructure with an ultraclean graphene-Bi_2SeO_5 interface. Right: the EELS mapping of a typical section of the four-layer GAA heterostructure. The characteristic peak of the Bi element and the C element is highlighted in red and white, respectively. **g**,**h**, A high-resolution cross-sectional STEM image of typically zoomed area in 2D GAA heterostructure (**g**) and interfacial details (**h**) shown in **f**, showing 5.4-nm-thick 2D Bi_2O_2Se integrated with 0.28-nm-EOT high-κ Bi_2SeO_5 with an atomically flat interface. The lattice spacing of both Bi_2O_2Se and Bi_2SeO_5 is also measured.

to state-of-the-art GAA architectures to optimize their performance and power benefit[15]. Such wrapped-gate configurations provide excellent electrostatic control, enabling extra freedom for aggressive size shrinking and performance improvement. In particular, the lateral 2D GAA nanosheet configuration shows flexibility for horizontal stacking, which is compatible with future M3D platforms (Fig. 1a).

For low-power and high-performance 2D gate-all-around field-effect transistor (GAAFET) devices, the gate dielectric and its interface with the 2D channel material in GAA heterostructure are crucial[16]. Such multigate structures require an atomically thin and conformal gate dielectric with low trap density and high electrostatic efficiency to make use of their expected benefits. However, the direct deposition of high-κ dielectrics (where κ is dielectric constant) onto 2D semiconductors leads to inevitable interface defects. In addition, it has been shown to be challenging to form conformally wrapped configurations with sub-0.5 nm equivalent oxide thickness (EOT) in van der Waals dielectrics and buffer-layer-containing hybridized dielectrics[17–20]. Therefore, despite the merit of atomically thin channel bodies and optimal gate numbers, no experimental results demonstrate that the energy efficiency and performance of 2D GAAFETs can quantitatively

surpass those of state-of-the-art silicon counterparts under the same operating voltage. The wafer-scale integration of 2D GAA structures with atomically smooth and conformal interfaces is highly desirable but has not yet been achieved[21].

Here, we demonstrate a 2D GAA heterostructure based on high-mobility 2D semiconductor Bi_2O_2Se and its high-κ ($\kappa = 21$) layered native-oxide dielectric Bi_2SeO_5 via the low-temperature M3D integration strategy. In this conformal 2D Bi_2O_2Se/Bi_2SeO_5 GAA architecture, single-crystalline high-κ dielectric Bi_2SeO_5 is epitaxially wrapped around a Bi_2O_2Se nanosheet, forming an atomically smooth lattice-matched van der Waals interface (Fig. 1b). Upon such epitaxial M3D integration, a wafer-scale multi-layer 2D GAA Bi_2O_2Se/Bi_2SeO_5 system with sub-0.3 nm EOT was stacked via layer-by-layer integration. Two-dimensional GAAFETs based on such 2D Bi_2O_2Se/Bi_2SeO_5 GAA epitaxial heterostructures were thus fabricated, showing ultralow interface trap density (~2×10^{11} cm^{-2} eV^{-1}), high electron mobility (μ) (>280 cm^2 V^{-1} s^{-1}), nearly ideal subthreshold swings (SS) (<62 mV dec^{-1}), high on–off ratio (I_{on}/I_{off}) (>10^8) and excellent device reliability. The as-fabricated short-channel 2D GAAFET with air gaps exhibits a low operation voltage of 0.5 V, a high on-state current of >1 mA μm^{-1}, a low intrinsic delay and an energy-delay product (EDP) of 1.9 ps and 1.84×10^{-27} Js μm^{-1}, respectively. In addition, multiple low-power 2D GAAFET-based logic units operate their logic functions at low supply voltages below 1 V. Our work demonstrates the epitaxial M3D integration of a 2D GAA system with higher performance and energy efficiency beyond the limits of its silicon counterparts, satisfying the ångström-node electrical specifications and device architecture requirements projected by the latest International Roadmap for Devices and Systems (IRDS) roadmap.

Fully wrapped 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructures were prepared by epitaxially integrating high-κ native-oxide Bi_2SeO_5 on the Bi_2O_2Se surface via an in situ ultraviolet (UV)-assisted intercalative oxidation[22,23] (Supplementary Fig. 1 and details in Methods). The layered Bi_2SeO_5 epilayer uniformly oxidized from the underlaying 2D semiconductor Bi_2O_2Se, thus forming a fully wrapped 2D GAA heterostructure, which is verified by a segmented 2D Bi_2O_2Se/Bi_2SeO_5 core–shell heterostructure created by selectively etching away oxide shells (Extended Data Fig. 1a). The cross-sectional high-resolution scanning transmission electron microscopy (STEM) of the as-synthesized 2D GAA heterostructure indicated that the Bi_2O_2Se core was fully wrapped by the layered single-crystalline *epi*-Bi_2SeO_5 shell with a lattice-matched, atomically smooth and conformal interface (Fig. 1c). The lattice strain was shown to exist only at the side edge of the 2D Bi_2O_2Se core and was relaxed within a few atoms distance (Extended Data Fig. 1b–d). Interestingly, the fully wrapped 2D Bi_2O_2Se channel can be thinned down to a 1.2-nm-thick bilayer nanosheet (1 unit cell thick) using the controllable oxidation strategy (Supplementary Fig. 2).

Density functional theory (DFT) calculations were further performed on interface energy ($E_{interface}$), a metric of interface quality (Extended Data Fig. 2). The 2D Bi_2O_2Se/Bi_2SeO_5 interface features an $E_{interface}$ several orders of magnitude lower than those of other commonly used channel–dielectric interfaces (for example, Si/*ald*-HfO_2, MoS_2/*ald*-HfO_2 and so on). These calculations suggest that the epitaxial formation of a Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure with a high-quality interface is thermodynamically favourable and experimentally feasible, which lays the foundation for scalable M3D integration and transistor fabrication.

We exploit layer-by-layer M3D integration to prepare wafer-scale multi-layer-stacked all-2D GAA configurations. As shown in Fig. 1d,e, 2-inch-sized 2D Bi_2O_2Se/*epi*-Bi_2SeO_5 GAA heterostructures and multi-layer graphene were alternately stacked. These four-layer-stacked all-2D GAA configurations (Fig. 1f) show the potential of fabricating the multichannel 2D GAAFETs (for details, see Methods and Supplementary Figs. 3–5). The typical electrical properties of one typical three-channel-stacked GAAFET are shown in Extended Data Fig. 3, which will be discussed in the electronic characteristics part. The cross-sectional STEM image and corresponding electron energy loss spectroscopy (EELS) maps further reveal that the as-prepared all-2D GAA structures have highly parallel layered configurations with clean interfaces. Notably, the ultrathin Bi_2SeO_5 epilayer with a thickness of ~1.6 nm (EOT ~0.28 nm) remains intact during the wafer-scale integration of the 2D Bi_2O_2Se/Bi_2SeO_5 heterostructures (Fig. 1f). As shown in Fig. 1h, the 2D Bi_2O_2Se nanosheet and the fully wrapped Bi_2SeO_5 epilayers maintain an atomically smooth and lattice-matched interface with an identical in-plane lattice constant of 0.4 nm and interlayer spacings of ~0.6 nm and ~0.8 nm, respectively. As-measured structural parameters are consistent with the theoretical lattice constants of the layered Bi_2O_2Se and Bi_2SeO_5, demonstrating that the wafer-scale M3D integration did not introduce observable defects or external residual stresses.

In addition to a high-quality semiconductor–dielectric interface, the gate–dielectric contact and source/drain–semiconductor contact were carefully designed. In 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET, an Au gate electrode was applied to form a high-κ-metal-gate with a high-quality contact interface (Supplementary Fig. 6). Subsequently, the epitaxial Bi_2SeO_5 dielectric in the source/drain region was etched away in high vacuum to expose the fresh 2D Bi_2O_2Se channel. The source/drain electrodes were thus deposited in situ to obtain a low contact resistance (R_c) of 140 Ω μm at a carrier density (N_s) of 2×10^{13} cm^{-2} (Extended Data Fig. 4).

We then fabricated and evaluated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs with 0.45 nm EOT (Fig. 2a,b). Figure 2c,d shows the structural details of the dielectric layer determined after electrical tests, in which the ~2.4-nm-thick (EOT 0.45 nm) Bi_2SeO_5 conformally integrated to the 2D Bi_2O_2Se channel with an atomically smooth interface. The output and transfer curves of the 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET (Fig. 2e,f) show enhancement-mode *n*-type characteristics with a positive threshold voltage (V_{th}) of 40 mV and an on–off ratio >10^6 across an ultranarrow supply voltage range of 0.45 V. Note that the current density was normalized by the per-channel footprint. Remarkably, the enhancement-mode 2D GAAFETs exhibit an ideal SS of ~62 mV dec^{-1} in both reverse and forward sweeps, approaching the thermionic limits (60 mV dec^{-1}). The ultralow SS is attributed primarily to the intrinsically low interface trap density (D_{it}) in the dangling-bond-free atomically smooth Bi_2O_2Se/Bi_2SeO_5 interface[24,25], which was extracted down to 2×10^{11} cm^{-2} eV^{-1} (Supplementary Fig. 7).

For the reliability evaluation, within the repeated dual-direction transfer sweep of 200 cycles, the as-fabricated 2D GAAFET maintained a high on–off ratio of 10^6, a low SS down to 62 mV dec^{-1} and tiny hysteresis (~15 mV) (Fig. 2f,g). The sub-0.5-nm-EOT GAAFET showed a low off-state leakage density below 2×10^{-3} A cm^{-2}, which satisfied the low-power IC standard (Supplementary Fig. 8). Furthermore, the shift of V_{th} and SS was as low as 3 mV and 3 mV dec^{-1}, respectively (Fig. 2h,i). These electrical characteristics demonstrate the outstanding reliability of 2D GAAFET, the excellent stability of the single-crystalline ultrathin Bi_2SeO_5 dielectric and the robustness of the atomically smooth heterointerfaces. The long-term stability analysis of our GAAFET is shown in Supplementary Fig. 9, indicating a better reliability and stability compared with Bi_2O_2Se-based fin field-effect transistor (FinFET) and MoS_2 transistors (Supplementary Fig. 10).

To objectively examine the electronic properties and reproducibility of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs, 120 GAA transistors were fabricated in different batches. All the GAA transistors had a channel length of ~3.0 μm and an ultralow EOT of ~0.75 nm (Extended Data Fig. 5). The transfer curves at a source–drain voltage (V_{DS}) of 0.5 V for those GAA transistors are summarized in Fig. 2j, showing the excellent reproducibility and uniform electrical properties (Extended Data Fig. 6). Further statistical analysis of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs showed a minimum SS value of 61 mV dec^{-1} and average I_{on}/I_{off}, field-effect mobility (μ), threshold voltage and on-state current density of 10^8, 243 cm^2 V^{-1} s^{-1},

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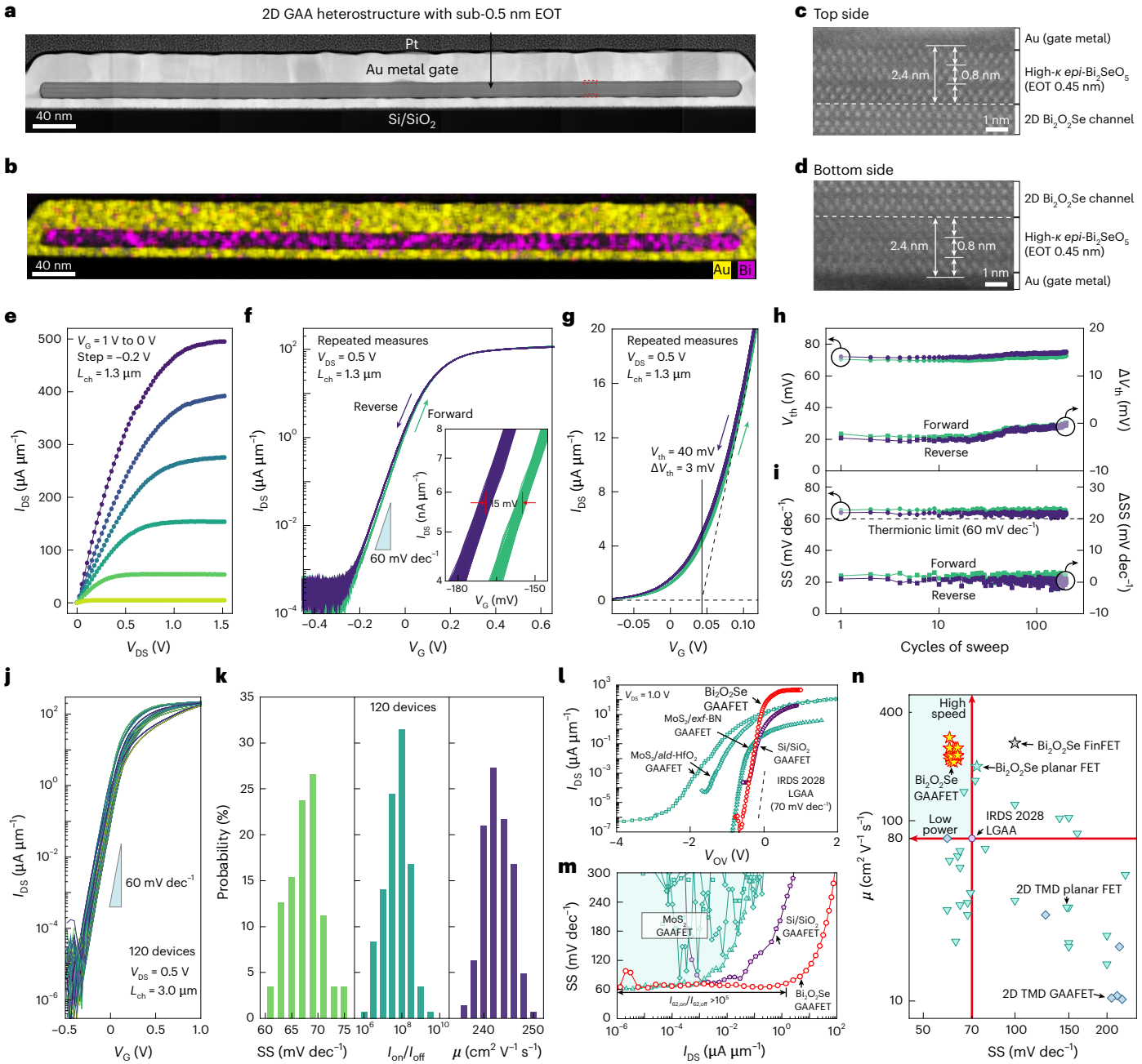

Fig. 2 | Electronic characteristics and comprehensive comparisons of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs. a, A cross-sectional STEM image of a typical Bi_2O_2Se/Bi_2SeO_5 GAAFET with an EOT of 0.48 nm. Note that the overall TEM image was assembled by seven single-shot segments to obtain high resolution. **b**, The EDX element mapping of the 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure shown in **a**, in which the GAA structure can be well defined. **c**,**d**, High-resolution cross-sectional STEM images of the 2D GAAFET shown in **a**, in which the interfacial details for both the top side (**c**) and the bottom side (**d**) can be recognized with the thickness of 2.4 nm (EOT 0.45 nm). **e**, Typical output characteristic curves of the GAAFET shown in **a**. The current density was normalized by the per-channel footprint. **f**,**g**, The repeated measurement plotted on log (**f**) and linear (**g**) scale of the GAAFET shown in **a** with 200 cycles of dual-direction sweep, in which the purple curves denote the reverse sweep and the green curves denote the forward sweep. Inset: the hysteresis detail of the 2D GAAFET for 200 cycles of dual-direction sweep. **h**,**i**, The absolute values (left axis) and the relative fluctuation (right axis) of the threshold voltages (V_{th}) (**h**) and SS (**i**) in 200 cycles of dual-direction sweep, in which the purple dots denote the reverse sweep and the green dots denote the forward sweep. The thermionic limit is indicated by the dashed line. **j**, The transfer characteristic curves of 120 typical Bi_2O_2Se/Bi_2SeO_5 GAAFETs at V_{DS} of 0.5 V and channel lengths of about 3 μm, indicating the near-ideal SS and high on–off ratio up to 10^9. **k**, The statistical histograms of SS, on–off ratio and field-effect mobility (μ) of 120 GAAFETs plotted in **j**. **l**,**m**, Typical transfer characteristics (**l**) and corresponding extracted SS (**m**) of one typical as-fabricated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET and 3D Si/SiO_2 GAAFET[26], 2D MoS_2 GAAFET integrated with *ald*-HfO_2 and *exf*-BN[17–19], where the red dots denote the as-prepared Bi_2O_2Se/Bi_2SeO_5 GAAFET and the purple/green dots denote other GAAFETs. **n**, Benchmarking of mobility versus SS of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET, 2D planar FET and 2D FinFET. The GAA targets projected by IRDS are also plotted.

0.05 V and 115 μA μm^{-1}, respectively (details in Supplementary 11). In addition, a reasonable comparison between 2D GAAFET and single-gate FET fabricated on an individual 2D Bi_2O_2Se/Bi_2SeO_5 heterostructure was performed with an identical device size and fabrication process (Extended Data Fig. 7 and Supplementary Fig. 12). The 2D GAAFET exhibited a ~2.5 times higher on-state current (with the same V_{DS}) and a ~1.4 times lower V_{DD} (upon the same on–off ratio) than that of single-gate transistors, clearly indicating the merit of electrostatic

efficiency of 2D GAA architecture[15]. Therefore, 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET features high gate-control efficiency and ultrahigh mobilities with producibility, holding promise for further logic applications. Note that the multichannel stacked 2D Bi_2O_2Se GAAFET exhibited higher performance (>600 μA μm^{-1}) and comparable SS (65 mV dec^{-1}), on–off ratio (10^7) and reliability compared with the single-channel ones (Extended Data Fig. 3).

The major concern regarding low-power logics lies in enhancing gate electrostatic controllability, which requires nearly ideal SS across more than four orders of current magnitude and a large current on–off ratio. Figure 2l,m illustrates a reasonable comparison of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs, the 3D Si-based GAAFETs (Samsung)[26] and 2D MoS_2 GAAFETs (Taiwan Semiconductor Manufacturing Company (TSMC) and academics)[17–19] with similar gate length. Among them, 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs reveal steeper SS (~62 mV dec^{-1}) over five decades (>10^5) current window, much wider than other reported GAAFET counterparts (<10^3) (Fig. 2m). Moreover, the atomically smooth interface of the 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure also enables higher field-effect mobility (μ) compared with 2D Bi_2O_2Se FinFETs, transition-metal dichalcogenide (TMD) FETs and IRDS target for GAAFETs in 2028 (Fig. 2n and details in Supplementary Information). The optimal SS and high mobility of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs make it a promising candidate for low-power and high-performance device applications. Benchmarking against silicon and 2D counterparts on the metrics of EOT, V_{DD}, on–off ratio and static consumption (P_{static}) further validates the low-power merits of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs (Supplementary Fig. 13).

To further optimize the performance and power efficiency of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET towards the electrical specifications at the ångström technology node, short-channel transistors were fabricated following the principle of design technology co-optimization. As illustrated in Fig. 3a, a short-channel Bi_2O_2Se/Bi_2SeO_5 GAAFET without source/drain–gate overlap was designed, in which an air-gap side wall was introduced to minimize the parasitic capacitance. Based on such architecture, a 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET array was fabricated with channel lengths (L_{ch}) and gate lengths (L_G) of 50–100 nm and 30–50 nm, respectively (Fig. 3b). A typical short-channel 2D GAAFET with overlap-free air gaps, channel length of 50 nm and gate length of 30 nm is illustrated in Fig. 3c–e. By analysing the structural details of the channel area in the as-fabricated short-channel 2D GAAFET, the 2D Bi_2O_2Se nanosheet thickness was ~4.2 nm and the EOT of the surrounding single-crystalline Bi_2SeO_5 dielectric was measured as ~0.28 nm. Both components satisfy the requirements of dimensional scaling for GAA transistors at the ångström technology node.

The output curves of the 30-nm-length 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET is plotted in Fig. 3f. In this enhancement-mode GAAFET, a typical ohmic-contact feature is clearly shown with a relatively low total resistance of 330 Ω μm, lower than most of the reported 2D transistors (Supplementary Fig. 14). In particular, an ultralow 0.5 V drain voltage drives Bi_2O_2Se/Bi_2SeO_5 GAAFET to gain high on-state current (I_{on}) surpassing 1 mA μm^{-1}, and only 0.8 V drain voltage is required to saturate the output current with 1.2 mA μm^{-1}. The corresponding transfer characteristics show ideal switching behaviour (I_{on}/I_{off} > 10^6), maximum transconductance ($G_{m,max}$ > 1.6 mS μm^{-1}) and a small hysteresis (~15 mV) (Fig. 3g, Extended Data Fig. 8 and Supplementary Fig. 15). Moreover, the $G_{m,max}$–channel length relationship exhibits a typical inverse proportion relationship (Extended Data Fig. 9). The V_{DD} of 2D GAAFET is scaled down to 0.5 V, enabling the control of the channel from 100 nA μm^{-1} (off state) to over 800 μA μm^{-1} (on state), which exceeds the scaling limitation of silicon transistors, exactly satisfying the requirement of the 2D-based GAAFET at the ångström node (Supplementary Fig. 16). More performance and statistical analysis of 30-nm-length 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET can be found in Supplementary Fig. 17 and Extended Data Fig. 10. Our short-channel 2D GAAFET showed that the maximum on-state current (I_{on}) and transconductance ($G_{m,max}$) at V_{DS} of 0.5 V were 1.28 mA μm^{-1} and 2.18 mS μm^{-1}, respectively, with an average V_t and on–off ratio of 0.4 V and 3 × 10^6, respectively. For further improvement of yield and device-to-device uniformity, the high-precision lithography equipment, self-alignment technology and uniform transfer strategy are highly desired.

For further evaluation of the performance advantages of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs, we performed a comprehensive analysis guided by the performance, power and area (PPA) principle. As shown in Fig. 3h, we first evaluate the absolute performance by directly comparing the typical transfer curve at V_{DS} = 0.5 V with state-of-the-art silicon complementary FET (CFET) (Intel)[4], 26-nm-gate-length silicon GAAFET (Interuniversity Microelectronics Centre (IMEC))[5] and 40-nm-gate-length TMD GAAFET (TSMC)[17]. Note that all transfer curves were normalized by an off-state current of 100 nA μm^{-1}, which is consistent with the silicon-based counterparts reported by Intel and IMEC. With similar channel lengths, the as-fabricated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET shows an on-state current 100 times higher than that of 2D TMD GAAFET and 1.4 times higher than the silicon-based GAAFET under a much lower driven voltage of 0.5 V (versus 0.65 V for Si CFET, 0.7 V for Si GAAFET and 1.0 V for TMD GAAFET). For the evaluation of performance and area, Fig. 3i benchmarks the on-state current versus gate length of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs, 2D Bi_2O_2Se FinFETs, Ge GAAFET, Si GAAFET and other 2D-based FETs. For a fair comparison, all on-state currents are extracted at saturation gate voltage, and the supply voltage is set at 0.6 V (standard projected by IRDS for 2D GAAFET[27]). Quantitatively, 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs yield a high on-state current of 1,082 μA μm^{-1}, surpassing all GAA counterparts and IRDS targets and rivalling the state-of-the-art 2D-based transistors. Note that some counterparts show a higher on-state current density at a larger V_{DS} (Supplementary Fig. 18).

Guided by the PPA principle and IRDS roadmap, two key parameters of intrinsic delays and EDP were used as the figure of merits for benchmarking performance and energy efficiency, respectively. The intrinsic delay (τ) and EDP can be described as

$$\tau = C_{total} V_{DD}/I_{on}$$

$$EDP = C_{total}^2 V_{DD}^3/I_{on},$$

where C_{total} represents the total capacitance, and V_{DD} and I_{on} represent the supply voltage and corresponding on-state current, respectively. Benefitting from the air-gap design, ultralow V_{DD} and relatively high I_{on}, 2D Bi_2O_2Se GAAFETs simultaneously exhibit the delay and EDP of 1.9 ps and 1.84 × 10^{-27} Js μm^{-1}, respectively (for calculation details, see Methods). From the perspective of the PPA principle, 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs perform better high-speed and low-power merits than the commercial FinFET (Intel)[28–30], Si GAAFET (IBM and IMEC)[5,6] and 2D FETs reported by academia[31], satisfying the HD target for the 2031 ångström node. The yield of the device versus different channel lengths with well-defined criteria is shown in Supplementary Fig. 19, showing a high yield for the long-channel-length device and a relatively lower yield for channel lengths smaller than 0.1 μm.

Multiple logic units including NOT (inverter), the NOR gate and the NAND gate were further fabricated by using 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs. As shown in Fig. 4a–c, a GAA-based n-type inverter exhibits a sharp switching behaviour at an operating voltage of 1 V with a voltage gain as high as 59 V V^{-1}. The output current (I_{out}) of this as-fabricated inverter is only about 5 nA, which guarantees a low dynamic power consumption (P_{out}) of 5 nW (Fig. 4d,e). Furthermore, benchmarked against silicon and other 2D counterparts for inverter voltage gain versus V_{DD}, the 2D Bi_2O_2Se GAAFET-based inverter clearly shows optimal gate gains in the low voltage range from 0.3 V to 1.0 V, which is benefitted by high-quality interfaces and GAA architecture for higher electrostatic efficiency (Fig. 4f and details in Methods and Supplementary Fig. 20). More complicated logic units such as the NOR gate and the NAND

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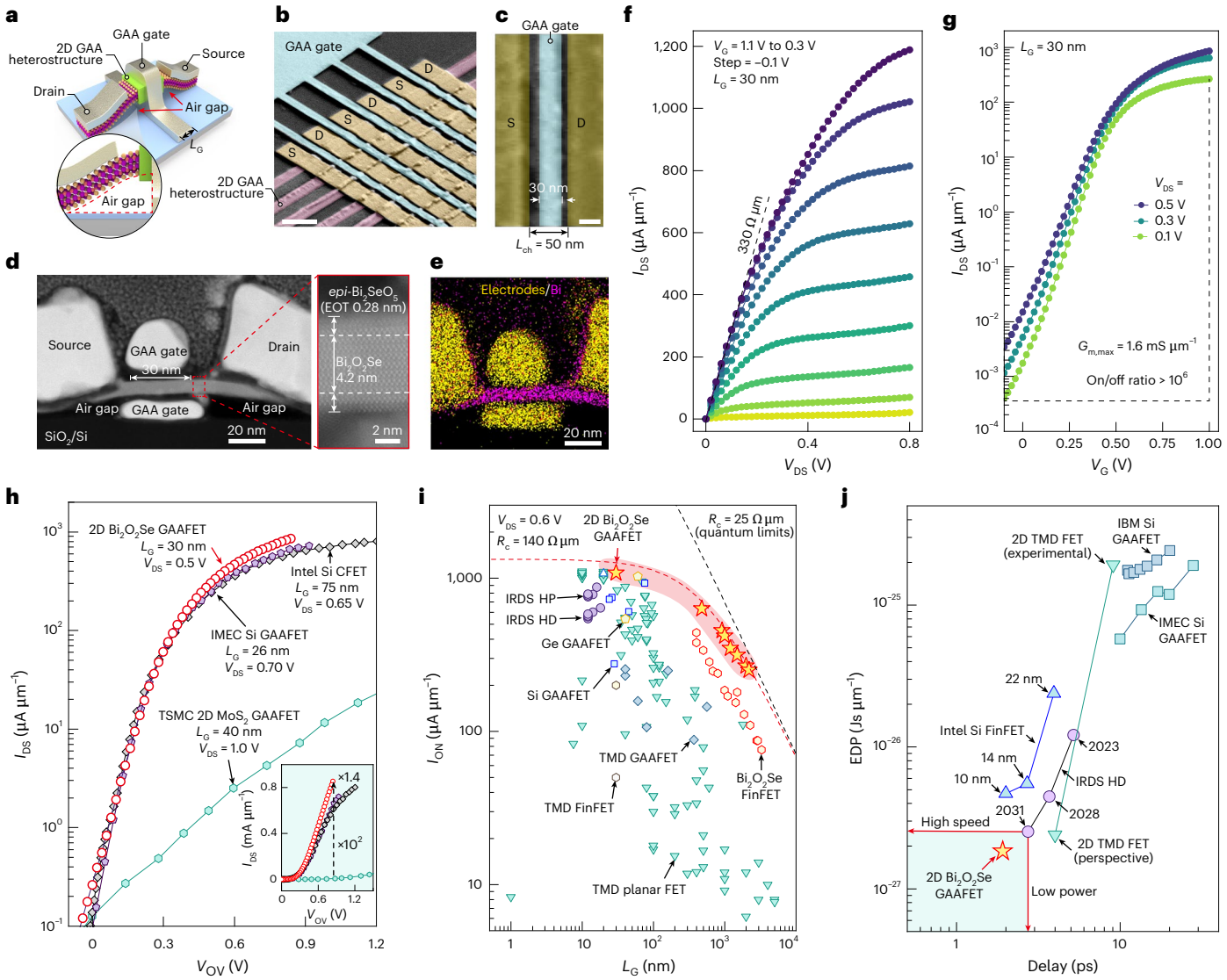

Fig. 3 | Structural details, electronic characteristics and comprehensive benchmarking of short-channel 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs with air-gap structure. a, A structural schematic of short-channel 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs with air-gap structure. **b**, A tilted-view SEM image of short-channel 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET arrays, in which the channel lengths (L_{ch}) vary from 50 nm to 100 nm with gate lengths (L_G) of 30 nm. Scale bar, 100 nm. **c**, A top-view SEM image of a 2D Bi_2O_2Se-based GAAFET with L_{ch} and L_G of 50 nm and 30 nm, respectively. Scale bar, 30 nm. **d**, Left: a high-resolution cross-sectional STEM image of the 2D Bi_2O_2Se/Bi_2SeO_5 shown in **c**, indicating a clear air-gap structure. Right: interfacial details for the 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET, showing the sub-0.3 nm EOT with an atomically flat interface. **e**, The energy EDX element mapping of the 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure shown in **a**. **f**,**g**, Typical output (**f**) and transfer (**g**) characteristic curves of the 30-nm-gate 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET shown in **d**, which operates at 0.5 V with an on-state current over 1 mA μm^{-1} and on–off ratio over 10^6. The current density was normalized by the per-channel footprint. **h**, A transfer characteristics comparison of the as-prepared 30-nm-gate 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET operated at 0.5 V (red dots), 26-nm-gate Si GAAFET operated at 0.7 V (IMEC, purple dots)[5], 75-nm-gate Si CFET operated at 0.65 V (Intel, grey dots)[4] and 40-nm-gate 2D MoS_2 GAAFET operated at 1.0 V (TSMC, blue dots)[17]. Note that all curves are normalized with the same rule. Inset: the linear scale transfer characteristics comparison. **i**, Benchmarking of the on-state current (I_{on}) at V_{DS} = 0.6 V versus L_G of 2D Bi_2O_2Se GAAFETs with Si GAAFET, TMD GAAFET, TMD FinFET, Ge n-type GAAFET, TMD planar FET and Bi_2O_2Se FinFET. The high-performance (HP) and high-density (HD) targets projected by IRDS are also plotted. **j**, Benchmarking of the intrinsic delay versus EDP of 2D Bi_2O_2Se GAAFETs versus commercial Si FinFET (Intel)[28–30], Si GAAFET (IMEC and IBM)[5,6] and 2D planar FETs[31]. The corresponding targets projected by IRDS are also plotted.

gate were also fabricated using 2D Bi_2O_2Se GAAFETs (Fig. 4g–j). The NOR gate and NAND gate operate at a low V_{DD} of 1.0 V to perform their logical functions. Our results demonstrate the scalability for future 2D-GAA-based low-power circuits.

Notwithstanding the advances in transistor properties and logic units, challenges still remain for 2D Bi_2O_2Se GAAFETs from current lab batches towards mass product. For future IC applications, efforts should concentrate on the large-scale synthesis of 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure, the reliable transfer method, the mass-product-compatible conformal electrodes deposition and p-type modulation. Based on these issues, we highlight the innovations in scalable CVD equipment, native-oxide integration, damage-free wafer-scale stacking strategy and the atomical layer deposition for electrode metallization. Enlightened by the recent research, the p-type channels via contact or work-function regulation are also being investigated.

In summary, we report a multi-layer-stacked GAA configuration based on 2D materials via epitaxial M3D integration, overcoming the power-scaling limitations of silicon-based nanotechnologies. With the atomically smooth interface and ultrascaled EOT, the as-fabricated 2D

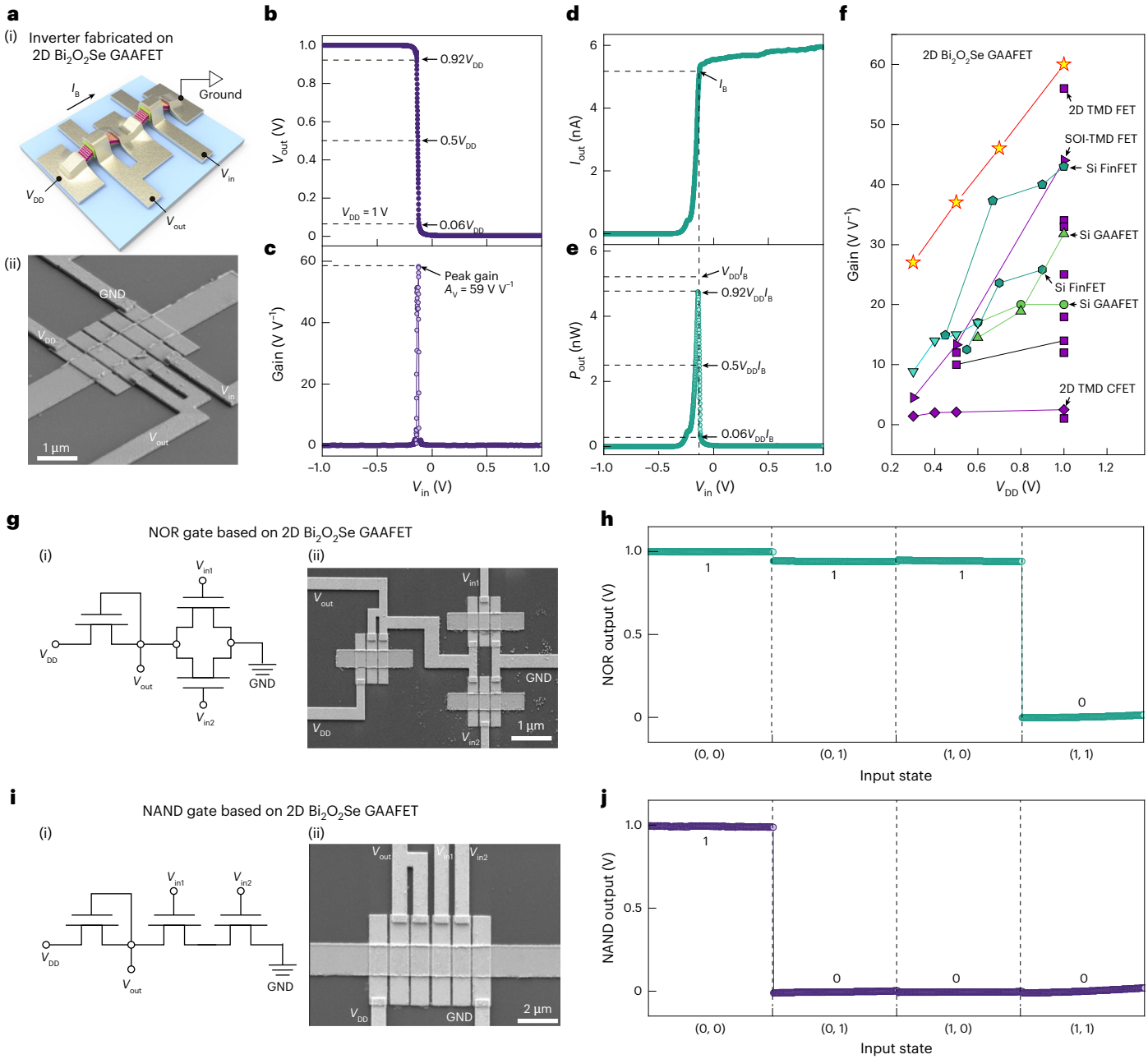

Fig. 4 | Low-power 2D Bi_2O_2Se/Bi_2SeO_5 GAA logics. a, Structural schematic (i) and tilted SEM image (ii) of an n-type MOS inverter fabricated on two 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs. **b**,**c**, The transfer characteristics (**b**) and corresponding voltage gains (**c**) at 1 V supply voltage of the inverter shown in **a**. **d**,**e**, The operating current (**d**) and corresponding static power consumption (**e**) of the inverter demonstrated in **a**. **f**, Benchmarking of voltage gains versus V_{DD} of inverters based on 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET, 2D TMD FET, Si FinFET and Si GAAFET. **g**, Circuit diagram (i) and SEM image (ii) of NAND gate based on 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET. **h**, Input–output logic functions of the NAND gate with an V_{DD} of 1 V. **i**, Circuit diagram (i) and SEM image (ii) of the NOR gate based on 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET. **j**, Input–output logic functions of the NAND gate with V_{DD} of 1 V. GND, ground; V_{in}, input voltage; V_{out}, output voltage; A_v, voltage gain.

Bi_2O_2Se/Bi_2SeO_5 GAAFETs exhibited valid gate efficiency, performance and robust reliability merits. By using such an excellent epitaxial strategy, the upcoming M3D integration of 2D complementary GAAFETs, 2D multibridge-channel FETs are expected in the foreseeable future. Nevertheless, this work demonstrates that 2D GAAFETs do exhibit comparable performance and energy efficiency to commercial silicon-based transistors, making them a promising candidate for post-silicon M3D integration at the ångström technology node.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41563-025-02117-w.

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Methods

Preparation of 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure

The 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure was prepared via controllable intercalative oxidation strategy. The oxidation process was performed in a UV–O_3 generator (Novascan 4′ UV/O_3) equipped with a low-pressure mercury lamp, which emits 185 nm vacuum UV and dissociates O_2 molecules into reactive oxygen atoms. A heating stage with a programmed timer was fixed on the oxidation chamber, which is crucial for the multistage oxidation process. By modulating the key parameters (reaction time, reaction temperature and oxygen concentration) and the design of the reaction process, GAA heterostructure with variable native-oxide thickness can be prepared on the basis of membrane samples, free-standing nanosheets or vertical fins. The detailed oxidation process is explained in Supplementary Fig. 1, and the transfer-related process is discussed in 'Low-temperature M3D technology for wafer-scale multi-layer-stacked Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure'.

GAA structure based on membrane samples. Stage I, exfoliation. The membrane samples were first exfoliated from growth substrates via interfacial modulation to expose the fresh faces.

Stage II, preheating. Because the oxidation process requires precise duration control, the mercury lamp needs to be preheated to stabilize at the desired temperature, ensuring the repeatable oxidation condition. The time for preheating should be no less than 60 s after the stabilization of temperature.

Stage III, medium-temperature oxidation. The intercalation reaction initiated at the edge of the 2D Bi_2O_2Se, where the $[Bi_2O_2]_n^{2n+}$ frameworks remain intact while the Se^{2-} anions were oxidized into $[SeO_3]^{2-}$ (ref. 22). In this stage, the intercalation process was designed to deepen layer by layer. To prepare the heterostructures with different native-oxide thicknesses, the reaction duration in this stage can be adjusted.

Stage IV, cooling-down and transferring. The substrates should be removed from the chamber and cool down as soon as possible to avoid possible overreaction. The samples were transferred onto a flexible substrate (such as polydimethylsiloxane (PDMS)) for strain relaxation, and the transfer medium was removed to explore another face.

Stage V, preheating. See also stage II.

Stage VI, medium-temperature oxidation. The oxidation process was symmetrically performed on another face.

Stage VII, cooling-down, transferring and patterning. The samples were transferred to the target substrate after cooling down. A patterning process was performed for subsequent GAA nanosheet fabrication.

Stage VIII, long-time low-temperature oxidation. After the transfer and patterning process, an extra long-time low-temperature oxidation process was designed to remove the possible polymer residue and ensure the entire encapsulation without the influence of the native-oxide thickness.

Stage IX, preheating process. See also stage II.

Stage X, medium-temperature oxidation. The postoxidation was designed to repair the possible damage of Bi_2SeO_5 lattice during the transfer process. For the fabrication of pre-embedded metal electrodes, this process can act as an annealing process for an improved dielectric–metal interface.

GAA structure preparation based on freestanding or vertical fin samples. Stage I, long-time low-temperature oxidation. To prepare a GAA structure based on free-standing samples, side edges of 2D Bi_2O_2Se nanosheet need to be entirely wrapped by Bi_2SeO_5, so a preoxidation was designed to initiate at a relatively low temperature for a long time to form the intact core–shell structure without large layer-to-layer distinction.

Stage II, preheating process. Because the oxidation process requires precise duration control, the mercury lamp needs to be preheated to stabilize at the desired temperature, ensuring the repeatable oxidation condition. The time for preheating should be no less than 60 s after the stabilization of temperature.

Stage III, medium-temperature oxidation. After the initiation, the intercalation process was designed to be deepened layer by layer. Note that, for freestanding or vertical fin samples, the exterior layers exhibited a higher reaction rate because of the relatively slight lattice strain to overcome. Once the outer layers were completely oxidized, the lattice strain applied to inner layers became larger, causing the oxidation process to self-terminate. To prepare the heterostructures with different native-oxide thicknesses, the reaction duration in this stage can be adjusted.

Stage IV, preheating process. See also stage II.

Stage V, high-temperature instantaneous oxidation. After the termination of stage III, an extra high-temperature oxidation process was performed to optimize the Bi_2O_2Se/Bi_2SeO_5 interface. The possible lattice vacancies, defects and distortion were restored in this process, which is essential for the fabrication of low-power transistors.

Stage VI, cooling down. The substrates should be removed from the chamber and cool down as soon as possible to avoid possible overreaction.

Stage VII, transfer process. The as-prepared Bi_2O_2Se/Bi_2SeO_5 heterostructure can be either directly transferred to the target substrate for structural characterization or encapsulated by metal for further microfabrications.

Stage VIII, long-time low-temperature oxidation. After the transfer process, an extra long-time low-temperature oxidation process was designed to remove the possible polymer residue and ensure the entire encapsulation without the influence of the native-oxide thickness.

Stage IX, preheating process. See also stage II.

Stage X, medium-temperature oxidation. The postoxidation was designed to repair the possible damage of the Bi_2SeO_5 lattice during the transfer process. For the fabrication of pre-embedded metal electrodes, this process can act as an annealing process for an improved dielectric–metal interface.

Fabrication and measurement of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET

Based on the GAA heterostructure prepared by the multistage oxidation process, the GAAFET can thus be fabricated by the following approaches. The key to the successful fabrication of GAAFET was the introduction of the metal electrodes that wrap the dielectric entirely. Based on this issue, two approaches were carried out.

Vertical encapsulating approach. In this approach, the metal gate electrodes were directly deposited onto the free-standing or vertical fin Bi_2O_2Se/Bi_2SeO_5 GAA heterostructures to form a gate-wrapped GAA structure before being transferred to target substrate. The magnetron sputtering system equipped with the low-power radio frequency mode (QAM-4W-STS, ULVAC Technologies) was used to wrap the dielectric without damage. The substrate was set to rotate during the deposition, and a conformal Au layer with thickness of no less than 25 nm was prepared. Note that the background vacuum should be as low as possible and the carrier gas flow should be controlled at about 15 sccm to obtain flat Au layers with small grain size. The Au-wrapped GAA heterostructure was then transferred to Si/SiO_2 substrate with location marks. Thermal release tape (TRT) was used as transfer medium in this approach to increase the transfer efficiency. After the release procedure, the substrate was immersed in boiling acetone to remove the polymer residue, followed by an extra UV–O_3 oxidation process to repair the possible damage of the native oxide layer ('Preparation of 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure'). The patterned Pd gate electrodes were then prepared by standard electron beam lithography (EBL) upon the Au all-around gate, followed by electron beam evaporation. The Pd electrodes not only provide connection for the Au

gate but also act as protection mask for the following etching process. The source and drain windows were thus defined by EBL, and the aqueous etchant with a component ratio of I_2:KI:H_2O = 0.5:2:70 was used to etch away the Au layer. Note that the etch reaction lasts no more than 3 s and needs to be quenched quickly in hot water (90 °C) to remove the etchant residue. The source and drain electrodes were then deposited by low-temperature electronic beam evaporation right after the etch of Bi_2SeO_5 via mild Ar plasma or diluted HF solution. This approach was suitable for either short-channel devices or long-channel devices (Supplementary Fig. 5).

Pre-embedded electrode approach. In this approach, a pre-embedded metal electrode was prepared in Si/SiO_2 substrate, and the GAA heterostructures were then transferred onto it, following the wrapping of side wall and surface to form an all-around gate. The pre-embedded electrode arrays can be patterned by maskless laser lithography system (MLA150) with a photoresist film (AR-P5350, All-resist EN) or EBL process, and Ti/Au was deposited by electron beam evaporation. Note that the evaporation rate should be controlled at no more than 0.1 Å s^{-1} with a cold substrate plate to reduce the roughness of the electrodes. The GAA structures can thus be directly transferred onto the electrodes. After the postoxidation process to complete the fully wrapped encapsulation and repair the possible mechanical damage of the dielectric ('Preparation of 2D Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure'), an extra annealing programme at 170 °C in air was designed to optimize the contact of the dielectric and the metal electrodes. The all-around gate was thus prepared by the magnetron sputtering system equipped with the low-power radio frequency mode (QAM-4W-STS, ULVAC). With the standard EBL process, the source/drain windows were defined and the top layer of Bi_2SeO_5 was thus etched by Ar plasma, followed by the deposition of metal electrodes. This approach was particularly suitable for the membrane samples and short-channel devices (Supplementary Fig. 4).

Note that both approaches were compatible with the site-specification transfer technology, and the multi-layered GAA devices can thus be fabricated for further investigation.

Low-temperature M3D technology for wafer-scale multi-layer-stacked Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure

The transfer process is shown in Supplementary Fig. 3. First, a 50 nm Al_2O_3 film was deposited on Bi_2O_2Se film by electron beam evaporation. After that, 500 nm nickel film was deposited on Al_2O_3 by magnetron sputtering. Then, the TRT was laminated onto the Ni as a handle layer to peel off the Bi_2O_2Se film from the growth substrate. UV–O_3 cleaner was used to partially oxidate the Bi_2O_2Se to β-Bi_2SeO_5, followed by spin-coating polypropylene carbonate (PPC) polymer and laminating PDMS onto PPC. The composite film was heated at 130 °C to release the TRT tape, and the Ni and Al_2O_3 film was etched by 1 mol l^{-1} $FeCl_3$ aqueous solution and 1 mol l^{-1} NaOH aqueous solution, respectively. After that, the unoxidized surface of Bi_2O_2Se was exposed, which can be oxidated by UV–O_3 cleaner to form the structure of Bi_2SeO_5/Bi_2O_2Se/Bi_2SeO_5. Then, the as-fabricated film was laminated onto few-layer graphene/SiO_2/Si followed by releasing the PDMS at 180 °C and removing the PPC with acetone. Then, few-layer graphene was transferred on it to achieve the structure of graphene/Bi_2SeO_5/Bi_2O_2Se/Bi_2SeO_5/graphene. By stacking the graphene and Bi_2SeO_5/Bi_2O_2Se/Bi_2SeO_5 alternatively, the mutistack of graphene and Bi_2SeO_5/Bi_2O_2Se/Bi_2SeO_5 can be fabricated.

Characterizations of Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure

SEM characterization. The morphology of segmental Bi_2O_2Se/Bi_2SeO_5 heterostructures and GAAFETs was characterized by a Hitachi S4800 field emission electron microscope with a acceleration voltage of 1 kV, lower imaging mode. The tilted images were acquired by tilting the sample holder by 45°.

Cross-sectional STEM characterization. Focused ion beam (FIB) samples were fabricated by using a FEI Scios 2 Dual Beam SEM/FIB system. Cross-sectional transmission electron microscopy (TEM) samples were fabricated following the standard FIB fabrication process. To reveal both 2D Bi_2O_2Se/Bi_2SeO_5 heterostructure interface and metal gate/dielectric interface, GAAFET devices were used for structural characterization samples after electrical testing.

The atomic structure of 2D Bi_2O_2Se/Bi_2SeO_5 heterostructure interface and as-fabricated 2D GAAFET can be studied by cross-sectional STEM. All cross-sectional STEM results, corresponding energy-dispersive X-ray (EDX) element mapping and electron energy loss element mapping were obtained using an aberration-corrected scanning transmission electron microscope (FEI Titan Cubed Themis G2 300, operated at 300 kV acceleration voltage).

Electrical measurement of Bi_2O_2Se/Bi_2SeO_5 GAAFETs

The electrical characteristics of the as-fabricated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs were determined on a semiconductor analyser (keysight B1500) equipped with a micromanipulator probe (LakeShore CRX-VF) under a vacuum of 10^{-4} mbar at room temperature. For the repeated dual-direction measurement, a sweep rate of 0.1 V s^{-1} and an interval of 1 s were set, and 50–200 sweep cycle times were carried out to investigate the reliability of as-fabricated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs.

DFT calculations

To calculate the surface energy of the as-prepared Bi_2O_2Se/Bi_2SeO_5 heterostructure, the atomical structure was established and optimized by the DFT method implemented in the Vienna Ab initio Simulation Package (VASP)[32,33]. The valence electron–ion core interaction was treated by the projector augmented wave method, and the Perdew–Burke–Ernzerhof functional with generalized gradient approximation was used to describe the exchange–correlation interaction. The DFT-D3 dispersion-correction method was adopted to describe the van der Waals interactions, and the plane-wave cut-off energy was set as 500 eV. Energy convergence criteria for electronic and ionic iterations were set to be 10^{-5} eV and 10^{-4} eV, respectively. The interface energy per area is calculated by

$$E_{\text{interface}} = \frac{E_{Bi_2O_2Se/Bi_2SeO_5} - (E_{Bi_2O_2Se} - E_{Bi_2SeO_5})/2}{A},$$

where $E_{Bi_2O_2Se/Bi_2SeO_5}$ is the energy of the Bi_2O_2Se/Bi_2SeO_5 heterostructure. $E_{Bi_2O_2Se}$ and $E_{Bi_2SeO_5}$ are the energy of Bi_2O_2Se and Bi_2SeO_5 in the same $[Bi_2O_2]_n^{2n+}$ framework of heterostructure, respectively. A represents the interface area between Bi_2O_2Se and Bi_2SeO_5 in the heterostructure.

The estimate of EOT

The EOT is defined as[16]

$$\text{EOT} = \frac{\varepsilon_r(SiO_2)t_{ox}}{\varepsilon_{ox}(Bi_2SeO_5)},$$

where $\varepsilon_r(SiO_2)$ represents the dielectric constant of SiO_2, and t_{ox} and ε_{ox} (Bi_2SeO_5) respectively represent the physical thickness and dielectric constant of the oxide used in the as-fabricated FET.

For the 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs in this work, the t_{ox} was the Bi_2SeO_5 thickness extracted from the high-resolution cross-section STEM images of the corresponding FET after electrical measurement. The dielectric constant of the Bi_2SeO_5 has been well investigated by our group[13,22], which was about 21. For the structures and devices shown in Figs. 1 and 3, the physical thickness of Bi_2SeO_5 was determined to be about 1.6 nm for two layers, and for the device shown in Fig. 2, the physical thickness was determined to be 2.4–4 nm for three to five layers. The EOTs were thus calculated 0.28 nm and 0.45–0.75 nm, respectively.

For the EOT target projected by IRDS, the roadmap pointed out that the capacitive equivalent thickness was 1.0 nm for Si-based FinFET in 2023 and no more than 0.9 nm for the forthcoming GAAFET[27]. The capacitive equivalent thickness (or inversion layer) consists of EOT and the physical extension of the inversion layer, which was approximately 0.4 nm (ref. 34). Therefore, the target EOT projected by IRDS was estimated to be 0.6 nm for Si-based FinFET and 0.5 nm for the forthcoming GAAFET technical node.

To avoid misestimates in EOT benchmarking, only the counterparts with available EOT values are included in Supplementary Fig. 13.

The extraction of V_{DD}

Because there is not a well-defined value of V_{DD} owing to variations in device parameters, we extract the minimum (I_{off}) and maximum (I_{on}) of I_{DS} from a typical subthreshold transfer curve and calculate the width of the supply–voltage window corresponding to the on–off ratio. For typical high-performance transistors in modern ICs, the I_{off} was recommended to be 100 nA μm^{-1}. This method was suggested by authoritative perspectives[15,35] and has been used in recent works based on 2D semiconductors[9,20]. The benchmarking of V_{DD} and the corresponding on–off ratio is shown in Supplementary Fig. 13. Our GAAFETs exhibit ultralow V_{DD} below 0.5 V while supplying a high on–off ratio exceeding 10^7.

The calculation of trap density (D_{it})

D_{it} is defined by

$$SS = \ln(10)\frac{k_B T}{q}\left(1 + \frac{qD_{it}}{C_G}\right),$$

where k_B is the Boltzmann constant, q is the elemental charge, T is the absolute temperature and C_G is the gate capacitance, which can be calculated by EOT ('The estimate of EOT').

The calculation of static power consumption

The static power consumption was a part of total power consumption, which was defined as[15]

$$P_{static} = I_{off} V_{DD},$$

where I_{off} is the off-state current and V_{DD} is defined as in 'The extraction of V_{DD}'.

To exemplify the calculation of power consumption, the detailed calculation process of the GAAFET in Supplementary Fig. 13 was as follows.

The off-state current was measured as 0.5 pA, and the V_{DD} was 0.48 V, supplying an on–off ratio over 10^7; thus, the P_{static} was calculated as 0.5 pA × 0.48 V = 2.4 × 10^{-13} W.

The calculation process was also suitable for other counterparts and IRDS targets.

The calculation of delay and EDP

The expression of gate delay (τ) and EDP are defined as[9]

$$\tau = C_{total} V_{DD}/I_{on}$$

$$EDP = C_{total}^2 V_{DD}^3/I_{on},$$

where V_{DD} represents the supply voltage defined in 'The extraction of VDD' and I_{on} represents the corresponding on-state current. The C_{total} is total capacitance per channel width, which contains gate capacitance and parasitic capacitance induced by the spacer. However, in our device configuration, the all-around gate controls the channel without overlap with the source/drain part. In addition, the air-gap side wall was introduced in our GAAFETs (Fig. 3a). Therefore, for our short-channel GAAFETs, the delay can be calculated as follows: $C_{total} = \varepsilon_r\varepsilon_0 \times L_G/d$ = (21 × 8.85 × 10^{-12} F m^{-1}/1.6 nm) × 30 nm = 3.835 fF μm^{-1}, $\tau = C_{total}V_{DD}/I_{on}$ = 3.835 fF μm^{-1} × 0.5 V/1 mA μm^{-1} = 1.9 ps. The corresponding EDP can be calculated as follows: EDP = $C_{total}^2 V_{DD}^3/I_{on}$ = (3.835 fF μm^{-1})^2 × (0.5 V)^3/1 mA μm^{-1} = 1.84 × 10^{-27} Js μm^{-1}.

For delay and EDP projected by IRDS targets, detailed device sizes and electrical specifications were all available. For 2D and silicon counterparts, these two parameters were directly extracted from corresponding literature.

The calculation and benchmarking of inverter voltage gain

The inverter voltage gain is defined as

$$\text{Gain} = |dV_{out}/dV_{in}|.$$

The voltage gains of silicon[36,37] and other 2D counterparts[20,38–51] were directly extracted.

Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

Code availability

All computational data are presented in the article. All DFT calculations were performed using VASP, which is commercially available at https://www.vasp.at/.

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Author contributions

H.P., C.T. and J.T. conceived the project and designed the experiments. J.T., C.T., Xin Gao, M.W. and C.X. performed the synthesis of the 2D GAA heterostructures. J.T., C.T., J.J. and C.Z. were involved in device fabrication and electrical characterization. J.J., C.T., C.Q. and L.-M.P were involved in short-channel device fabrication. J.T. and Xiaoyin Gao conducted the STEM and EDX characterizations and analysed the results. F.D. and Y.Y. performed the theoretical calculations. H.P. supervised this research. J.T., C.T. and H.P. co-wrote the paper. All authors contributed to discussions.

Competing interests

The authors declare no competing interests.

Additional information

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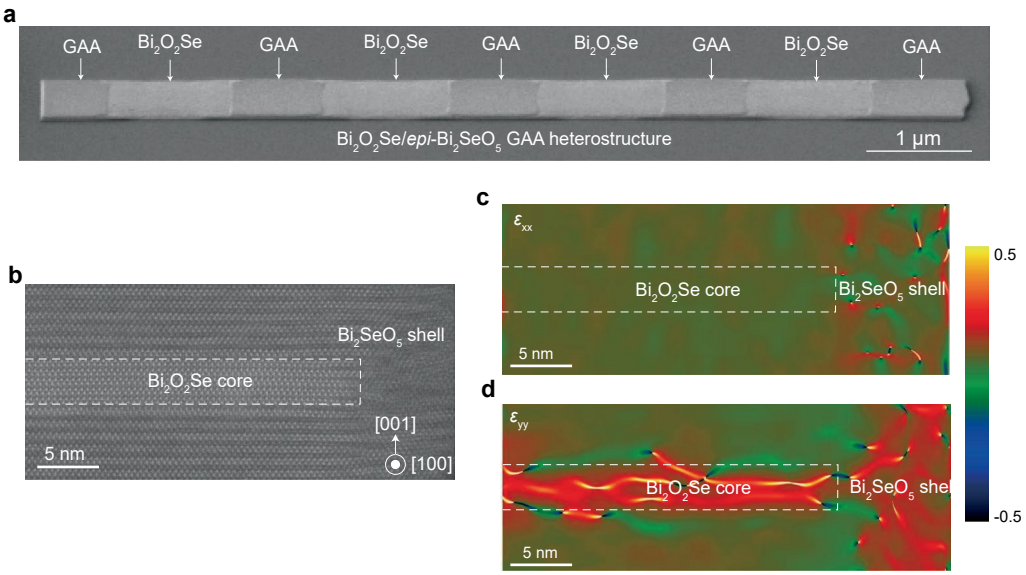

Extended Data Fig. 1 | Segmental Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure and corresponding strain mapping. a, Tilted-view SEM image of segmental Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure, in which the Bi_2SeO_5 shell was selectively etched away while remaining the intact Bi_2O_2Se core. **b**, the cross-section STEM image of the side part of the 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs. **c**, strain mapping across the x axis (ε_{xx}). **d**, strain mapping across the x axis (ε_{yy}).

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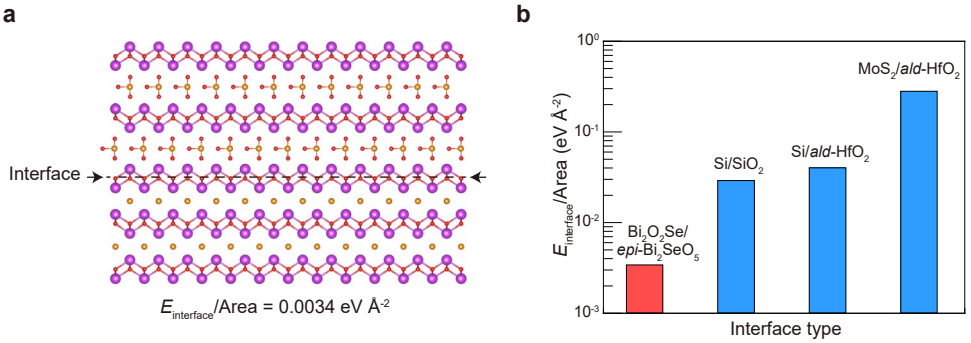

Extended Data Fig. 2 | Calculation of interface energy of semiconductor-oxide heterostructures. a, the schematic illustration of 2D Bi_2O_2Se/Bi_2SeO_5 interface. **b**, The interface formation energy ($E_{interface}$) of Bi_2O_2Se/Bi_2SeO_5 interface, Si/SiO_2 interface[52], Si/*ald*-HfO_2 interface[53] and MoS_2/*ald*-HfO_2 interface[54] calculated by DFT, indicating the Bi_2O_2Se/Bi_2SeO_5 GAA heterostructure is thermodynamically stable.

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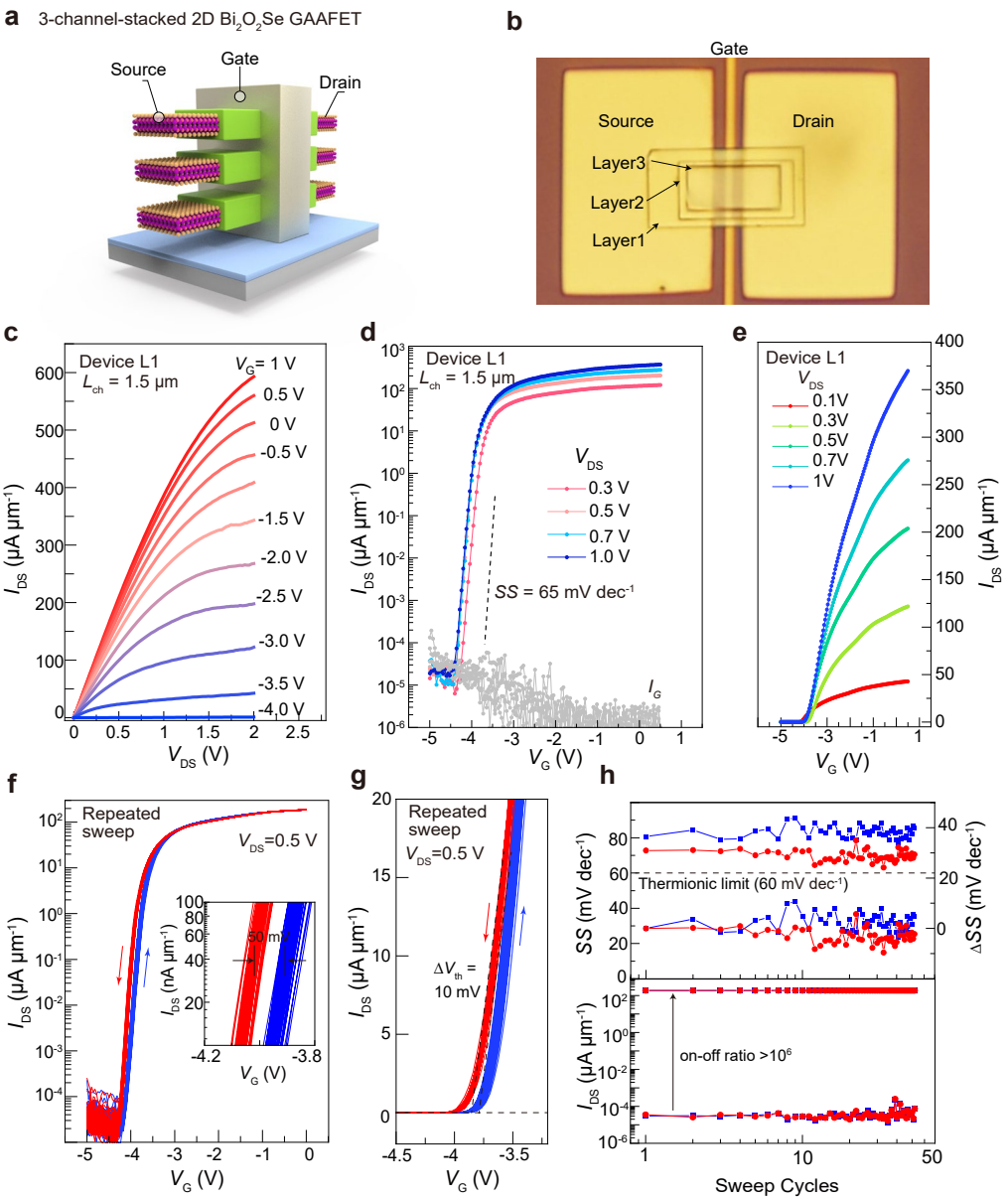

Extended Data Fig. 3 | The electrical properties of a typical 3-layered stacked Bi_2O_2Se/Bi_2SeO_5 GAAFET. a, **b**, Structural schematics (**a**) and optical image (**b**) of as-fabricated 3-layered stacked Bi_2O_2Se/Bi_2SeO_5 GAAFET. **c**–**e**, output (**c**) and transfer (**d**, **e**) characteristics of the as-fabricated 3-layered stacked Bi_2O_2Se/Bi_2SeO_5 GAAFET. **f**, **g**, The repeated measurement of the 3-layerd stacked GAAFET shown in (**b**) with 50 cycles dual-direction sweep. Inset: the hysteresis detail of the 2D GAAFET for 50 cycles dual-direction sweep. **h**, The absolute values (left axis, top), the relative fluctuation (right axis,top) of the subthreshold swings (*SS*) and the off-state, on-current in 50 cycles dual-direction sweep. The thermionic limit of SS was included by dashed line.

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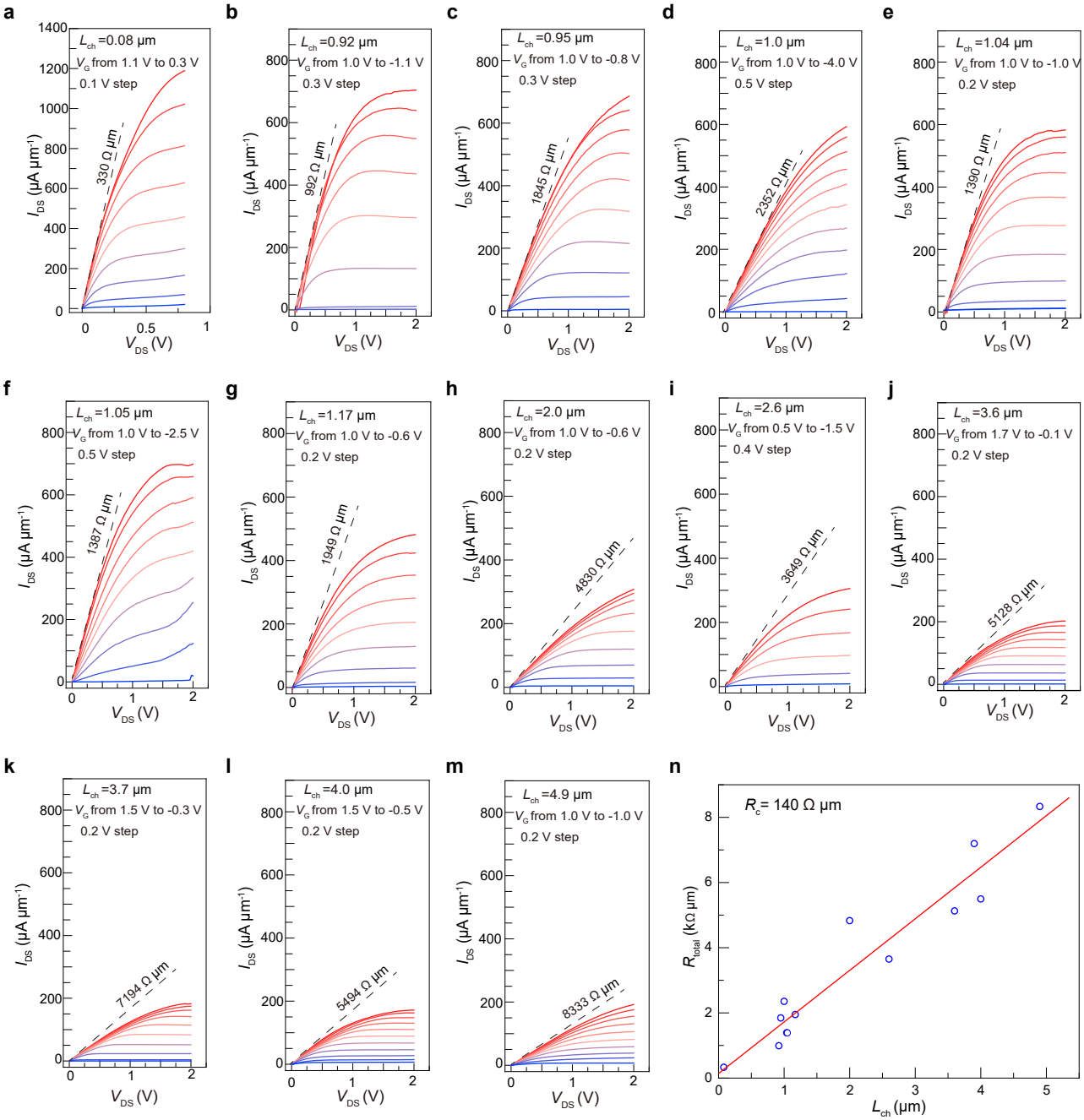

Extended Data Fig. 4 | Contact resistance for 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET. **a**–**m**, Output curves for channel lengths ranging from 30 nm to 4900 nm. **n**, Transfer length model plot of total resistance (R_{total}) versus channel length (L_{ch}) from 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs. The lines represent linear fit to data and the extraction of contact resistance (R_c) was expressed in the following equation: $R_{total} = R_{ch} + 2R_c$, where R_{ch} is channel resistance, R_{tot} is the total resistance.

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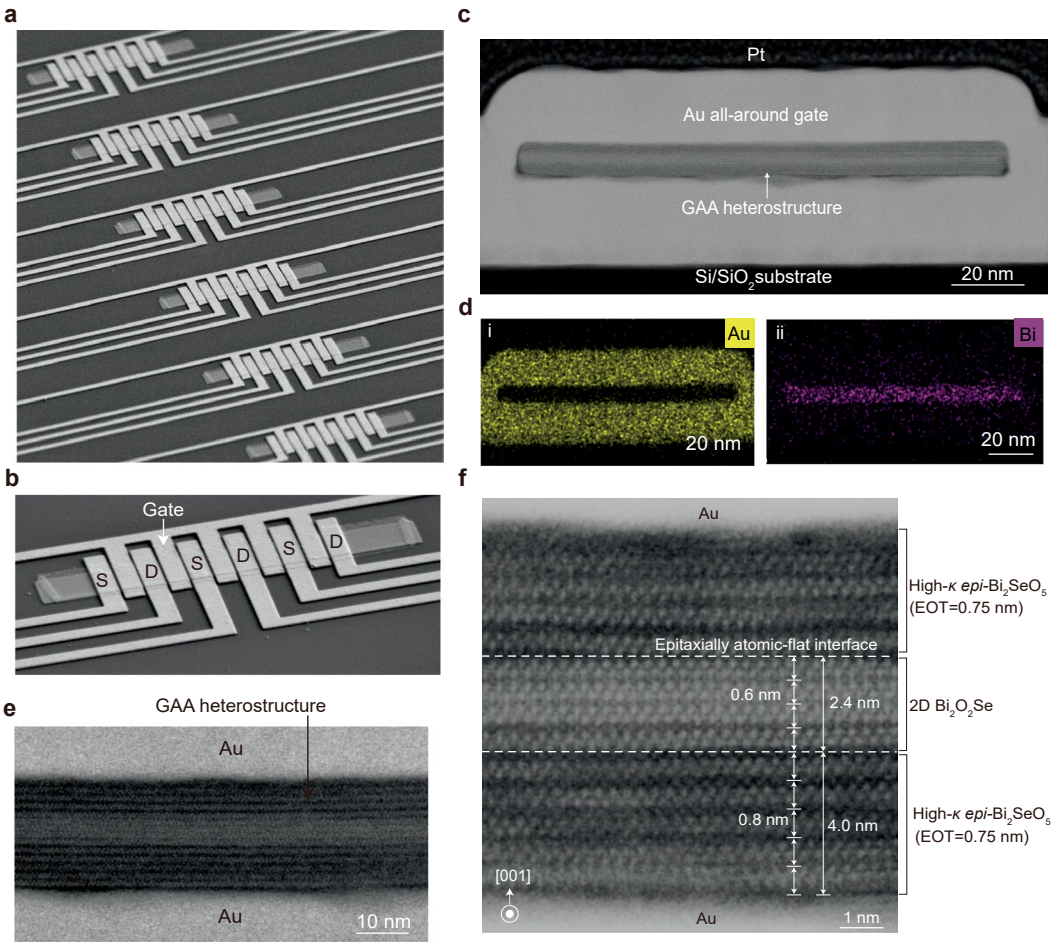

Extended Data Fig. 5 | Structural characteristics of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET arrays. a, **b**, Tilted-view SEM image of Bi_2O_2Se/Bi_2SeO_5 GAAFET arrays, in which the Bi_2SeO_5 shell was selectively etched away while remaining the intact Bi_2O_2Se core. **c**, Cross-sectional STEM image of a typical 2D Bi_2O_2Se/Bi_2SeO_5 GAFET, showing an intact GAA structure with a physical width of about 100 nm. **d**, The energy dispersive X-ray (EDX) element mapping of the 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET shown in ©, in which the GAA structure can be well-defined. **e**, **f**, High-resolution Cross-sectional STEM image of the 2D GAA heterostructure shown in ©, showing a heterostructure containing 2.4-nm-thick Bi_2O_2Se channel and 4.0-nm-thick Bi_2SeO_5 dielectric per side with atomically flat interface.

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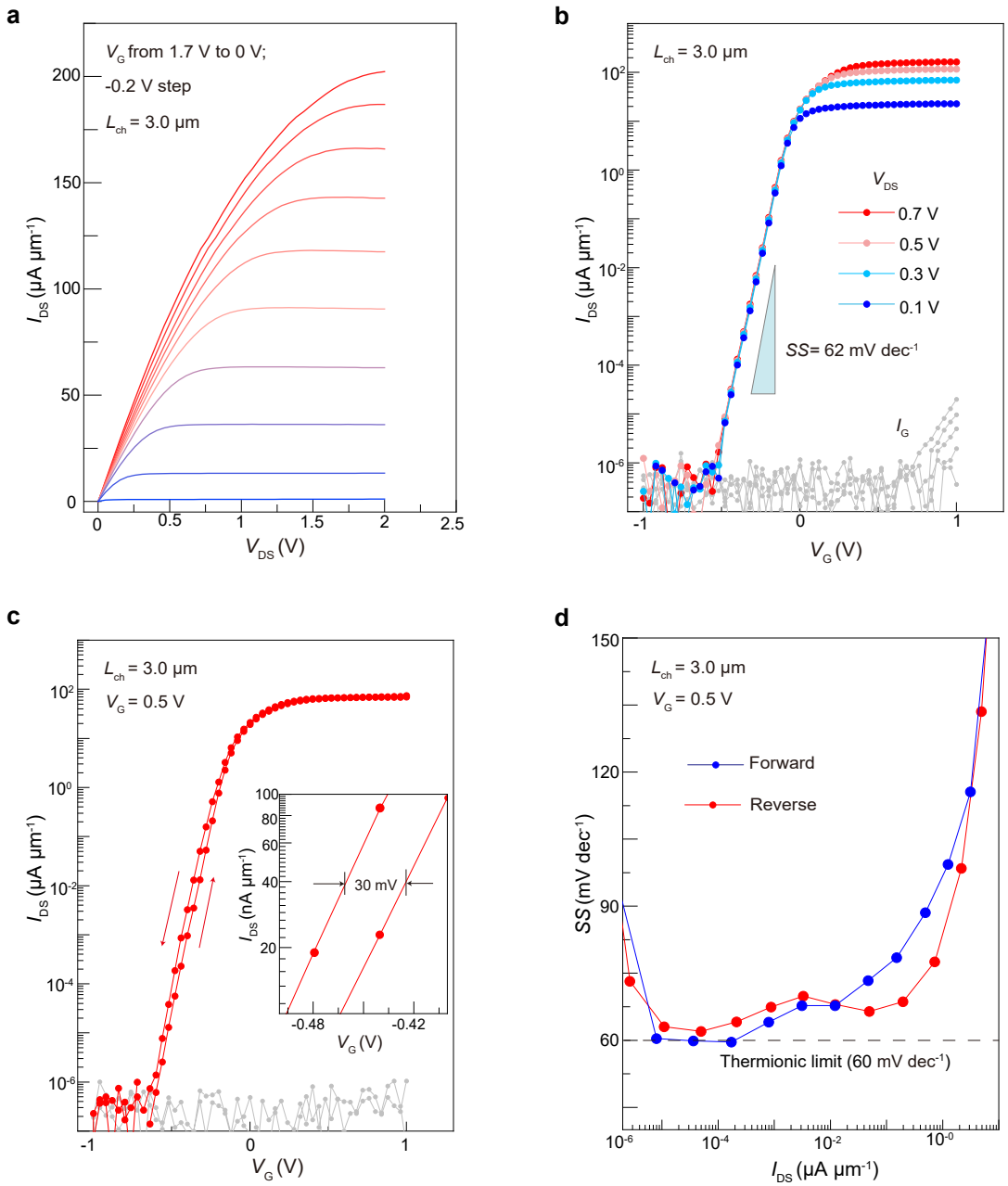

Extended Data Fig. 6 | Typical electrical properties of as-prepared 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET arrays. a, **b**, Typical output characteristic curves (**a**) and transfer curves (**b**) of Bi_2O_2Se/Bi_2SeO_5 GAAFET arrays. **c**, **d**, hysteresis (**c**) and *SS* (**d**) analysis of as-prepared Bi_2O_2Se/Bi_2SeO_5 GAAFET arrays.

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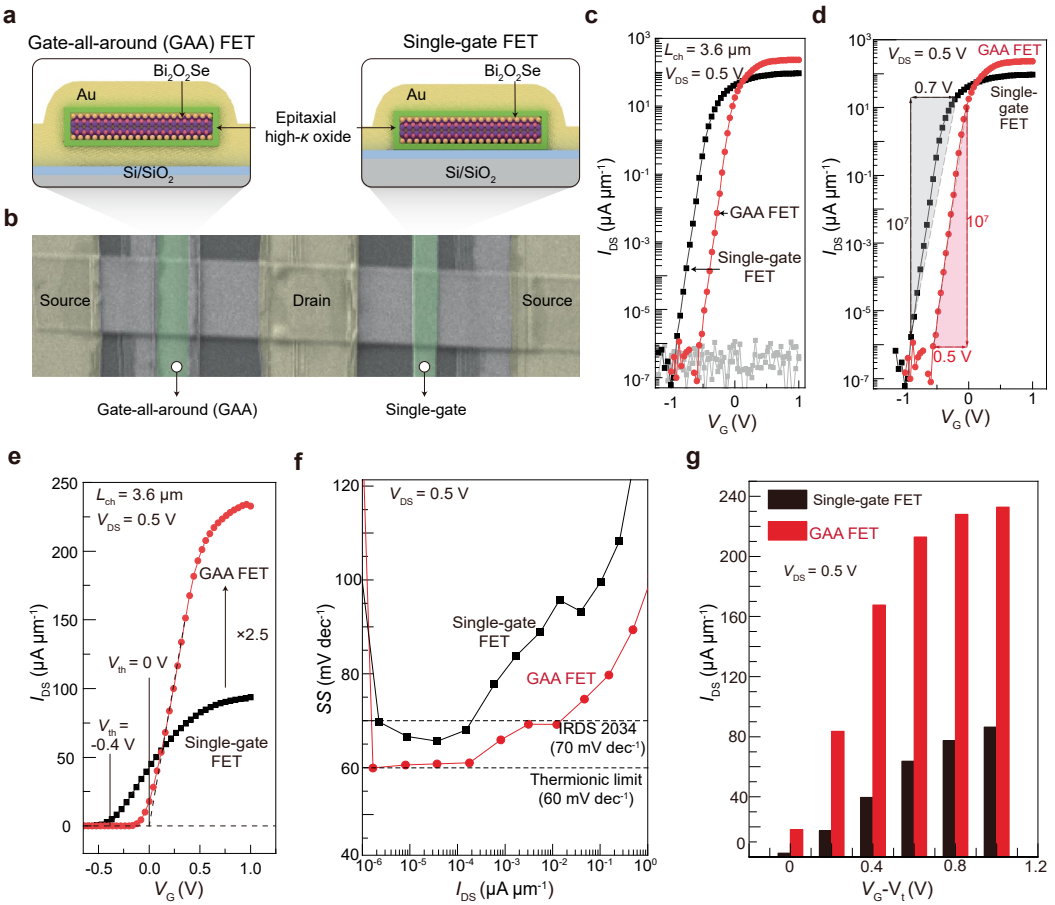

Extended Data Fig. 7 | Comprehensive comparisons of 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET and single-gate FET. a, **b**, Schematic illustration (**a**) and SEM image (**b**) of the as-prepared 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET and single-gate FET, in which the channel thickness is about 2.4 nm integrated by the van der Waals dielectric with an EOT of 0.75 nm. **c**–**e**, The transfer characteristic curves of the GAAFET (red dots) and single-gate FET (black dots), in which the GAAFET showed a higher gate-controllability efficiency with a larger on-off ratio and smaller threshold voltage. The leakage current of both transistors was also pointed. **f** The subthreshold swings of the as-fabricated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET (red dots) and single-gate FET (black dots), in which the dash line denotes the thermionic limit of subthreshold swing, and the target value for 2D GAAFETs projected by IRDS was also shown. Both devices show near-thermionic-limit subthreshold swings and meet the target projected by IRDS in 2034. **g**, The on-state current comparison of the as-fabricated 2D Bi_2O_2Se/Bi_2SeO_5 GAAFET (red column) and single-gate FET (black column).

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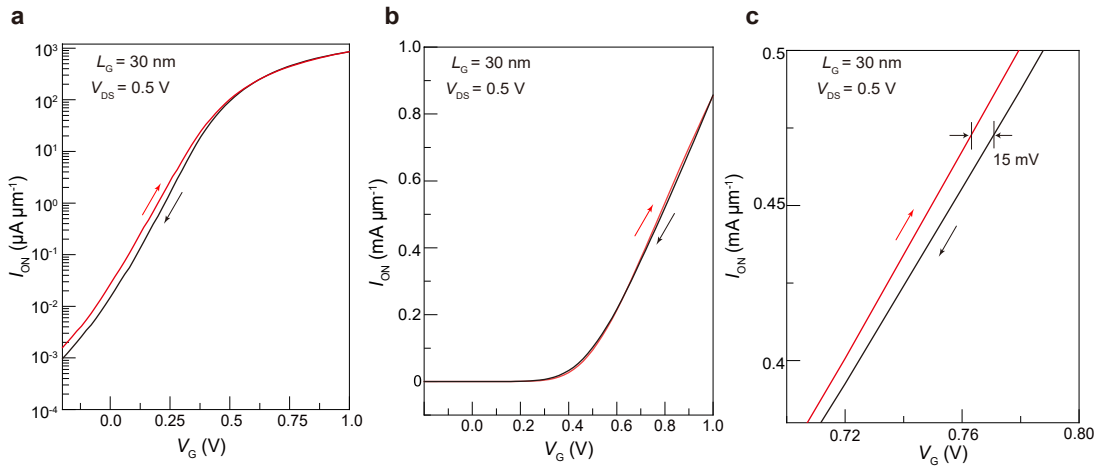

Extended Data Fig. 8 | Hysteresis of the 30-nm-gate-length 2D GAAFET. a, **b**, The hysteresis of as-prepared short-channel 2D GAAFET. **c**, The detailed hysteresis of (**b**).

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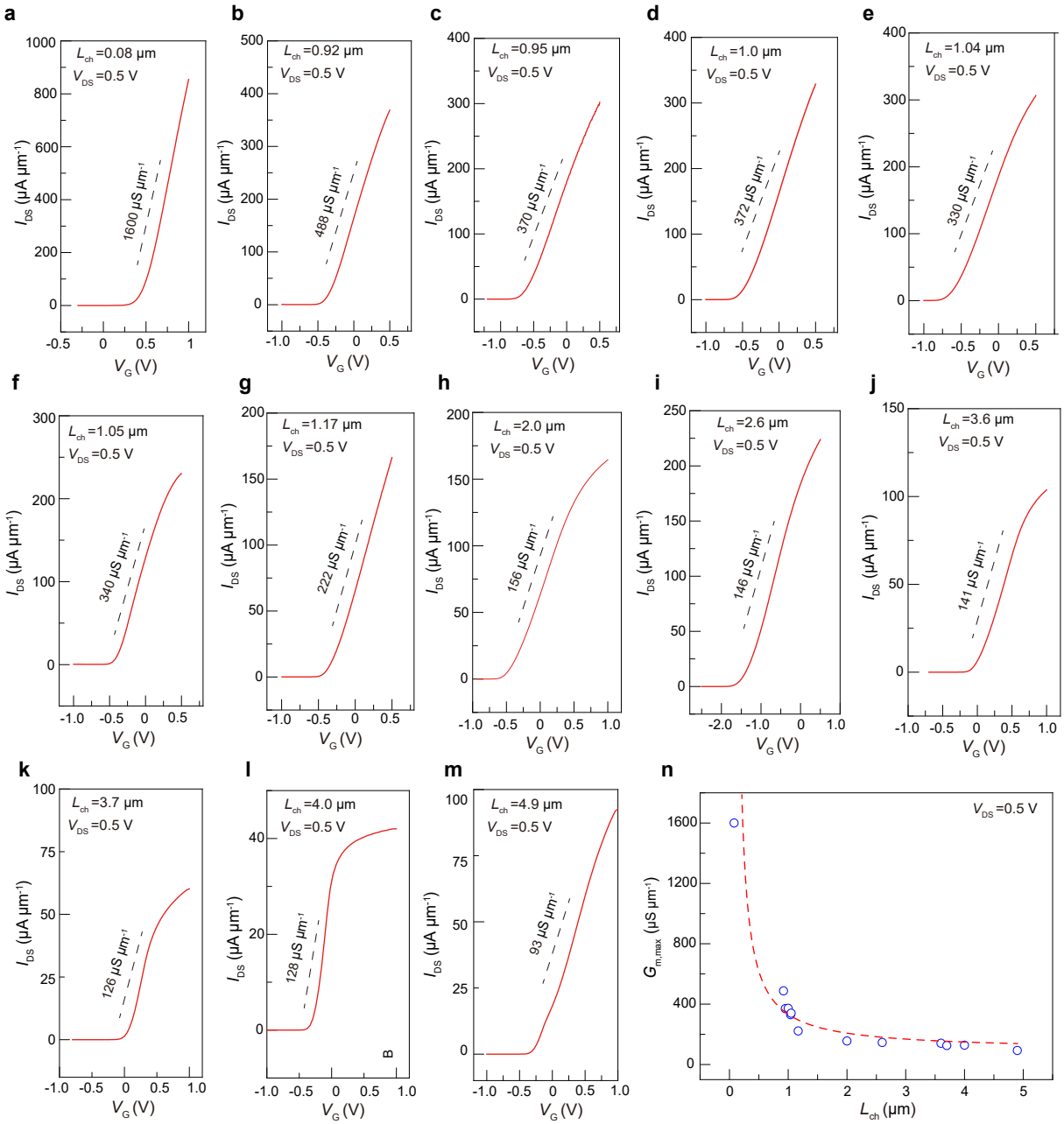

Extended Data Fig. 9 | Transconductance ($G_{m,max}$) and channel-length (L_{ch}) relationship of 2D GAAFETs. a–m, $G_{m,max}$ of as-prepared GAAFET in different channel length. Note the V_{DS} was set as 0.5 V. **n**, The Transconductance ($G_{m,max}$) and channel-length (L_{ch}) relationship of 2D GAAFETs.

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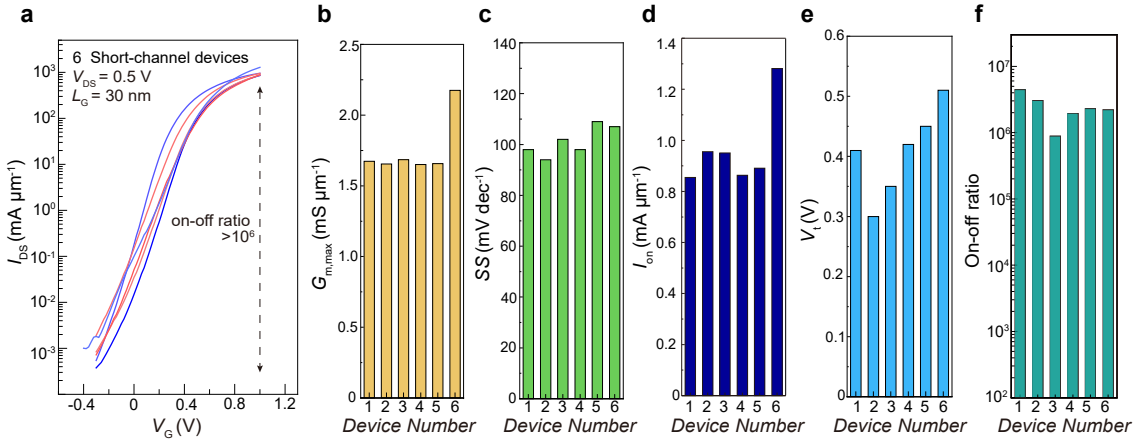

Extended Data Fig. 10 | The variability of short-channel 2D Bi_2O_2Se/Bi_2SeO_5 GAAFETs. a, The transfer characteristic of 6 individual short-channel 2D GAAFETs with gate length of 30 nm. **b**–**f**, The statistical histogram of $G_{m,max}$ (V_{DD} = 0.5 V) (**b**), SS (**c**), on-state current (**d**), V_{th} (**e**), and on-off ratio (**f**).