CSCI 424
Computer Architecture
Fall 2016

Homework #1

Distributed: August 30, 2016
Due: September 8, 2016 via Blackboard by 11:00pm
Points: 50

Instructions:

a. No collaboration is allowed.
b. Upload the PDF as <CS424_HW1_lastname_firstname>.pdf (e.g. Student Last Name = Bob, Student First Name = Alice, then submit CS424_HW1_Bob_Alice.pdf).

1. (4 pts) Computer A executes the MIPS ISA and computer B executes the x86 ISA. On average, programs execute 1.5 times as many MIPS instructions as x86 instructions. Computer A has an average CPI of 1.5 and computer B an average CPI of 3. If computer B runs at a 3GHz clock frequency, what speed does computer A have to run at to be at least as fast as computer B?

2. (7 pts) Assume a typical program has the following instruction type breakdown:

   30% loads
   10% stores
   40% adds (adds, compares, and, sub, etc.)
   8% multiplies
   2% divides
   8% conditional branches (assume perfect prediction)
   2% unconditional branches (jumps, calls, returns, etc.)

   Assume the processor that this program will be running on has the following instruction latencies (CPIs):

   loads: 4 cycles
   stores: 6 cycles
   adds: 2 cycles
   multiplies: 12 cycles
   divides: 40 cycles

conditional branches: 4 cycles

unconditional branches: 2 cycles

If you could pick one type of instruction to make twice as fast (half as many cycles to complete) in the next-generation of this processor, which instruction type would you pick? Why?

3. (9 pts) Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3.0 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
   a. Which processor has the highest performance expressed in instructions per second?
   b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
   c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

4. (15 pts) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3.0 GHz and CPIs of 2, 2, 2, and 2.
   Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2?
   a. What is the global CPI for each implementation?
   b. Find the clock cycles required in both cases.

5. (15 pts) Assume a program requires the execution of 50×10^6 FP instructions, 110×10^6 INT instructions, 80×10^6 L/S instructions, and 16×10^6 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2.0 GHz clock rate.
   a. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?
   b. By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?
   c. By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?