**CSCI 424**
**Computer Architecture**
**Fall 2016**

**Homework #6**

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| **Distributed**: | November 03, 2016 |
| **Due**: | November 10, 2016 via Blackboard by 11:00pm |
| **Points**: | 50 |

Instructions:

a. No collaboration is allowed.
b. Upload the PDF as <CS424_HW6_lastname_firstname>.pdf (e.g. Student Last Name = Bob, Student First Name = Alice, then submit CS424_HW6_Bob_Alice.pdf).

1. (15 pts) Below is a sequence of twelve 32-bit memory address references given as word addresses.

   1, 18, 2, 3, 4, 20, 5, 21, 33, 34, 1, 4

   a) Assuming a direct-mapped cache with one-word blocks and a total size of 16 blocks, list if each reference is a hit or a miss assuming the cache is initially filled with word address 0, 1, 2, …15 memory data. Show the state of the cache after the last reference. What is the hit rate for this reference string?
   b) Now, assuming a direct-mapped cache with two-word blocks and a total size of 8 blocks, list if each reference is a hit or a miss assuming the cache is initially empty. Show the state of the cache after the last reference. What is the hit rate for this reference string?
   c) Now, assuming a set-associative cache with two ways, two-word blocks and a total size of 8 blocks, list if each reference is a hit or a miss assuming the cache is initially empty (assume LRU replacement). Show the state of the cache after the last reference. What is the hit rate for this reference string?

2. (10 pts) In general, cache access time is proportional to cache capacity. Assume that main memory accesses take 100 nsec and that memory accesses are 35% of all instructions. For a processor that has a 2KB L1 cache with an 8% L1 miss rate and a 0.50 nsec L1 hit time
   a) If the L1 hit time determines the cycle time for the processor, what is its

clock rate?

b) What is the AMAT? Assuming a base CPI of 1 without any memory stalls, what is the actual CPI when memory system effects are considered?
c) What is the AMAT for the processor if you were to add a 1MB L2 cache with a 95% miss rate and a 5.00 nsec hit time? Assuming a base CPI of 1 without any memory stalls, what is the actual CPI because of adding the L2 cache?

3. (25 pts) In this second set of SimpleScalar experiments you are going to explore the memory hierarchy. Continue to use a fastforward of 300,000 and simulate 2,000,000 instructions for each benchmark run for all four integer benchmarks and both floating point benchmarks.

**Baseline Datapath:**
For the baseline simulations configure a single-issue datapath as we did in HW#5. Instead of predict-not-taken, use the bimod branch predictor (with a predictor table size of 2048 and a BTB with 512 sets, associativity of 4 – these are the default branch predictor settings, you do not have to set them). Use a memory bus width of 8 bytes (the default), a memory latency of 100 and 10 (100 cycle access latency for first word and 10 cycles for the rest), and a TLB latency of 15 cycles.

Use the default setting for the memory hierarchy, i.e., il1:256:32:1:l (an 8KB L1 instruction cache with 256 blocks, 32 byte blocks and direct mapped; note that the last character is the letter l (not the number 1)), dl1:256:32:1:l, ul2:1024:64:4:l (a 256KB unified L2 cache with 64 byte blocks and 1024 blocks total, 4-way set associative and LRU replacement), itlb:16:4096:4:l (a 64 entry (4-way set associative) iTLB with a page size of 4096), and dtlb:32:4096:4:l (see page 6 in The SimpleScalar Tool Set handout for more details). Also, use the default cache speeds, i.e., dl1lat = 1, dl2lat = 6, il1lat = 1, and il2lat = 6.

**Larger L2 Cache:**
Quadruple the size of the unified L2 cache and double its latency (i.e., ul2:4096:64:4:l, dl2lat = 12 and il2lat = 12).

**Larger L1 and L2 Caches:**
Keeping the quadrupled L2 cache, now also quadruple the size of the L1 caches and double their latencies. Keep both L1 caches direct mapped.

**Set Associative L1 Data Cache:**
Keeping both the quadrupled L2 and L1 caches, make just the L1 data cache 4-way set associative. Also, increase the latency of the L1 data cache to 3 cycles. Run two sets of experiments, one using LRU replacement and one using FIFO replacement for the L1 data cache.

For each set of experiments (there are a total of 5: Baseline, Larger L2, Larger L1 and L2, Set Associative L1 Data Cache LRU, and Set Associative L1 Data Cache FIFO), report in tabulated form the sim_IPC, il1 cache hits and misses, dl1 cache hits and misses, ul2 cache hits and misses, itlb hits and misses, and dtlb hits and misses. Compare the five different machines and provide an explanation for the changes in performance and hit/miss ratios.