CS 654 Homeworks 2–3

Due dates:
Problems 1, 2, 3.1, and 3.2 are due Monday September 26
Problems 3.3, 3.5, 3.7, 3.11, and 3.12a-d, are due Monday Oct 3

1. Suppose a computer's address size is k bits (using byte addressing), the cache size is S bytes, the block size is B bytes, and the cache is A-way associative. Assume that B is a power of 2, so $B = 2^b$. Figure out what the following quantities are in terms of S, B, A, b and k: the number of sets in the cache, the number of index bits in the address, and th e number of bits needed to implement the cache (assume that each block line has one valid bit).

2. Explain in a short paragraph why cache size and VM page size are interdependent. Suggest an architectural change so that cache sizes larger than the page size can be implemented. Give a short example.

3. Do problems 3.1, 3.2, 3.3, 3.5, 3.7, 3.11 and 3.12 a,b,c,d, from the book. This is from the case studies on page 248.