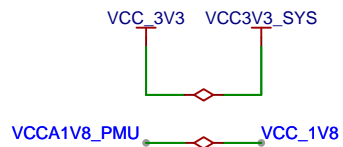
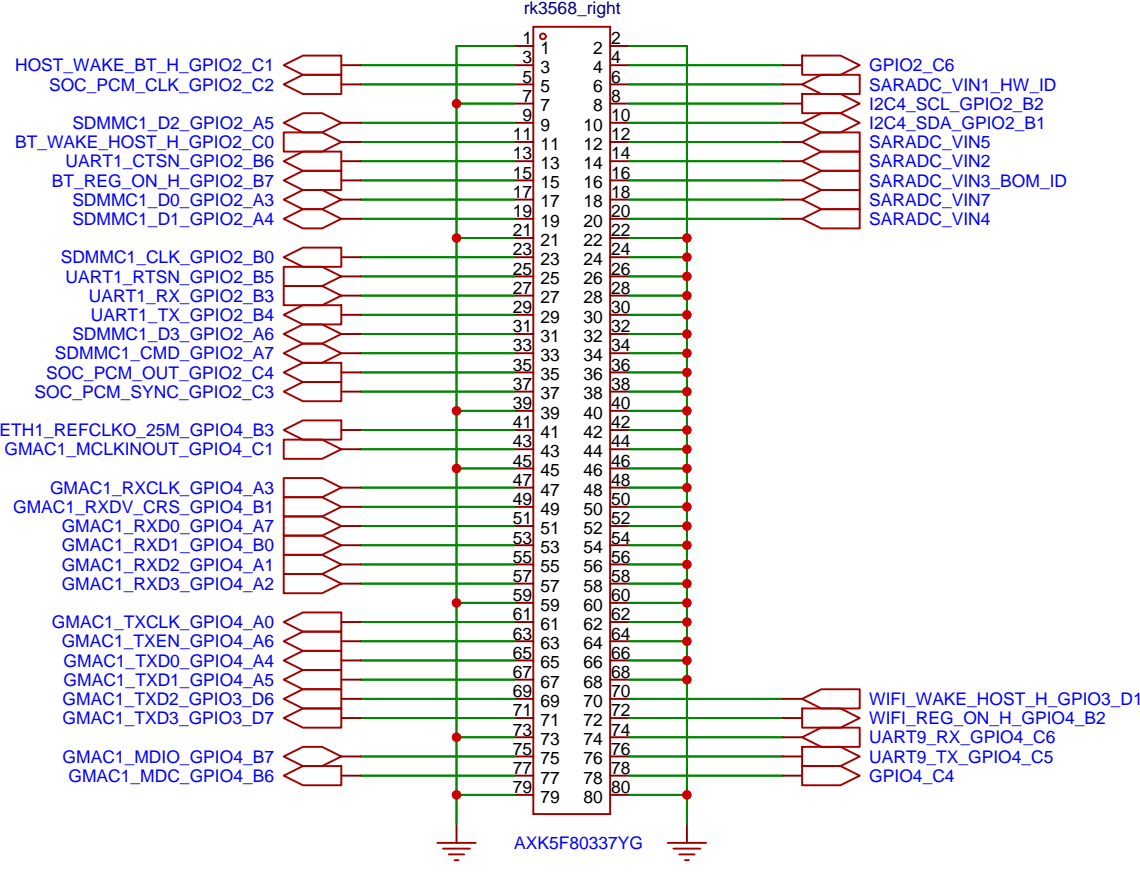
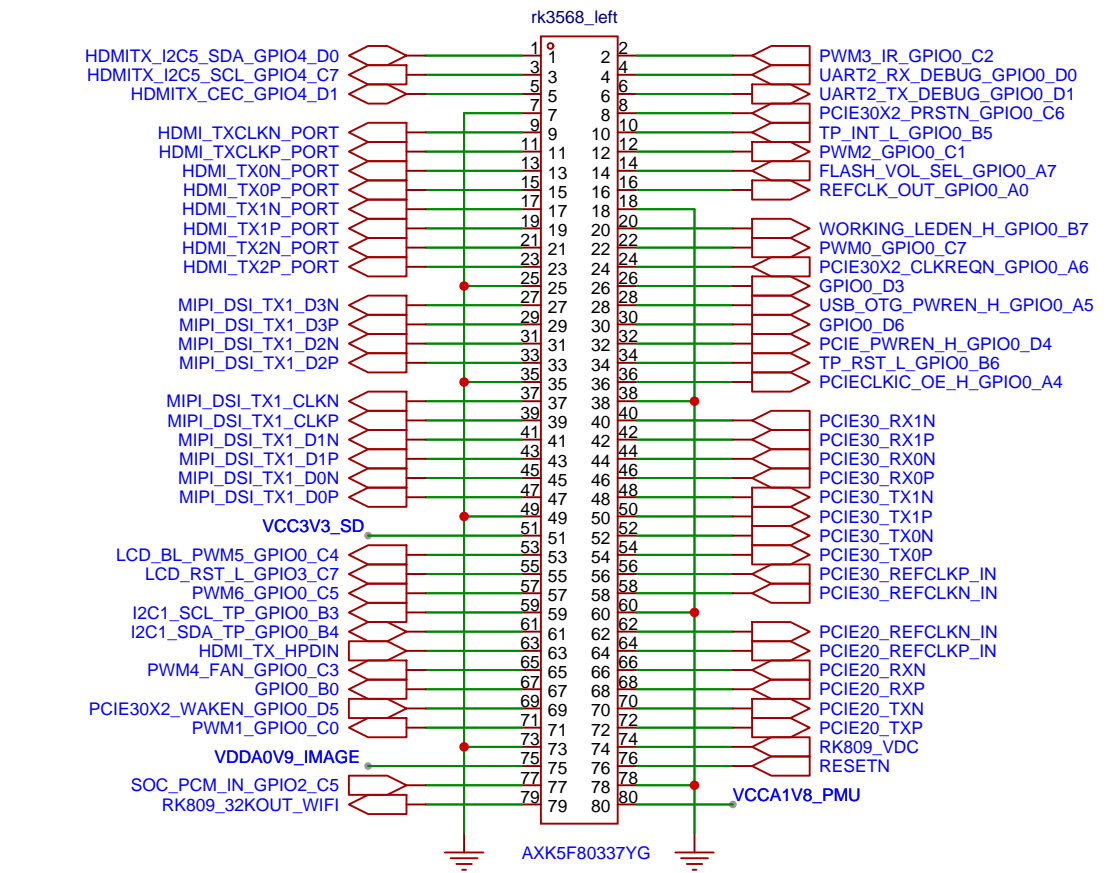
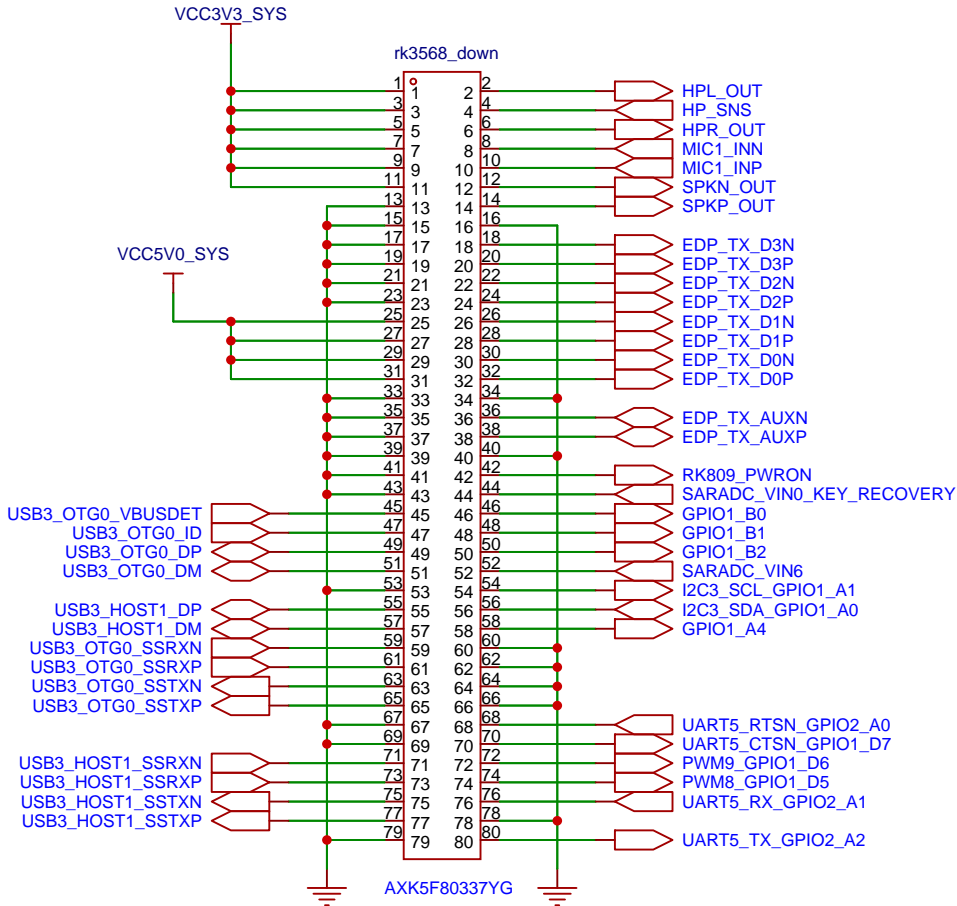
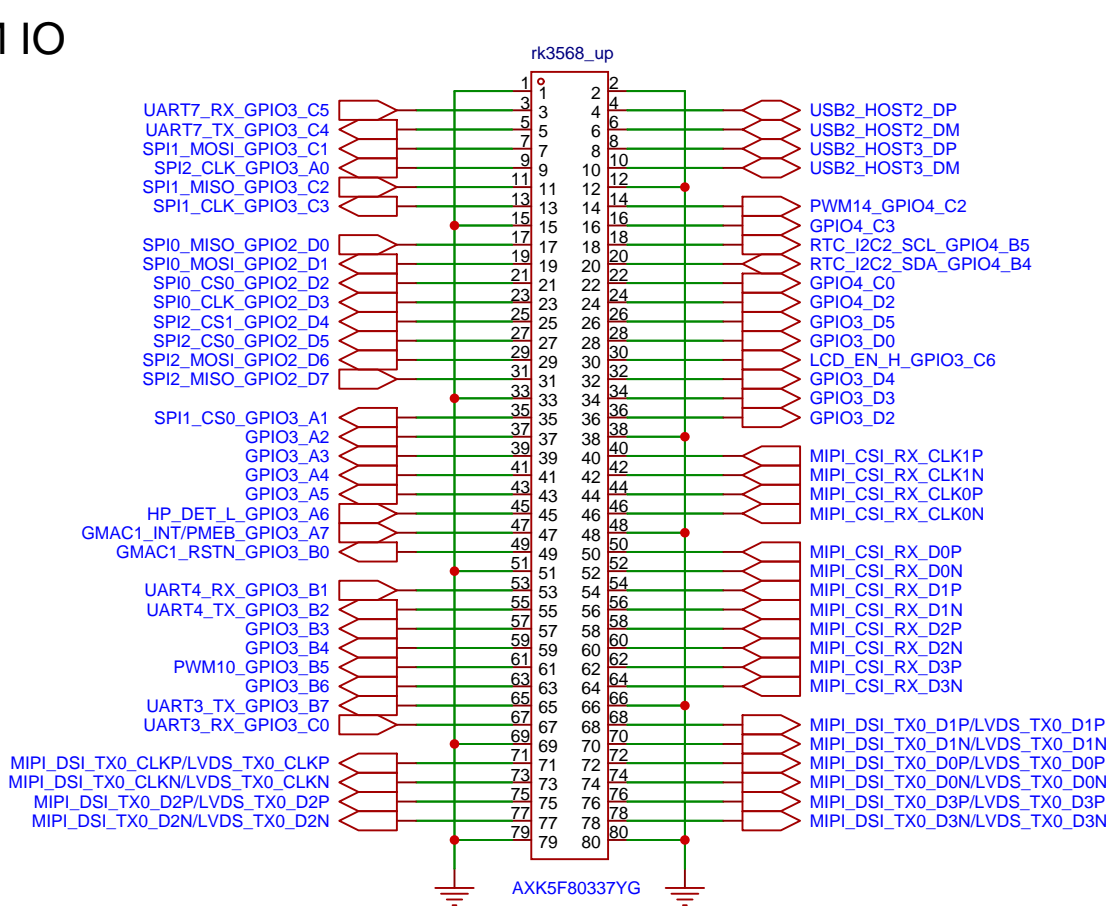
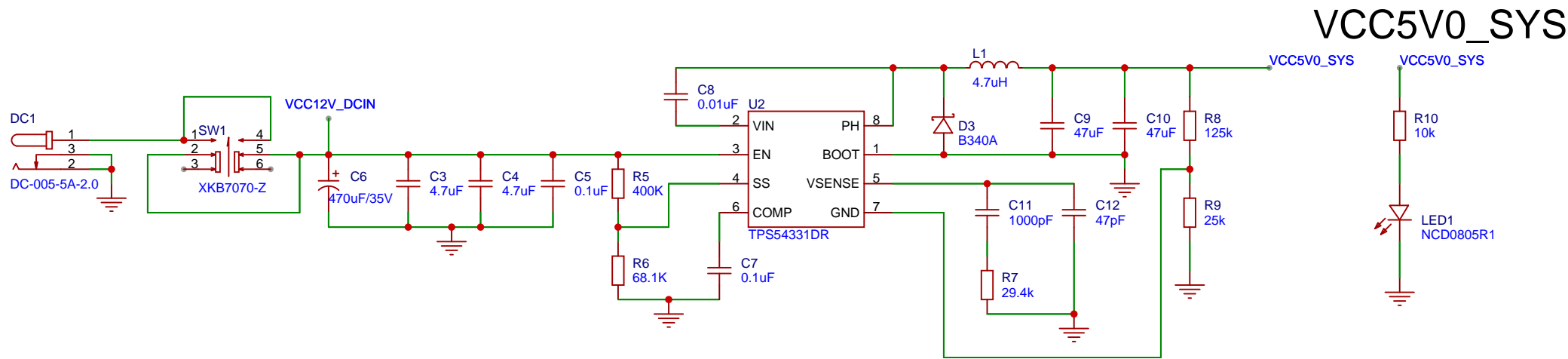


BOTTOM IO

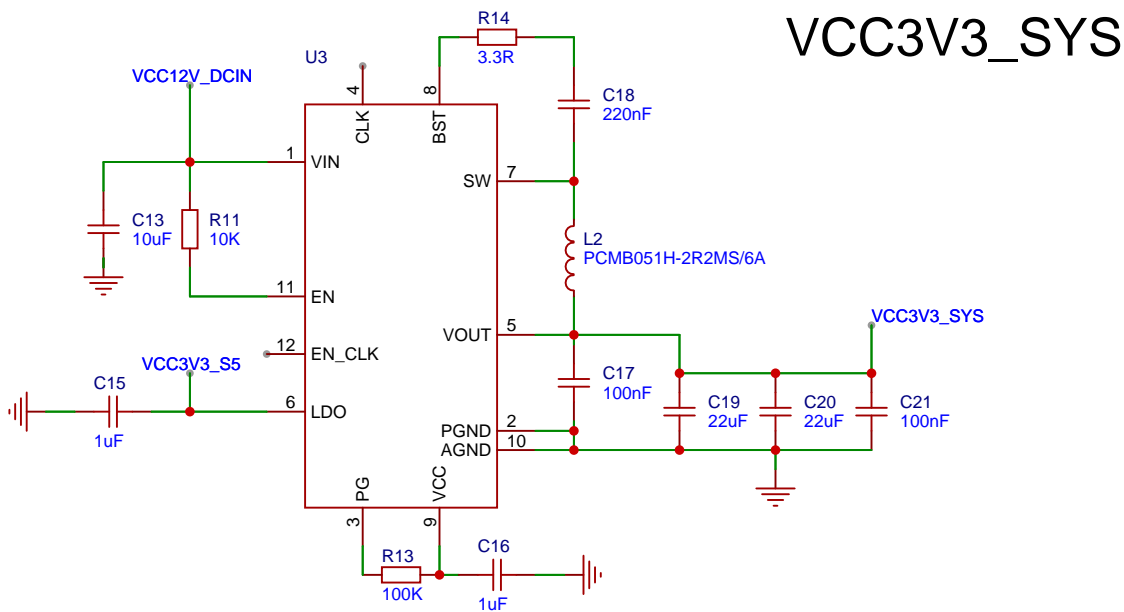


原理图	rk3568			更新日期	2024-08-11
				创建日期	2024-07-31
图页	rk3568_bottom			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	1 共 9
		V1.0	A3	LT	

12V/3A DCIN

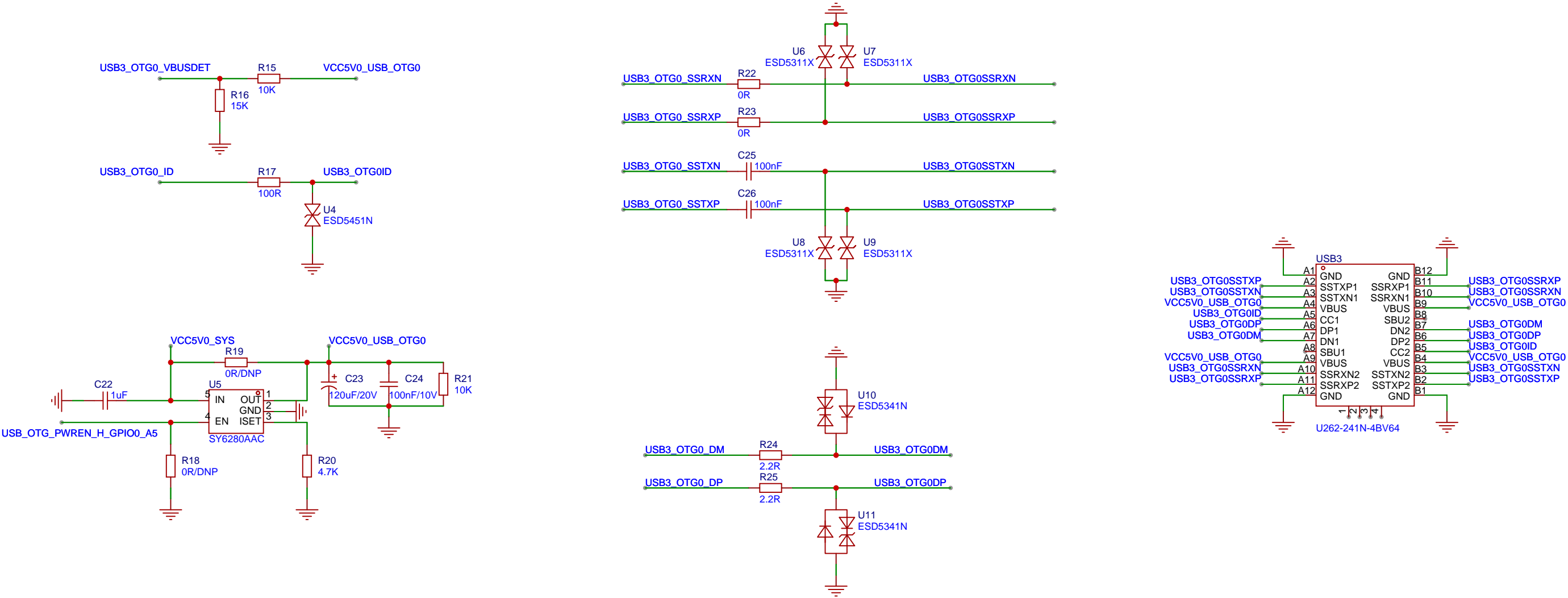


DC/DC 3.3V

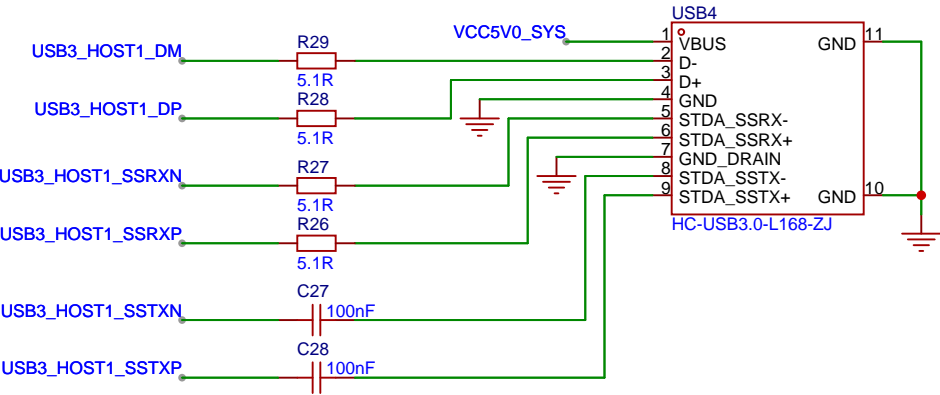


原理图	rk3568			更新日期	2024-08-04
				创建日期	2024-08-01
图页	rk3568_power			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	2 共 9
嘉立创EDA		V1.0	A3	LT	

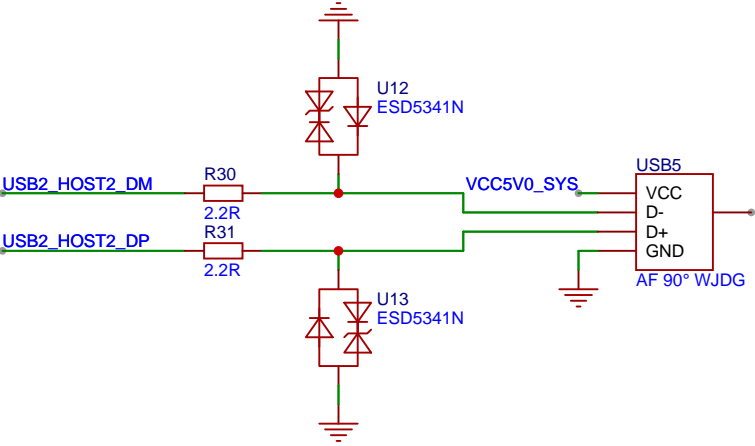
USB3.0 OTG



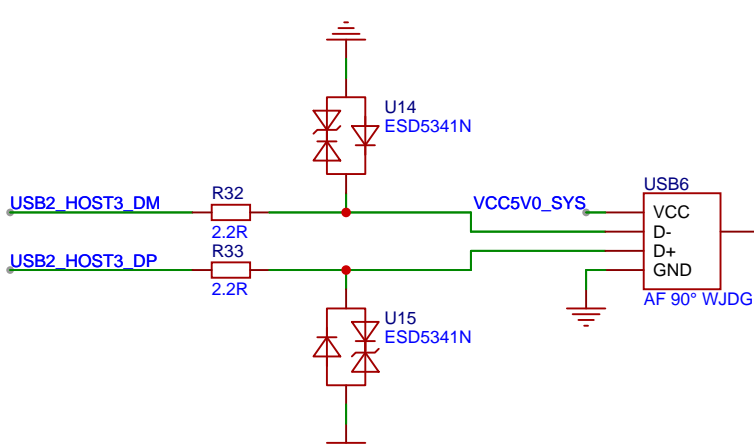
USB3.0 HOST1



USB2.0 HOST2

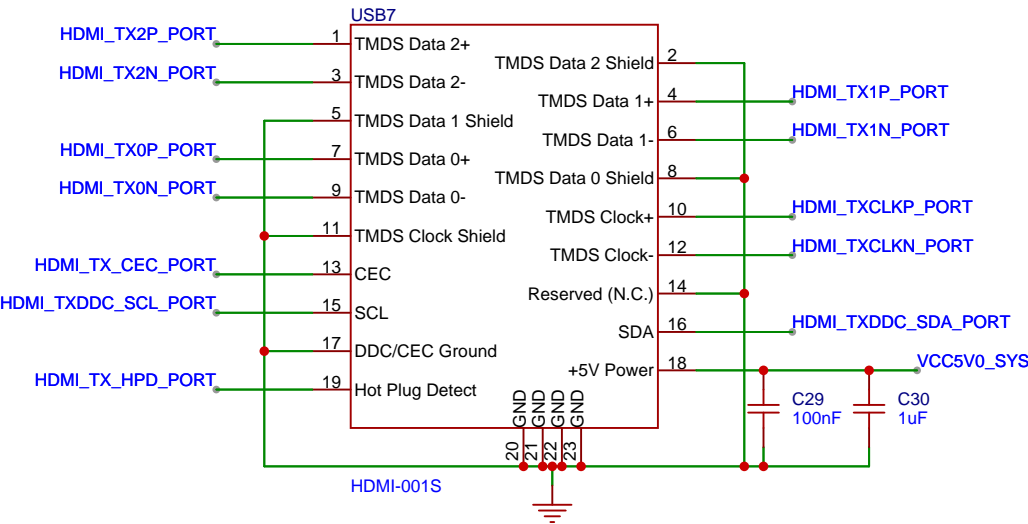
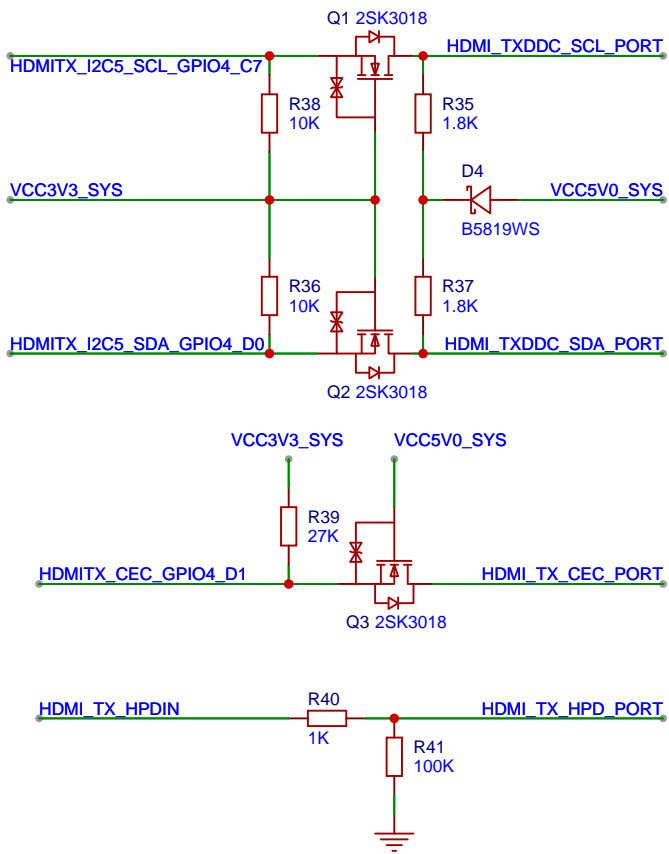


USB2.0 HOST3

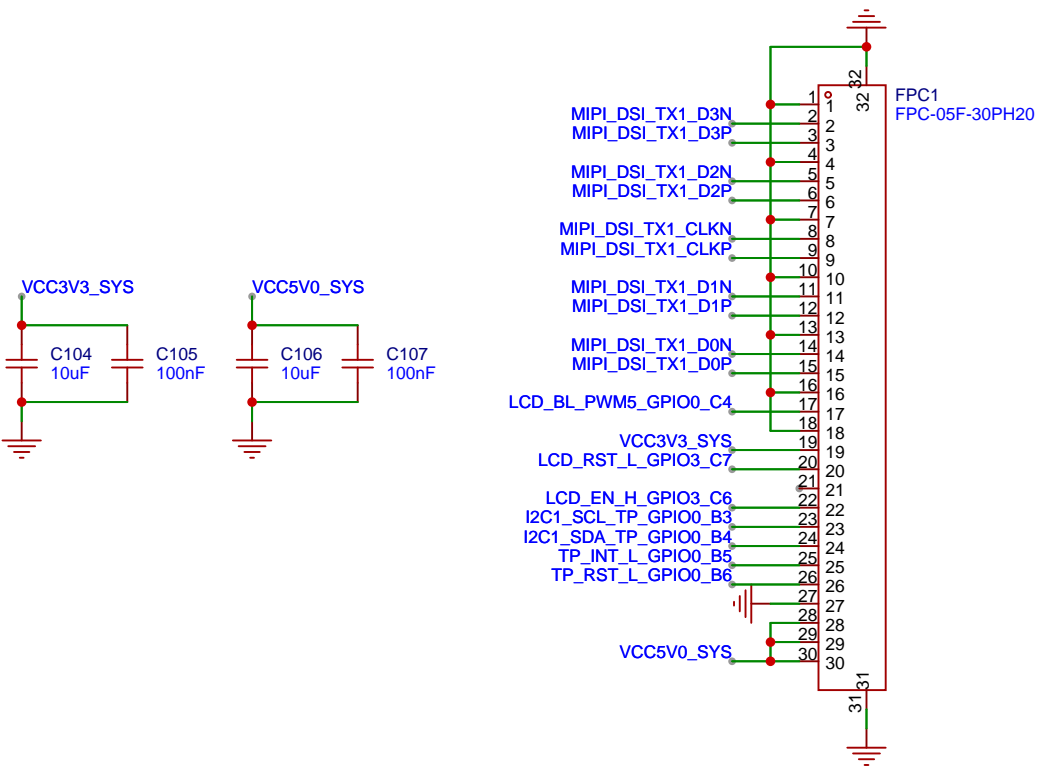


原理图	rk3568			更新日期	2024-08-11
				创建日期	2024-08-02
图页	rk3568_usb			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	3 共 9
		V1.0	A3	LT	

HDMI2.0 TX

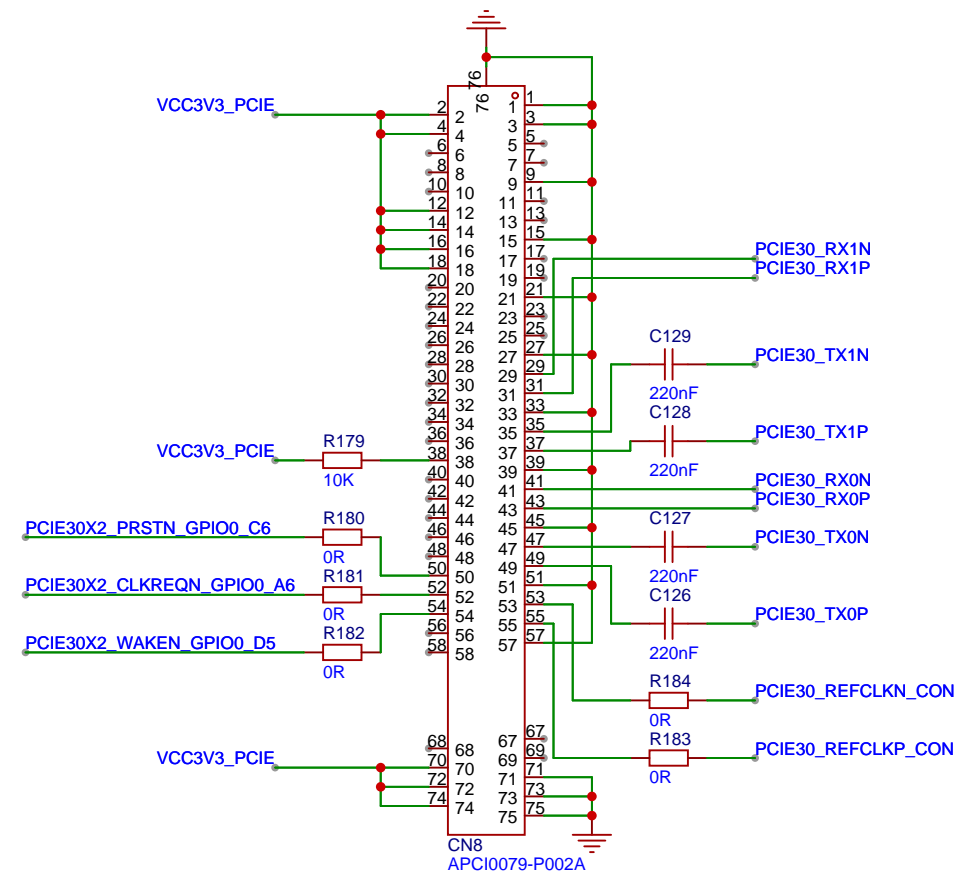
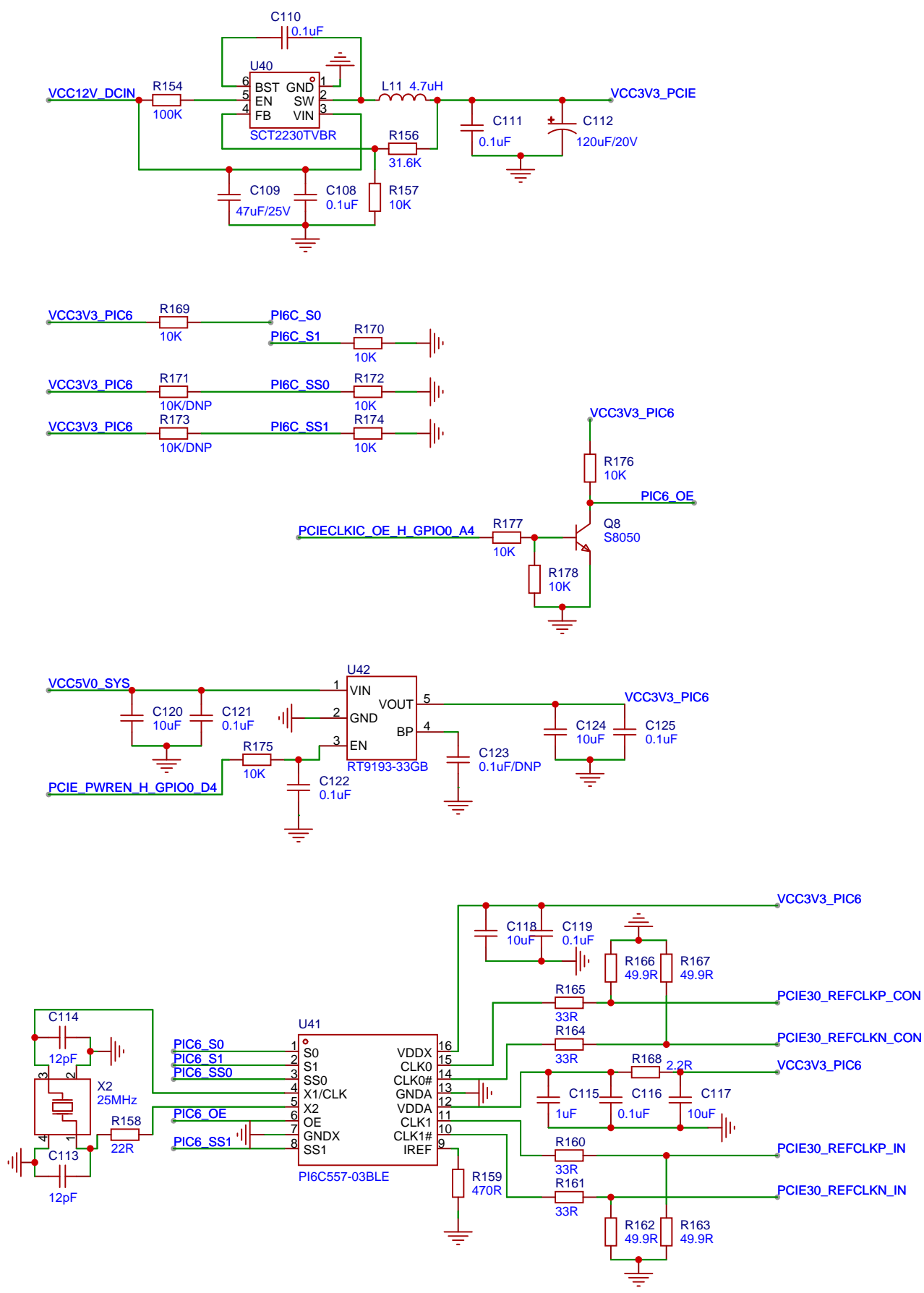


MIPI LCD



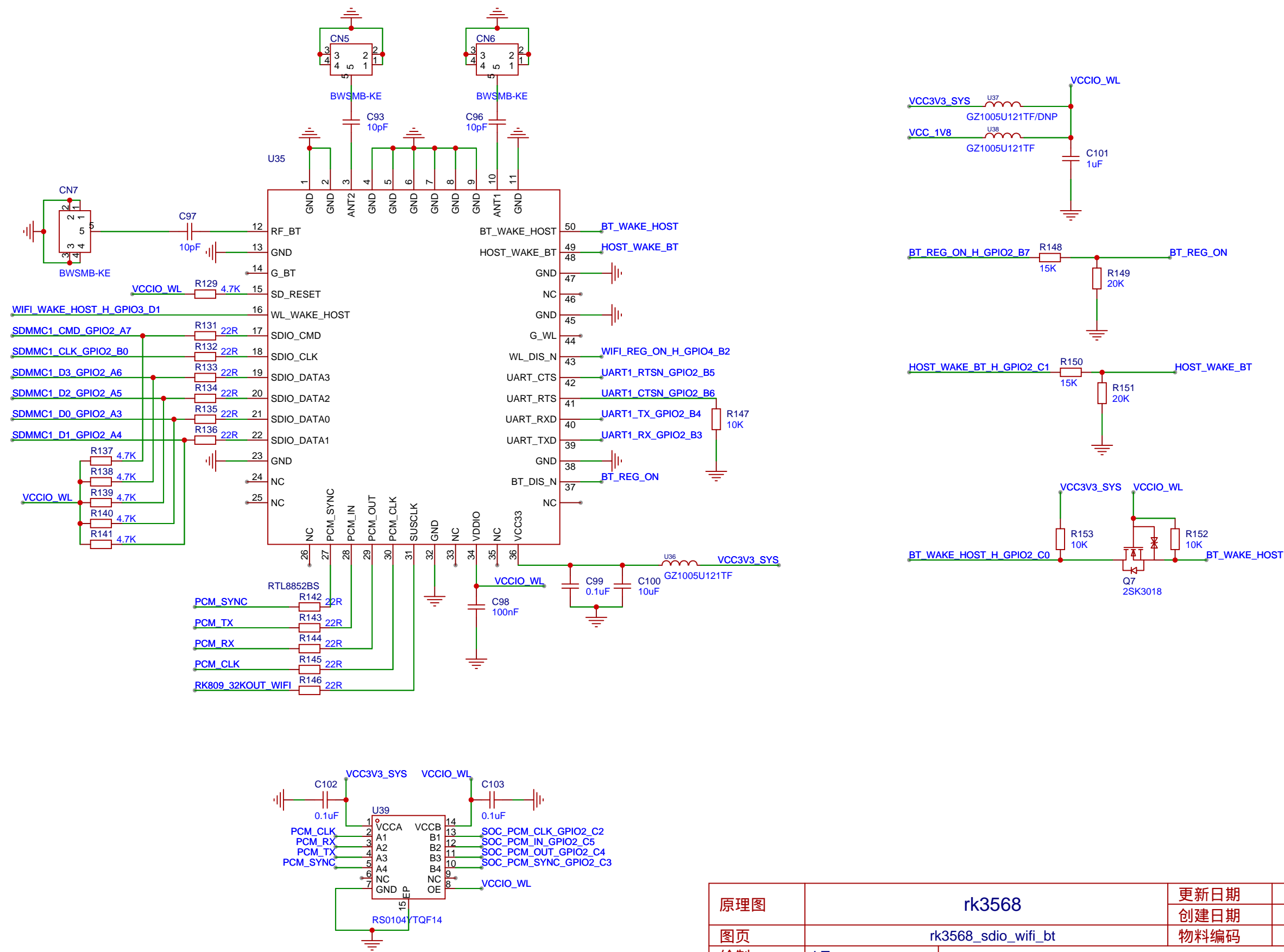
原理图	rk3568			更新日期	2024-08-11
				创建日期	2024-08-02
图页	rk3568_mipi_hdmi			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	4 共 9
		V1.0	A3	LT	

PCIE30X2 M.2



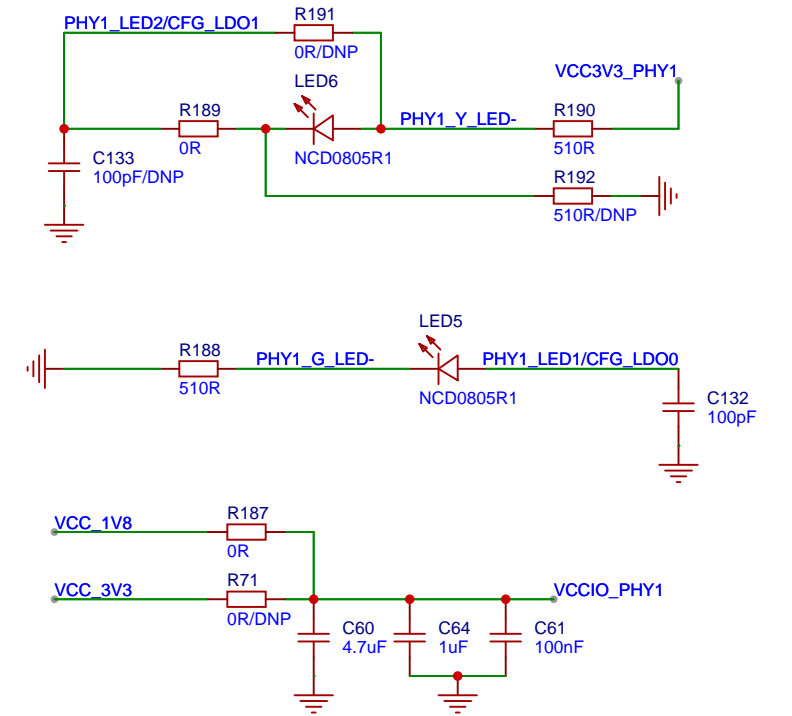
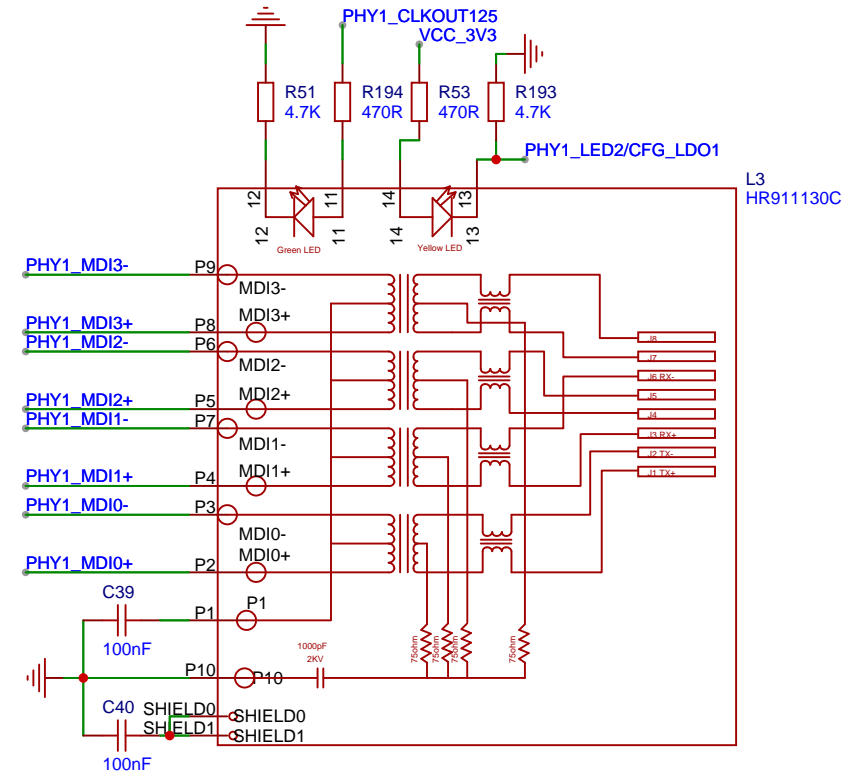
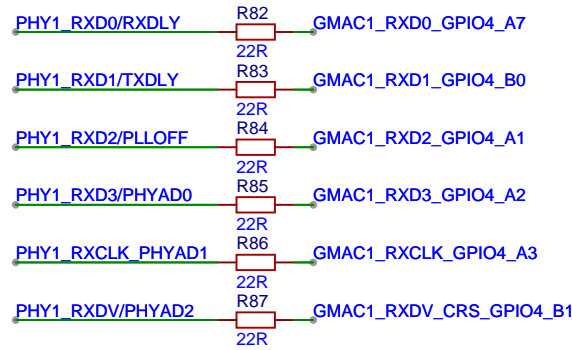
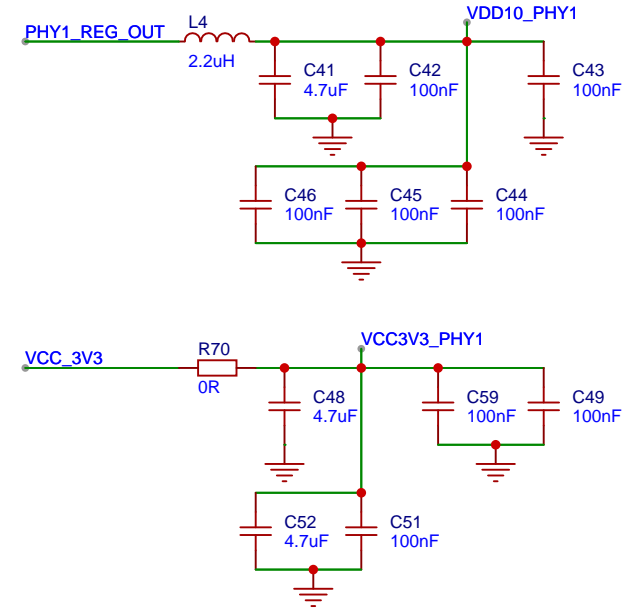
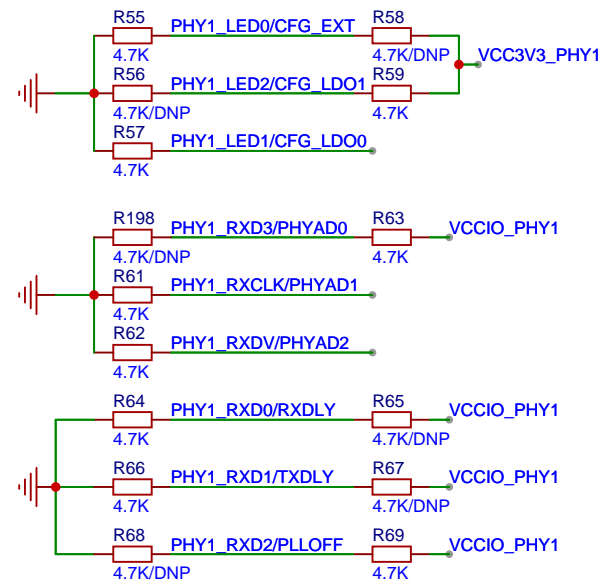
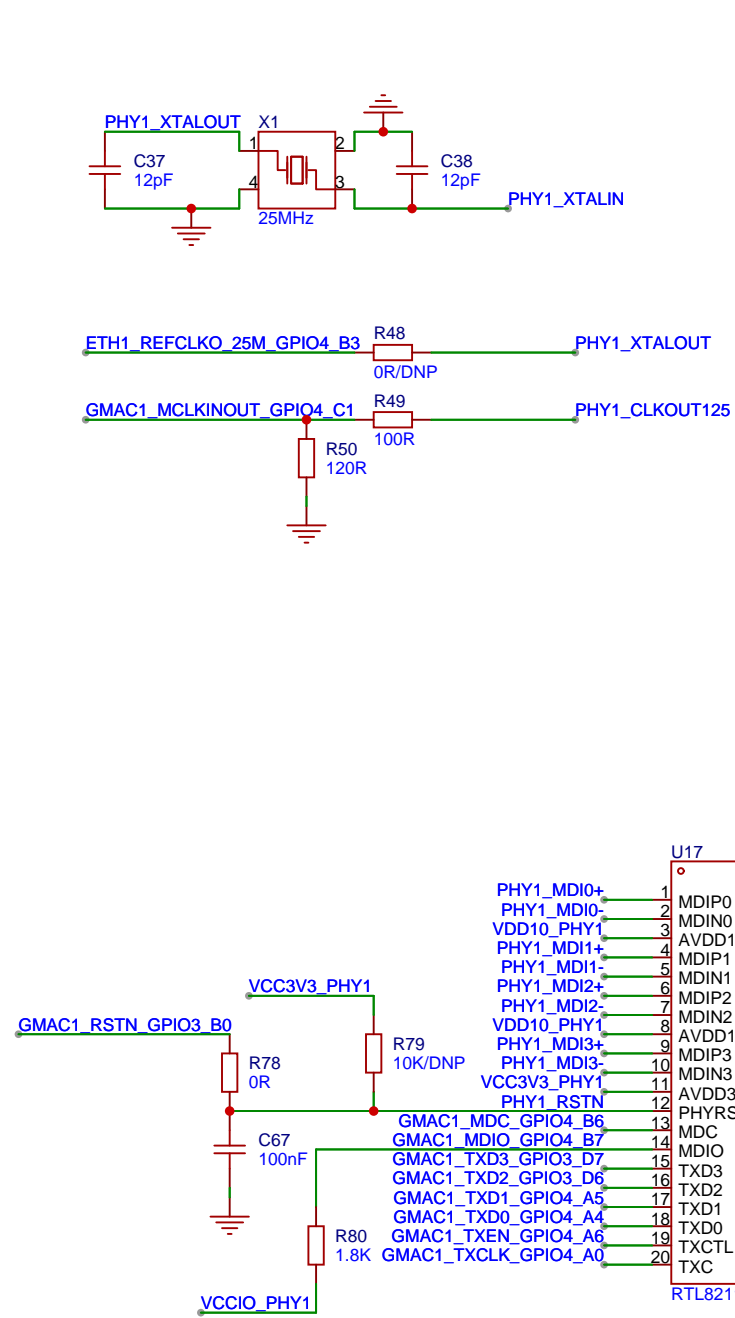
原理图	rk3568		更新日期	2024-08-11	
			创建日期	2024-08-07	
图页	rk3568_pcie30x2_m2		物料编码		
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	5 共 9
		V1.0	A3	LT	

WIFI BT



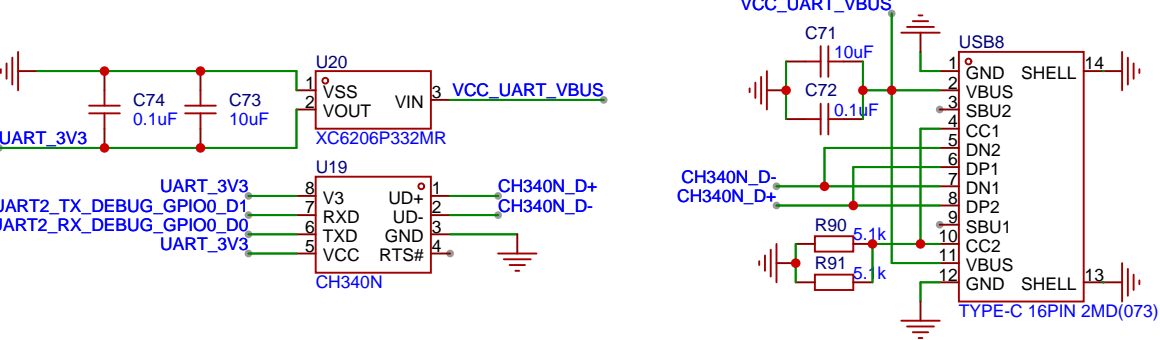
原理图	rk3568			更新日期	2024-08-11
				创建日期	2024-08-02
图页	rk3568_sdio_wifi_bt			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	6 共 9
		V1.0	A3	LT	

GMAC1 PHY

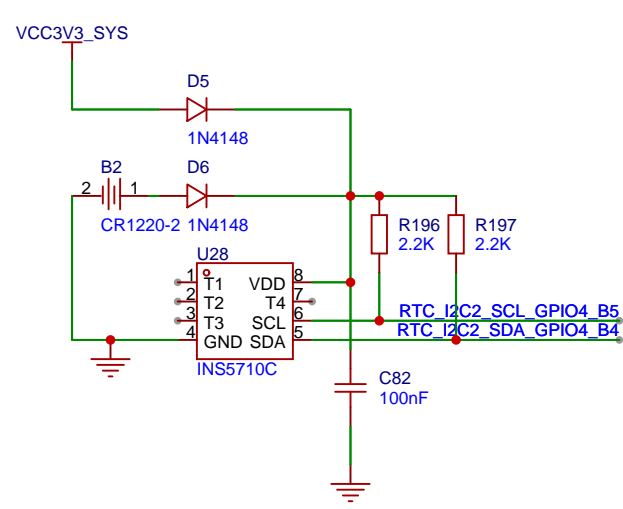


原理图	rk3568			更新日期	2024-08-11		
				创建日期	2024-08-02		
图页	rk3568_gmac1_phy			物料编码			
绘制	LT	rk3568_xc7a100t					
审阅							
		版本	尺寸	页	7	共	9
		V1.0	A3	LT			

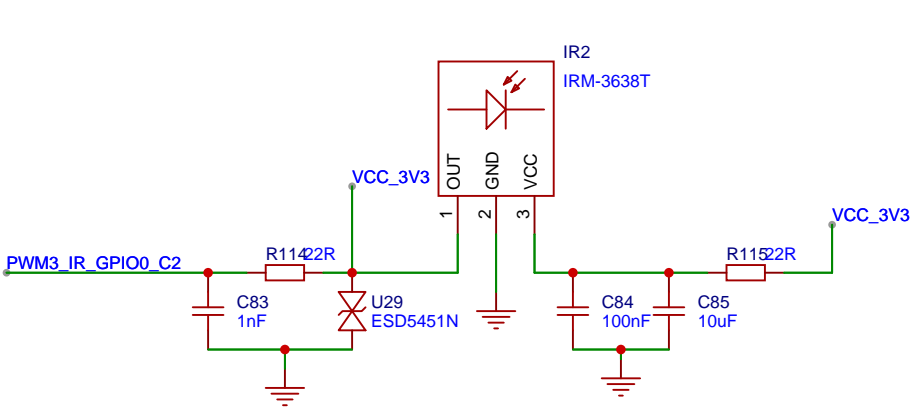
DEBUG UART



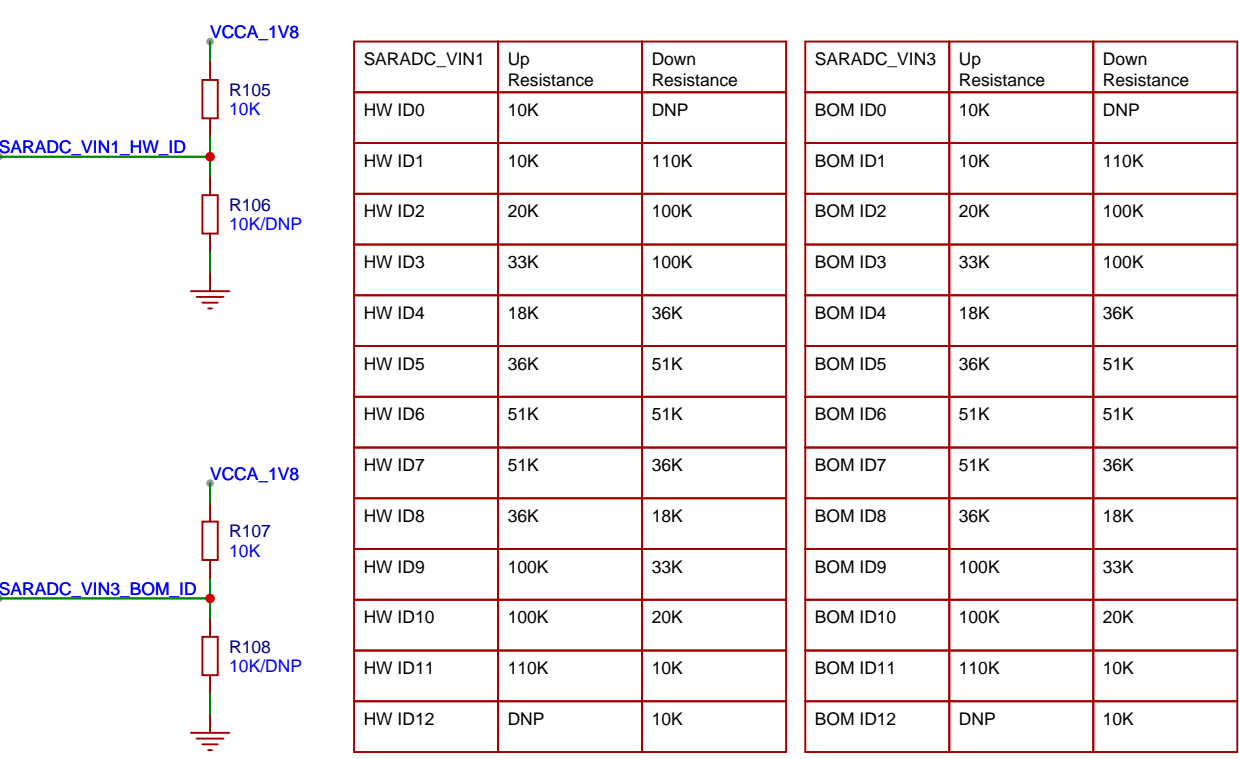
RTC IC



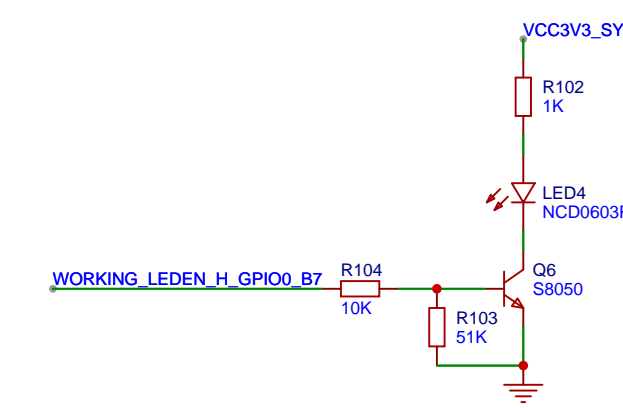
IR RECEIVER



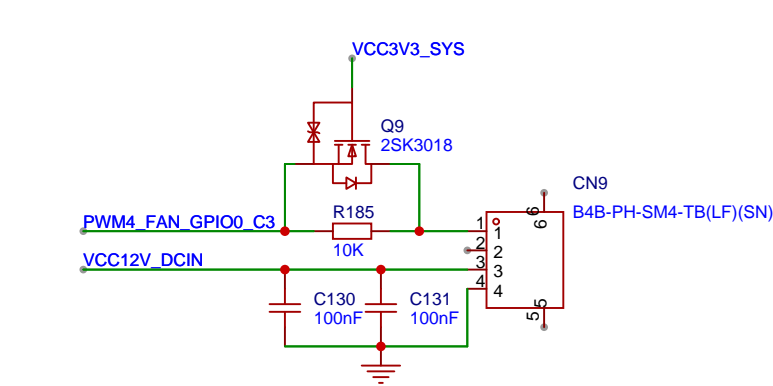
SARADC ID



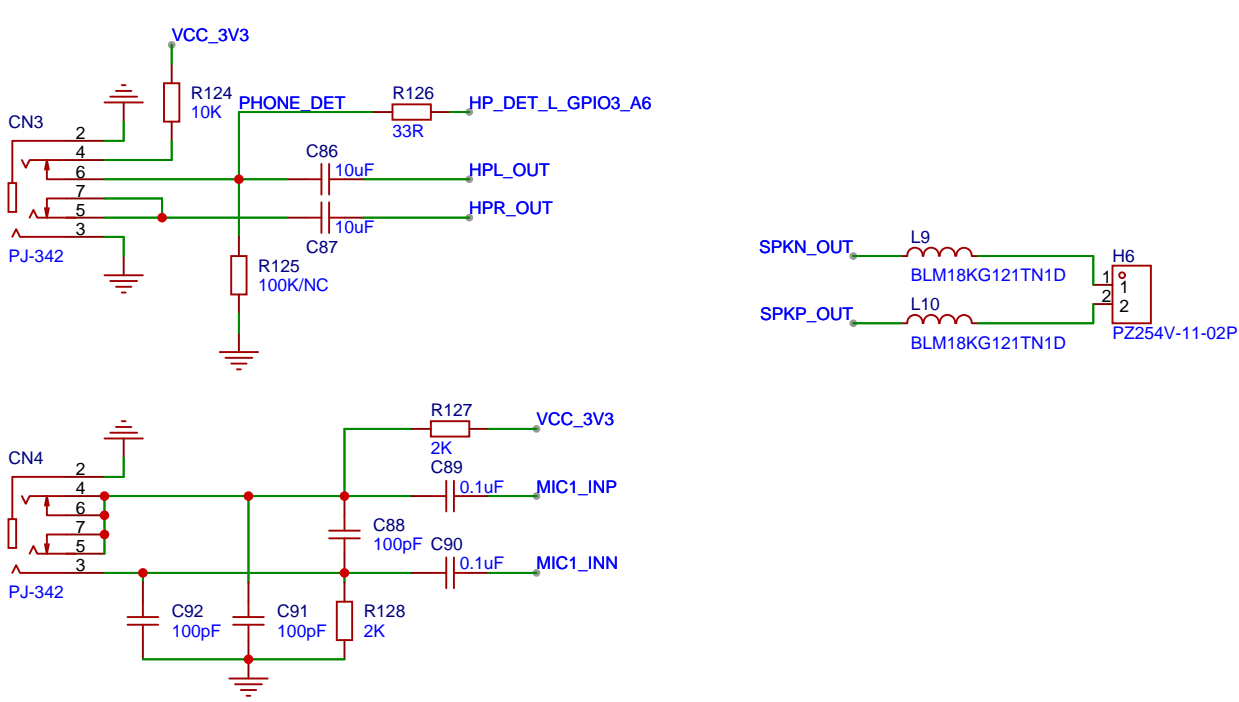
WORKING LED



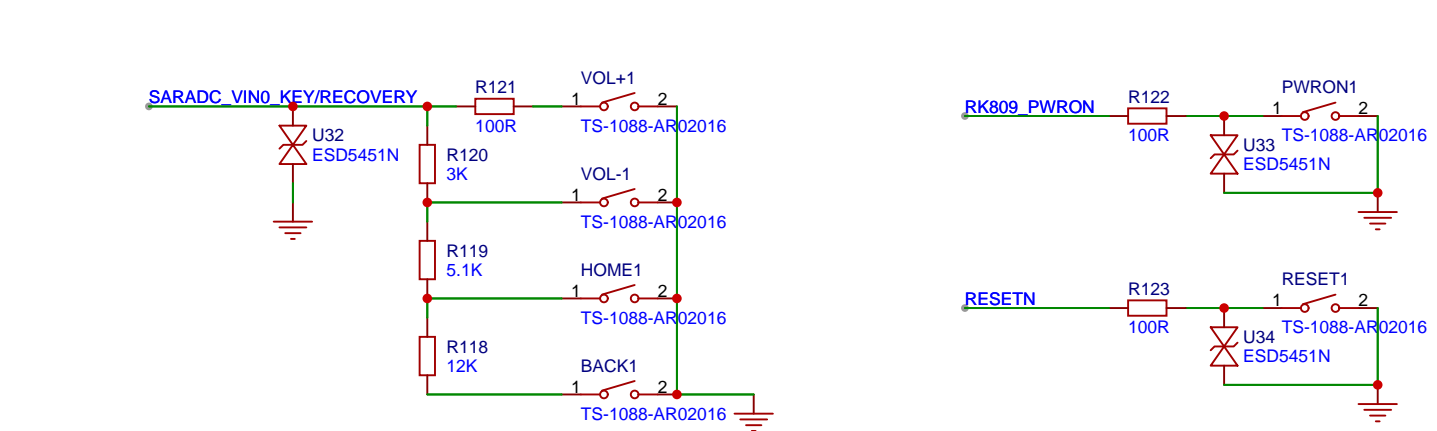
FAN



AUDIO

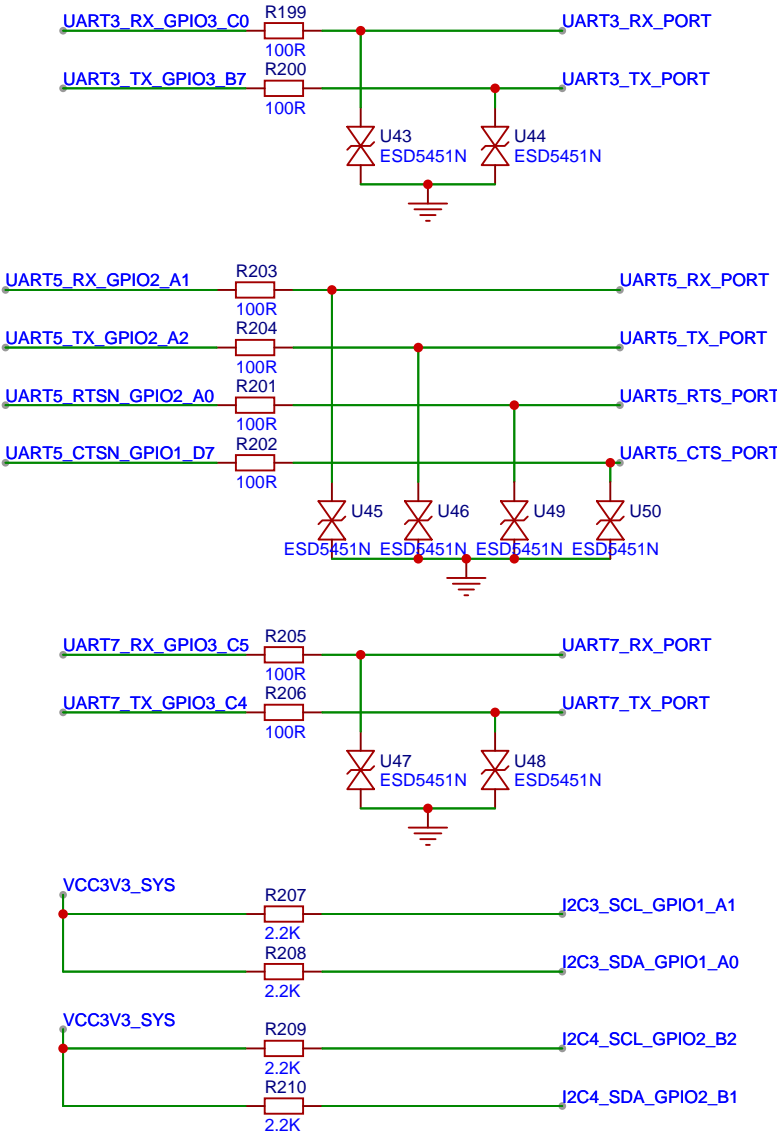
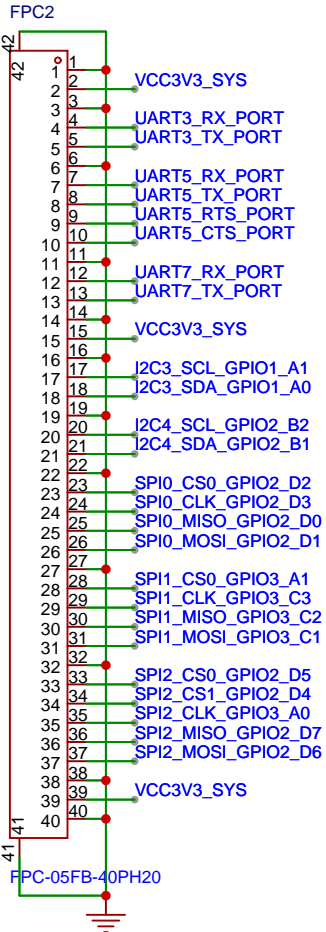
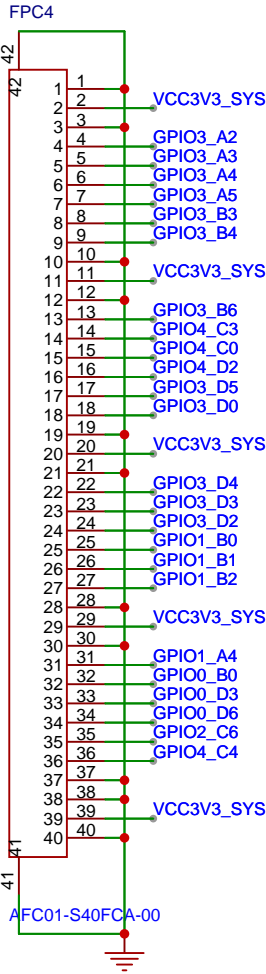


KEY

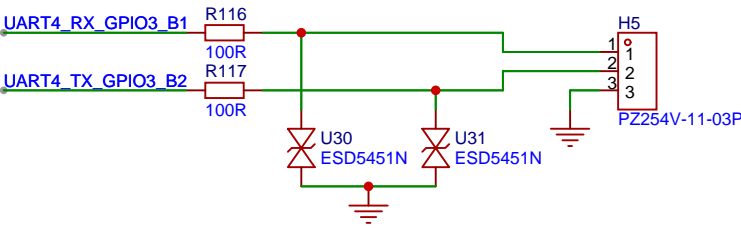


原理图	rk3568			更新日期	2024-08-11
				创建日期	2024-08-02
图页	rk3568_board_peripheral			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	8 共 9
嘉立创EDA		V1.0	A3	LT	

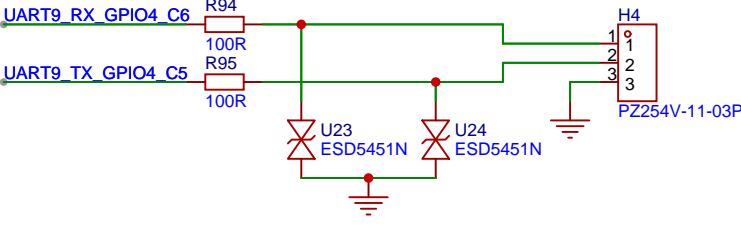
USER INTERFACE




UART4



UART9



原理图	rk3568			更新日期	2024-08-11
				创建日期	2024-08-02
图页	rk3568_user_interface			物料编码	
绘制	LT	rk3568_xc7a100t			
审阅					
		版本	尺寸	页	9 共 9
		V1.0	A3	LT	