ALEXANDER SOTO

786-271-6301 | http://alexander.soto.io | alexander@soto.io

EDUCATION

08.2008 – 12.2011

CARNEGIE MELLON UNIVERSITY • Pittsburgh, PA

Bachelor of Science in Electrical and Computer Engineering, Minor in Business Administration
University Honors • GPA: 3.63/4.00 • Eta Kappa Nu Honor Society, GEM Fellow, Boeing Scholar, Dean's List x3

LANGUAGES

Python, JavaScript, Java, C, Perl, Bash, MATLAB, Assembly (MIPS, x86-64), Verilog, VHDL, HTML5, and CSS3

EXPERIENCE

12.2011 – Present

TUNESSENCE • Pittsburgh, PA

Founder, CEO, and Software Engineer

- Founded a software company to build the Rosetta Stone of music.
- Raised $195,000 from investors including CMU and the AlphaLab accelerator program.
- Recruited, motivated, and led a team of six utilizing the scrum agile methodology.
- Conceived, designed, and developed interactive guitar teaching web application.
- Product included a sheet music editor, guitar tab editor, music score follower with polyphonic pitch detection, guitar tab player, streaming video, streaming audio, and a content management system for guitar lessons.
- Architected the application with my co-founder and personally coded large portions in JavaScript and Python.
- Wrote web scrapers and scripts to automate ad creation, leading to a 90% decrease in marketing costs.
- Responsible for system administration. Wrote Python scripts to automate building, testing, and deployment.
- Led product through multiple iterations based on customer feedback including UI/UX improvements.
- Attracted over 12,000 monthly unique visitors and over 1,000 registered users.
- Responsible for marketing, business development, investor relations, projections, accounting, and budgeting.

06.2011 – 08.2011

QUALCOMM • San Diego, CA

Digital Design and Emulation Engineering Intern

- Designed and implemented – in Verilog – the host FPGA of an emulation platform containing over 50 FPGAs.
- Created an interface that links the emulation platform to an x86 PC via PCI-E, decreasing FPGA configuration time by 95% and enabling remote capabilities, making the emulation machines accessible via the Internet.
- Wrote Linux drivers that control the PCI-E interface of the emulation system.
- Designed a thermal control system for the platform, which involved multiple internal and external sensors.
- Wrote a series of configurable Perl scripts to aid in verifying and debugging Verilog code.

05.2010 – 08.2010

NVIDIA • Santa Clara, CA

Hardware Application Engineering Intern

- Wrote a program to automatically test a GPU's thermal solution and compare it with reference designs.
- Determined unnecessary GPU tests, leading to a 40% decrease in test time with no loss in coverage.
- Characterized thermal performance of partner chassis designs with high performance GPUs.
- Determined the effect of varying fan speeds on a heat sink's thermal resistance to optimize cooling performance while maintaining reasonable acoustic levels.
- Worked on the implementation and testing of automatic overclocking software.

05.2009 – 08.2009

ABERDEEN TEST CENTER (U.S. DEPARTMENT OF DEFENSE) • Aberdeen, MD

Engineering Technician Intern

- Improved software - written in C - used for data acquisition by the Army in tanks and helicopters.
- Simplified data flow to enable error checking the file and wrote a simulator for more robust testing.
- Led the support of a video acquisition system and redesigned it for future iterations.
- Automated the reprogramming of FPGA based data collection systems through Linux scripts.
- Assembled and tested a prototype network data collection system. Helped train system's users at Fort Dix, NJ.

PROJECTS

MIPS Processor • *Introduction to Computer Architecture*

- Implemented a 5-stage pipelined MIPS processor. Includes forwarding, branch prediction, exception handling, user and kernel modes, virtual memory, and a TLB.
- Wrote a small kernel in assembly supporting system calls, exception handling, and TLB management.

FPGA Coprocessor • *Advanced Digital Design Project*

- Designed a system - Verilog and Linux drivers - that links an FPGA to a PC via PCI-E. Includes a DMA DDR2 controller and custom ISA. Enables software to speed up computationally expensive tasks on hardware.

Chess Bot • *Fundamental Data Structures and Algorithms*

- Wrote a chess AI in Java using alpha-beta pruning, iterative deepening, and transposition tables.