ALEXANDER M. SOTO

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EDUCATION

CARNEGIE MELLON UNIVERSITY — PITTSBURGH, PA
Bachelor of Science in Electrical and Computer Engineering — December 2011
Minor: Business Administration
Overall GPA: 3.63/4.00

WORK EXPERIENCE

QUALCOMM — SAN DIEGO, CA
Intern – Digital Design – Emulation Team — June 2011 – Aug. 2011

- Worked on designing a hardware emulation platform containing over 50 FPGAs.
- Designed and implemented – in Verilog – the host FPGA of the emulation platform.
- Created an interface that links the host FPGA to an x86 PC via PCI-E, which decreased overall FPGA configuration time by 95%.
- Enabled remote capabilities, making each machine accessible worldwide.
- Wrote Linux drivers that control the PCI-E interface of the emulation system.
- Designed the thermal control system of the emulation platform, which involved internal sensors on each FPGA as well as external sensors measuring ambient air temperature.
- Wrote a series of configurable Perl scripts to aid in verifying and debugging Verilog code.

NVIDIA — SANTA CLARA, CA
Intern - Hardware - Application Engineering — May 2010 – Aug. 2010

- Wrote a program to test customer's GPU fan settings to quickly compare thermal solutions with reference designs and tweak settings accordingly.
- Determined which GPU production tests were unnecessary, and relayed the information to the software department. Led to a 40% decrease in test time with no loss in coverage.
- Characterized thermal performance of partner chassis designs with high performance GPUs.
- Determined the effect of varying fan speeds on a heat sink's thermal resistance to optimize cooling performance while maintaining reasonable acoustic levels.
- Worked in the implementation and testing of automatic overclocking software.
- Characterized the power usage of applications run on the GPU, primarily scientific ones.

ABERDEEN TEST CENTER - U.S. DEPARTMENT OF DEFENSE — ABERDEEN, MD
Intern - Engineering Technician — May 2009 – Aug. 2009

- Improved software - written in C - used for data acquisition by the Army.
- Created a data buffer and simplified data flow to allow for error checking of the file.
- Wrote a simulator to test software improvements of the data acquisition system.
- Led the support of a video acquisition system and redesigned it for future iterations.
- Scripted the reprogramming of FPGA based data collection systems between tests.
- Assembled and tested a network data collection system based on a prototype design. Assisted in the training of this system at Fort Dix, NJ.

PROJECTS

FPGA for Lunar Rover Initiative, *Advanced Digital Design Project* — Fall 2011

- Accelerated vision algorithms used to locate a lunar rover in orbit by porting software to hardware.
- Created a modular system that interfaced an FPGA with a PC via PCI-E. Included an onboard DDR2 controller and custom instruction set.
- Wrote a Linux driver to facilitate communication between custom hardware and a PC.

MIPS Processor, *Introduction to Computer Architecture* — Spring 2011

- Implemented a 5-stage pipelined MIPS processor. Included forwarding, branch prediction, exception handling, virtual memory, and a cache with a custom TLB.
- Wrote an exception handler in assembly supporting system calls, page-faults, and more.

SKILLS

Programming Languages: C, Java, Python, Perl, JavaScript, C++, Verilog, and VHDL
Programs: Xilinx ISE, Cadence, MATLAB

HONORS

Eta Kappa Nu Honor Society, Member
GEM Fellow, The National GEM Consortium: 2011
Boeing Scholar, CMU - Department of Electrical and Computer Engineering: 2009
Dean's List, Carnegie Institute of Technology: Spring 2009, Spring 2010, Spring 2011