Pre-Lab Worksheet #5   NAME: _Alexander Williams_   LAB Section: B0__
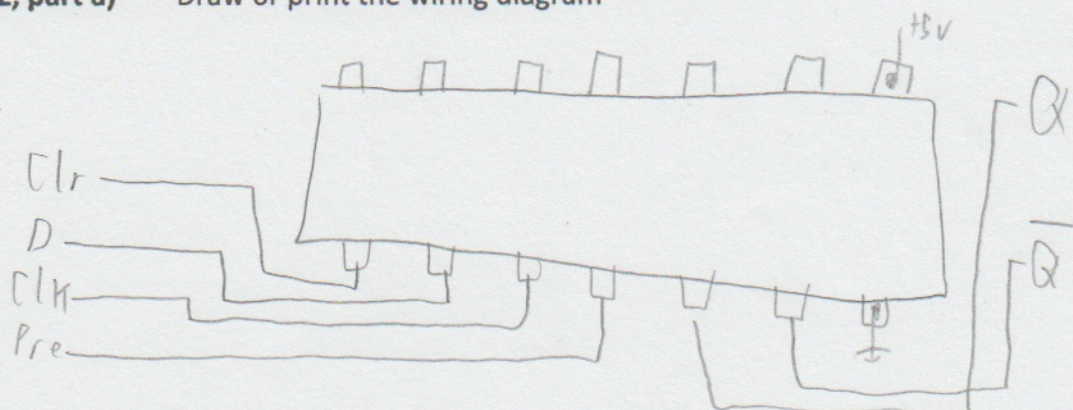
Pre-Lab 1, part a) Truth table:

C	S	R	Q	Q+
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	X

Pre-Lab 1, part b)   Draw or print the circuit constructed using one 7400.
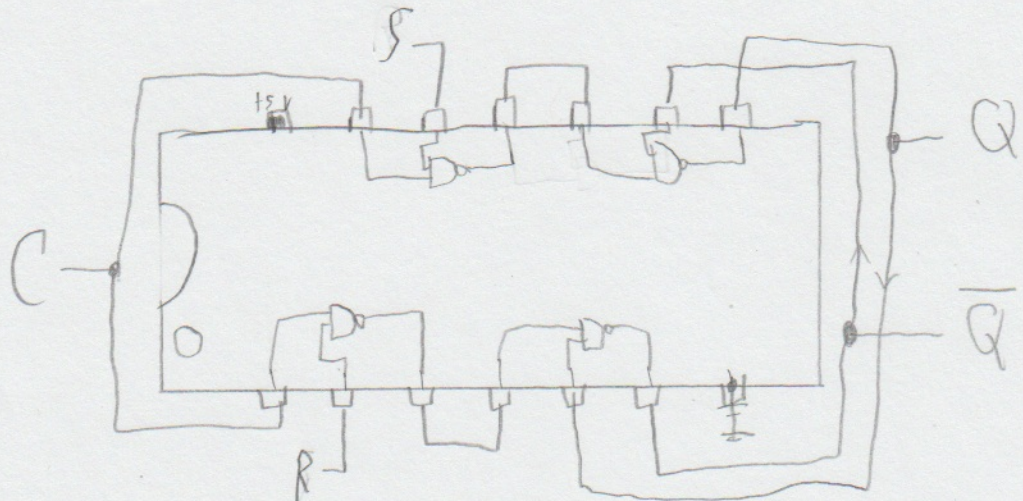
Pre-Lab 2, part a)   Draw or print the wiring diagram

Pre-Lab 2, part b)   Truth Table:

Preset	Clear	Clk	D	Q	Q+
0	0	0	0	0	X
			1	0	X
		1	0	0	X
			1	0	X
		0	0	0	1
	1		1	1	1
		1	0	0	1
			1	0	1
1	0	0	0	0	0
			1	0	0
		1	0	1	0
			1	0	0
	1	0	0	0	0
			1	0	1
		1	0	0	0
			1	0	1

Pre-Lab2, part c) Are the preset and clear inputs active **high** or active **low**? Explain your answer

both are active low, they only preset/clear when low

Pre-lab 3, part a)   Answers can be obtained from the data sheet for the 74192

➤ What values should be applied to the inputs of the counter to obtain the **CLEAR** function?

<u>MR</u>   What is the output that is expected from the counter when it is cleared? ___0___

➤ What values should be applied to the inputs of the counter to obtain the **LOAD** function?
MR, PL, both low
_____ What is the output that is expected from the counter when it is loaded?

<u>Value in Pn inputs</u>

➤ What values should be applied to the inputs of the counter to cause it to count down?
TC 2 : down
_____ What is the output that is expected from the counter when it is counting down?

one less then what it was

➤ Is this circuit a leading edge or trailing edge triggered counter? <u>leading edge</u>