

VHDL Quick-Start Templates!

Templates for most common VHDL components, ex: state machines, basic components, test benches, etc. Quickly get started while following a style guide recommended by Xilinx.

I have also included a [Demo](#) showing how these different templates can be used together to build a complex system in seconds.

Resources

Great place to get a good idea of proper VHDL coding practices

https://webdocs.cs.ualberta.ca/~amaral/courses/329/labs/VHDL_Guideline.html

The encyclopedia of VHDL. Large database with pretty much everything you need to know.

<https://www.ics.uci.edu/~jmoorkan/vhdlref/>

For the more interested...

This is a great explanation of the wonders of a 2-process VHDL entity, one being combinational and another being sequential. <https://www.gaisler.com/doc/vhdl2proc.pdf>

Templates

State Machine

Templates can be used for both Moore or Mealy finite state machines (FSMs).

Finite State Machines (FSM) are sequential circuit used in many digital systems to control the behavior of systems and dataflow paths. Examples of FSM include control units and sequencers. -Xilinx

[State Machine Template](#)

Asynchronous Entity

[Asynchronous Entity](#)

Synchronous Entity

[Synchronous Entity](#)

Entity Using Combinational Process

[Entity With Combinational Process](#)

Testbench

[Testbench](#)

Example Files/Useful Files

[Clock Frequency Divider](#)

Full-Scale Implementation

I have used the example files as a demonstration of what a complete digital design could look like. I will walk you through the following components and will explain how they all work together.

Note: this is not a tutorial but rather a walkthrough of an example of a complete digital design

State Machine: Central control unit for the digital system

Transmitter: Transmitter Unit

Receiver: Receiver Unit

Transmitter Clock (Frequency Divider): Divide central clock frequency for the transmitter unit

Timer: Timer used for state change in the state machine

System Link: File to import and link all different entities. This is the Unit Under Test (UUT) in the testbench.

Testbench: All design tests

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