

VHDL Quick-Start Templates!

Templates for most common VHDL components, ex: state machines, basic components, test benches, etc. Quickly get started while following a style guide recommended by Xilinx.

I have also included a [Demo](#) showing how these different templates can be used together to build a complex system in seconds.

Templates

State Machine

Templates can be used for both Moore or Mealy finite state machines (FSMs).

Finite State Machines (FSM) are sequential circuit used in many digital systems to control the behavior of systems and dataflow paths. Examples of FSM include control units and sequencers. -Xilinx

[State Machine Template](#)

Asynchronous Entity

[Asynchronous Entity](#)

Synchronous Entity

[Synchronous Entity](#)

Entity Using Combinational Process

[Entity With Combinational Process](#)

Testbench

[Testbench](#)

Example Files

[Clock Frequency Divider](#)

Full-Scale Implementation

I have used the example files as a demonstration of what a complete digital design could look like. I will walk you through the following components and will explain how they all work together.

Note: this is not a tutorial but rather a walkthrough of an example of a complete digital design

State Machine: Central control unit for the digital system

Transmitter: Transmitter Unit

Receiver: Receiver Unit

Frequency Divider: Divide central clock frequency for use with the transmitter and receiver units

Timer: Timer used for state change in the state machine

Testbench: All design tests

CURRENTLY WRITING