# Alex Ayling

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## Summary

Ph.D. candidate in Electrical Engineering at Caltech with 6+ years of hands-on experience in high-speed analog IC design, mm-wave and microwave RFIC design, phased arrays, and wireless systems. Led multiple successful chip tape-outs in 22 nm CMOS FDSOI, 28nm CMOS, 65nm CMOS, and 130nm SiGe BiCMOS. Direct experience designing and testing integrated circuits blocks such as phase shifters, frequency multipliers, mixers, amplifiers, power amplifiers, high-speed LO distribution, high-speed ESD protection, biasing, and custom digital blocks. Strong background in system-level design, EM modeling, wafer probing, RF module characterization, and system-level validation.

## Education

**PhD in Electrical Engineering**
California Institute of Technology — Expected Feb. 2026
Cumulative GPA: 3.6
Advisor: Professor Ali Hajimiri
Research: Scalable CMOS beamformer RFICs for mm-wave/microwave phased arrays.

**Master of Science in Electrical Engineering**
University of Illinois - Urbana Champaign — May 2020
Cumulative GPA: 3.75
Advisor: Professor Elyse Rosenbaum
Research: ESD Integrated circuit reliability.

**Bachelor of Electrical Engineering** — May 2018
**Minor in Mathematics** — May 2018
*With distinction*
University of Minnesota - Twin Cities
Cumulative GPA: 3.87
Honors: Dean's List Fall 2014 - Spring 2018. Iron Range scholarship recipient.
Advisor: Professor Keshab K. Parhi

## Skills

**Programs:** Cadence Virtuoso, Spectre, EMX, Momentum, HFSS, CST, ADS, Altium, Solidworks
**Computer Languages:** C / C++, SKILL, PERL, Python, MATLAB, VerilogA
**Technology Experience:** 16nm finFET, 22nm FDSOI**,** 65nm CMOS, 130nm SiGe BiCMOS
**Equipment:** High-speed oscilloscopes, spectrum analyzer, VNA, frequency extenders, phase-noise analyzer, semiconductor wafer probing, antenna range measurements, flip-chip bonder, wire bonding, transmission line pulse (TLP) measurements.

## Work Experience

**Graduate Research Assistant** Oct. 2020-present

*Caltech, Pasadena - CA*

- Independent research on RFIC topics related to scalable mm-wave and microwave phased arrays for communications, sensing, and wireless power transfer.
- Led two successful RFIC tape outs in 22nm CMOS FDSOI at D-band and X-band (see projects section.)

**High-Speed/mm-Wave ASICs Research Intern** May 2025-Aug 2025

*Nokia Bell Labs, New Providence - NJ*

- Designed an ultra-wideband mixer at D-band (110-170GHz) in IHP 130nm SiGe BiCMOS.
- Tape out submission expected November 2025.

**ESD Research Intern** May 2019-Aug 2019

*Analog Devices Inc, Wilmington - MA*

- Distributed ESD protection for high-speed data-converter frontends in 16nm finFET.
- Tape out of mis-trigger immune active feedback-based high-voltage tolerant ESD power clamp in 28nm bulk CMOS.

**Graduate Research Assistant** Aug. 2018-May 2020

*University of Illinois – Urbana-Champaign, Champaign - IL*

- Independent research on topics related to ESD protection of high-speed wireline I/O circuits.
- Led collaboration with Analog Devices Inc. investigating distributed ESD protection topologies for high-speed data converter front ends in 16nm finFET.
- Led two successful tape outs in 28nm CMOS and 65nm CMOS of ESD protection circuits.

## Projects

**Flexible and Scalable Arrays for Wireless Power Transfer Using Custom CMOS Beamformers**

- Lead chip designer managing a group of five PhD students.
- X-band (10GHz) beamformer integrates frequency synthesis (PLL), high-speed LO distribution, CMOS phase shifter, digital control, and power amplifier for 8-channels.
- Phase shifter self-calibrates with a delay-locked loop (DLL) to reduce phase error across PVT.
- Taped out in a 22nm CMOS FDSOI process.
- Wafer probing and connectorized measurements validating performance.
- Achieves a total DC-RF efficiency of 42% with 16.3dBm output power per channel.
- RFICs packaged and used in a 64-element, fully flexible phased array.
- Submitted to International Microwave Symposium 2026 (IMS2026.)

**Flip-Chip Aperture Coupled D-band Active Radiator Tiles in 22-nm CMOS FDSOI [1]**

- Developed the flip-chip aperture coupled antenna, which eliminates the need for costly transitions on/off chip at D-band, relaxing packaging requirements.
- Circuits (PA, LO buffer, frequency multipliers, phase-shifter etc.) designed in 22nm FDSOI and integrated with the antenna.
- Taped out and measured performance of the system on an mm-wave far-field range.
- Demonstrated a 2x4 array at D-band (140GHz) using two chips with 0.5λ-0.6λ element spacing. Achieved +23.5 dBm EIRP, a scan range of ±40˚, bandwidth of 128.8-143.5GHz, and a power dissipation of 77mW per element.

**Microwave Array for Power-transfer Low-orbit Experiment (MAPLE) [3]**

- Tested wireless power transfer in Low Earth Orbit (LEO) for 10 months.
- 32 element flexible X-band array driven by two custom RFICs in 6U CubeSat.

- First demonstration of complete wireless power transfer system in space.
- Detection on Earth using custom ground station (operational lead).
- Lead mechanical/thermal designer, lead embedded engineer, co-lead spacecraft operations, co-lead orbital tracking and ground station design.

**Sub-nanosecond Reverse Recovery Measurement for ESD Devices [9]**

- Developed a transmission line pulse (TLP) measurement for reverse recovery of ESD devices.
- Validated technique with 65-nm CMOS test structures.
- Developed a non-quasistatic diode model in VerilogA that accurately predicts reverse and forward recovery behavior of ESD diodes.

**High-voltage Tolerant ESD Rail Clamp in 28-nm Bulk CMOS [8]**

- Designed an ESD rail clamp in 28-nm bulk CMOS that uses active feedback to maintain conduction during ESD events.
- Tape out of test structures in 28-nm CMOS.
- Measured the ESD performance and mis-trigger immunity with TLP testing.

## Peer-Reviewed Publications

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Google Scholar Profile: Alex Ayling - Google Scholar

**Journal Articles**

[1] Alex Ayling, and Ali Hajimiri
Flip-Chip Aperture Coupled D-Band Active Radiator Tiles in 22-nm CMOS FDSOI
*IEEE Journal of Solid-State Circuits (JSSC), 2024.*
*https://doi.org/10.1109/JSSC.2024.3485062*

[2] Jesse Brunet, Alex Ayling, and Ali Hajimiri
Transmitarrays for Wireless Power Transfer on Earth and in Space
*IEEE Journal of Microwaves, 2024*
*https://doi.org/10.1109/JMW.2024.3459859*

[3] Alex Ayling*, Austin Fikes*, Oren S. Mizrahi*, Ailec Wu*, Raha Riazati, Jesse Brunet, Behrooz Abiri, Florian Bohn, Matan Gal-Katziri, Mohammed Reza M. Hashemi, Sharmila Padmanabhan, Damon Russell, and Ali Hajimiri.
Wireless power transfer in space using flexible, lightweight, coherent arrays
*Acta Astronautica, 2024*
*https://doi.org/10.1016/j.actaastro.2024.08.006*

**Conference Papers**

[4] Ailec Wu, Imaad Syed, Alex Ayling and Ali Hajimiri
On-Board Array Self-Calibration Using Amplitude-Only Proximal-Field Sensors and Machine-Learning-Based Phase Retrieval
2025 IEEE/MTT-S International Microwave Symposium - IMS 2025
https://doi.org/10.1109/IMS40360.2025.11103983

[5] Alex Ayling, and Ali Hajimiri
Fine Pitch D-Band Transmit Modules with Flip-Chip Aperture Coupled Antennas
*IEEE/MTT-S International Microwave Symposium - IMS 2024*
*https://doi.org/10.1109/IMS40175.2024.10600369*

[6] Austin Fikes, Eleftherios Gdoutos, Michael Kelzenberg, Alex Ayling, Oren S. Mizrahi, Jonathan Sauder, Charles Sommer, Alan Truong, Alexander Wen, Ailec Wu, Richard Madonna, Harry Atwater, Ali Hajimiri, and Sergio Pellegrino
The Caltech Space Solar Power Demonstration One Mission
*IEEE International Conference on Wireless for Space and Extreme Environments (WiSEE) 2022*
*Best paper in workshop award*
*https://doi.org/10.1109/WiSEE49342.2022.9926883*

[7] Alex Ayling, Ailec Wu, and Ali Hajimiri
Mutual Power Optimization of Photovoltaics and Wireless Power Transfer for Space Based Solar Power
*IEEE/MTT-S International Microwave Symposium - IMS 2022*
*https://doi.org/10.1109/IMS37962.2022.9865358*

[8] Alex Ayling, Javier Salcedo, Srivatsan Parthasarathy, Jean-Jacques Hajjar, and Elyse Rosenbaum
Balancing the Trade-off Between Performance and Mis-trigger Immunity in Active Feedback-based High-voltage Tolerant Power Clamps
*2020 42nd Annual EOS/ESD Symposium (EOS/ESD)*
*Balancing the Trade-off Between Performance and Mis-trigger Immunity in Active Feedback-based High-voltage Tolerant Power Clamps | IEEE Conference Publication | IEEE Xplore*

[9] Alex Ayling, Shudong Huang, and Elyse Rosenbaum
Sub-nanosecond Reverse Recovery Measurement for ESD Devices
*2020 IEEE International Reliability Physics Symposium (IRPS)*
*https://doi.org/10.1109/IRPS45951.2020.9129596*

[10] Alex Ayling, Satya Venkata Sandeep Avvaru, and Keshab Parhi
Not All Feed-Forward MUX PUFs Generate Unique Signatures
*2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*
*https://doi.org/10.1109/ISVLSI.2019.00017*