

ALEX B ELENJIMATTOM

SR. ASIC DESIGN VERIFICATION ENGINEER, INDIA

EXPERIENCES

NVIDIA Graphics Pvt Ltd - Senior ASIC Verification Engineer - 8 years

□ Bangalore, India)

- Experience in Computer Architecture, Dynamic Recompilation Micro-code validation, Silicon Debug, CPU Boot Validation on FPGA and Functional Simulator, Silicon Bring-up, Post Silicon Testing and Debug, System level DV for Memory Subsystem, Block level DV for CPU Runahead feature, Unit DV for Runahead, Unit DV for L1 Cache, UVM, System Verilog, RTL debug, DV effort estimation, test planning and execution

PROJECTS

Orin and Future CPU

RTL Perf, Unit DV - UVM

- Ongoing Project for future CPU - Developing testplan and testbench infrastructure from scratch using UVM for CPU L1 Cache Verification
- Owned testbench enhancement for System Coherency Fabric performance testing on RTL using UVM for Orin

Future CPU

OOO CPU performance on Perf Model simulator

- Developed native instruction snippets to exercise interesting performance scenarios to help architect the latest CPU

Xavier

Silicon Bringup, Silicon Testing

- Travelled to Santa-Clara office and did first silicon sample bring-up and silicon debug
- Silicon Bringup owner for level one native stimulus planning and testing for CPU
- Silicon debug across various CPU core units, root caused the issues to RTL / Dynamic Recompiler code / stimulus bugs using in-house silicon debug tools

Xavier

Block(Core) level Runahead Feature Verification Owner, Memory Unit and L1 Cache DV - UVM

- Block(CPU Core) level Runahead feature verification Lead for a transactional memory model CPU
- Developed and executed Runahead feature verification testplan at block level (Core)
- Executed runahead feature verification at memory unit (Ld/St execution unit and L1 cache)

Tegra X2

System level DV, MicroCode Validation, Micro Architectural Boot Verification on FPGA and Silicon, Silicon Bringup

- Testplan execution for the Memory Subsystem Design Verification on SOC for CPU transactions, including test writing, and failure debug on RTL
- Validation of dynamic recompilation software used in Denver2(Transactional memory model machine with Dynamic recompilation in HW), using constrained random ARM assembly code generators
- The 6 core (2 Denver2 and 4 A57) SOC supported a bunch of CPU configurations using a complex boot sequence (micro Architectural boot for the dynamic re-compiler and ARM Architectural boot), validated the boot sequence on functional simulators and FPGA
- Silicon Bring-up planning and execution on FPGA and Silicon, brought up the CPU on Day0

Denver

ARM-v8 Architectural Compliance, Silicon Bring-up, Post-Silicon Testing - PERL and Shell Scripting

- Worked with ARM - Bangalore to get ARM architectural compliance for Denver, was responsible for driving the team to get 100% ARMv8-A architectural compliance across functional simulators and RTL runs
- Automated the ARM Compliance Suite Build, Release and Regression infrastructure to reduce the turnaround (ARM code drop to Nvidia Simulator run) time from 20-man days to 5-man days by enhancing the infrastructure
- Involved in test planning and execution of Silicon Bringup and testing for the first in house 64 bit ARMv8 CPU
- Setup 40 Silicon machine farm machines and LSF infrastructure using Perl, enabled entire CPU team engineers to get remote time-shared access to the limited number of silicon samples, during early Silicon bringup

M-Tech Projects in IIT Roorkee

IIT Roorkee

- Completed 4 projects on Machine Learning - Type 2 Fuzzy Logic for Classification and Control Problems
- Implemented ML solutions on Nvidia Tesla-C1060 GPGPU using CUDA v3.2 and obtained 60X to 200X fastness on Matlab simulations using GPGPU Vs High performance CPU

CONTACT INFO

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EDUCATION

- [Indian Institute of Technology](#), Roorkee - India, 2009 - 2011
M-Tech in System Engg and Operations Research - CGPA 9.2/10
- [Mar Athanasius College of Engineering](#), Kerala - India, 2005 - 2009
B-tech in Electrical and Electronics Engineering

SKILLS

- Design Verification
- UVM
- System Verilog
- Verification Planning and Effort Estimation
- Computer Architecture, CPU Cache and Memory Architecture
- HW-SW interaction - Dynamic Recompilation in HW
- Debugging - RTL, Functional Simulator, Silicon, Chip Bring-up
- Perl, Unix, Shell, Perforce, Deep Learning

COURSES

[Dulos - UVM Adopter Course](#)

[Coursera - Deep Learning Specialization](#)

- [Neural Networks and Deep Learning](#)
- [Improving Deep Neural Networks: Hyperparameter tuning, Regularization and Optimization](#)
- [Structuring Machine Learning Projects](#)
- [Convolutional Neural Networks](#)
- [Sequence Models](#)