ALEX B ELENJIMATTOM

SENIOR VERIFICATION ENGINEER, CANADA

EXPERIENCES

2011
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2024

NVIDIA Graphics Pvt Ltd - Senior ASIC Verification Engineer - 13 years

☐ Calgary-Remote, Canada (2023 May to April 2024), Bangalore - India (2011-2023))

- Experience in CPU RTL Performance Verification, SOC coherent interconnect RTL Performance Verification, UVM/System Verilog, Unit DV for CPU L1 cache, Unit DV for CPU Runahead feature, Block level feature verification owner for Runahead, System level DV for Memory Subsystem, DV effort estimation - test planning and execution, CPU Boot Validation on FPGA and Functional Simulator, Silicon Bring-up, Post Silicon Testing and Debug, RTL de-bug, Computer Architecture, Dynamic Recompilation Micro-code validation

PROJECTS

April '24
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Aug '20

Drive Thor- Nvidia AI chip for cars

UCF RTL Performance Verification Lead for Atlan and Thor

- Performance verification Lead for CPU and SOC coherent interconnect (UCF) Performance verification on RTL
- Responsible for pre-silicon fabric performance test planning, phasing, and execution, leading a team of 15 engineers
- Worked on RTL performance verification for NVIDIA's automobile tegra products Orin, Dane and Atlan, Thor

Aug '20
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Aug '18

Orin and ARM CPU

RTL Perf, Unit DV - UVM

- Developing test plan and testbench infrastructure from scratch using UVM for CPU L1 Cache Verification for in-house ARM CPU
- Responsible for verification of critical features like Snoops, Evictions, Load Victim Tags, Barrier uops (test plan, tb-infra, feature bring up, feature accept, coverage closure) at L1 Cache Unit Testbench
- Owned testbench enhancement for System Coherency Fabric performance testing on RTL using UVM for Orin

Jul '18
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May '18

CPU [Nvidia Internal]

OOO CPU performance on Perf Model simulator

- Developed native instruction snippets to exercise interesting performance scenarios to help architect the latest CPU

Apr '18
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Dec '17

Xavier

Silicon Bringup, Silicon Testing

- Travelled to Santa-Clara office and did first silicon sample bring-up and silicon debug
- Silicon Bringup owner for level one native stimulus planning and testing for CPU
- Silicon debug across various CPU core units, root caused the issues to RTL / Dynamic Recompiler code/stimulus bugs using in-house silicon debug tools

2017
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2015

Xavier

Block(Core) level Runahead Feature Verification Lead, Memory Unit and L1 Cache DV - UVM

- Block(CPU Core) level Runahead feature verification Owner for a transactional memory model CPU
- Developed and executed Runahead feature verification testplan at block level (Core)
- Executed Runahead feature verification at memory unit (Ld/St execution unit and L1 cache)

2015
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2013

Tegra_X2

System level DV, MicroCode Validation, Micro Architectural Boot Verification on FPGA and Silicon, Silicon Bringup

- Testplan execution for the Memory Subsystem Design Verification on SOC for CPU transactions, including test writing, and failure debug on RTL
- Validation of dynamic recompilation software used in Denver2(Transactional memory model machine with Dynamic recompilation in HW), using constrained random ARM assembly code generators
- The 6-core (2 Denver2 and 4 A57) SOC supported a bunch of CPU configurations using a complex boot sequence (micro Architectural boot for the dynamic re-compiler and ARM Architectural boot), validated the boot sequence on functional simulators and FPGA
- Silicon Bring-up planning and execution on FPGA and Silicon, brought up the CPU on Day0

2013
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2011

Denver

ARM-v8 Architectural Compliance, Silicon Bring-up, Post-Silicon Testing - PERL and Shell Scripting

- Worked with ARM - Bangalore to get ARM architectural compliance for Denver, and was responsible for driving the team to get 100% ARMv8-A architectural compliance across functional simulators and RTL runs
- Automated the ARM Compliance Suite Build, Release, and Regression infrastructure to reduce the turnaround (ARM code drop to Nvidia Simulator run) time from 20-man days to 5-man days by enhancing the infrastructure
- Involved in test planning and execution of Silicon Bringup and testing for the first house 64 bit ARMv8 CPU
- Setup 40 Silicon machine farm machines and LSF infrastructure using Perl, enabling entire CPU team engineers to get remote time-shared access to the limited number of silicon samples, during early Silicon bringup

2011
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2009

M-Tech Projects in IIT Roorkee

IIT Roorkee

- Competeled 4 projects on Machine Learning - Type 2 Fuzzy Logic for Classification and Control Problems
- Implemented ML solutions on Nvidia Tesla-C1060 GPGPU using CUDA v3.2 and obtained 60X to 200X fastness on Matlab simulations using GPGPU Vs High performance CPU

CONTACT INFO

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EDUCATION

- **Indian Institute of Technology**, Roorkee - India, 2009 - 2011
  M-Tech in System Engg and Operations Research - CGPA 9.2/10

- **Mar Athanasius College of Engineering**, Kerala - India, 2005 - 2009
  B-tech in Electrical and Electronics Engineering

SKILLS

- Design Verification
- UVM
- System Verilog
- Verification Planning and Effort Estimation
- Computer Architecture, CPU Cache and Memory Architecture
- HW-SW interaction - Dynamic Recompilation in HW
- Debugging - RTL, Functional Simulator, Silicon, Chip Bring-up
- Perl, Unix, Shell, Perforce, Deep Learning

COURSES

Dulos - UVM Adopter Course

Coursera - Deep Learning Specialization

- Neural Networks and Deep Learning
- Improving Deep Neural Networks: Hyperparameter tuning, Regularization and Optimization
- Structuring Machine Learning Projects
- Convolutional Neural Networks
- Sequence Models