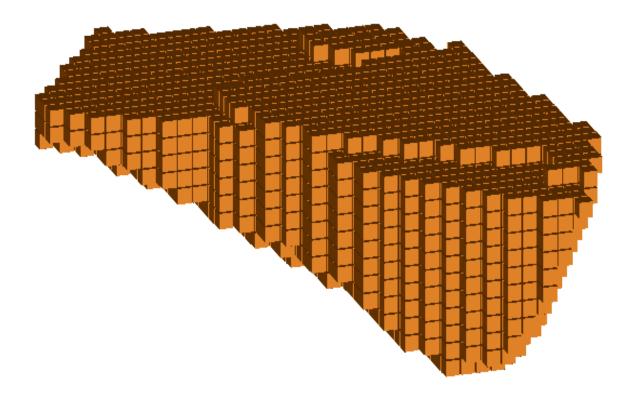


# MiningMath Associates

# **Dense Cholesky CUDA implementation**

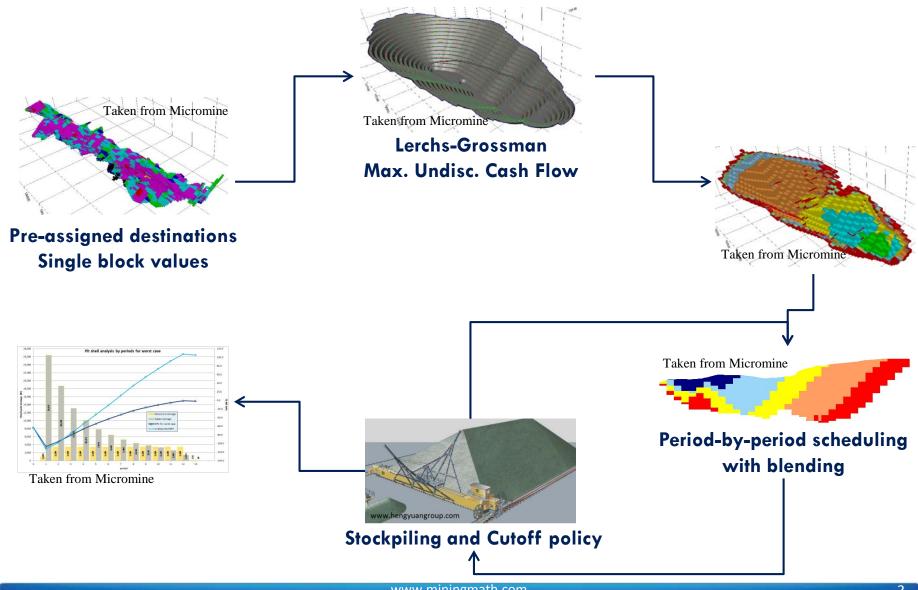


## **Block Model**



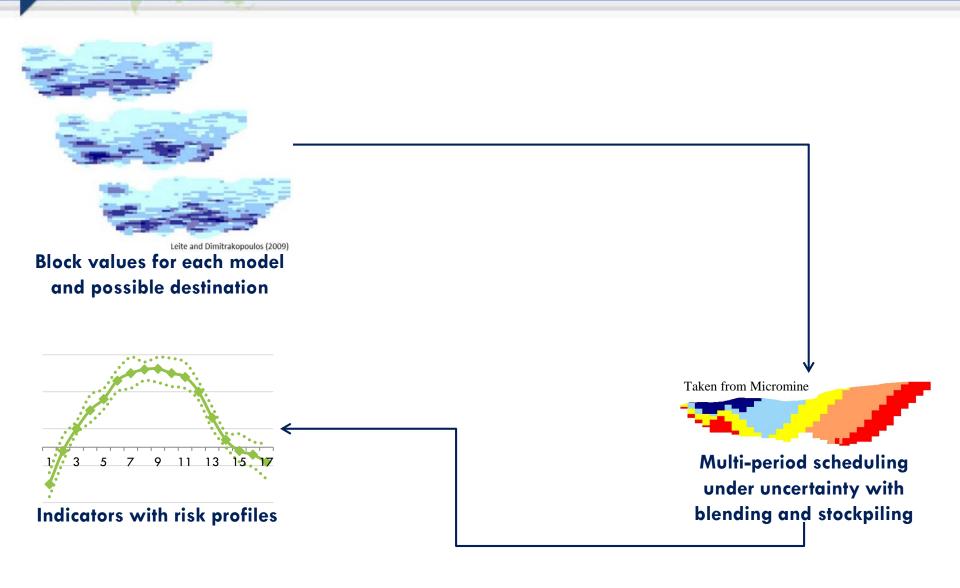


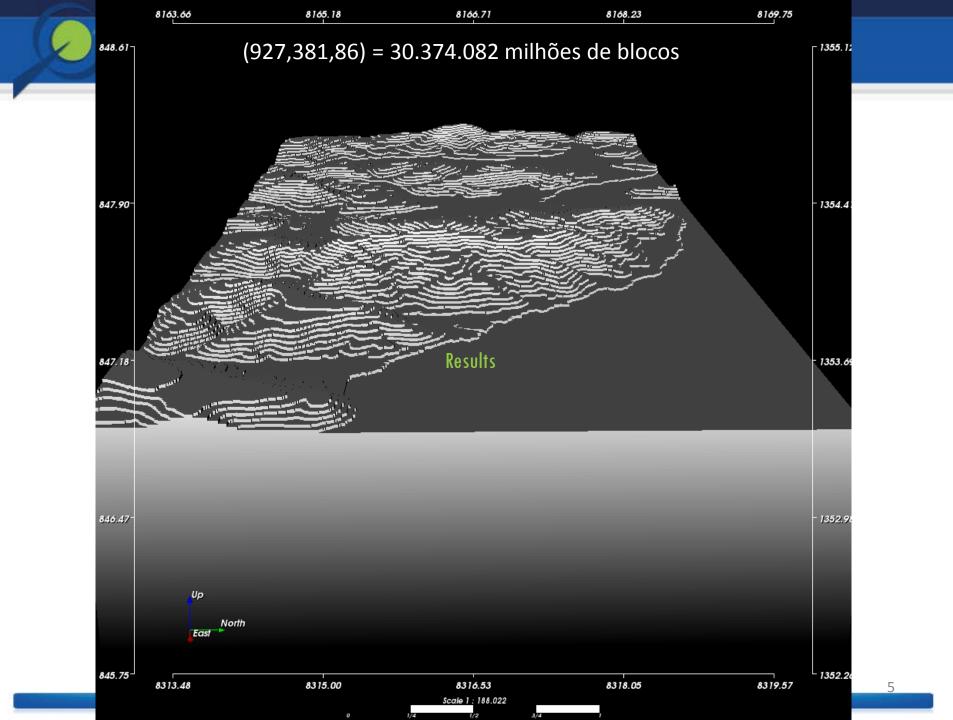
### The current state of the mine planning technology

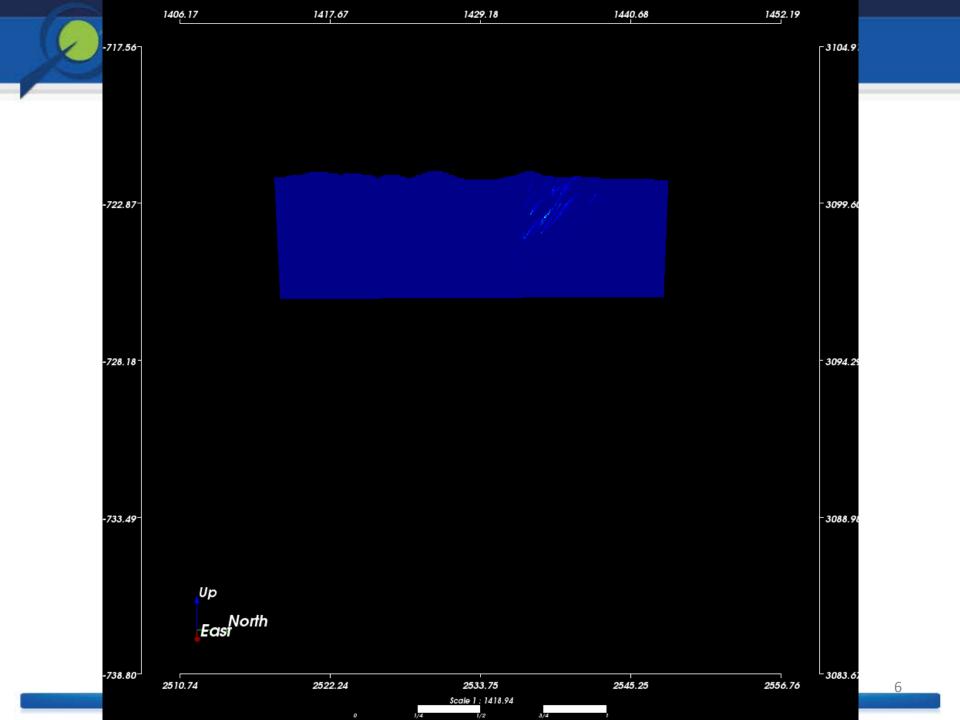


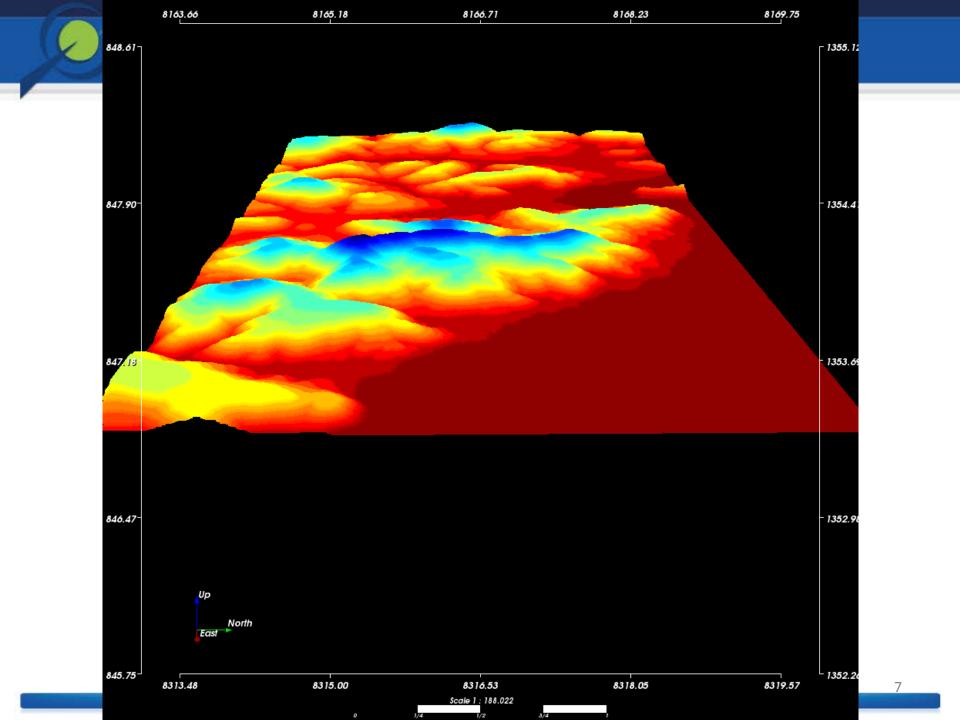


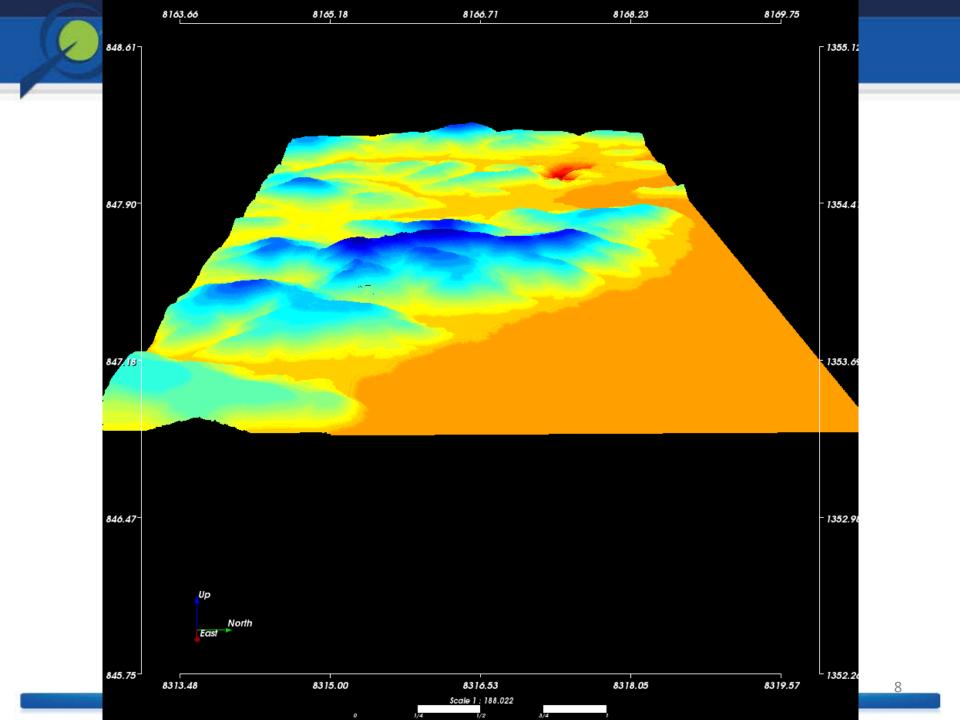
#### Mine planning using SimSched Direct Block Scheduler

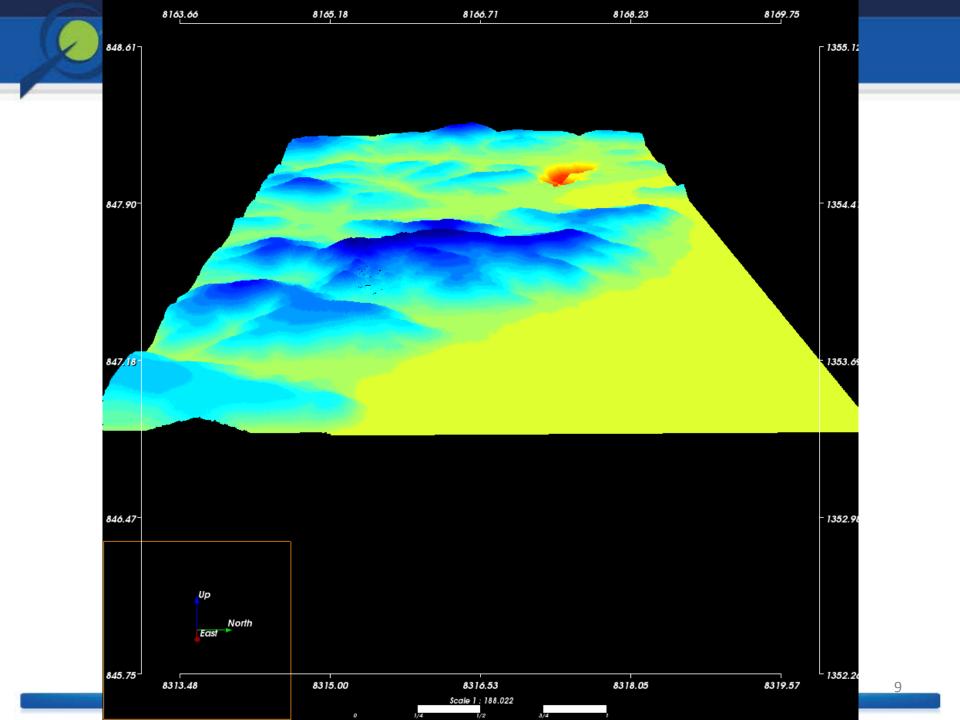


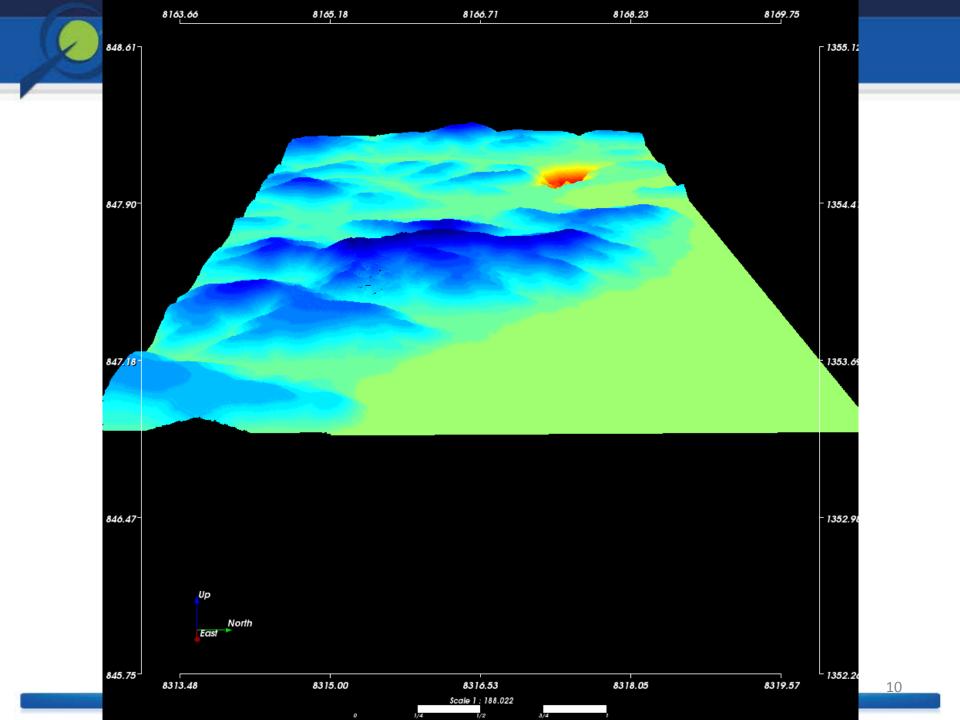


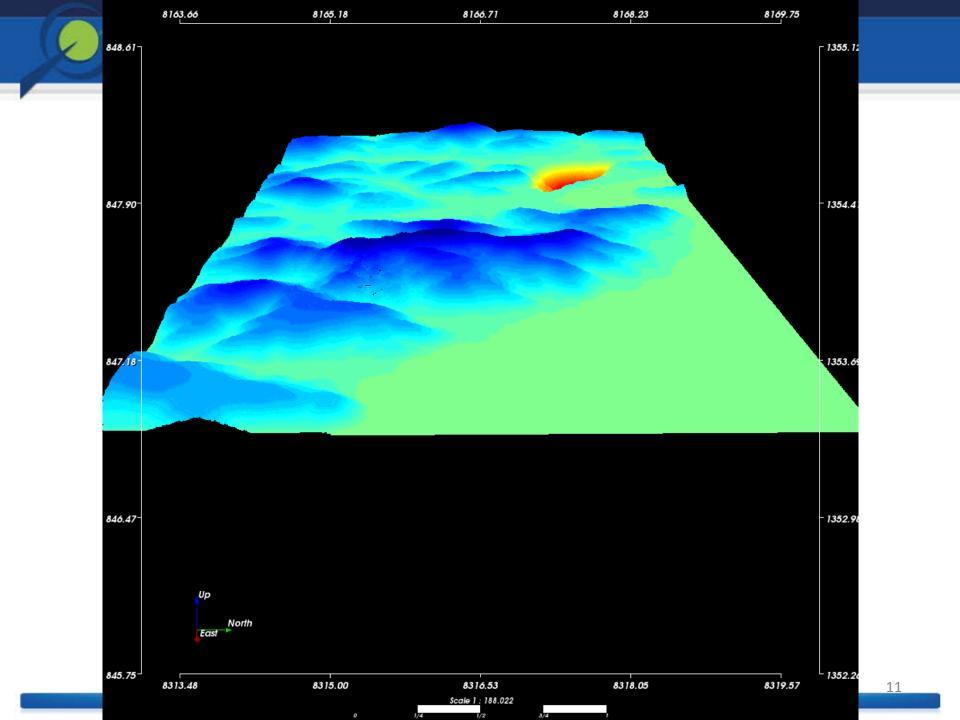


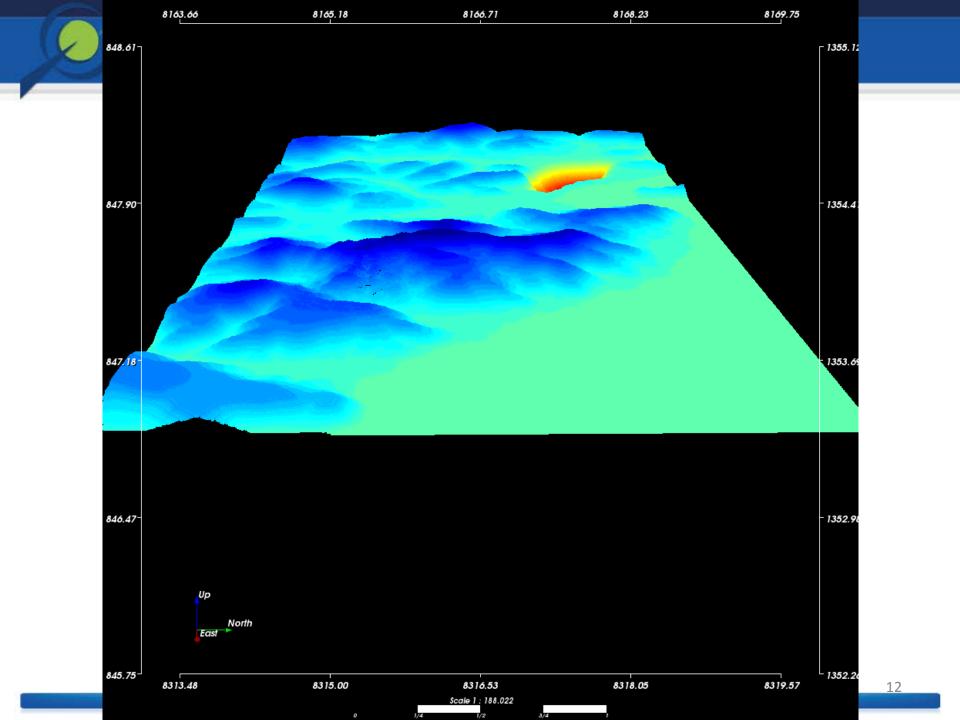


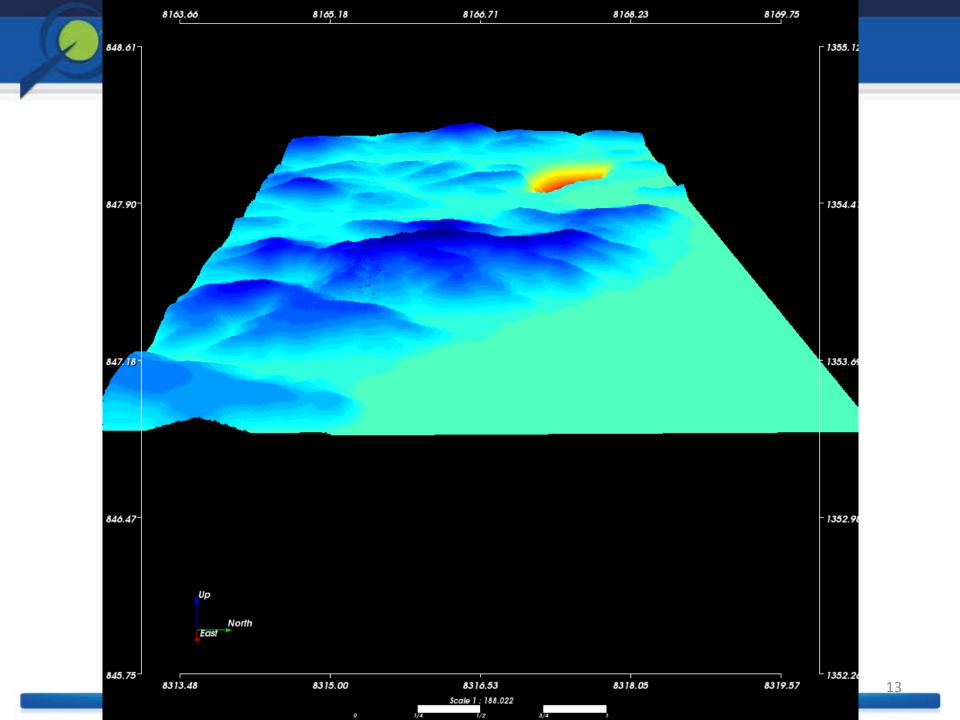


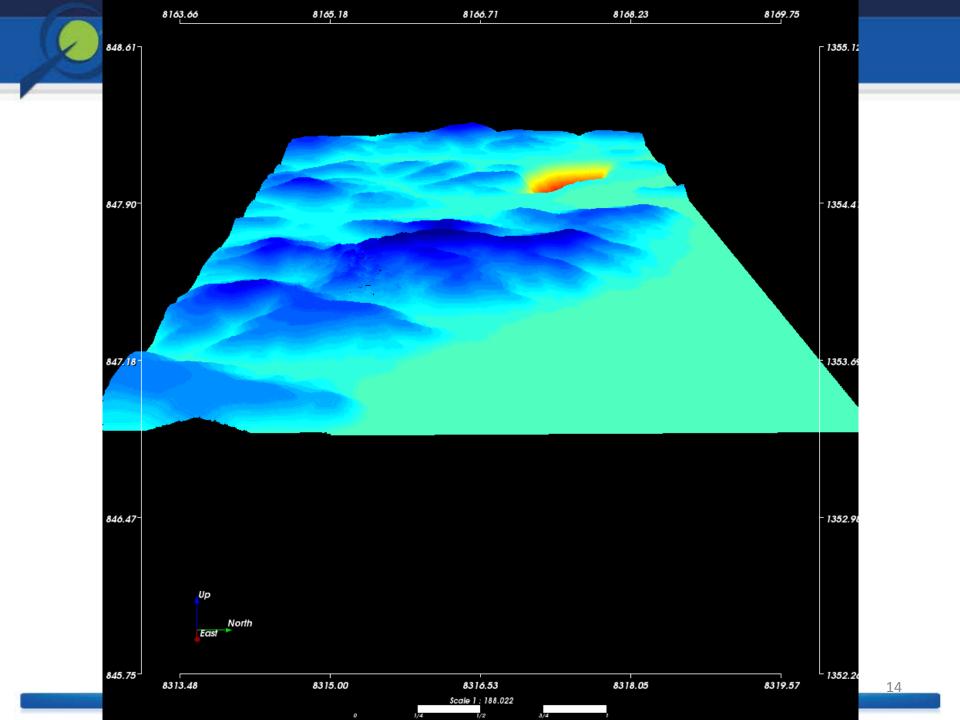


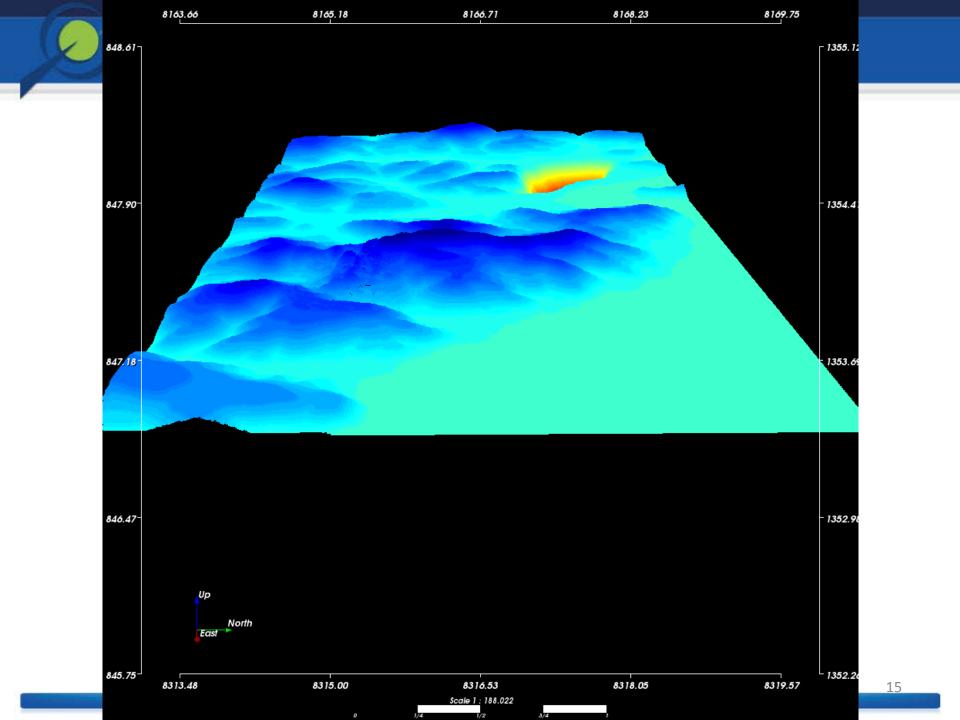


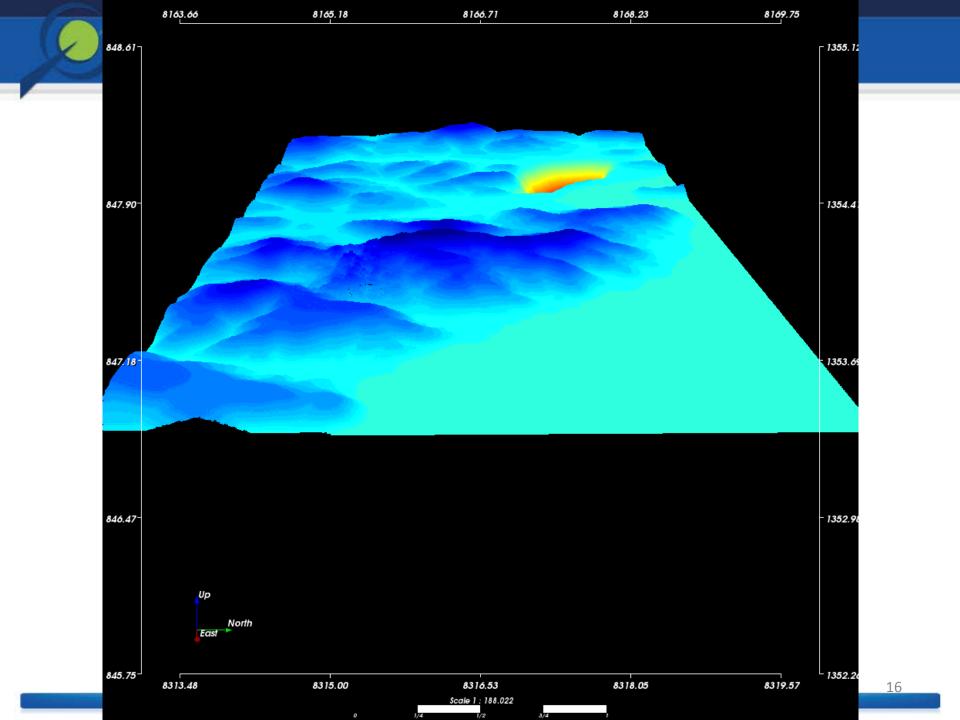


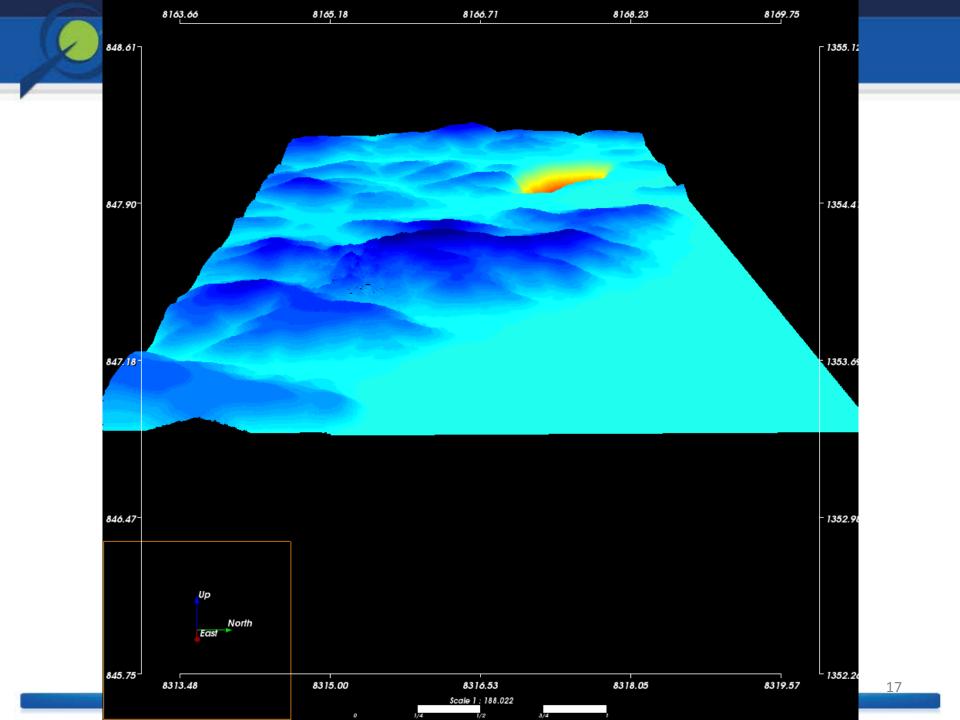


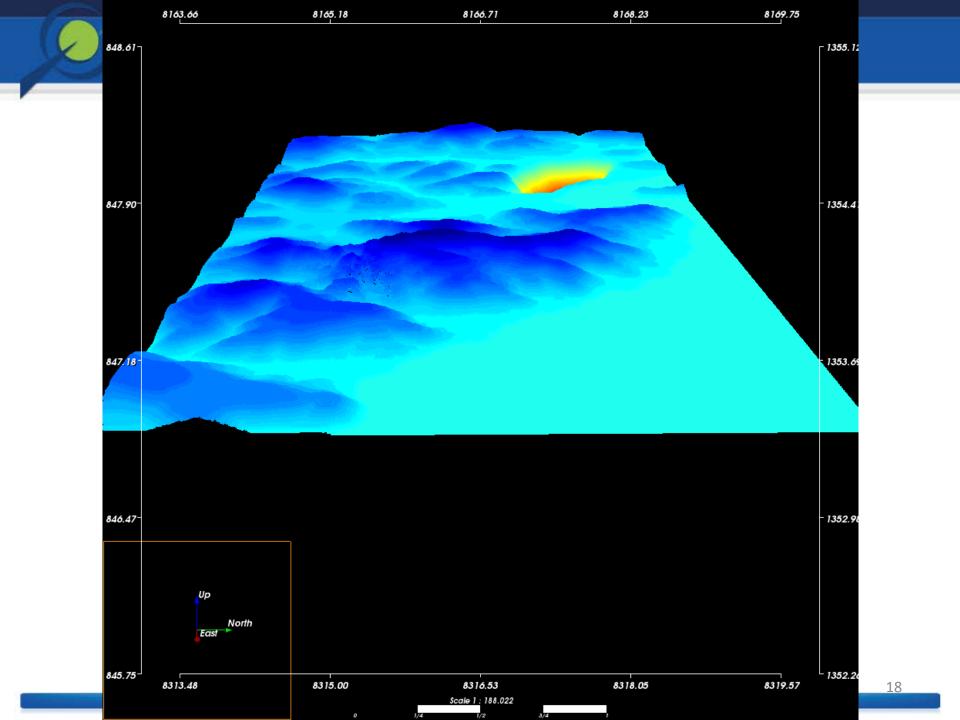


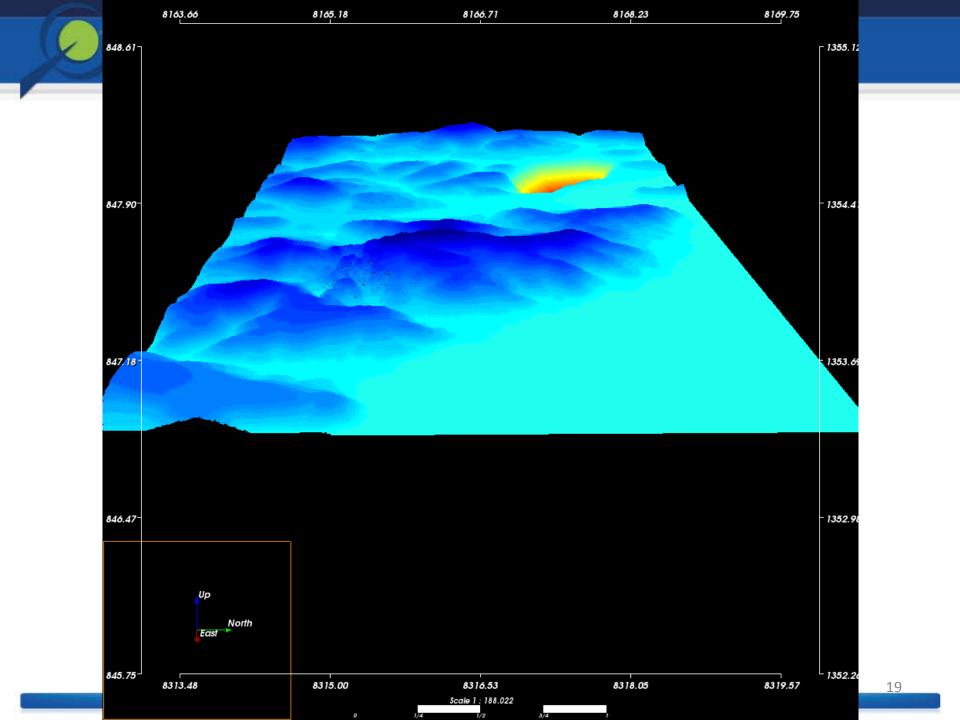


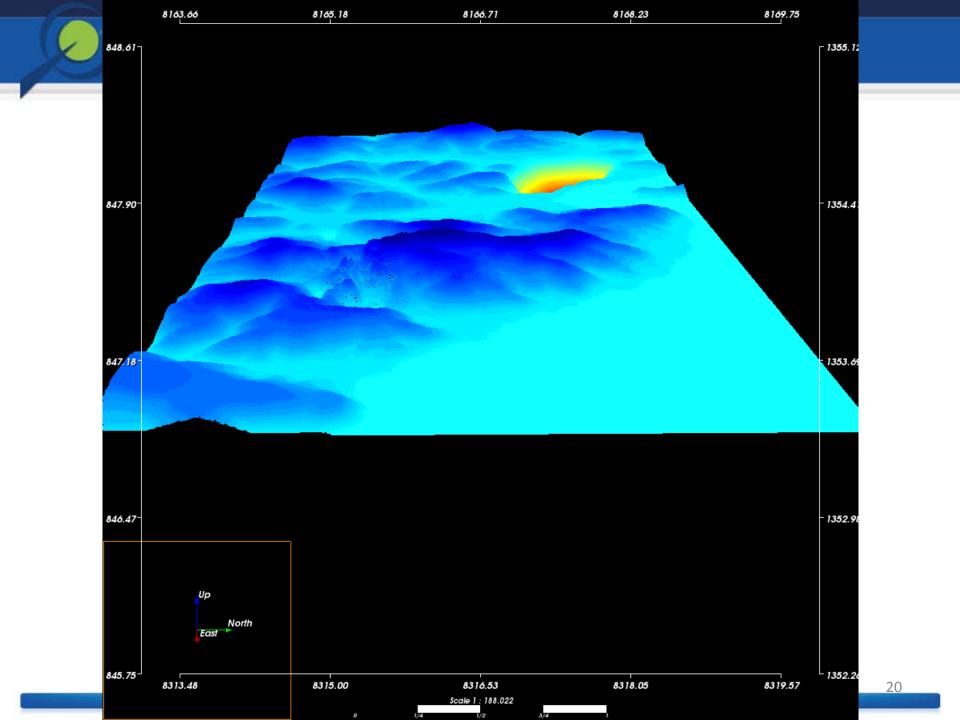


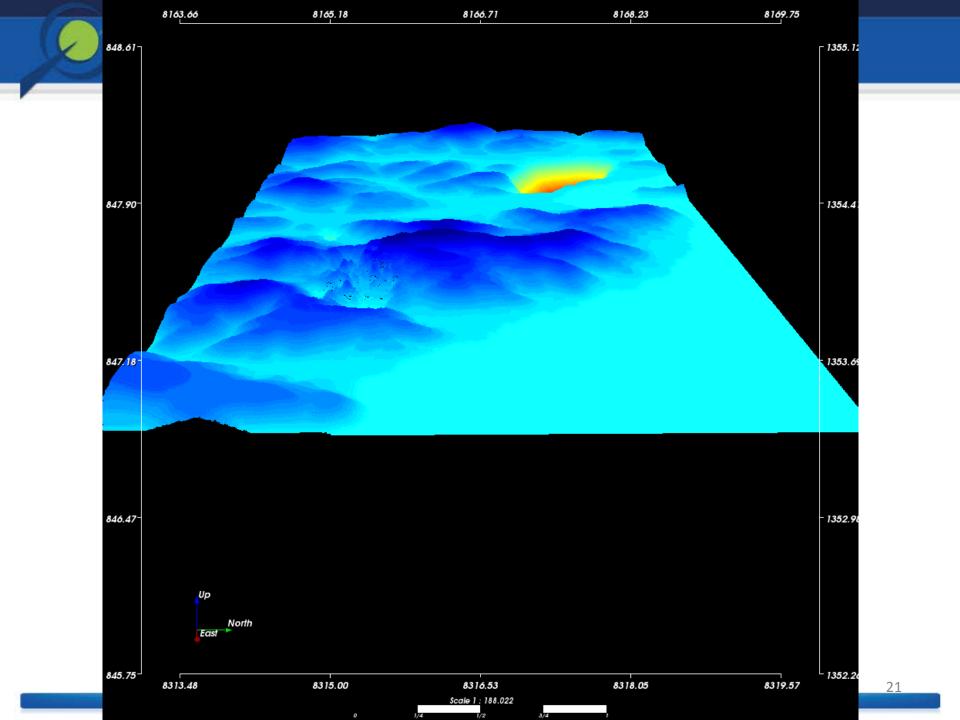


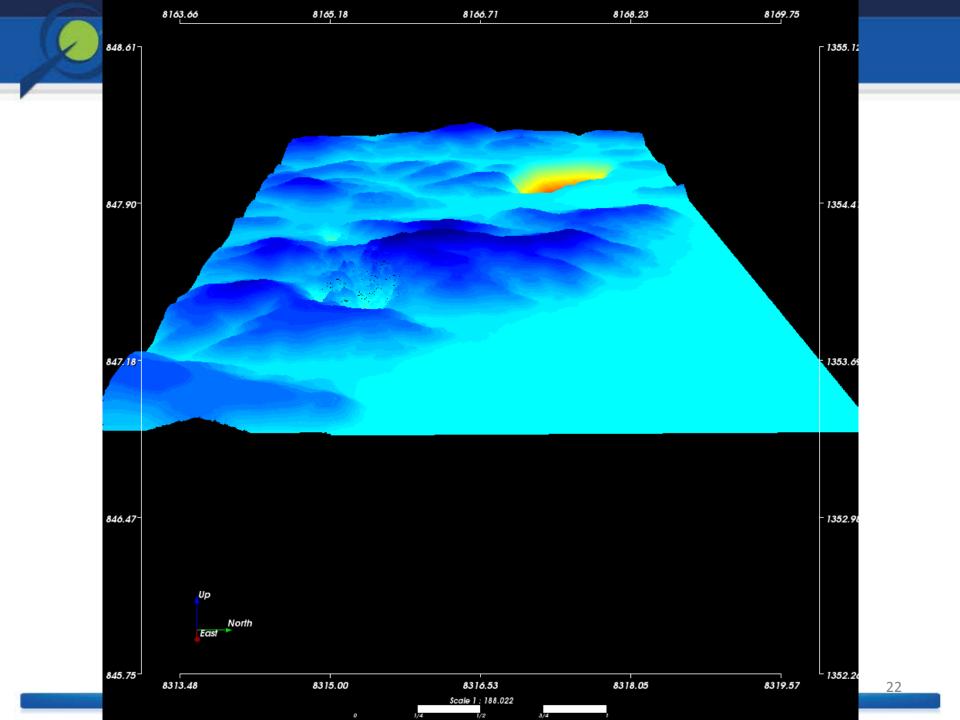


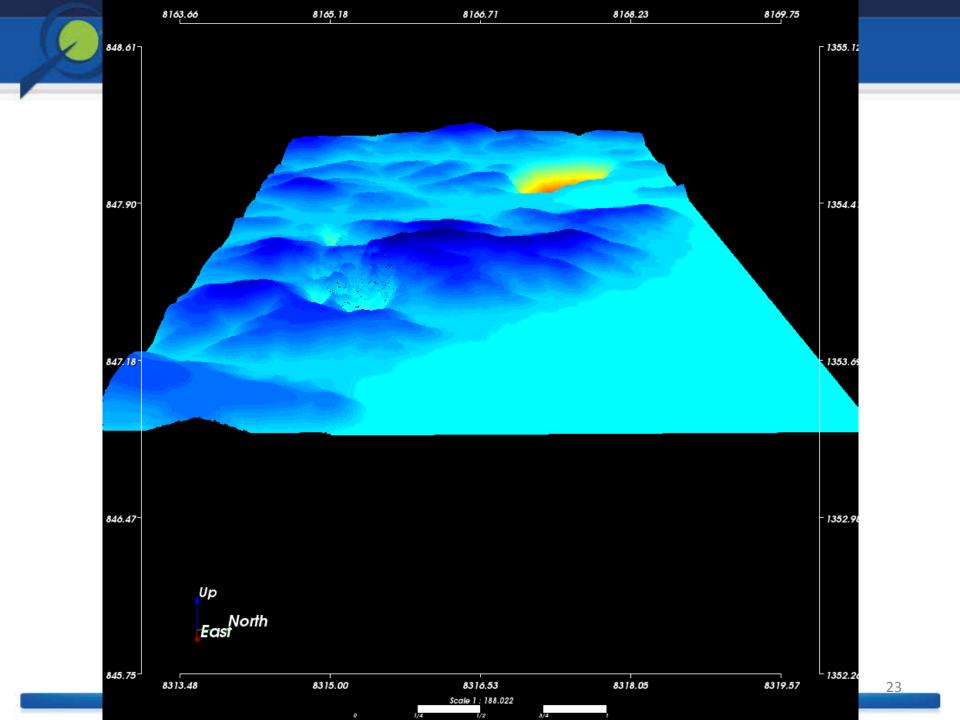


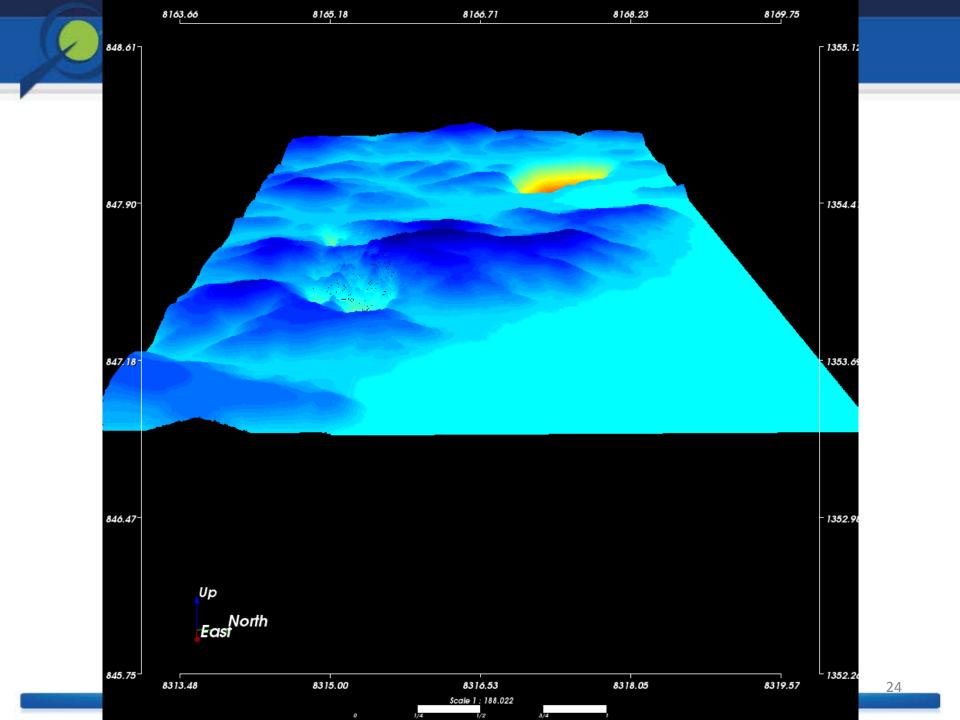


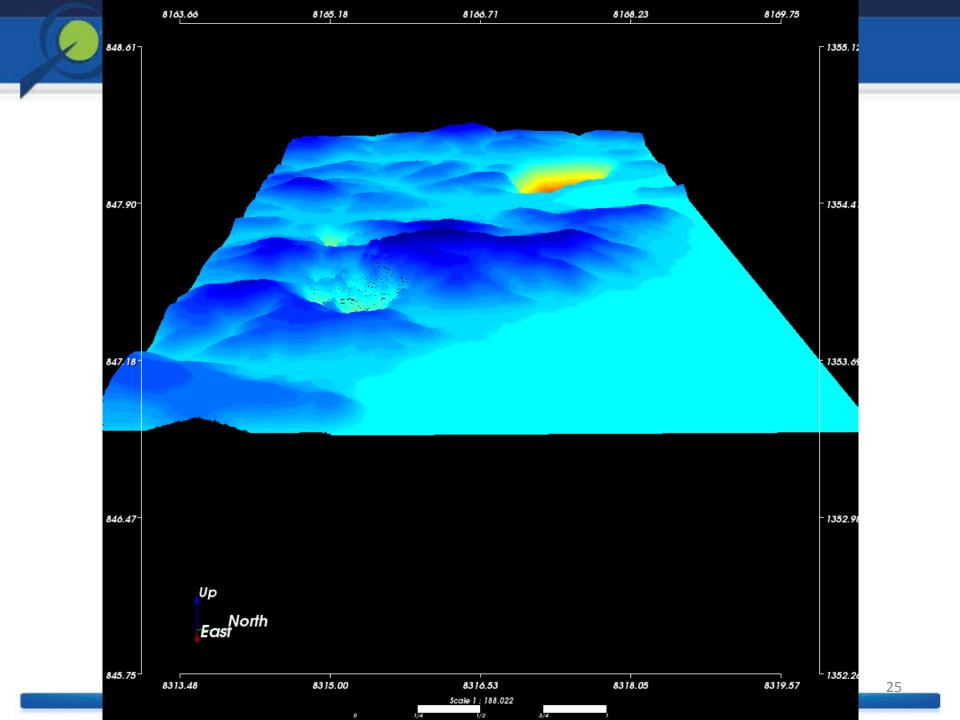


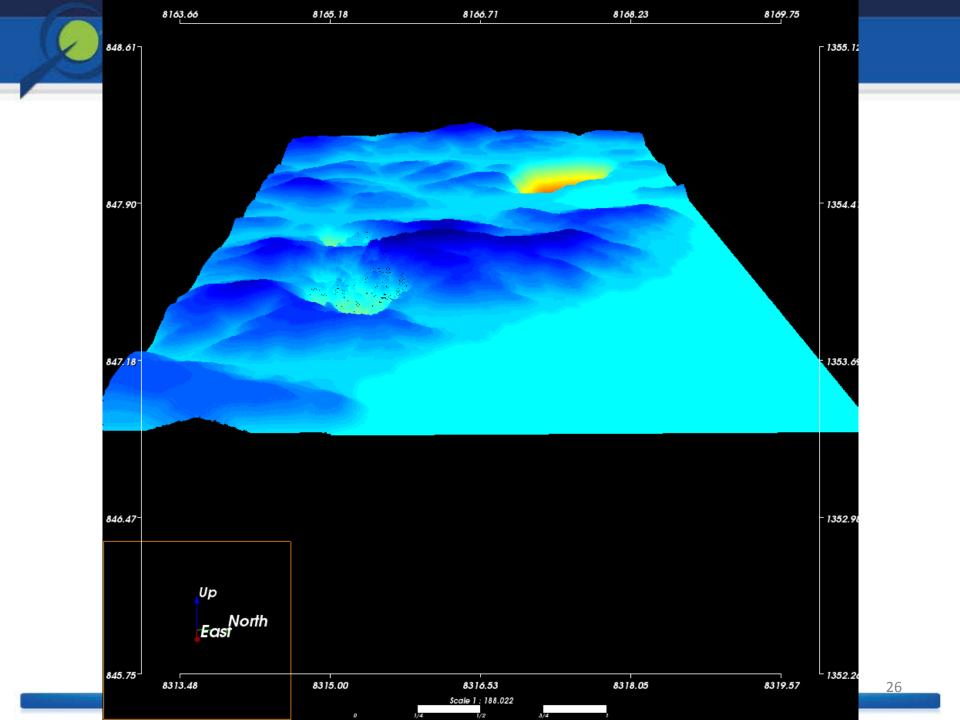


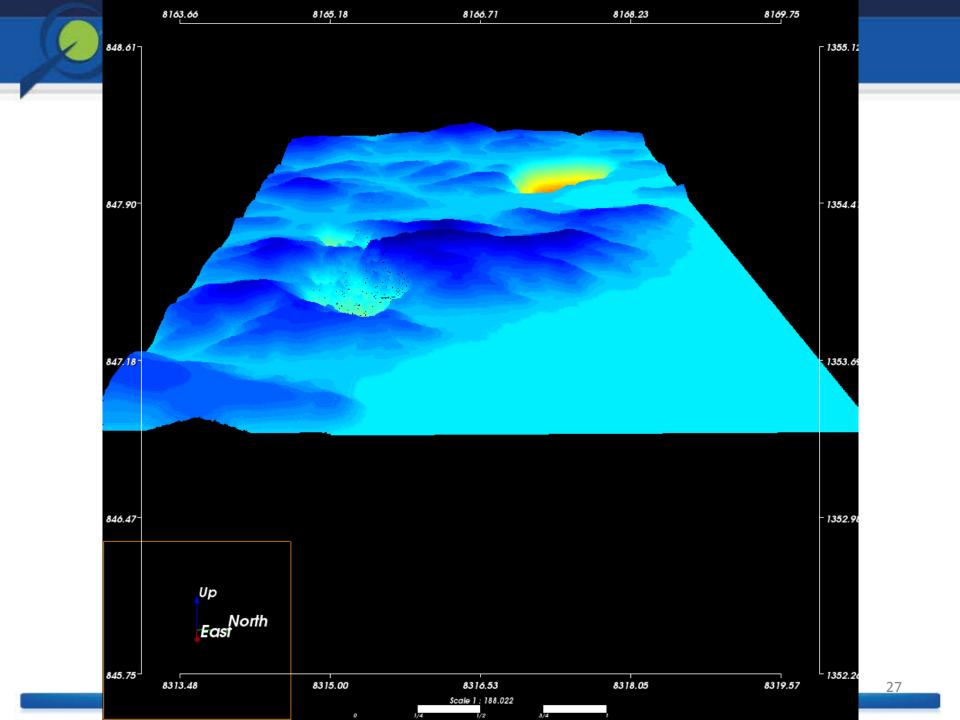


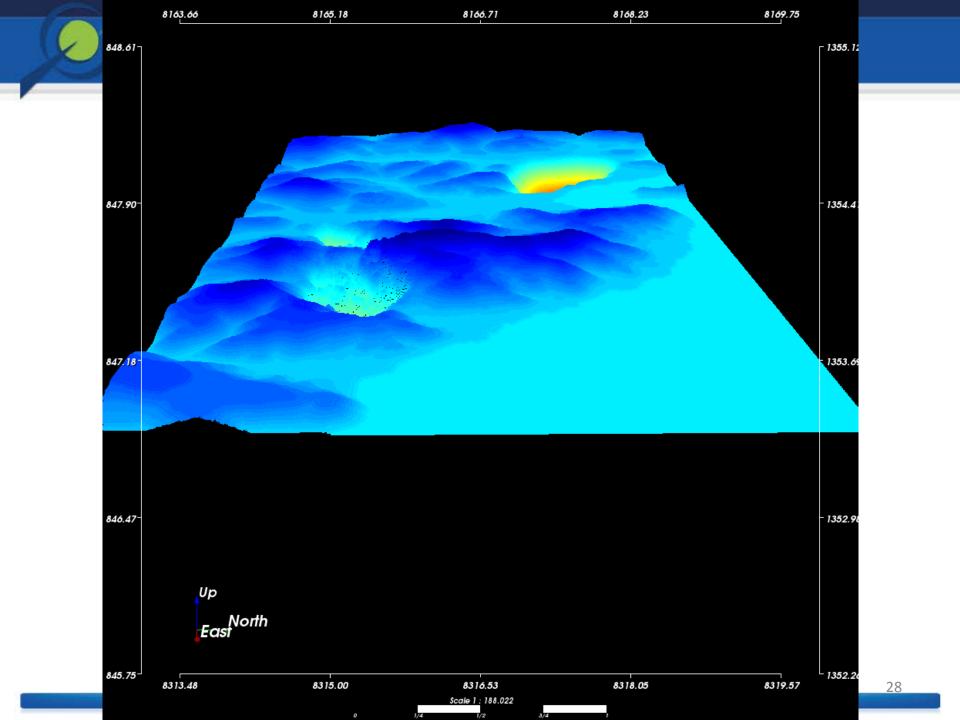


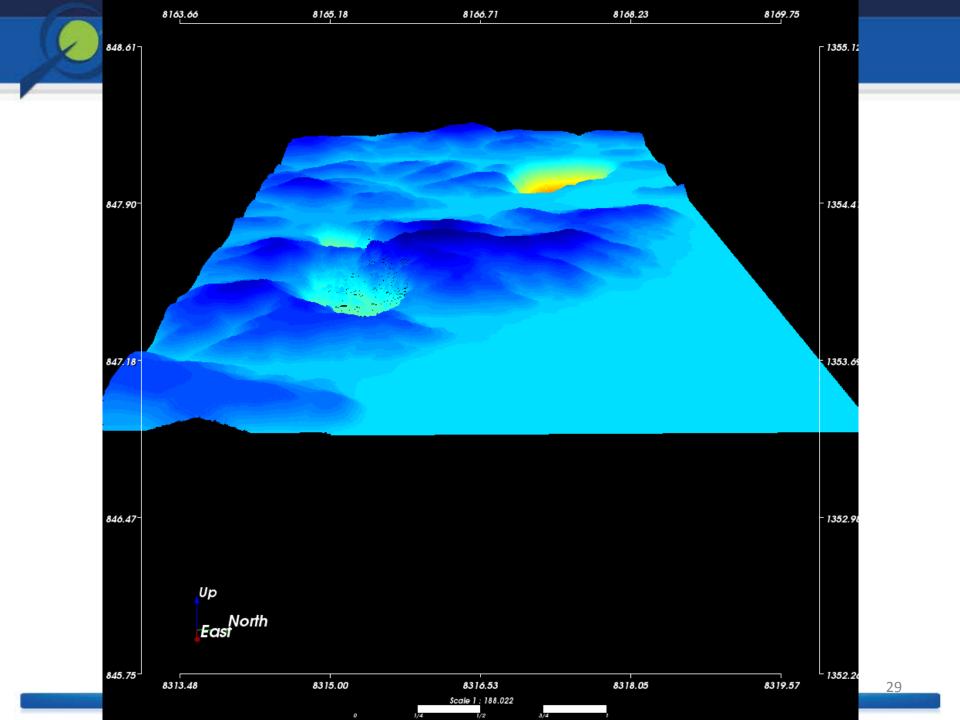


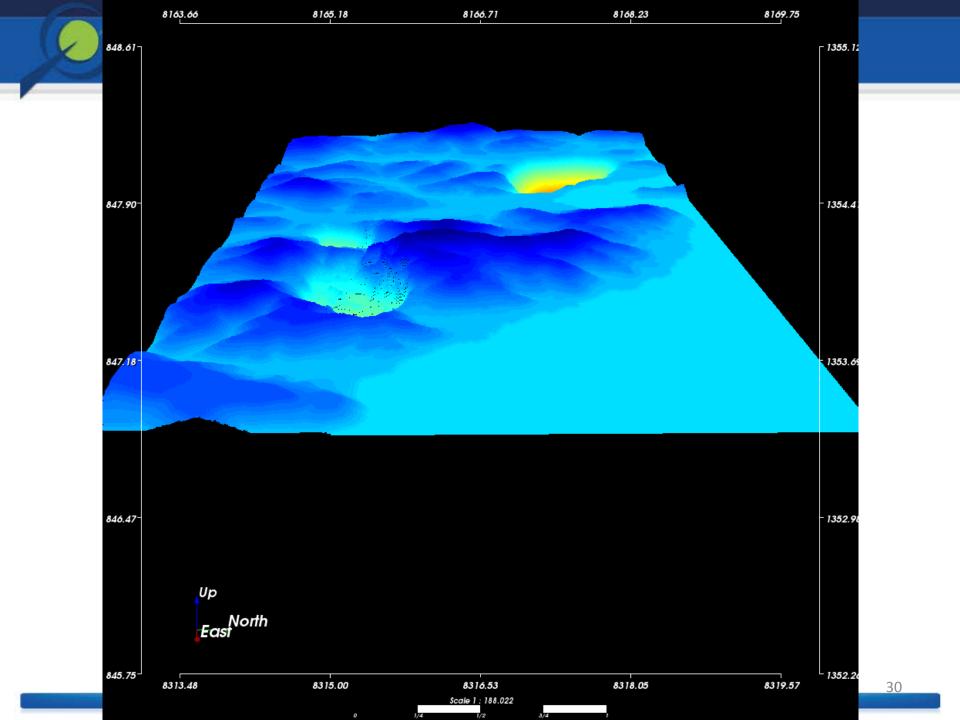


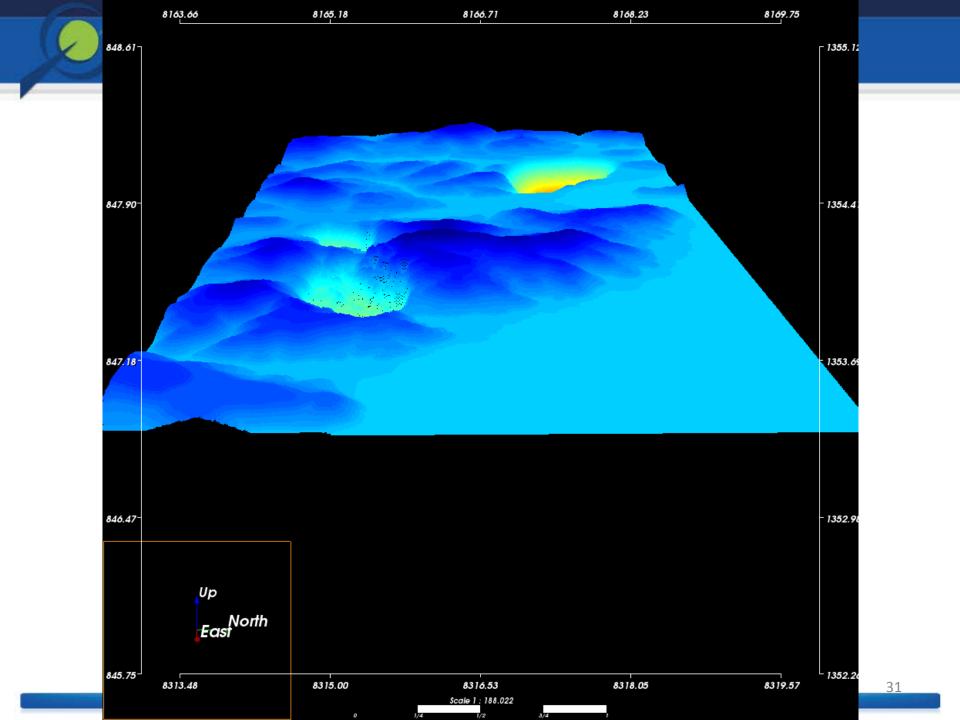


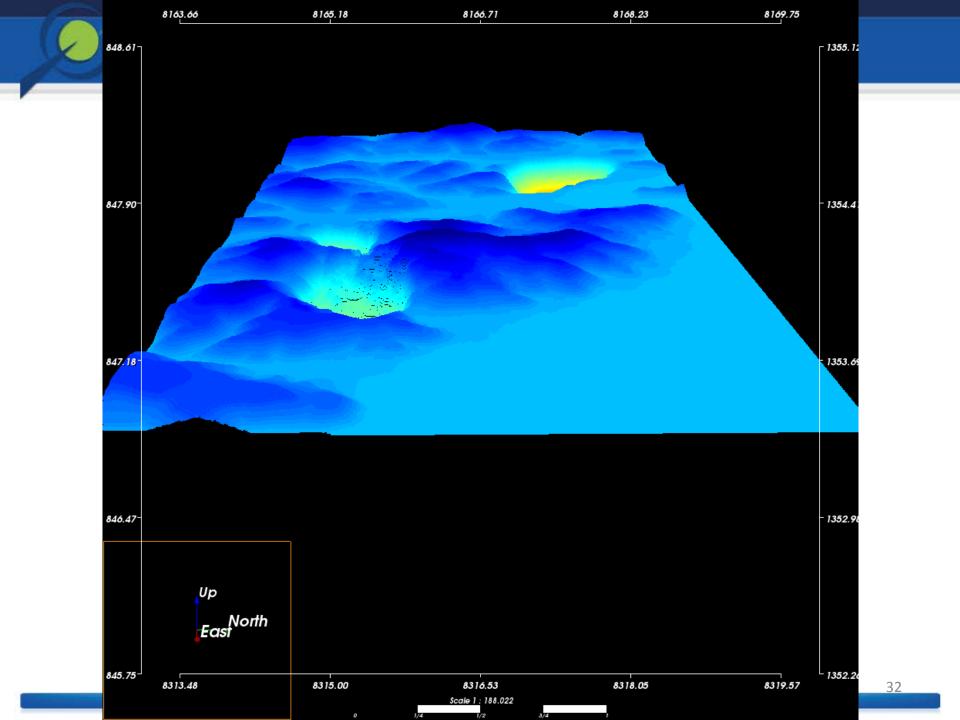


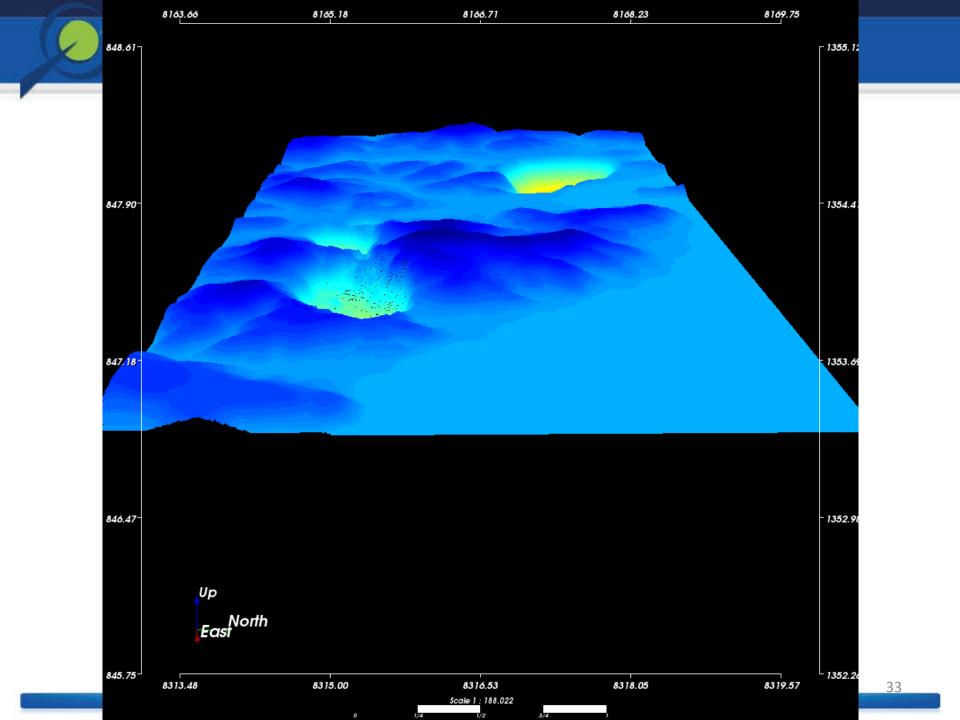


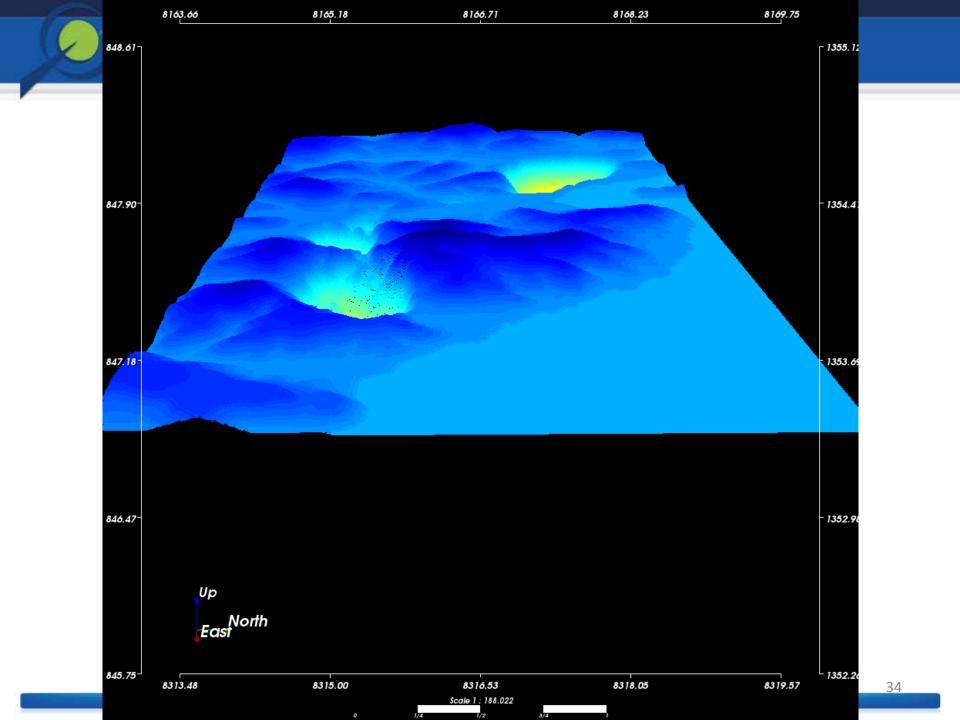


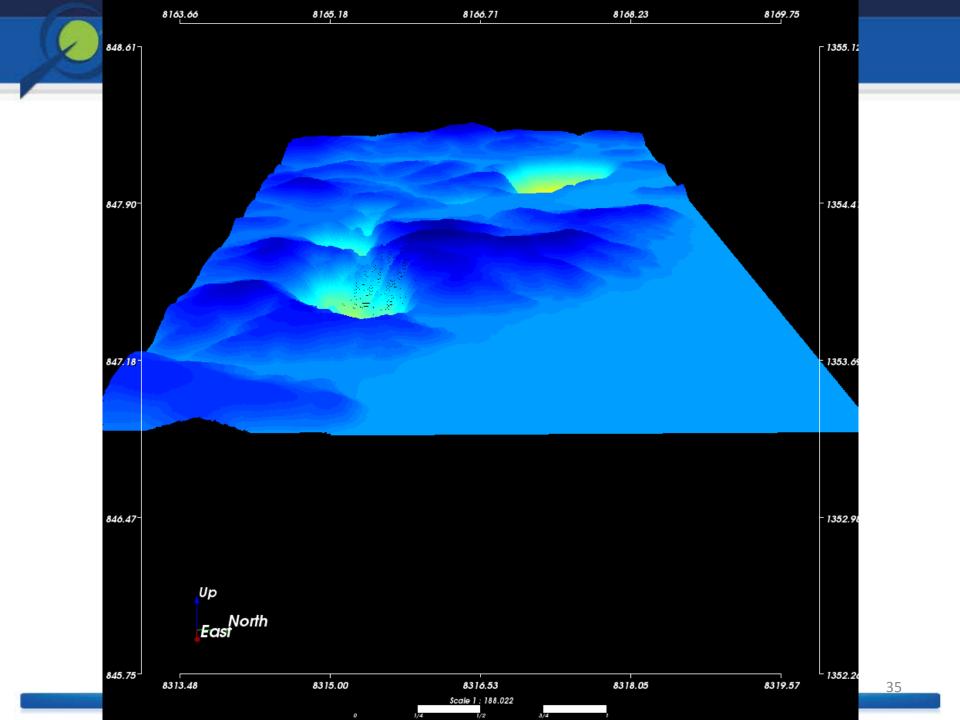


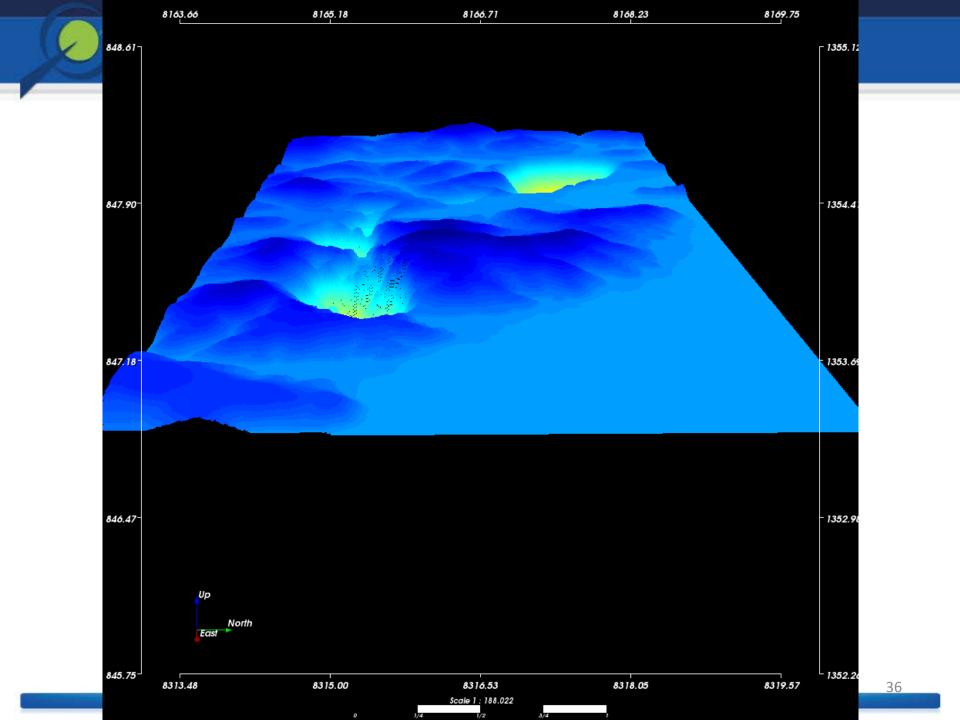


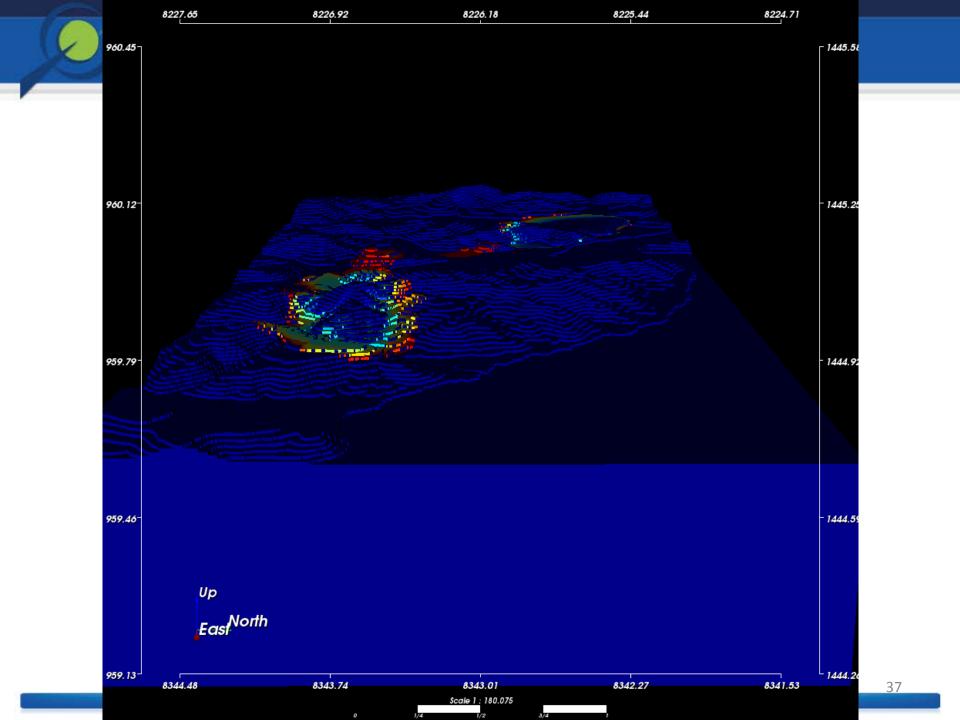


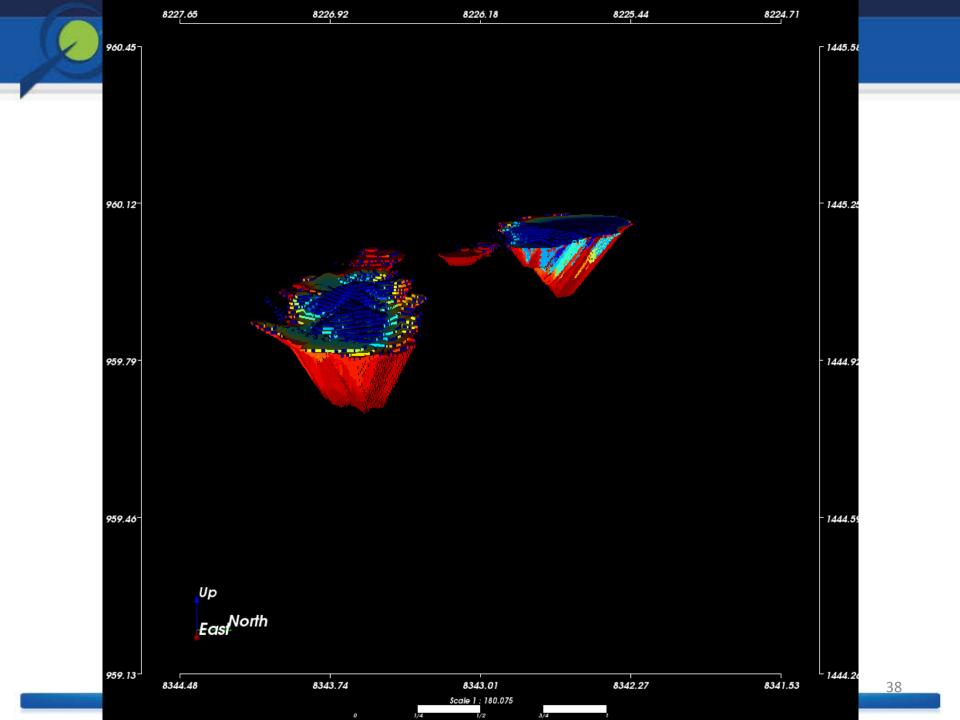












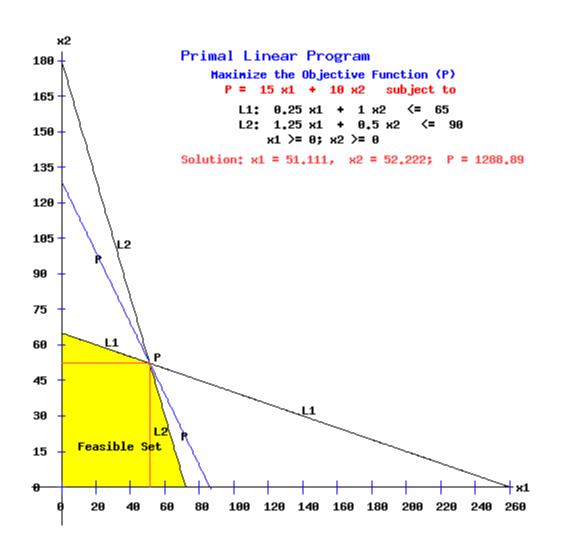
## **Linear Problem**

max. 
$$c^T x$$

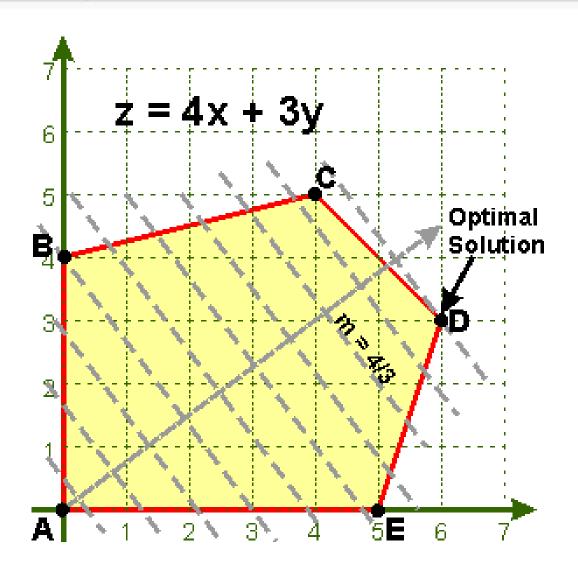
s.t. 
$$Ax \leq b$$

$$x \ge 0$$

# Simplex



# **Interior Point**





# LINPACK AND MATRIX

Organized around matrix decompositions

LU

Cholesky

QR

singular value

# Cholesky

- Small block model ~ 66k blocks
  - Sparse Cholesky 23000 x 23000 for one iteration
    - 529M elements
    - 207k non zero elements
  - Dense CPU single solution
    - Over 30 min
  - Sparse CPU single solution (not state of the art)
    - Few seconds
- CHOLMOD (suitesparse from NVIDIA)
  - 3x speedup over CPU multithread implementation

# Cholesky

$$A = \begin{pmatrix} a_{11} & a_{21} & a_{31} \\ a_{21} & a_{22} & a_{32} \\ a_{31} & a_{32} & a_{33} \end{pmatrix}$$

$$= \begin{pmatrix} l_{11} & 0 & 0 \\ l_{21} & l_{22} & 0 \\ l_{31} & l_{32} & l_{33} \end{pmatrix} \begin{pmatrix} l_{11} & l_{21} & l_{31} \\ 0 & l_{22} & l_{32} \\ 0 & 0 & l_{33} \end{pmatrix} \equiv LL^{T}$$

$$= \begin{pmatrix} l_{11}^{2} & l_{21}l_{11} & l_{31}l_{11} \\ l_{21}l_{11} & l_{21}^{2} + l_{22}^{2} & l_{31}l_{21} + l_{32}l_{22} \\ l_{31}l_{11} & l_{31}l_{21} + l_{32}l_{22} & l_{31}^{2} + l_{32}^{2} + l_{33}^{2} \end{pmatrix}$$

$$l_{kk} = \sqrt{a_{kk} - \sum_{j=1}^{k-1} l_{kj}^2}$$

$$l_{ik} = \frac{1}{l_{kk}} \left( a_{ik} - \sum_{j=1}^{k-1} l_{ij} l_{kj} \right)$$

# Cholesky

```
1: procedure CHOLESKY(A)
2: int i, j, k;
3: for k := 0 to n - 1 do
   A[k,k] := \sqrt{A[k,k]}; /* Obtain the square root of the diagonal element. */
   for j := k + 1 to n - 1 do
   A[k,j] := A[k,j]/A[k,k]; /* The division step. */
6:
   end for
    for i := k + 1 to n - 1 do
       for j := i to n-1 do
9:
         A[i,j] := A[i,j] - A[k,i] \times A[k,j]; /* The elimination step. */
10:
       end for
11:
     end for
12:
13: end for
```

# Single Thread

```
j int chol gold(const Matrix A, Matrix U) {
     unsigned int i, j, k;
     unsigned int size = A.num rows * A.num columns;
     // Copy the contents of the A matrix into the working matrix U
      for (i = 0; i < size; i++)
         U.elements[i] = A.elements[i];
     // Perform the Cholesky decomposition in place on the U matrix
      for (k = 0; k < U.num rows; k++) {</pre>
         // Take the square root of the diagonal element
         U.elements[k * U.num rows + k] = sqrt(U.elements[k * U.num rows + k]);
          if (U.elements[k * U.num rows + k] <= 0) {</pre>
             printf("Cholesky decomposition failed. \n");
             return 0;
         // Division step
          for (j = (k + 1); j < U.num rows; j++)
              U.elements[k * U.num rows + j] /= U.elements[k * U.num rows + k]; // Division step
         // Elimination step
          for (i = (k + 1); i < U.num rows; i++)
             for (j = i; j < U.num rows; j++)
                 U.elements[i * U.num rows + j] -= U.elements[k * U.num rows + i] * U.elements[k * U.num rows + j];
     // As the final step, zero out the lower triangular portion of U
      for (i = 0; i < U.num rows; i++)
         for (j = 0; j < i; j++)
             U.elements[i * U.num rows + j] = 0.0;
      return 1;
```

```
= #ifndef MATRIX H
  #define MATRIX H
  // Thread block size
                                                         Z CPU-Z
  #define MATRIX SIZE 2048
                                                           CPU Caches Mainboard Memory SPD Graphics About
  #define NUM PTHREADS 4
                                                            Processor-
  #define NUM OMPTHREADS NUM PTHREADS
                                                                               Intel Core i5 3330
                                                                 Name
                                                                                                       (intel) inside
                                                                                      Max TDP 77 W
                                                                          Ivy Bridge
                                                             Code Name
  // Matrix dimensions
                                                               Package
                                                                               Socket 1155 LGA
  #define NUM COLUMNS MATRIX SIZE // Number of c
                                                                                                       CORE" i5
                                                                       22 nm Core Voltage 0.808 V
                                                            Technology
  #define NUM ROWS MATRIX SIZE // Number of rows
                                                                             Intel(R) Core(TM) i5-3330 CPU @ 3.00GHz
                                                            Specification
                                                                Family
                                                                                   Model
                                                                                                   Stepping
                                                                                                              9
  // Matrix Structure declaration
                                                                                Ext. Model
                                                                                           3A
                                                                                                              E1
                                                             Ext. Family
                                                                                                   Revision
  typedef struct {
                                                            Instructions | MMX, SSE (1, 2, 3, 3S, 4.1, 4.2), EM64T, VT-x, AES, AVX
            //width of the matrix represented
       unsigned int num columns;
                                                            Clocks (Core #0)
                                                                                      Cache
            //height of the matrix represented
                                                                        3109.31 MHz
                                                                                      L1 Data 4 x 32 KBytes
                                                            Core Speed
                                                                                                             8-way
       unsigned int num rows;
                                                                          x 31.0
                                                              Multiplier
                                                                                      L1 Inst. 4 x 32 KBytes
                                                                                                             8-way
            //number of elements between the begin
                                                                         100.3 MHz
                                                            Bus Speed
                                                                                      Level 2 4 x 256 KBytes
                                                                                                             8-way
           // rows in the memory layout (useful f
                                                                                                 6 MBytes
                                                             Rated FSB
                                                                                      Level 3
                                                                                                            12-way
       unsigned int pitch;
                                                                                          Cores 4
            //Pointer to the first element of the
                                                             Selection Processor #1
                                                                                                       Threads 4
       float* elements;
                                                           CPU-Z Version 1.61.5.x64
   } Matrix;
                                                                                                Validate
                                                                                                             OK
  #endif // MATRIX H
```

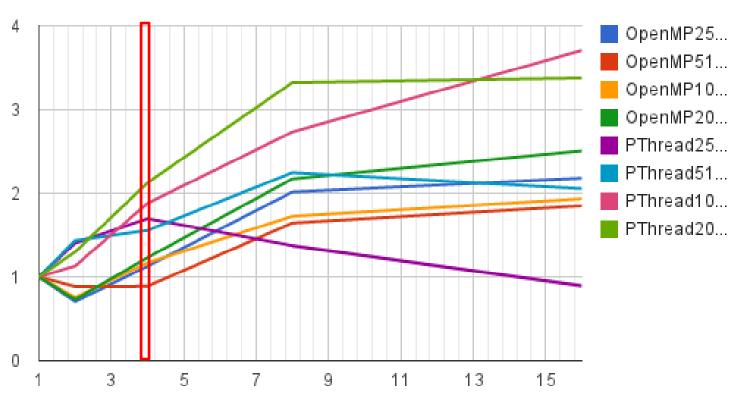
```
en in place on the U matrix
for(k = 0; k < U.num rows; k++)
        //Only one thread does squre root and division
        if(id==0)
                // Take the square root of the diagonal element
                U.elements[k * U.num rows + k] = sqrt(U.elements[k * U.num rows + k]);
                if(U.elements[k * U.num rows + k] <= 0){</pre>
                                 printf("Cholesky decomposition failed. \n");
                                 return 0;
                // Division step
                for(j = (k + 1); j < U.num_rows; j++)</pre>
                        U.elements[k * U.num rows + j] /= U.elements[k * U.num rows + k]; // Division step
        //Sync threads!!!!!
        sync pthreads (barrier, id);
       //For this k iteration, split up i
        //Size of i range originally
        int isize = U.num rows - (k + 1);
        int items per thread, items last thread;
        range_splitter(isize, NUM_PTHREADS, &items_per_thread, &items_last_thread);
        //Divy up work
        //Elim work
        int elimi start, elimi end;
        int offset = (k + 1); //To account for not starting at i=0 each time
```

```
// Perform the Cholesky decomposition in place on the U matrix
for(k = 0; k < U.num rows; k++)
       //Only one thread does squre root and division
        if(id==0)
                // Take the square root of the diagonal element
                U.elements[k * U.num rows + k] = sqrt(U.elements[k * U.num rows + k]);
                if(U.elements[k * U.num rows + k] <= 0){</pre>
                                 printf("Cholesky decomposition failed. \n");
                                 return 0;
                // Division step
                for(j = (k + 1); j < U.num_rows; j++)</pre>
                        U.elements[k * U.num rows + j] /= U.elements[k * U.num rows + k]; // Division step
       sync pthreads (barrier, id);
       //For this k iteration, split up i
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       int isize = U.num rows - (k + 1);
        int items per thread, items last thread;
       range_splitter(isize, NUM_PTHREADS, &items_per_thread, &items_last_thread);
       //Divy up work
       //Elim work
       int elimi start, elimi end;
        int offset = (k + 1); //To account for not starting at i=0 each time
```

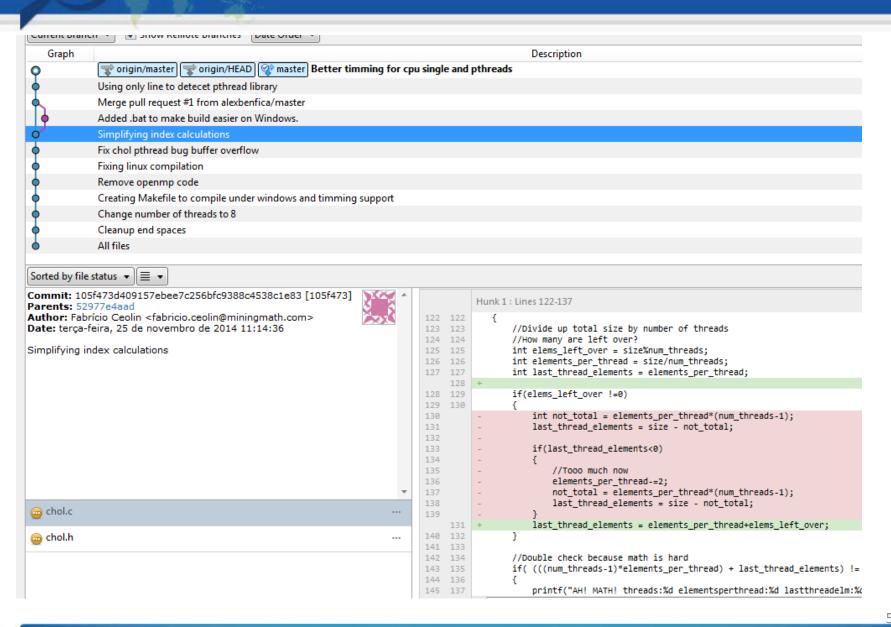
```
// Perform the Cholesky decomposition in place on the U matrix
for(k = 0; k < U.num rows; k++)
       //Only one thread does squre root and division
        if(id==0)
                // Take the square root of the diagonal element
                U.elements[k * U.num rows + k] = sqrt(U.elements[k * U.num rows + k]);
                if(U.elements[k * U.num rows + k] <= 0){</pre>
                                 printf("Cholesky decomposition failed. \n");
                                 return 0;
                // Division step
                for(j = (k + 1); j < U.num_rows; j++)</pre>
                        U.elements[k * U.num rows + j] /= U.elements[k * U.num rows + k]; // Division step
        //Sync threads!!!!!
        sync pthreads (barrier, id);
       //For this k iteration, split up i
        //Size of i range originally
        int isize = U.num rows - (k + 1);
       range_splitter(isize, NUM_PTHREADS, &items_per_thread, &items_last_thread);
        //Elim work
       int elimi start, elimi end;
        int offset = (k + 1); //To account for not starting at i=0 each time
```

Speedup (over serial CPU)

#### Speedup vs. Number of Threads



# Pthread: our optimizations



# Pthread: our optimizations

```
D:\Dropbox\Devel\Win\CudaProject\Drexel-ECEC622-Midterm1\build>CholThread.exe
Creating a 2048 x 2048 matrix with random numbers between [-.5, .5]...done.
Generating the symmetric matrix...done.
Generating the positive definite matrix...done.
Performing Cholesky decomposition on the CPU using the single-threaded versio

Run time: 9.4130001068 s.
Cholesky decomposition on the CPU was successful.

Performing Cholesky decomposition on the CPU using the PTHREAD version.

Run time: 3.0450000763 s.

Speedup from single to phreads = 3.091297 x.

Double checking for correctness by recovering the original matrix.
```



# CUDA device query: Geforce GTS 450

```
CUDA Device Query (Runtime API) version (CUDART static linking)
Detected 1 CUDA Capable device(s)
Device 0: "GeForce GTS 450"
 CUDA Driver Version / Runtime Version
                                                    6.5 / 6.5
 CUDA Capability Major/Minor version number:
 Total amount of global memory:
                                                   1024 MBytes (1073741824 bytes)
 (4) Multiprocessors, (48) CUDA Cores/MP:
                                                   192 CUDA Cores
                                                   1620 MHz (1.62 GHz)
 GPU Clock rate:
 Memory Clock rate:
                                                    1804 Mhz
 Memory Bus Width:
                                                    128-bit
                                                    262144 bytes
 L2 Cache Size:
                                                   1D=(65536), 2D=(65536, 65535), 3D=(2048, 2048, 2048)
1D=(16384), 2048 layers
 Maximum Texture Dimension Size (x,y,z)
 Maximum Layered 1D Texture Size, (num) layers
 Maximum Layered 2D Texture Size, (num) layers
                                                   2D=(16384, 16384), 2048 layers
                                                    65536 bytes
 Total amount of constant memory:
 Total amount of shared memory per block:
                                                    49152 bytes
 Total number of registers available per block: 32768
 Warp size:
                                                    32
 Maximum number of threads per multiprocessor:
                                                   1536
 Maximum number of threads per block:
                                                    1024
 Max dimension size of a thread block (x,y,z): (1024, 1024, 64)
Max dimension size of a grid size (x,y,z): (65535, 65535, 65535)
                                                    2147483647 bytes
 Maximum memory pitch:
 Texture alignment:
                                                    512 bytes
 Concurrent copy and kernel execution:
                                                    Yes with 1 copy engine(s)
 Run time limit on kernels:
                                                    Yes
 Integrated GPU sharing Host Memory:
                                                    No
 Support host page-locked memory mapping:
                                                    Yes
 Alignment requirement for Surfaces:
                                                    Yes
 Device has ECC support:
                                                   Disabled
 CUDA Device Driver Mode (TCC or WDDM):
                                                    WDDM (Windows Display Driver Model)
 Device supports Unified Addressing (UVA):
 Device PCI Bus ID / PCI location ID:
                                                    1 / 0
 Compute Mode:
    < Default (multiple host threads can use ::cudaSetDevice() with device simultaneously) >
deviceQuery, CUDA Driver = CUDART, CUDA Driver Version = 6.5, CUDA Runtime Version = 6.5, NumDevs = 1, Device0 = GeForce GTS 450
```



# CUDA device query: Geforce GTS 450

```
CUDA Device Query (Runtime API) version (CUDART static linking)
Detected 1 CUDA Capable device(s)
Device 0: "GeForce GTS 450"
 CUDA Driver Version / Runtime Version
                                                    6.5 / 6.5
 CUDA Capability Major/Minor version number:
 Total amount of global memory:
                                                   1024 MBytes (1073741824 bytes)
 (4) Multiprocessors, (48) CUDA Cores/MP:
                                                   192 CUDA Cores
                                                   1620 MHz (1.62 GHz)
 GPU Clock rate:
 Memory Clock rate:
                                                    1804 Mhz
 Memory Bus Width:
                                                    128-bit
                                                    262144 bytes
 L2 Cache Size:
                                                   1D=(65536), 2D=(65536, 65535), 3D=(2048, 2048, 2048)
1D=(16384), 2048 layers
 Maximum Texture Dimension Size (x,y,z)
 Maximum Layered 1D Texture Size, (num) layers
 Maximum Layered 2D Texture Size, (num) layers
                                                   2D=(16384, 16384), 2048 layers
                                                    65536 bytes
 Total amount of constant memory:
 Total amount of shared memory per block:
                                                    49152 bytes
 Total number of registers available per block: 32768
 Warp size:
                                                    32
 Maximum number of threads per multiprocessor:
                                                   1536
 Maximum number of threads per block:
                                                    1024
 Max dimension size of a thread block (x,y,z): (1024, 1024, 64)
Max dimension size of a grid size (x,y,z): (65535, 65535, 65535)
                                                    2147483647 bytes
 Maximum memory pitch:
 Texture alignment:
                                                    512 bytes
 Concurrent copy and kernel execution:
                                                    Yes with 1 copy engine(s)
 Run time limit on kernels:
                                                    Yes
 Integrated GPU sharing Host Memory:
                                                    No
 Support host page-locked memory mapping:
                                                    Yes
 Alignment requirement for Surfaces:
                                                    Yes
 Device has ECC support:
                                                   Disabled
 CUDA Device Driver Mode (TCC or WDDM):
                                                    WDDM (Windows Display Driver Model)
 Device supports Unified Addressing (UVA):
 Device PCI Bus ID / PCI location ID:
                                                    1 / 0
 Compute Mode:
    < Default (multiple host threads can use ::cudaSetDevice() with device simultaneously) >
deviceQuery, CUDA Driver = CUDART, CUDA Driver Version = 6.5, CUDA Runtime Version = 6.5, NumDevs = 1, Device0 = GeForce GTS 450
```

## **CUDA** sqrt

```
int threads_per_block_sqrt = 512;
int blocks_sqrt = MATRIX_SIZE / threads_per_block_sqrt;
dim3 thread_block(threads_per_block_sqrt, 1, 1);
dim3 grid(blocks_sqrt, 1);
chol_kernel_cudaUFMG_sqrt <<<grid, thread_block>>>(gpu_u.elements);
```

# **CUDA** sqrt kernel

```
__global___ void chol_kernel_cudaUFMG_sqrt(float * U) {
    // Get a thread identifier
    int tx = blockIdx.x * blockDim.x + threadIdx.x;
    int tx_diag = tx * MATRIX_SIZE + tx;
    U[tx_diag] = sqrt(U[tx_diag]);
}
```

### **CUDA** div

```
int block_x_div = 16;
int block_y_div = 16;
int thread_x_div = 4;
int thread_y_div = 4;
dim3 grid_div(block_x_div, block_y_div, 1);
dim3 thread_block_div(thread_x_div, thread_y_div, 1);
int elements_per_thread_div = ((MATRIX_SIZE * MATRIX_SIZE) / 2) / (thread_x_div * thread_y_div * block_x_div * block_y_div);
chol_kernel_cudaUFMG_division <<<grid_div, thread_block_div >>>(gpu_u.elements, elements_per_thread_div);
```

### **CUDA** div kernel

```
global void chol kernel cudaUFMG division(float * U, int elem per thr) {
  // Get a thread identifier
   int tx = blockIdx.x * blockDim.x + threadIdx.x;
  int ty = blockIdx.y * blockDim.y + threadIdx.y;
   int tn = ty * blockDim.x * gridDim.x + tx;
                                                            4 5 6 7 8 9 10 11 12 13 14 15
   for(unsigned i=0;i<elem per thr;i++) {</pre>
                                            O
       int iel = tn * elem per thr + i;
       int xval = iel % MATRIX SIZE;
                                              3
       int yval = iel / MATRIX SIZE;
                                              4
       if(xval == yval) {
           continue;
                                              8
                                              9
       // if on the lower diagonal...
                                             10
       if(yval > xval){
                                             11
           xval = MATRIX SIZE - xval - 1;
                                             12
           yval = MATRIX SIZE - yval - 1;
                                             13
                                             14
                                             15
       int iU = xval + yval * MATRIX SIZE;
       int iDiag = yval + yval * MATRIX SIZE;
       U[iU] /= U[iDiag];
```

#### **CUDA** elimination

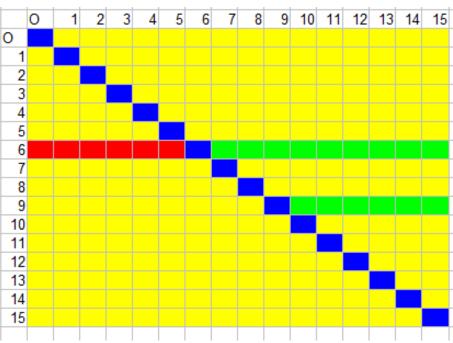
```
int block_y_eli = 1;
//Each thread within a block will take some j iterations
int thread x eli = 256;
int thread y eli = 1;
                                                                   1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
//Each kernel call will be one iteration of out K loop
for (int k = 0; k < MATRIX SIZE; k++) {
   //Want threads to stride across memory
                                                            3
   //i is outer loop
                                                            4
   //j is inner loop
   //so threads should split the j loop
                                                            5
   //Each thread block will take an i iteration
                                                            6
   // i=k+1;i<MATRIX SIZE
    int isize = MATRIX_SIZE - (k + 1);
                                                            9
    if(isize==0){
                                                           10
        isize++;
                                                           11
                                                           12
    int block_x_eli = isize;
                                                           13
                                                           14
   //Set up the execution grid on the GPU
                                                            15
    dim3 thread_block(thread_x_eli, 1, 1);
    dim3 grid(block x eli, 1);
    //Call kernel with for this K iteration
    chol kernel cudaUFMG elimination <<<gri>d, thread block>>>(gpu u.elements, k);
chol_kernel_cudaUFMG_zero <<<grid_div, thread_block_div>>>(gpu_u.elements, elements_per_thread_div);
```

### **CUDA** elimination kernel

```
global void chol kernel cudaUFMG elimination(float * U, int k) {
                                                      2 3 4 5 6 7 8 9 10 11 12 13 14 15
  //This call acts as a single K iteratior-
  //Each block does a single i iteration
  int i = (k+1) + blockIdx.x;
                                               3
  //Each thread does some part of j
  //Stide in units of 'stride'
  //Thread 0 does 0, 16, 32
  //Thread 1 does 1, 17, 33
                                               9
  //..etc.
                                              10
  int jstart = i + threadIdx.x;
                                              11
                                              12
  int jstep = blockDim.x;
                                              13
                                              14
 // Pre-calculate indexes outside loop
                                              15
  int kM = k * MATRIX SIZE;
  int iM = i * MATRIX SIZE;
                                           Address _
  int ki = kM + i;
  //Do work for this i iteration
  for (int j=jstart; j<MATRIX SIZE; j+=jstep) {</pre>
      U[iM + j] = U[ki] * U[kM + j];
                                           Thread ID 0
```

#### **CUDA** zero kernel

```
global void chol kernel cudaUFMG zero(float * U, int elem per thr) {
  // Get a thread identifier
  int tx = blockIdx.x * blockDim.x + threadIdx.x;
  int ty = blockIdx.y * blockDim.y + threadIdx.y;
  int tn = ty * blockDim.x * gridDim.x + tx;
                                                 O
  for(unsigned i=0;i<elem per thr;i++){</pre>
      int iel = tn * elem per thr + i;
      int xval = iel % MATRIX SIZE;
                                                  4
      int yval = iel / MATRIX SIZE;
      if(xval == yval) {
          continue;
                                                   8
                                                  9
                                                  10
                                                  11
      // if on the upper diagonal...
                                                  12
      if(yval < xval){</pre>
                                                  13
          xval = MATRIX SIZE - xval - 1;
                                                  14
          yval = MATRIX SIZE - yval - 1;
                                                  15
      int iU = xval + yval * MATRIX SIZE;
      U[iU] = 0;
```





TYPE	SINGLE	PTHREAD	OUR PTHREAD	CUDA	OUR CUDA
SINGLE	1.00				
PTHREAD	2.20	1.00			
OUR PTHREAD	3.10	1.41	1.00		
CUDA	24.00	10.91	7.74	1.00	
OUR CUDA	33.00	15.00	10.65	1.38	1.00

### **Conclusion**

- Improvements
  - It is possible to speedup using our algorithm with CUDA
  - No room for shared memory in our implementation
    - (We've tried other methods, without success)

### **Conclusion**

- Future work
  - Pthread
    - Split sqrt and division over threads
  - Study Sparse Matrix algorithm
    - suitesparse with metis
    - Test CUDA and CPU multithread

# Questions?



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