Learning Activity 0: Introduction to Verilog

The goal of this project was to create two 2 bit counters with four count up/down functionalities using Verilog. Each implementation used different approaches to come up with the same result: one used a structural implementation which has a defined output for all states, and the other used a behavioral description of the circuit. The counter requirements are shown in the table below where s_1 and s_0 are inputs:

s_1	s_0	Function
0	0	Count up modulo-4 counter (simple binary up-counter; roll over 3 to 0)
0	1	Count down modulo-4 counter (simple binary down-counter; roll over 0 to 3)
1	0	Count up modulo-3 counter (roll over 2 to 0)
1	1	Count down modulo-3 counter (roll over 0 to 2)

The first implementation used a structural method to describe the counter. The first step of this method used a state transition diagram to find all possible states of the counter. The diagram is shown below:

State Transition Diagram:

Current State, Q_1Q_0	Next State, Q_1^+,Q_0^+ $s_1s_0 = 00$	Next State, Q_1^+,Q_0^+ $s_1s_0 = 01$	Next State, Q_1^+,Q_0^+ $s_1s_0 = 10$	Next State, Q_1^+,Q_0^+ $s_1s_0 = 11$
00	01	11	01	10
01	10	00	10	00
10	11	01	00	01
11	00	10	00	00

Next, I used K-maps to minimize the logical expressions of each variable to implement the design in an efficient way. The K-maps are shown below.

Kmap for Q_0^+:

(s_1s_0)	(Q_1Q_0)	00	01	11	10
00		**1**	**0**	**0**	**1**
01		**1**	**0**	**0**	**1**
11		**0**	**0**	**0**	**1**
10		**1**	**0**	**0**	**0**

Solving the K-Map for Q_0^+ gives:
$Q_0^+ = s_1'Q_0' + s_0Q_1Q_0' + s_0'Q_1'Q_0'$

Kmap for Q_1^+:

(s_1s_0)	(Q_1Q_0)	00	01	11	10
00		**0**	**1**	**0**	**1**
01		**1**	**0**	**1**	**0**
11		**1**	**0**	**0**	**0**
10		**0**	**1**	**0**	**0**

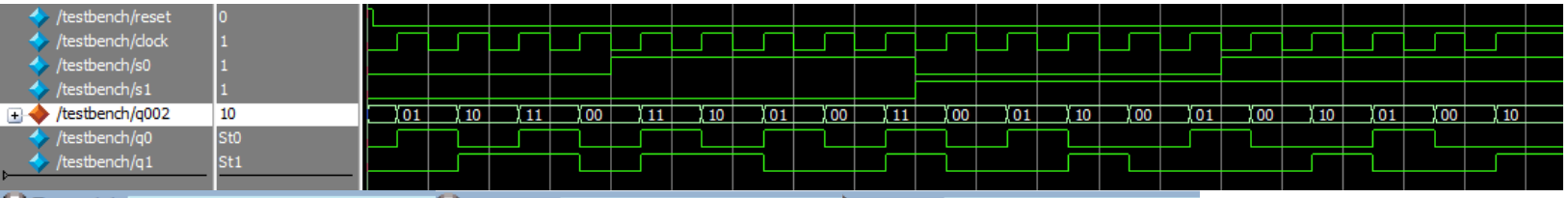
Solving the K-Map for Q_1^+ gives:
$Q_0^+ = s_0Q_1'Q_0' + s_0'Q_1'Q_0 + s_1's_0Q_1Q_0 + s_1's_0'Q_1Q_0'$

After the K-maps were solved, I created Verilog code that implemented the counter by using the above logic to assign values to flip flops. The schematic for the circuit is shown on the next page (pg 3.).

Next I implemented the behavioral version of the circuit. This version used two two bit vectors to store the current state and next state of the counter. Then a case statement determined what logic the process used. Finally the outputs were connected to the current state of the counter. The schematic is shown on page 4.

After creating the two circuits, I tested each circuit using ModelSim and the provided testbench. Both circuits showed the outputs shown below. All the test cases passed which verifies both designs.

Test Bench Results for Structural Verilog ModelSim Simulation:



Transcript

```
#
# PASSED
# ACTUAL 00
# EXPECTED 00
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b00
# DESCRIPTION Modulo-4 up
# TIME 50
#
# PASSED
# ACTUAL 01
# EXPECTED 01
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b00
# DESCRIPTION Modulo-4 up
# TIME 150
#
# PASSED
# ACTUAL 10
# EXPECTED 10
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b00
# DESCRIPTION Modulo-4 up
# TIME 250
#
# PASSED
# ACTUAL 11
# EXPECTED 11
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b00
# DESCRIPTION Modulo-4 up
# TIME 350
#
# PASSED
# ACTUAL 00
# EXPECTED 00
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b00
# DESCRIPTION Modulo-4 up
# TIME 400
#
# PASSED
# ACTUAL 11
# EXPECTED 11
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b01
# DESCRIPTION Modulo-4 down
# TIME 550
#
```

Transcript

```
#
# PASSED
# ACTUAL 10
# EXPECTED 10
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b10
# DESCRIPTION Modulo-3 up
# TIME 1250
#
# PASSED
# ACTUAL 00
# EXPECTED 00
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b10
# DESCRIPTION Modulo-3 up
# TIME 1350
#
# PASSED
# ACTUAL 01
# EXPECTED 01
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b10
# DESCRIPTION Modulo-3 up
# TIME 1400
#
# PASSED
# ACTUAL 00
# EXPECTED 00
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b11
# DESCRIPTION Modulo-3 down
# TIME 1550
#
# PASSED
# ACTUAL 10
# EXPECTED 10
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b11
# DESCRIPTION Modulo-3 down
# TIME 1650
#
# PASSED
# ACTUAL 01
# EXPECTED 01
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b11
# DESCRIPTION Modulo-3 down
# TIME 1750
#
```

Transcript

```
PASSED
ACTUAL 10
EXPECTED 10
TESTED SIGNAL NAME (q1,q0)
INPUTS (s1,s0) = 2'b01
DESCRIPTION Modulo-4 down
TIME 650

PASSED
ACTUAL 01
EXPECTED 01
TESTED SIGNAL NAME (q1,q0)
INPUTS (s1,s0) = 2'b01
DESCRIPTION Modulo-4 down
TIME 750

PASSED
ACTUAL 00
EXPECTED 00
TESTED SIGNAL NAME (q1,q0)
INPUTS (s1,s0) = 2'b01
DESCRIPTION Modulo-4 down
TIME 850

PASSED
ACTUAL 11
EXPECTED 11
TESTED SIGNAL NAME (q1,q0)
INPUTS (s1,s0) = 2'b01
DESCRIPTION Modulo-4 down
TIME 900

PASSED
ACTUAL 00
EXPECTED 00
TESTED SIGNAL NAME (q1,q0)
INPUTS (s1,s0) = 2'b10
DESCRIPTION Modulo-3 up
TIME 1050

PASSED
ACTUAL 01
EXPECTED 01
TESTED SIGNAL NAME (q1,q0)
INPUTS (s1,s0) = 2'b10
DESCRIPTION Modulo-3 up
TIME 1150
```

```
#
# PASSED
# ACTUAL 00
# EXPECTED 00
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b11
# DESCRIPTION Modulo-3 down
# TIME 1850
#
# PASSED
# ACTUAL 10
# EXPECTED 10
# TESTED SIGNAL NAME (q1,q0)
# INPUTS (s1,s0) = 2'b11
# DESCRIPTION Modulo-3 down
# TIME 1900
```