Learning Activity 4

By Alex Clunan

ECE 4435 Computer Architecture & Design

March 2, 2025

1 Problem Statement

Design 32 bit constant, immediate extend, and register file components and connect them to the datapath.

2 Analytical Design

The 32 bit constant component was made by defining the desired value as a parameter, and assigning the output to that parameter. The immediate extend component was made by using a case statement with a ImmSrc input signal that decides what instruction type is occurring. Then the output is assigned to the correct extension of the intermediates.

Finally the register file was created. The file itself is created in an array of reg variables. These variables are written inside of an always statement, which has the positive edge of the clock and reset signals on the sensitivity list. The logic inside checks if the reset is high, and then sets all the registers to 0 using a for loop. If the reset is low, the write enable is high, and the write address is not 0, then the write data is written to the register addressed by the write address. Lastly, the read outputs were assigned to their respective register based on the two read addresses.

These components were then connected with all the other components using the given datapath file.

3 Numerical Verification

There was no verification for this stage of the assignment.

4 Summary

The 32 bit constant, immediate extend, and register file components were created. Then the datapath was used to connect all the previously used files. Attached is a full schematic of the datapath. This completes the datapath portion of our RISC-V CPU.