Alexander Brennan Clunan

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EDUCATION

University of Virginia School of Engineering & Applied Science, **Charlottesville, VA** **2022 - Present**

Candidate for Bachelor of Science in Electrical Engineering Anticipated Graduation: May 2026

- **GPA:** 3.940/4.000

JOB EXPERIENCE

University of Virginia, Charlottesville, VA **8/2023 - Present**

Teaching Assistant (TA) – Applied Physics: Electricity and Magnetism

- Teaching Assistant: Grade assignments, hold office hours, run labs, create answer keys, and coordinate with the instructor.
- Promoted to Head TA (8/2024) - Manage a team of 15 TAs, ensure grading deadlines are met, design homework and lab exercises, and help teach class content in office hours. Created a helpdesk email system designed to simplify interactions with TAs for the 480+ students in the class. Nominated for best ECE TA Award in the 2024-2025 and 2025-2026 school years.

Teaching Assistant (TA) – FPGA Digital Design **8/2025 - Present**

- Assisted students with Verilog, VHDL, and other digital design concepts. Held office hours and provided feedback on student projects, including troubleshooting hardware and code.

Ultrata LLC, Remote Charlottesville, VA **6/2025 - Present**

Software Engineering Intern

- Benchmarked performance data of Ultrata's S3 interface vs. MinIO using a proprietary benchmarking tool.
- Modified the C standard library for compatibility with the Intelligent Memory Fabric (IMF), modifying key library functions.
- Created a C++ allocator class to enable compatibility of C++ STL Vectors with IMF.
- Developed a fully functional Linux FUSE filesystem from scratch that interfaces with IMF in C/C++.

Charlottesville-Albemarle Volunteer Rescue Squad, Charlottesville, VA **8/2023 - 2/2024**

Emergency Medical Technician (EMT)

- Provided direct patient care and treatment on scene and in the ambulance. Administered medications if necessary. Transported patients to appropriate hospitals and briefed hospital staff on treatment.

RESEARCH EXPERIENCE

Swami Lab - University of Virginia **1/2025 - Present**

- **Low Latency Processing of Impedance Signals** – Developed a low-latency (<70 ms) system using a Raspberry Pi (RPi) that processes impedance signals from cells in a microchannel and triggers a sorting valve with <1 ms timing variation. Verified timing using an oscilloscope, arbitrary signal generator, and RPi generated signals.

Naval Research Enterprise Internship Program Fall Engagement - NSWC, Philadelphia Division **10/2025 - 12/2025**

- .**Condition Based Maintenance of Hydraulic Systems** - Collaborated with a team of 5 to create a whitepaper about optimal pump maintenance procedures. Specifically worked on computer/AI systems implementation topics.

OTHER EXPERIENCE

Field Programmable Gate Array (FPGA) Design Projects

- **Implemented PONG** in Verilog from scratch using pushbutton controls and a VGA output as a personal project.
- Created a two way **AES-128** text based **two-way encrypted radio communication system** using multiple PYNQ-Z1 boards.
- Designed an FPGA based synthesizer with an LFO, mixer, different waveform settings, and a delta-sigma 1-bit DAC output.

Python Audio Processing –Created a waveform generator that synthesized audio based on a Fourier Series representation as a personal project. Also created multiple audio effects including delay, reverb, and modulation as part of a class project.

RISC-V CPU

- Made a combined **RISC-V CPU** and **UART Transceiver** with support for arithmetic, logical, memory, branch, and jump instructions. Verified CPU and UART functionality with HDL testbenches and a RISC-V assembly program using ModelSim.

High Speed SRAM Schematic Design

- Designed a fully custom 64kb **SRAM** array schematic with FreePDK45 using Cadence. Compared different sense amp designs, decoder designs, and array dimensions and also improved performance through variation of component transistor width and wordline overvolting. Ran **SPICE** simulations across **PVT** boundaries to verify and best optimize a given metric.

Spiking Neural Network (SNN) Performance Analysis on the Akida PCIe Board

- Created and trained a CNN on MNIST and converted it to an SNN to compare performance on neuromorphic hardware.

Programming/Software Experience - C, C++, Verilog, Python, Quartus, Vivado, Vitis, Cadence Virtuoso, Linux, gdb, MATLAB, Microsoft Office, Lattice iCEcube/Diamond Programmer, VHDL, ModelSim, KiCad, I2C, SPI.