Lab Assignment 9
ICS 331 Logic Design & Microprocessors
Fall 2016

Completion Due: 11/22/16

Single Cycle DLX implementation

The DLX implementation will include the following modules

a) ALU environment (complete the details, 22.1.3)
b) Shifter Environment (complete the details, 22.1.4)
c) Instruction field extraction (IR environment section 22.1.5, without the inputs of IRce and clk, and without the parallel load clock-enabled register for IR)
d) PC computation (PC is a 32-bit binary string calculate PCI = PC + 1 and PCB = PCI + immediate constant, select between PCI and PCB based on a signal named "btaken")
e) Control (more details will be provided)
f) ALU Control (more details will be provided)
g) Register file environment (GPR environment 22.1.7, will be provided)
h) Instruction Memory interface (will be provided)
i) Data Memory Interface (will be provided)

Part1 Modules

i) Complete the details for the ALU environment and the Shifter environments.
ii) Implement the Instruction field extraction for I-type and R-type instructions.
iii) Implement the PC computation environment.