

## UNIT 2.

# FUNCTIONAL ELEMENTS OF A COMPUTER

### Activities-4 (review)

Computer Systems  
CFGS DAW

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## Nomenclatura

A lo largo de este tema se utilizarán distintos símbolos para distinguir elementos importantes dentro del contenido. Estos símbolos son:



Importante



Atención



Interesante

## UD02. FUNCTIONAL ELEMENTS OF A COMPUTER

### Activities-4

**(Exercise 1)** We have a hypothetical computer with this instruction set. Each character in the instruction field corresponds to a bit.

Code	Instruction	Description
LOAD RX, MMMM	00rxmmmm	Loads content of memory <i>mmmm</i> in Register <i>rx</i>
STORE MMMM, RX	01rxmmmm	Stores content of Register <i>rx</i> in memory <i>mmmm</i>
ADDi RX, RY	1000rxry	Performs $rx+ry$ and sends the result to the register <b>R1</b>
SUBi RX, RY	1100rxry	Performs $rx-ry$ and sends the result to the register <b>R2</b>
MULTi RX, RY	1111rxry	Performs $rx*ry$ and sends the result to the register <b>rx</b>

The memory has the following information (numbers are in binary representation):

Address	Content	Register	Content
0000		R1	00000000
0001		R2	00000000
0010		R3	00000000
0011			
0100			
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

And the following instructions of a program to be executed (numbers are in hexadecimal representation):

```
i1: LOAD R1, #A
i2: LOAD R2, #F
i3: ADDi R1,R2
i4: STORE #5, R1
i5: MULTi R1, R3
i6: MULTi R2, R3
i7: LOAD R1, #B
i8: LOAD R2, #E
i9: SUBi R2, R1
i10: STORE #4, R2
```

Execute each instruction and update the values of registers and memory addresses and their content. It is recommended to resolve these types of exercises using pen and paper, and without a calculator



**Remember, MAR and MDR registers are used to access the memory and get/save data.**

**i1: LOAD R1, #A**

Get the data from address #A (1010 in binary) and sends it to register R1

Address	Content	Register	Content
0000		R1	00000111 ←
0001		R2	
0010		R3	
0011			
0100			
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**i2: LOAD R2, #F**

Get the data from address #A (1010 in binary) and sends it to register R2

Address	Content	Register	Content
0000		R1	00000111
0001		R2	00000110 ←
0010		R3	
0011			
0100			
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**i3: ADDi R1,R2**

The ALU performs the addition R1+R2 and sends the result to R1

$$\begin{array}{r}
 00000111 \\
 + 00000110 \\
 \hline
 00001101
 \end{array}$$

Address	Content	Register	Content
0000		R1	00001101 ←
0001		R2	00000110
0010		R3	
0011			
0100			
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**i4: STORE #5, R1**

Address	Content	Register	Content
0000		R1	00001101
0001		R2	00000110
0010		R3	
0011			
0100			
0101	<b>00001101</b>		
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**i5: MULTi R1, R3**

R1xR3 and sends the result to R1  
(check how to multiply in Page 9.  
Unit 1)

```

      00001101
      00000000
      -----
      00000000

```

Address	Content	Register	Content
0000		R1	<b>00000000</b>
0001		R2	00000110
0010		R3	00000000
0011			
0100			
0101	00001101		
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**i6: MULTi R2, R3**

R2xR3 and sends the result to R3  
(check how to multiply in Page 9.  
Unit 1)

```

      00000110
      00000000
      -----
      00000000
  
```

Address	Content	Register	Content
0000		R1	00000000
0001		R2	<b>00000000</b>
0010		R3	00000000
0011			
0100			
0101	00001101		
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**I7: LOAD R1, #B**

Get the data from address #B (1011 in binary) and sends it to register R1

Address	Content	Register	Content
0000		R1	00001111
0001		R2	
0010		R3	
0011			
0100			
0101	00001101		
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**i8: LOAD R2, #E**

Get the data from address #E (1110 in binary) and sends it to register R2

Address	Content	Register	Content
0000		R1	00001111
0001		R2	00100001 ←
0010		R3	
0011			
0100			
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

**I9: SUBi R2, R1**

R2-R1 and sends the result to register R2  
(check how to subtract in Unit 1)

```

00100001
00001111
-----
00010010

```

Address	Content	Register	Content
0000		R1	00001111
0001		R2	<b>00010010</b> ←
0010		R3	
0011			
0100			
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		



**i10: STORE #4, R2**

**Sends the content of register R2 to the memory address #4 (0100)**

Address	Content	Register	Content
0000		R1	00001111
0001		R2	00010010
0010		R3	
0011			
0100	00010010		
0101			
0110			
0111			
1000			
1001			
1010	00000111		
1011	00001111		
1100			
1101			
1110	00100001		
1111	00000110		

