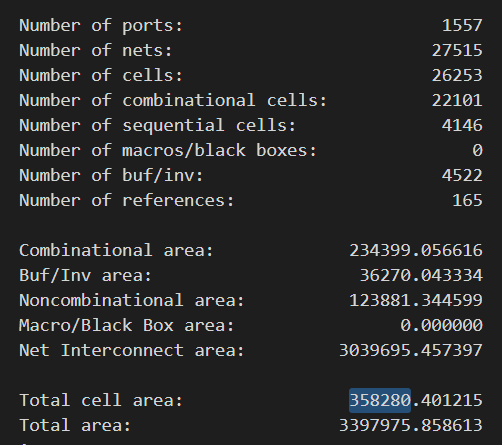
110-2 DSD Final Project Scores (RISC-V)

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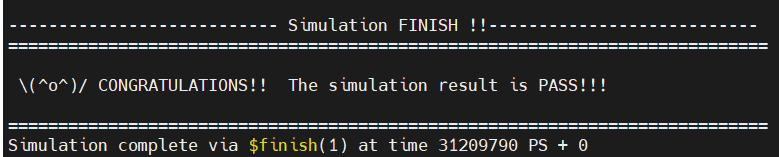
電機三 謝言鼎 B08901068

**1. Baseline**

(1) Area: (um2) 358280 um2

截圖: 

(2) Total Simulation Time of given hasHazard testbench: (ns) 31209.790 ns

截圖: 

(3) Area\*Total Simulation Time: (um2 \* ns)

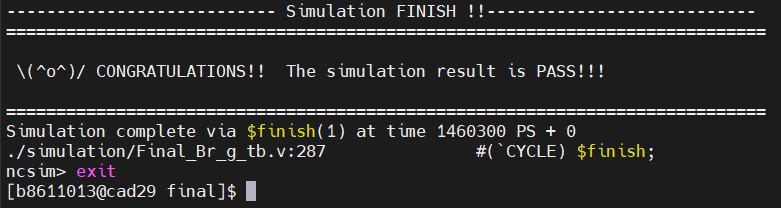
1.118E10 um2 \* ns

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

2.3 ns

**2. BrPred**

(1) Total execution cycles of given I\_mem\_BrPred: 1460.3 ns

截圖: 

(2) Total execution cycles of given I\_mem\_hasHazard:

We haven’t pass the RTL simulation yet …

截圖:

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um2)

280890 - 273547 = 7343 um2

\* note that the two designs here are both synthesized under cycle time 3.3 ns

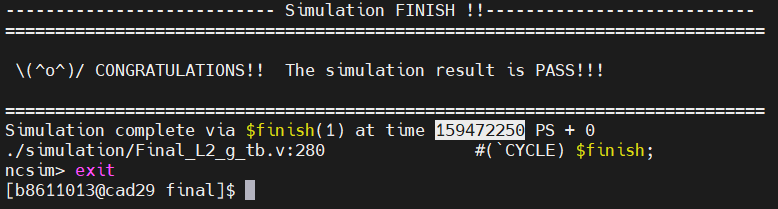
**3. L2 Cache**

(1) Average memory access time: (ns)

We are not sure hot to calculate …

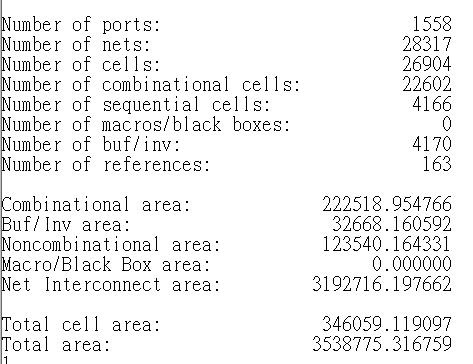
(2) Total execution time of given I\_mem\_L2Cache: (ns)

159472.250 ns

截圖: 

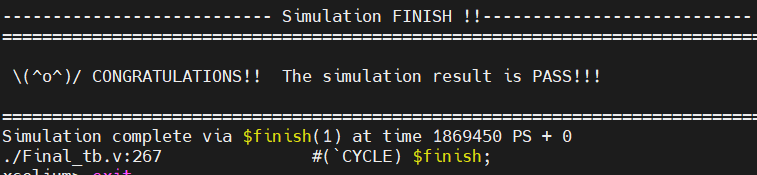
**4. Compressed instructions**

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um2)

截圖: 

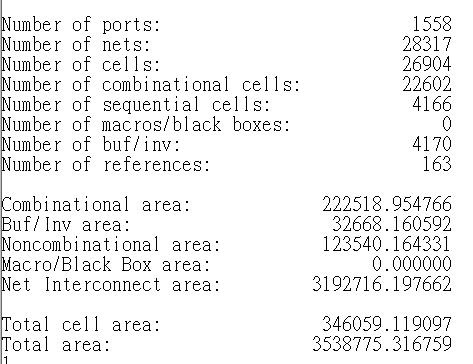
346059-325444 = 20615 um^2

(2) Total Simulation Time of given I\_mem\_compression: (ns) 1869.45 ns

截圖: 

**5. Quick sort**

(1) Area: (um2)

截圖: 

(2) Total Simulation Time of given I\_mem\_compression: (ns)

截圖: 476528.25ns

