Takt	0	1	2	3	Beschreibung
PC					*Wert Befehlszähler*
PC_in					
PS_Add,in					*Adresseingang Programmspeicher von MUX*
PS_D,out					*Datenausgang Programmspeicher*
PC Buffer Out					*Befehlszähler Stackpuffer Ausgang*
PC to Stack					*MUX Ausgang von Befehlszähler zum Stack*
PC Buffer In					*Befehlszähler Stackpuffer Eingang*
PC from Stack					*DEMUX Eingang von Stack zum Befehlszähler*
IR					*Wert Befehlsregister*
Opcode					
Address (PS)					*Dekodierte Adresse Programmspeicher*
Offset (PS)					*Dekodierter Offset Programmspeicher*
Address (DS)					*Dekodierte Adresse Datenspeicher*
Offset (DS)					*Dekodierter Offset Datenspeicher*
Data					*Dekodierte Immediate Daten*
Rd					*Dekodiertes Rs*
Rs					*Dekodiertes Rd*
RF_in					*Dateneingang Register File*
r0					*Wert r0*
r1					*Wert r1*
r2					*Wert r2*
r3					*Wert r3*
r4					*Wert r4*
r5					*Wert r5*
r6					*Wert r6*
r7					*Wert r7*
OP1					*Ausgang RF OP1 / Eingang ALU OP 1*
OP2					*Ausgang RF OP 2 / Eingang ALU OP 2*
ALU_out					*ALU Ergebnis*
Page_in					*Dateneingang Page Register*
PR					*Wert Page Register*
SP					*Wert Stackpointer*
DS_Add,in					*Adresseingang Datenspeicher von MUX*
DS_D,out					*Datenausgang Datenspeicher*
DS_D,in					*Dateneingang Datenspeicher*

ALU 2 Operanden

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	ADD r1, r2			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	ADD r1, r2		
Opcode		ADD		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd		r1		
Rs		r2		
RF_in		7		
r0	0	0	0	
r1	5	5	7	
r2	2	2	2	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1		5		
OP2		2		
ALU_out		7		
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in				
DS_D,out				
DS_D,in				

ALU 1 Operand

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	SLL r1			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	SLL r1		
Opcode		SLL		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd		r1		
Rs				
RF_in		10		
r0	0	0	0	
r1	5	5	10	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0		
OP1		5		
OP2				
ALU_out		10		
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in				
DS_D,out				
DS_D,in				

mov (Register - Register)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	MOV r2, r0			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	MOV r2, r0		
Opcode		MOV		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd		r2		
Rs		r0		
RF_in		2		
r0	2	2	2	
r1	5	5	5	
r2	0	0	2	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1		0		
OP2		2		
ALU_out		2		
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in				
DS_D,out				
DS_D,in				

psh (Register - Stack)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	PSH r1			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	PSH		
Opcode				
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd				
Rs		r1		
RF_in				
r0	0	0	0	
r1	5	5	5	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2		5		
ALU_out		5		
Page_in				
PR	0	0	0	
SP	0	0	1	
DS_Add,in		0		
DS_D,out				
DS_D,in		5		
DS(0)			5	
DS(1)				
DS(2)				

pll (Stack - Register)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	PLL r0			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	PLL r0		
Opcode		PLL		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd		r0		
Rs				
RF_in		5		
r0	0	0	5	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	
SP	1	1	0	
DS_Add,in		0		
DS_D,out		5		
DS_D,in				
DS(0)	5	5	5	
DS(1)				
DS(2)				

stz (Register - DS)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	STZ r0, 1			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	STZ r0, 1		
Opcode		STZ		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)		1		
Data				
Rd				
Rs		r0		
RF_in				
r0	7	7	7	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	29	29	29	
OP1				
OP2		7		
ALU_out		7		
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in		30		
DS_D,out				
DS_D,in		7		
DS(29)				
DS(30)			7	
DS(31)				

ldz (DS - Register)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	LDZ r4, 2			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	LDZ r4, 2		
Opcode		LDZ		
Address (PS)				
Offset (PS)				
Address (DS)		2		
Offset (DS)				
Data				
Rd		r4		
Rs				
RF_in		3		
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	3	
r5	0	0	0	
r6	0	0	0	
r7	29	29	29	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in		31		
DS_D,out		3		
DS_D,in				
DS(29)				
DS(30)				
DS(31)	3	3	3	

st (Register - Datenspeicher)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	ST 0, r2			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	ST 0, r2		
Opcode		ST		
Address (PS)				
Offset (PS)				
Address (DS)		0		
Offset (DS)				
Data				
Rd				
Rs		r2		
RF_in				
r0	0	0	0	
r1	0	0	0	
r2	46	46	46	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2		46		
ALU_out		46		
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in		0		
DS_D,out				
DS_D,in		46		
DS(0)			46	
DS(1)				
DS(2)				

ld (Datenspeicher - Register)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	LD r0, 1			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	LD r0, 1		
Opcode		LD		
Address (PS)				
Offset (PS)				
Address (DS)		1		
Offset (DS)				
Data				
Rd		r0		
Rs				
RF_in		46		
r0	0	0	46	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in		1		
DS_D,out		46		
DS_D,in				
DS(0)				
DS(1)	46	46	46	
DS(2)				

ldi (Immediate - Register)

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	LDI r3, 7			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	LDI r3, 7		
Opcode		LDI		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data		7		
Rd		r3		
Rs				
RF_in		7		
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	7	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in				
DS_D,out				
DS_D,in				

jpa

Takt	0	1	2	3
PC	0	1	11	
PC_in	1	11	12	
PS_Add,in	0	10	11	
PS_D,out	JPA 10	PS(10)		
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR		JPA 10	PS(10)	
Opcode		JPA		
Address (PS)		10		
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd				
Rs				
RF_in				
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	0
SP	0	0	0	0
DS_Add,in				
DS_D,out				
DS_D,in				

bra

Takt	0	1	2	3
PC	3	4	9	
PC_in	4	9	10	
PS_Add,in	3	8	9	
PS_D,out	BRA 5	PS(8)		
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR		BRA 5	PS(8)	
Opcode		BRA		
Address (PS)				
Offset (PS)		5 - 1		
Address (DS)				
Offset (DS)				
Data				
Rd				
Rs				
RF_in				
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	0
SP	0	0	0	0
DS_Add,in				
DS_D,out				
DS_D,in				

brbs / brbc (taken)

Takt	0	1	2	3
PC	0	1	8	
PC_in	1	8	9	
PS_Add,in	0	7	8	
PS_D,out	BRBS Z, 7	PS(7)		
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR		BRBS Z, 7	PS(7)	
Opcode		BRBS		
Address (PS)				
Offset (PS)		7 - 1		
Address (DS)				
Offset (DS)				
Data				
Rd				
Rs				
RF_in				
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR				
SP				
DS_Add,in				
DS_D,out				
DS_D,in				

call/ret

Takt	0	1	2	3	4	5	6
PC	300	301	301	101	102	102	302
PC_in	301	101	101	102	103	302	303
PS_Add,in	300	100	100	101	102	301	302
PS_D,out	CALL 100	PS(100)	PS(100)	RET		PS(301)	
PC Buffer Out	0	0	0x2D	0x2D	0x2D	0x2D	0x2D
PC to Stack		0x01	0x2D				
PC Buffer In	0	0	0	0	0	0x2D	0x2D
PC from Stack					0x2D	0x01	
IR		CALL 100	CALL 100	PS(100)	RET	RET	PS(301)
Opcode		CALL	CALL	z.B. NOP	RET	RET	
Address (PS)		100	100				
Offset (PS)							
Address (DS)							
Offset (DS)							
Data							
Rd							
Rs							
RF_in							
r0	0	0	0	0	0	0	0
r1	0	0	0	0	0	0	0
r2	0	0	0	0	0	0	0
r3	0	0	0	0	0	0	0
r4	0	0	0	0	0	0	0
r5	0	0	0	0	0	0	0
r6	0	0	0	0	0	0	0
r7	0	0	0	0	0	0	0
OP1							
OP2							
ALU_out							
Page_in							
PR	0	0	0	0	0	0	0
SP	0	0	1	2	2	1	0
DS_Add,in		0	1		1	0	
DS_D,out					0x2C	0x01	
DS_D,in		0x01	0x2D				
DS(0)			0x01	0x01	0x01	0x01	0x01
DS(1)				0x2D	0x2D	0x2D	0x2D
DS(2)							

brbs / brbc (not taken)

Takt	0	1	2	3
PC	0	1	8	
PC_in	1	2	9	
PS_Add,in	0	1	8	
PS_D,out	BRBS Z, 7	PS(2)		
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR		BRBS Z, 7	PS(2)	
Opcode		BRBS		
Address (PS)				
Offset (PS)		7 - 1		
Address (DS)				
Offset (DS)				
Data				
Rd				
Rs				
RF_in				
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR				
SP				
DS_Add,in				
DS_D,out				
DS_D,in				

NOP

Takt	0	1	2	3
PC	0	1	2	
PC_in	1	2	3	
PS_Add,in	0	1	2	
PS_D,out	NOP			
PC Buffer Out	0	0	0	
PC to Stack				
PC Buffer In	0	0	0	
PC from Stack				
IR	---	NOP		
Opcode		NOP		
Address (PS)				
Offset (PS)				
Address (DS)				
Offset (DS)				
Data				
Rd				
Rs				
RF_in				
r0	0	0	0	
r1	0	0	0	
r2	0	0	0	
r3	0	0	0	
r4	0	0	0	
r5	0	0	0	
r6	0	0	0	
r7	0	0	0	
OP1				
OP2				
ALU_out				
Page_in				
PR	0	0	0	
SP	0	0	0	
DS_Add,in				
DS_D,out				
DS_D,in				