EGCP 1010
Digital Logic Design (DLD)
Laboratory #1

Introduction to the

DLD Laboratory

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on

September 12, 2007

Lab Partner:
None

Objective:

The goal of this laboratory is to teach the student to use the laboratory equipment, perform procedures, and learn proper techniques of DLD. The student should become familiar with the Low-Power Schottky (LS) Transistor-Transistor Logic (TTL) chip family. The student should also become familiar with the Complete Analog/Digital Electronics Trainer (CADET II) Socket Board, the FLUKE 45 Digital Multimeter (DMM), and laboratory accessories such as wires, wire stripper, and chip pullers.

Procedure and Results:

For this lab the class was introduced to part numbering, pin numbering, TTL chips (74LS series), proper lab procedures, proper lab report procedures, and National Semiconductor TLL Data Sheets. From plugging in a DMM to a CADET II Trainer the data is Table 1 was obtained.

Table 1: Supply Voltages Present on CADET II Socket Board

Voltage Source	Terminal Color	Minimum Voltage (if adjustable) (volts)	Maximum Voltage (of fixed voltage) (volts)
Fixed	Red	Not Applicable (N/A)	5.00
Variable Positive	Yellow	1.27	19.38
Variable Negative	Blue	-1.26	-19.10

Next, a 74LS00 (four (4) NAND)chip was connected to the +5V power supply and ground. The inputs for gate one (1) were connected to binary switches S1 and S2. The inputs were switched from zero (0) to one (1) in every possible combination and the results were recorded. The inputs for gate two (2) were then connected to binary switches S1 and S2 to ensure that the same results would be given. The results are shown in Table 2 below.

Table 2: Output Voltages of Two (2) Different NAND Gates of a Single 74LS00 Chip

Row	INPUT A (logic value)	INPUT B (logic value)	Output Voltage Gate 1 (volts)	Output Voltage Gate 2 (volts)
0	0	0	4.59	4.59
1	0	1	4.59	4.59
2	1	0	4.59	4.59
3	1	1	0.11	0.11

The results from gate one (1) and gate two (2) were almost identical. When both input A and input B were both set to one (1), gate two actually varied between 0.11 and 0.12. 0.11 was recorded because it seemed to be the most frequent result.

Next, voltage measurements were taken at several input voltages to see what the output voltage was at that input voltage. One of the inputs of the 74LS02 chip was grounded. This allowed the other input to be adjustable between 0 and +5 Volts by using a variable resistor. The results from these tests are shown in Table 3. The voltage characteristic curve is shown in Figure 1.

Table 3: Output Voltages for Various Input Voltages

INPUT A (logic value)	INPUT B (logic value)	Output Voltage (volts)		INPUT A (logic value)	INPUT B (logic value)	Output Voltage (volts)
1	0.00	4.19		1	0.96	3.39
1	0.50	3.97		1	1.05	2.61
1	0.75	3.81		1	1.11	1.97
1	0.90	3.63		1	1.16	0.37
1	1.00	3.07		1	1.18	0.12
1	1.10	2.03		1	1.24	0.11
1	1.30	0.11		1	1.30	0.11
1	1.50	0.11		1	1.40	0.11
1	2.00	0.11		1	1.48	0.11
1	5.00	0.11		1	1.64	0.11

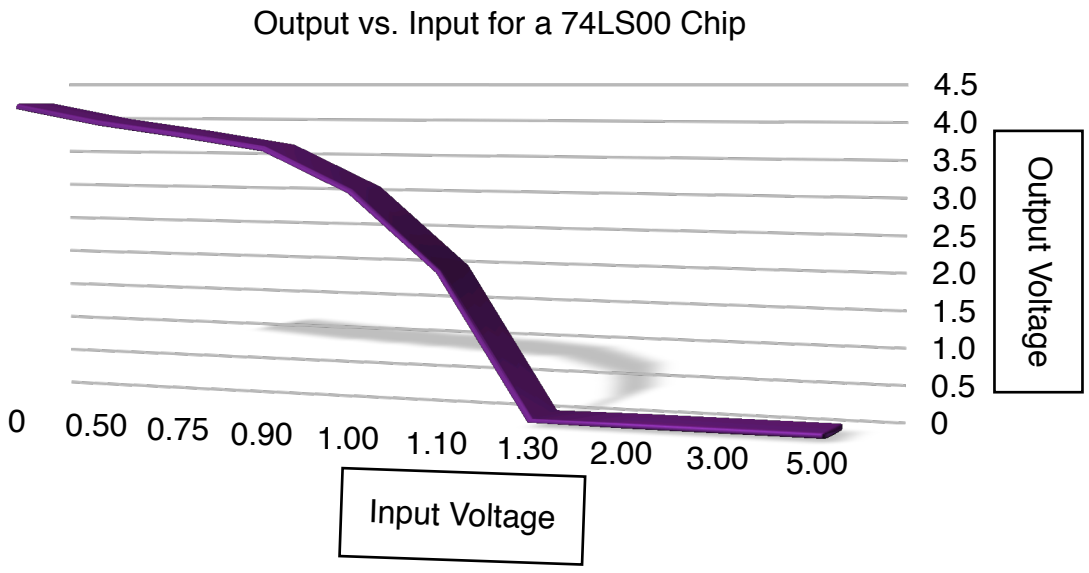

Figure 1: Output vs. Input For A 74LS00 With One Input Grounded

As shown in Table 3 and Figure 1, the output had a high of 4.19 Volts. The output decreased slowly at first as the input voltage increased, but shortly after the input voltage increased passed one (1), the output voltage decreased rapidly, dropping to a steady output of 0.11 Volts.

Finally, results were taken with a floating pin, meaning one of the inputs to the gate was not connected. With input A, which was still connected to S1, set to high (1), the output was 0.11 Volts. This was similar to row three (3) of Table 2, which represented a logic high.

Conclusion and Suggestions:

To me, this lab illustrated the uses of circuits, chips, and gave a physical representation of the digital logic which I have been learning about in class. It taught me the uses of the CADET II Trainer board along with the DMM which we attached to the CADET II Trainer. It gave me a better understanding of TTL chips. The lab went quite smoothly once I figured out the general configuration of the CADET II, which took me about 15 minutes.

I accidently bent one of the pins on the 74LS00 chip I was using before I realized how fragile they were. Luckily it bent back fairly easily, and I pushed it back in to test it and make sure it still worked. Moments after this, we were cautioned about how flimsy the chips were. A warning during the instructions, before we actually started using the chips, would have been useful to avoid that issue.

Questions:

I. Using the TTL Data Sheet for the 74SL00, determine the "correct" output voltage range for a logic High and a logic Low. These are typically referred to as V_{OH} (Voltage Output High) and V_{OL} (Voltage Output Low). Compare your results to your data. Was your chip within tolerance?

V_{OH} = Min _2.7_ volts; typical _3.4_ volts.
V_{OL} = Max _0.5_ volts; typical _0.35_ volts.
My chip performed within tolerance.

II. Using the TTL Data Sheet for the 74SL00 determine the "correct" input voltage for a logic High and logic Low. These are typically referred to as V_{IH} (Voltage Input High) and V_{IL} (Voltage Input Low). Compare your results to the data sheet. Was your chip within tolerance?

V_{IH} = Min _2_ volts.
V_{IL} = Max _0.8_ volts.
My chip performed within tolerance.

III. Find the part number and number of gates per chip for the following gates.

Table 4: TTL Gate Names, Part Numbers, and Number of Gates

Number	Gate Name	TTL Part Number	Number of Gates Per Chip
1	3 Input NAND Gate	74LS10	3
2	2 Input XOR Gate	74LS86	4
3	INVERTER Gate	74LS04	6
4	2 Input AND Gate	74LS08	4
5	2 Input OR Gate	74LS02	4
6	3 Input AND Gate	74LS11	3