Laboratory 3: Inverter Layout

ECE 429: Introduction to VLSI Design

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Acknowledgement: I acknowledge all of the work (including figures and codes) belongs to me and/or persons who are referenced.

Signature: Alexander Lukens

1. Introduction

In this laboratory session, students will be introduced to layout design for CMOS circuits. This will involve defining the various physical regions of a CMOS design, following the strict design rules set in place by the FreePDK45 library. This design will be completed in the Cadence Design suite by defining a "layout" cellview for the inverter cell created in Laboratory 2. After completing the layout to the correct specifications, students will verify that the functionality of their design is identical to that of the "schematic" cellview using Calibre LVS. Then, students will utilize Calibre PEX to extract the parasitic capacitances from the layout design and export this to a SPICE Netlist. This output has the benefit of being much more specific to real-world constraints than the netlist created from the schematic cellview.

After running the design through a SPICE simulation, students will use Cosmoscope to plot their results and compare these results to obtained from Laboratory 2.

2. Theory/Pre-Lab

CMOS designs use numerous design "masks" to define the various separate regions that make up the physical design. These designs can be very complex, so Electronic Design Automation (EDA) software is utilized to create a physical layout for the circuit. One such EDA software suite is Cadence Virtuoso. In Cadence virtuoso, each of the individual layers can be modeled and tested against the physical design rules for a certain process, reducing the time required to design an integrated circuit dramatically.

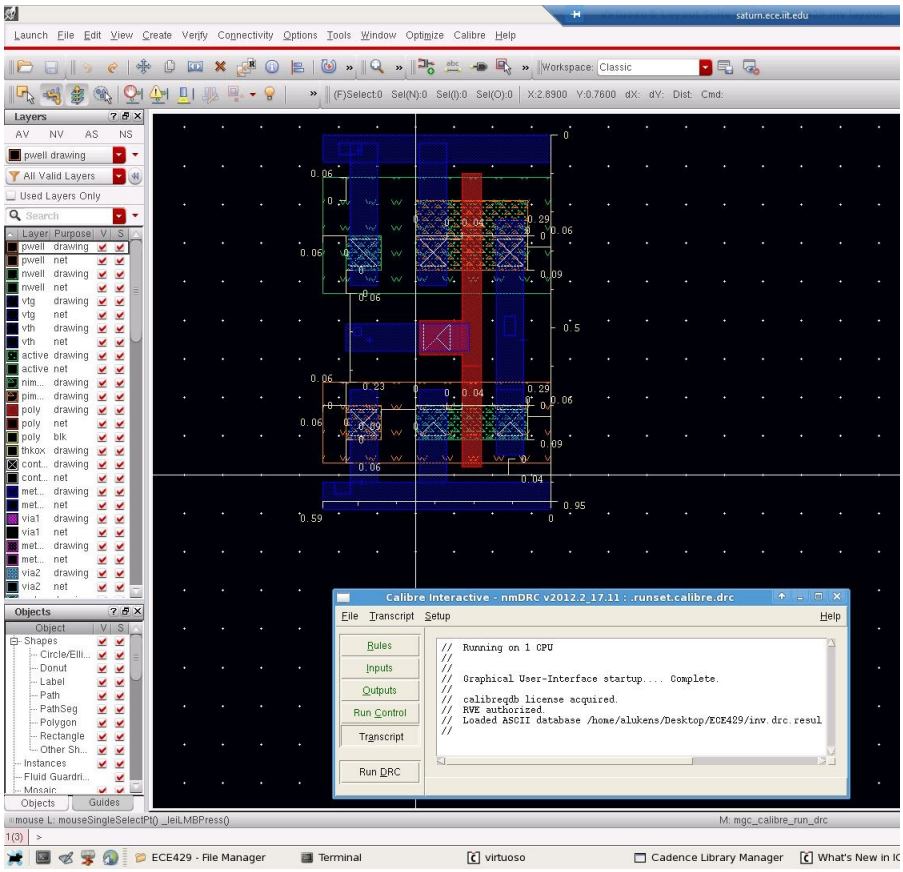
Inside Cadence Virtuoso, there are a variety of tools available to further decrease the probability of design errors and overall design time. The first tool is design rule checking (DRC). This allows for the physical layout of a circuit to be checked for compliance with the design rules of a certain process (on which the circuit will eventually be produced). This ensures that when the circuit is created, it will not fail due to physical spacing errors. Another tool is Layout vs Schematic (LVS) testing. LVS testing allows the physical layout produced in Cadence Virtuoso to be compared with a schematic cellview to ensure that they will function identically. This means that the overall design can first be created as a schematic (to first ensure the digital logic design functions correctly) before spending time designing the physical layout.

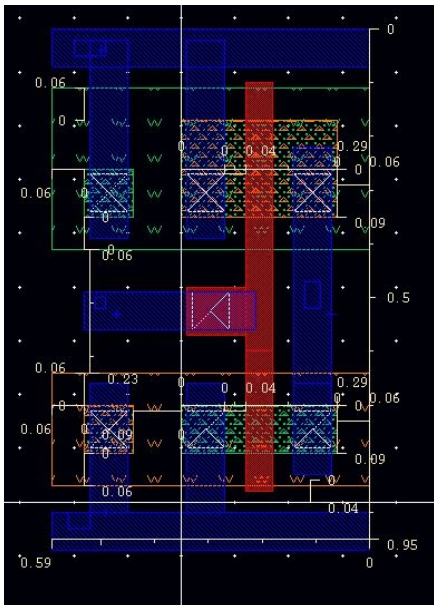
After the validity of the physical layout is confirmed, Calibre PEX can be utilized to export the layout, with complex attributes like parasitic capacitance, to a SPICE Netlist. This will allow for the simulation and modeling of the circuit. The results from the SPICE simulation can be run through Cosmoscope to display the response of the circuit and approximate how it will respond when operated in real-life.

3. Implementation

In this laboratory, students will design and verify a CMOS inverter layout. To start, students opened Cadence Virtuoso and created a new cellview of type "layout" under the inverter

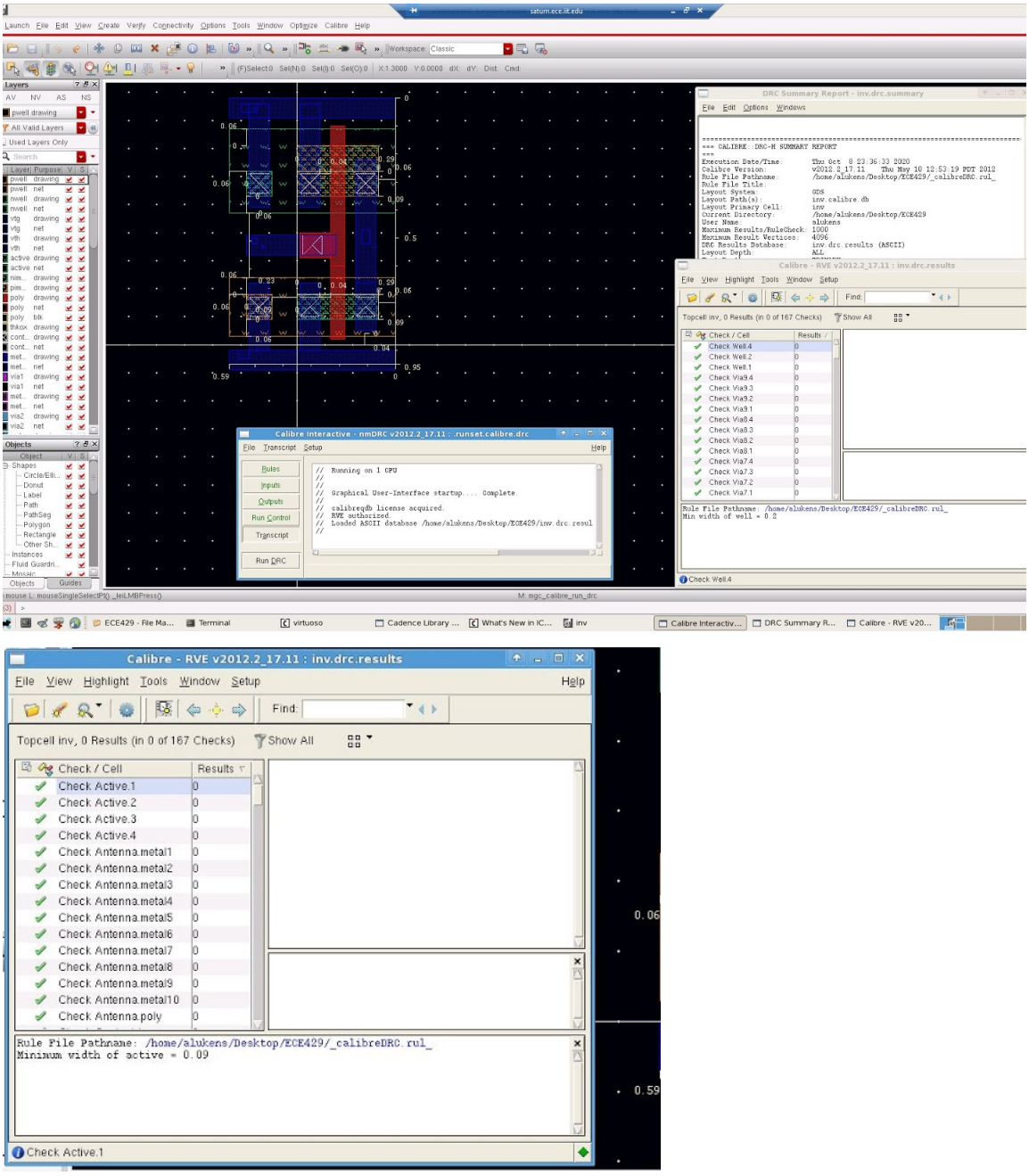
cell. This cellview will hold the physical implementation for how the circuit can be created using the FreePDK45 library's design constraints. The finalized design, including PMOS, NMOS, well, voltage rails, and metal contacts is shown below.





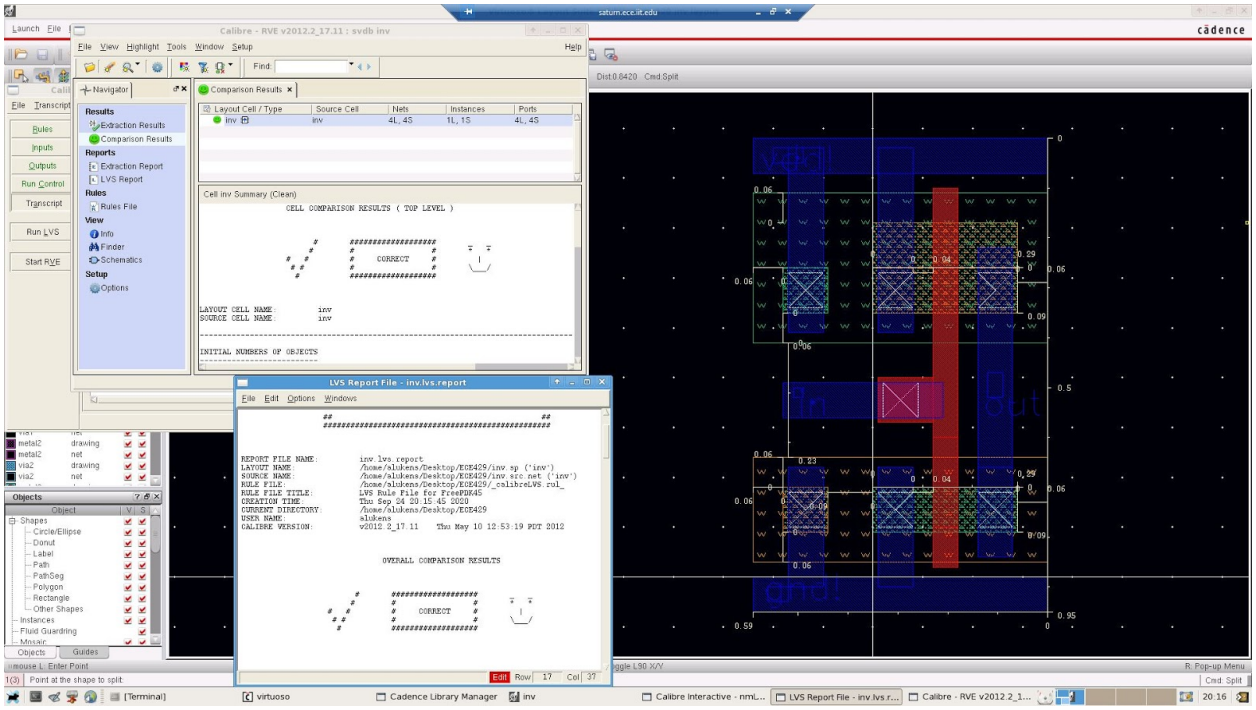
Finalized Layout Cellview for inverter

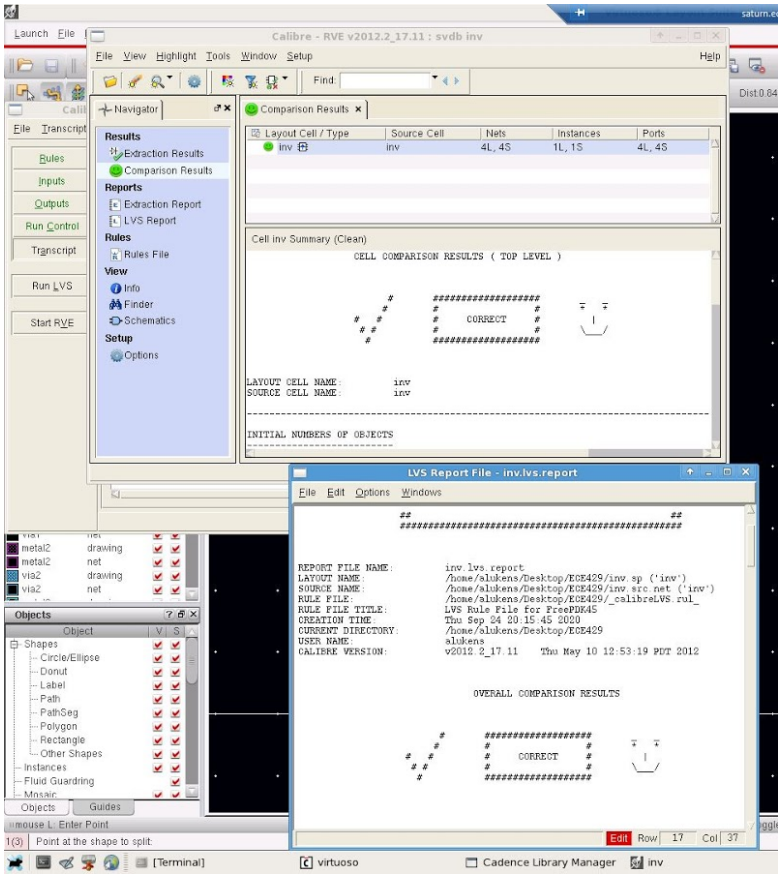
Throughout the process of designing the layout for the CMOS inverter, the design rules were checked several times to ensure compliance with the FreePDK45 library's rules. Checking for compliance often decreases the chance that a designer will have to backtrack and redo an area of a design, potentially wasting time. To check for compliance, the Virtuoso software includes a tool called Calibre that will check the entire layout very rapidly, and give an itemized list of design rule violations. It is also possible to catch errors before they happen by using the "ruler" tool built into Cadence Virtuoso that allows the user to measure distances inside the layout. The results of the Calibre DRC is shown below.



Design Rule Checking (DRC) Results

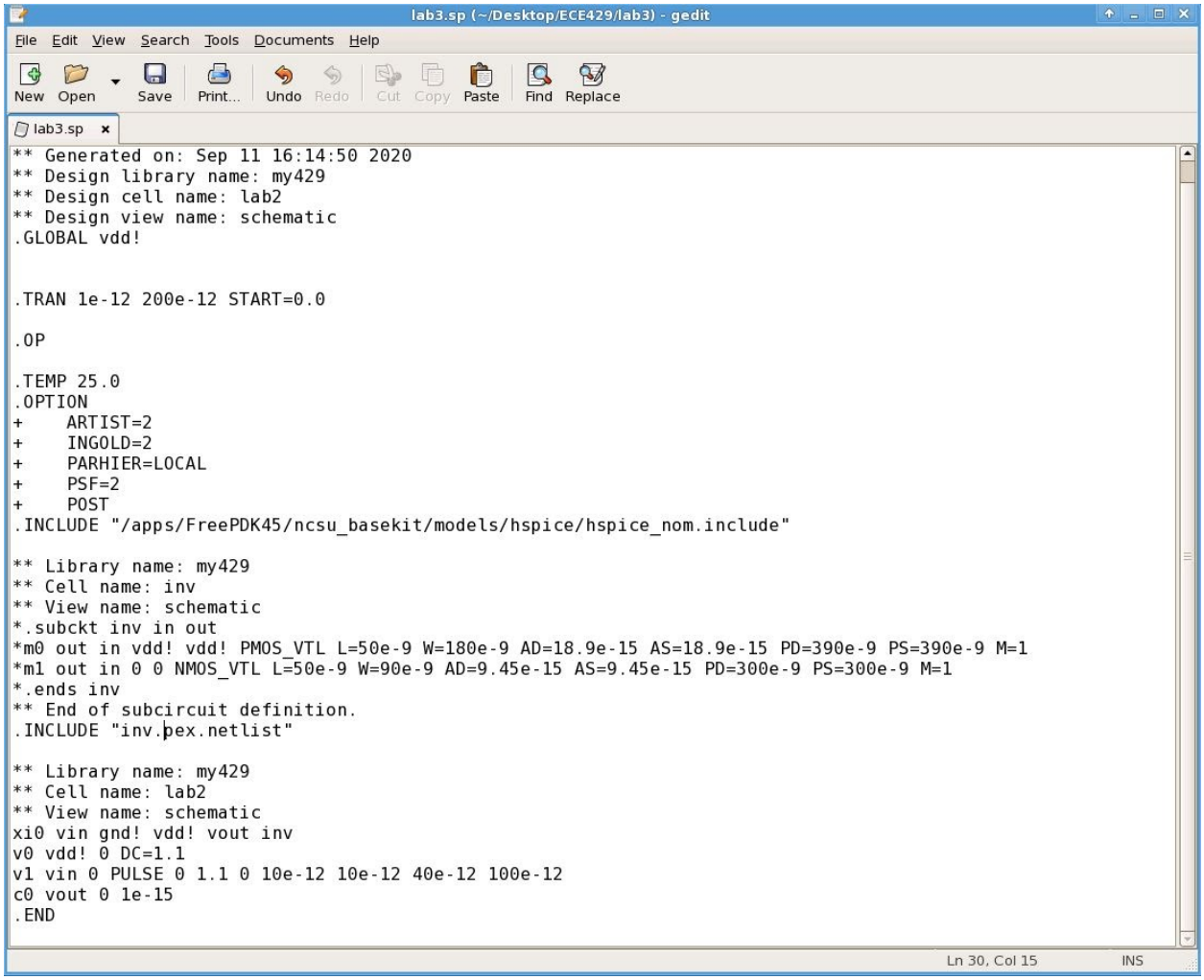
After ensuring compliance with the FreePDK45 design rules, students ensured that the layout functions identically to the schematic cellview for the inverter. This check is done to ensure that when the layout is utilized in an actual design, that the circuit will function as the schematic implies. The tool that completes this check is Calibre Layout vs Schematic (LVS). In order to correctly judge the functionality of the layout, all pins present on the schematic cellview (in, out, Vdd, GND) must all be correctly labeled on the layout. This is done by placing labels on the corresponding areas of the layout.





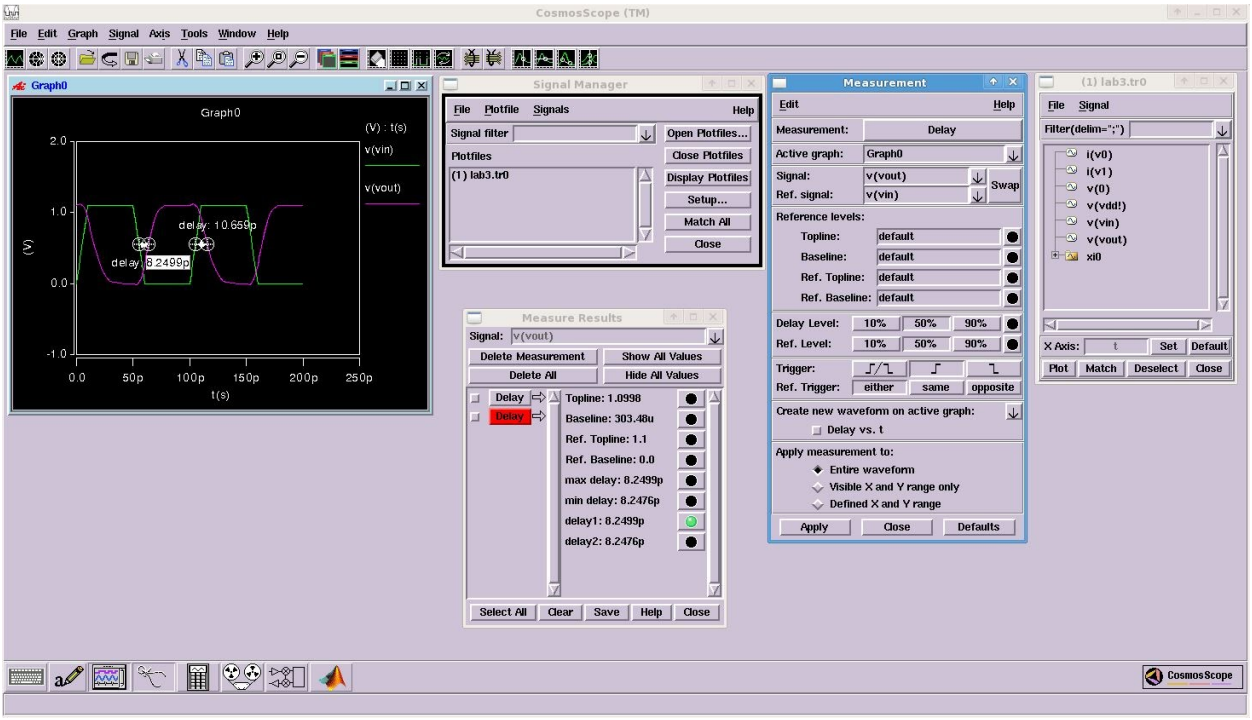
Calibre LVS Results

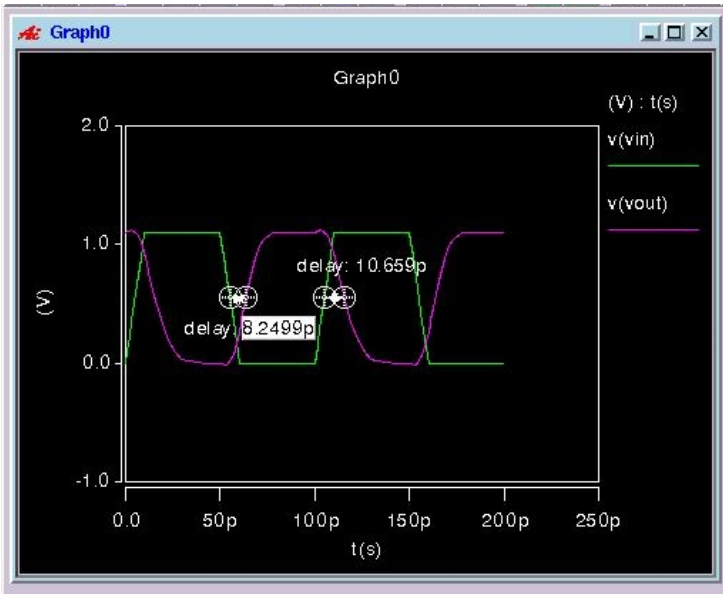
Once the design passes Calibre LVS, the layout can be considered functionally identical to the schematic version of the cell. Some attributes that may vary are load capacitance, rise/fall times, etc. In order to simulate the circuit layout in SPICE, Calibre PEX, or Parasitic Extraction can be performed that will determine the parasitic capacitances of the transistors, which can be utilized to perform a very accurate simulation of the cell. The netlist produced from Calibre LVS, and modified to save waveforms, is shown below.



Modified SPICE Netlist from PEX

HSPICE simulation was then performed on the layout cellview of the inverter using the netlist, and the results were imported into Cosmoscope for analysis. As expected, the transient analysis of the layout is very similar to the results obtained using the testing circuit (from laboratory 2). Using the schematic from laboratory 2, the rising time was found to be 7.13ps, and the falling time to be 9.163ps. Using the layout created during this laboratory session, the rising time was found to be 8.25ps, and the falling time was found to be 10.66ps. The graph obtained from the layout SPICE simulation is shown below.





SPICE results with delay calculations

Deliverables

• What determines the minimum transistor width and length for a specific technology?

The minimum transistor width and length for a process are determined by the ability of the specific technology to make consistent features at a given transistor size. In other words, the minimum length and width are determined to be the size the process can accurately and reliably

produce the transistor. The smaller the process technology, the more precise the design can be, allowing for smaller transistors to be made

• Why should well-taps connect to implanted regions instead of the wells directly?
Connecting well-taps to an implanted region allows for better connection and bidirectional current flow to the potential the tap is connected to. Specifically, connecting to an implanted region reduces the resistance to the potential, resulting in a stronger connection to the potential.

• What are the benefits of a twin-well process?
A twin well process allows designers to dope regions of PMOS and NMOS transistors independently, allowing for advanced CMOS designs that utilize multiple Vth potentials (controlled by doping level). If only a single well process was used, the doping levels could only be controlled in one of the regions.

• How do the delays of your inverter layout compare to that of the schematic in Lab2? Do you expect them to be larger or smaller? Why?
The delays found in this laboratory are similar to the delays found in laboratory 2. The delays are slightly larger than those found using the schematic in laboratory 2, due to my non-optimal layout of the gate. If the quickest layout was selected, the delays would be smaller.

4. Conclusion

This lab should be considered a success. Students were successfully able to design and implement a CMOS layout for the inverter cell created in Laboratory 2. The layout obtained during this laboratory provided a physical implementation for the cell that can be utilized in more complex designs. Furthermore, the layout cellview simulation has a higher accuracy than the simulation performed on the schematic cellview.

At the conclusion of this laboratory, students have gained valuable experience in CMOS layout and verification using Cadence Virtuoso and design tools such as Calibre LVS and DRC. These skills can be applied to larger and more complex circuits to accurately simulate the real world performance of a CMOS design.

In future laboratory sessions, the inverter layout created here will be used to design and implement more complex circuits using CMOS logic. Students will also utilize their skills in CMOS layout to compare and verify the functionality of a layout compared to the more general schematic design.

5. References

- Choi, Ken. “ECE 429 Laboratory 3 Manual.” Illinois Institute of Technology, 24 Sept. 2020.

- Kim, Victoria. “ECE 429 Guideline for Writing Report & Grading Criteria.” Illinois Institute of Technology, 24 Sept. 2020.