ECE 429 Laboratory 6: Carry-Ripple Addition I

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Acknowledgement: I acknowledge all of the work (including figures and codes) belongs to me and/or persons who are referenced.
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1 Introduction

In this laboratory, students will create the schematic cellview for a full adder. This will require students to design and implement the transistor level schematic of a full-adder using the mirror adder model. This results in a circuit that is far more complex than circuits designed in previous laboratory sessions.

After the schematic is created, it will be compared to the functionality of a Verilog file performing an addition operation using Formality ESP. Students will then calculate the propagation delay

2 Theory\Pre-lab

This laboratory is the first of 3 that will implement the hierarchical design model first introduced in laboratory 5. Hierarchical design refers to the design of a CMOS circuit using a combination of multiple cells. Furthermore, in hierarchical design, more complex cells are made from simplified cells. This allows some abstraction in a VLSI design, as the complex cells can be implemented instead of each single transistor. This drastically simplifies the design process of complex circuits, while retaining full detail retention of the components in the design.

During the next 3 labs, a full-adder cell will be created, and then this cell will be used multiple times to implement a 4-bit ripple adder. By using a full-adder in the hierarchical design structure, 4 duplicates of this cell can be utilized and linked together to create a 4-bit adder. This drastically reduces the time required to design the adder, compared to designing it completely from scratch.

A transistor schematic of a single bit mirror adder is shown below:

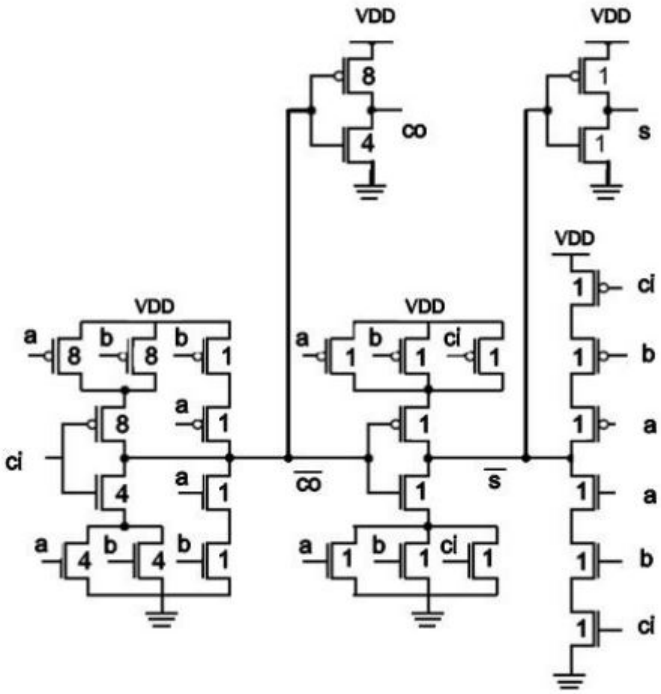

Figure 1: Transistor Schematic for Full Adder

3 Implementation

The first step in implementing a full adder using CMOS logic is to create a cell to hold the various cellviews in Cadence Virtuoso, and then design the schematic cellview. The final result is shown below.

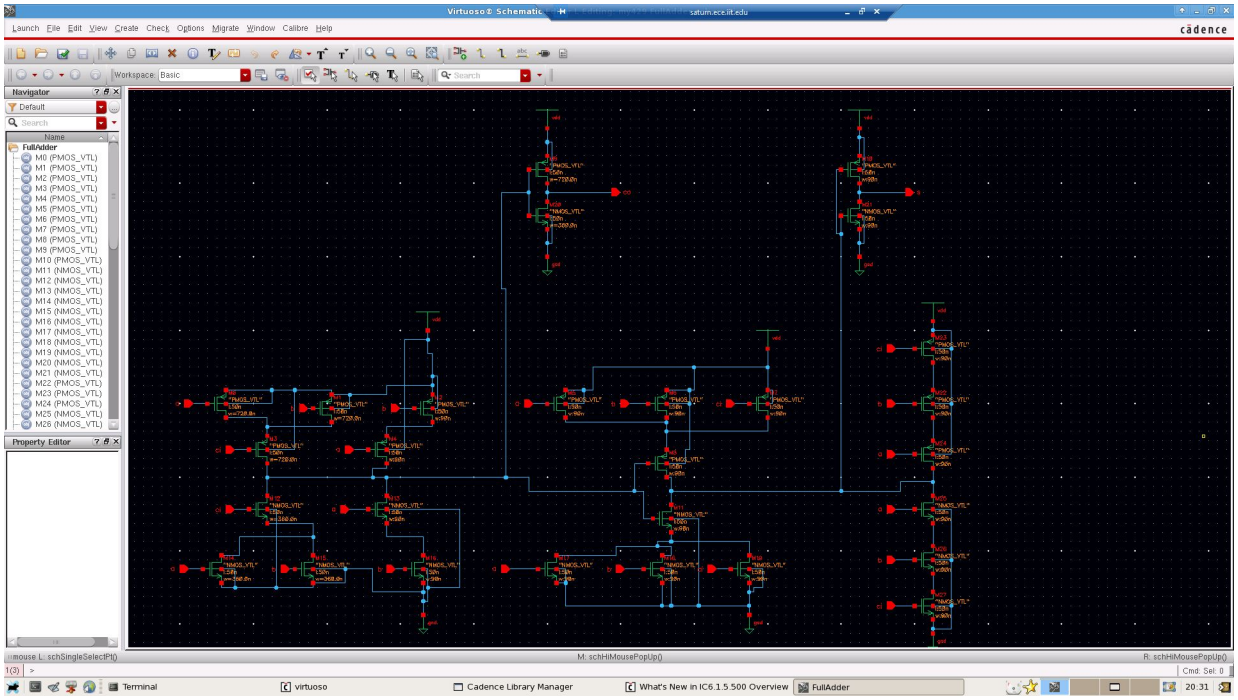

Figure 2: Schematic Cellview for Full Adder

To test this design, a testing circuit was created. This circuit will have three voltage source objects connected to each of the full adder inputs to allow the designer to test various input transitions into the full adder. The outputs from the full adder will be connected to capacitors to provide output load capacitance.

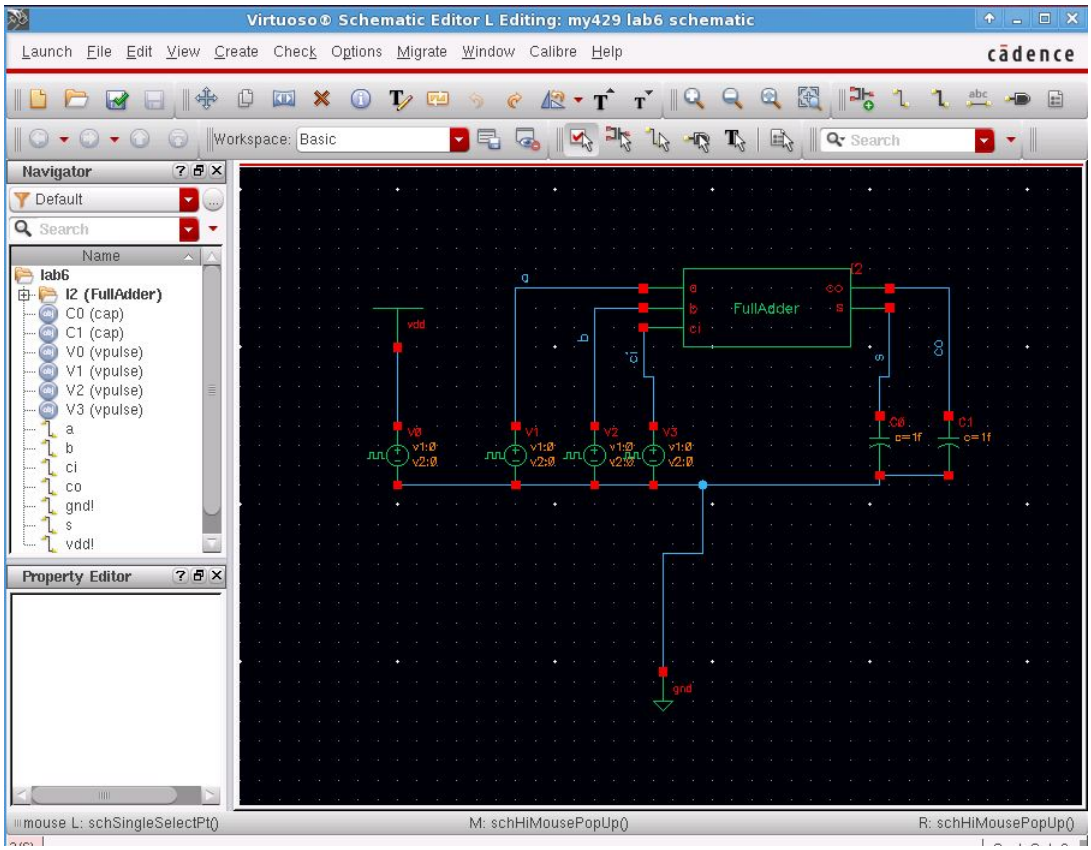

Figure 3: Testing Circuit for Full Adder

In order to test various input transitions, a SPICE netlist was exported for the testing circuit. Then, the input transitions were manipulated to test for the propagation delays when the inputs a,b,ci go from 010→011 and 100→101. The modified netlists and result values are shown below

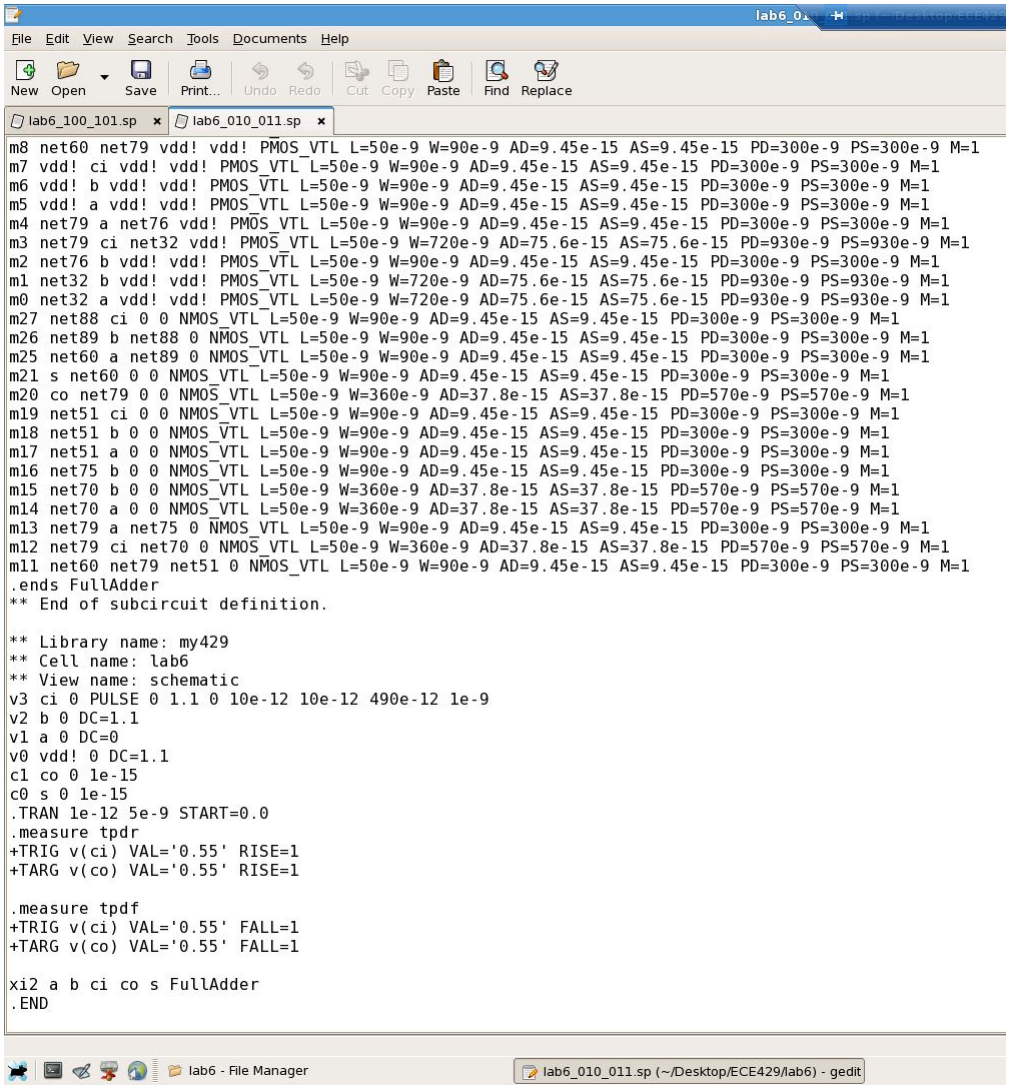

Figure 4: 010→011 Transition Netlist

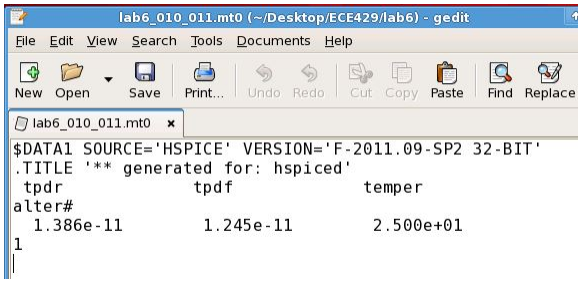

Figure 5: 010→011 Propagation Delays

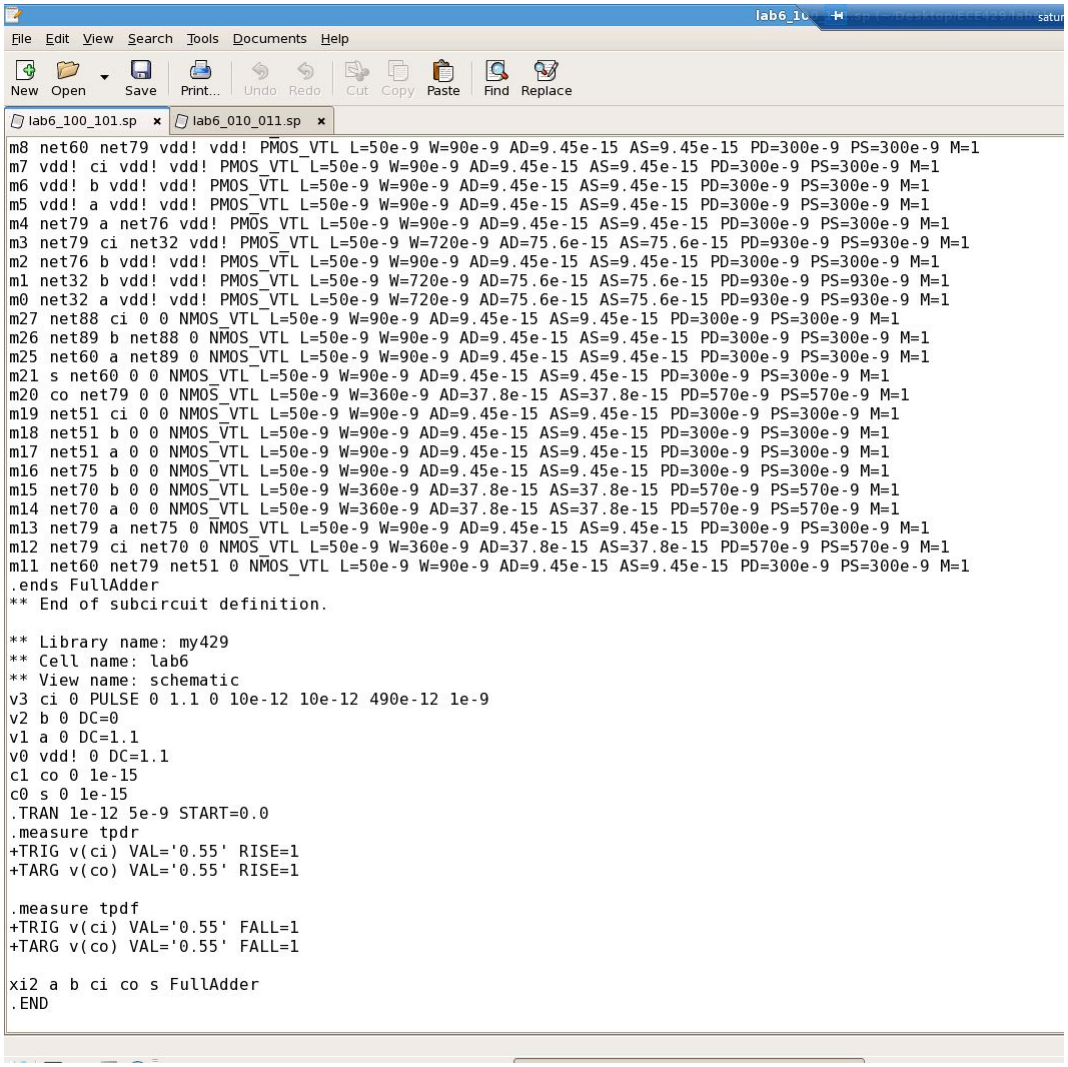

Figure 6: 100→101 Transition Netlist

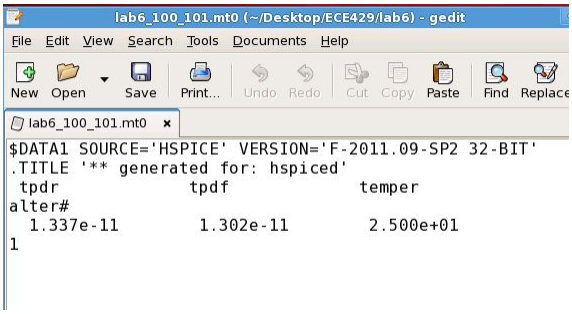

Figure 7: 100→101 Propagation Delays

In order to fully ensure the functionality of the full adder, the schematic design was tested against a verilog file performing the function of a full adder. This verilog file and the result from Formality ESP equivalence testing are shown below.

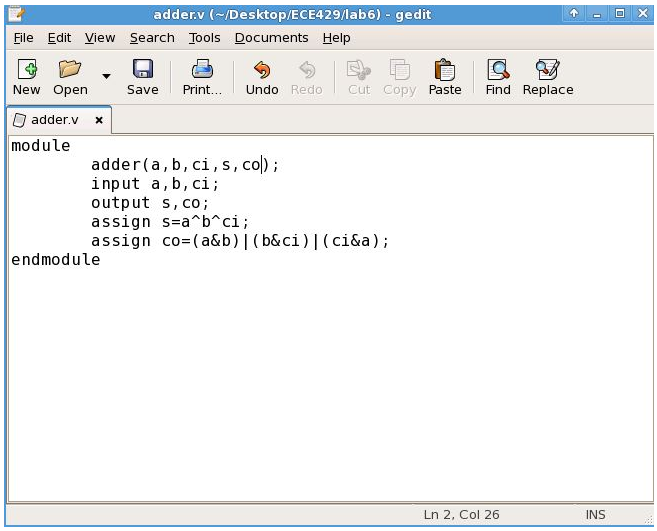

Figure 8: Adder.v Verilog File

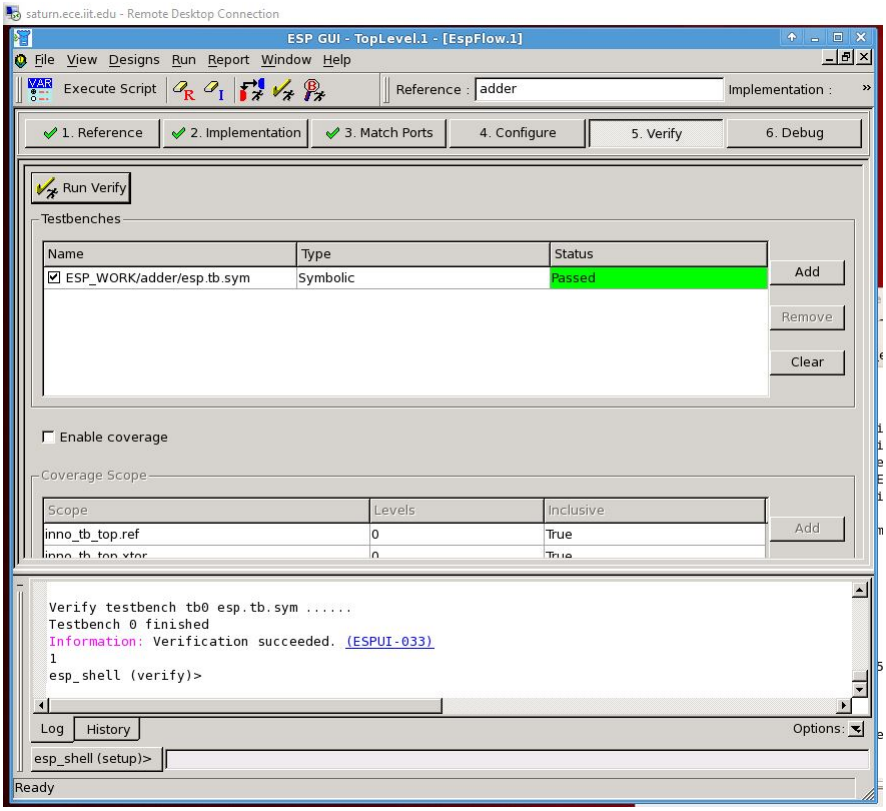

Figure 9: Equivalence Checking Results

4 Deliverables

- ***It is known that the most timing-critical path in a full adder is from ci to co. For the circuit to compute co, why are the transistors sized differently and why is ci used as the inner inputs?***

  The carry-in to carry-out path is the most time critical in a ripple adder, because when multiple adders are connected together, the next ripple adder is waiting on the carry-out value of the previous adder. By using CI as the inner input, the rise/fall time due to CI is minimized, as all other transistor capacitance are charged (by the A and B values) by the time the CI signal is received. This in turn minimizes the path delay of the ripple adder, decreasing the overall delay of the circuit. By using different sized transistors, the resistance and capacitance of the CI/CO circuit are selected to decrease the delay of the path.

5 Bonus Work

In order to produce a model for the propagation delay of the mirror adder from ci to co, the linear delay model can be used. This model produces a delay shown by

$$d = g * h + p \tag{1}$$

where g is the logical effort of the gate, h is the electrical effort of the gate, and p is the parasitic delay of the gate. To find the delay of a path including multiple gates, the path delay can be computed.

$$D = N * F^{1/N} + P \tag{2}$$

Where N is the number of stages, F is the total path effort, and P is the total parasitic delay of the path

To apply this to the mirror adder created in this lab, the Tpdr and Tpdf delays should be sampled at several output capacitance values. This will produce a linear relation between the propagation delay and output capacitance. A netlist testing this situation can be created by editing the netlists used previously in this laboratory. For brevity, only one netlist simulation was performed (a,b,ci) = (0,1,0)$\rightarrow$(0,1,1)

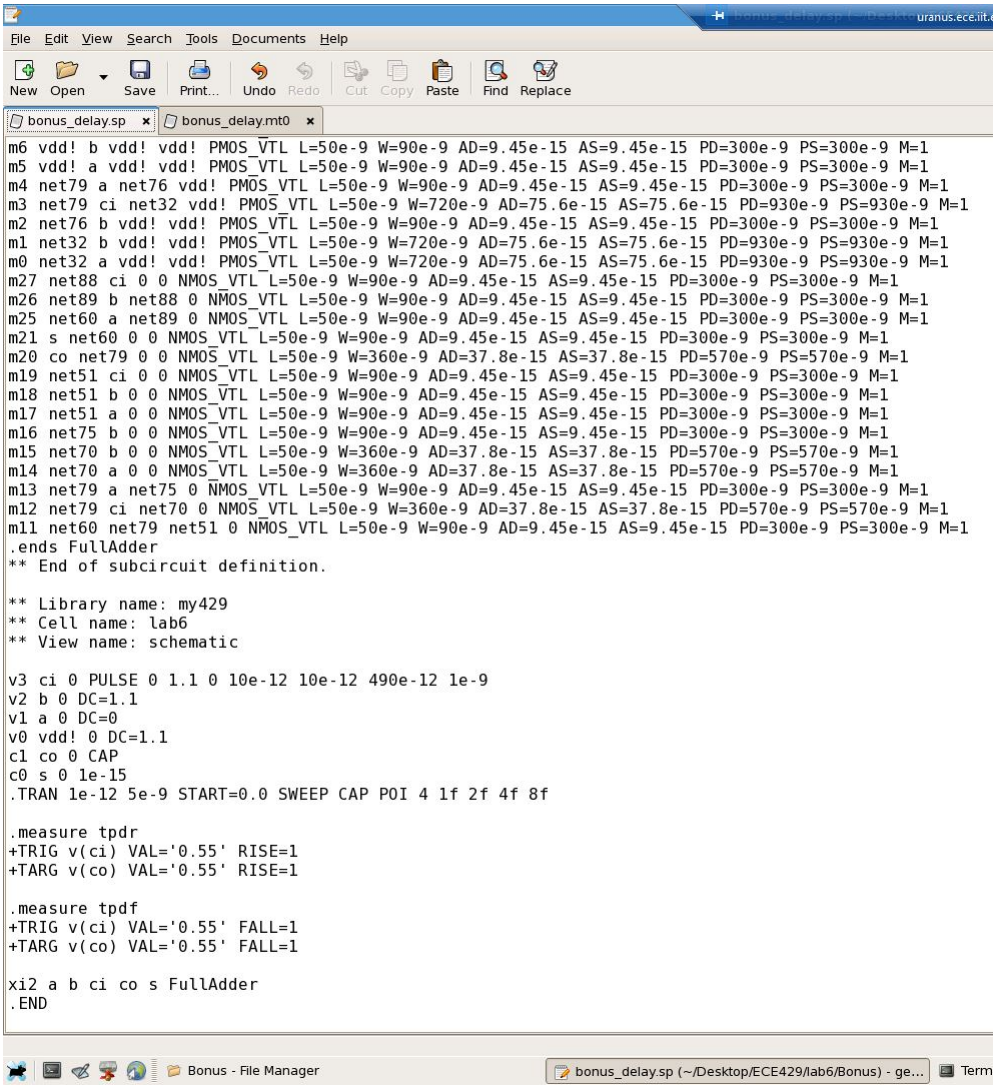

Figure 10: Bonus work Netlist

The experimental results found by simulating this netlist in HSPICE are shown below

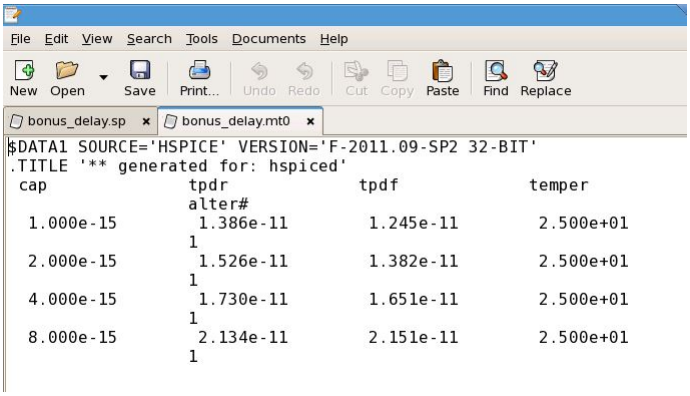

Figure 11: Bonus work mt0 data

Using the data obtained from the SPICE simulation, a graph can be created and extrapolated to determine the equation for the propagation delay of the path ci→co.

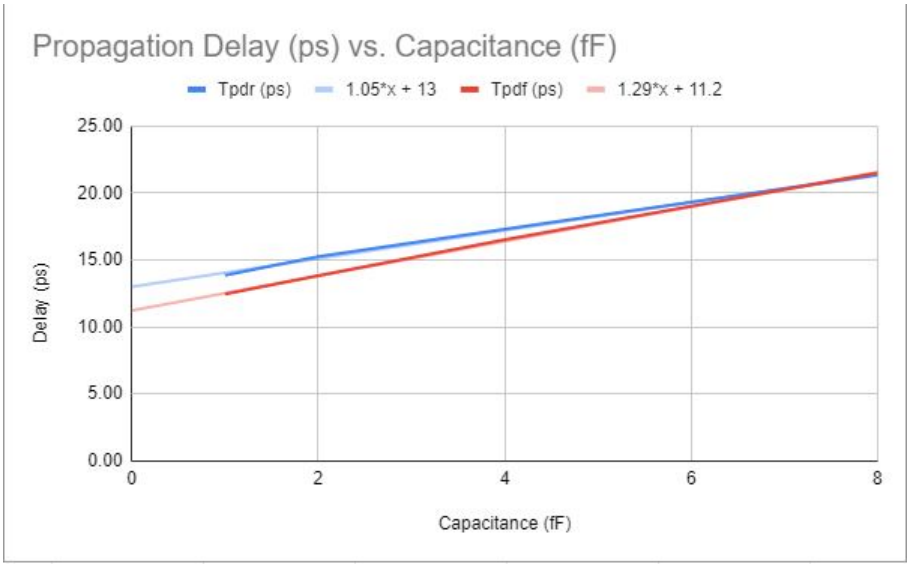

Figure 12: Bonus work Plotted data

Averaging the trendlines for the data results in the equation for the propagation delay being found as:

$$D = 1.17 * C_{out} + 12.1 \tag{3}$$

This equation shows that the parasitic delay of the path is 12.1 ps, and the effort of the gate with respect to output capacitance is 1.17C ps.

6 Conclusions

To conclude, this laboratory session should be considered a success. Students were successfully able to design and implement a full adder using CMOS logic. Students utilized a template for a ripple adder design to determine transistor sizing and implement the PMOS and NMOS networks in Cadence Virtuoso. The design was then successfully tested for equivalence with a full adder Verilog file using Formality ESP, and the propagation delays of various input transitions were determined using SPICE simulations. In subsequent laboratory sessions, this full adder design will be further developed to include a layout cellview, and the design will be expanded construct a 4-bit ripple adder.

Students will use the skills obtained in this laboratory to design increasingly complex CMOS circuits using the Cadence EDA suite. Students will also use formal circuit verification techniques practiced in this laboratory session to ensure the functionality of CMOS designs. Using SPICE simulations, students will also be able to optimize their designs for minimum propagation delay.

7 Resources

- Choi, Ken. "ECE 429 Laboratory 6 Manual." Illinois Institute of Technology, November 2, 2020.
- Kim, Victoria. "ECE 429 Guideline for Writing Report & Grading Criteria." Illinois Institute of Technology, November 2, 2020.