ECE 429 Laboratory 7: Carry-Ripple Addition II

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Acknowledgement: I acknowledge all of the work (including figures and codes) belongs to me and/or persons who are referenced.
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1 Introduction

In this laboratory, students will continue to elaborate on their ripple adder design by implementing a layout cellview of the full adder. This design will require students to carefully plan and place their physical layout, abide by all design rules of the FreePDK45 process library, and compare the functionality of the layout to the schematic cellview. The complexity of the full adder design will require students to utilize multiple metal layers and vias for the first time. At the conclusion of this laboratory, students will be much more proficient in designing CMOS layouts.

2 Theory\Pre-lab

CMOS designs use numerous design "masks" to define the various separate regions that make up the physical design. These designs can be very complex, so Electronic Design Automation (EDA) software is utilized to create a physical layout for the circuit. One such EDA software suite is Cadence Virtuoso. In Cadence Virtuoso, each of the individual layers can be modeled and tested against the physical design rules for a certain process, reducing the time required to design an integrated circuit dramatically.

Inside Cadence Virtuoso, there are a variety of tools available to further decrease the probability of design errors and overall design time. The first tool is design rule checking (DRC). This allows for the physical layout of a circuit to be checked for compliance with the design rules of a certain process (on which the circuit will eventually be produced). This ensures that when the circuit is created, it will not fail due to physical spacing errors. Another tool is Layout vs Schematic (LVS) testing. LVS testing allows the physical layout produced in Cadence Virtuoso to be compared with a schematic cellview to ensure that they will function identically. This means that the overall design can first be created as a schematic (to first ensure the digital logic design functions correctly) before spending time designing the physical layout.

For the prelab assignment, students were tasked with creating a stick diagram for a Full adder based on the textbook figure 11.5. The created stick diagram is shown below.

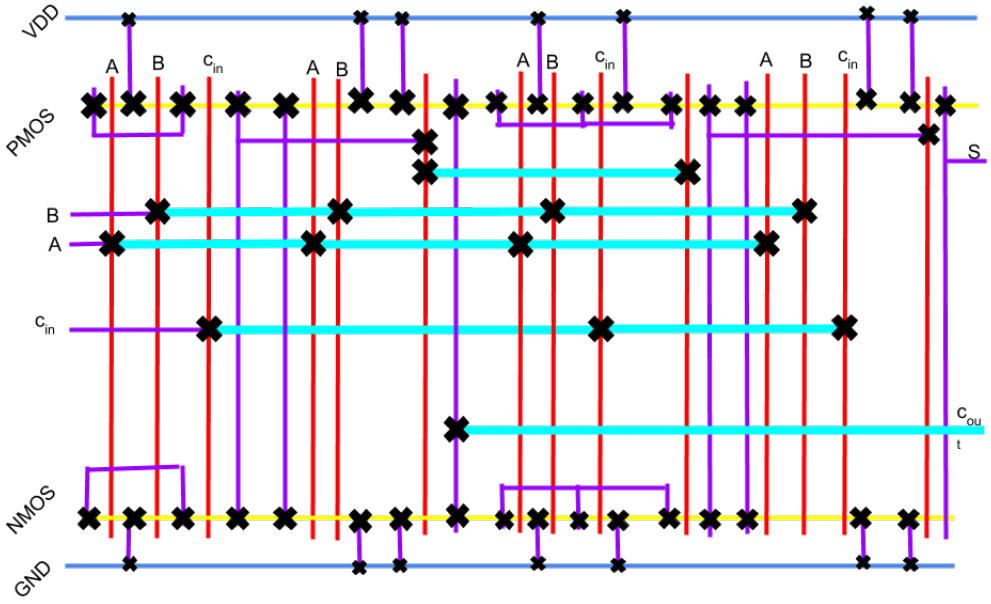

Figure 1: Full Adder Stick Diagram

3 Implementation

To create the layout, students utilized the stick diagram for a full adder, as created for the pre-lab, as a template. This complex design required the utility of metal2 layer interconnect (shown as pink in the diagram)¿

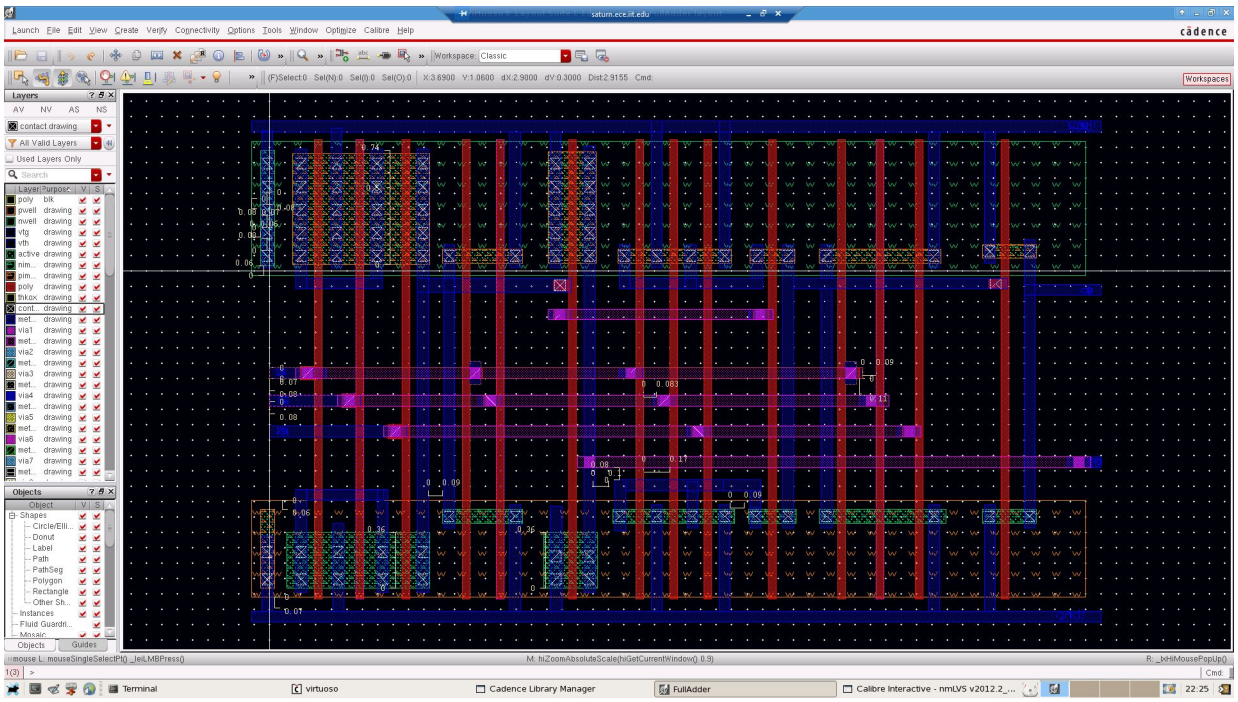

Figure 2: Layout Cellview for Full Adder

A tedious portion of the design was ensuring compliance with all design rules, as mandated by the FreePDK45 Process Library. The final results of the DRC check are shown below.

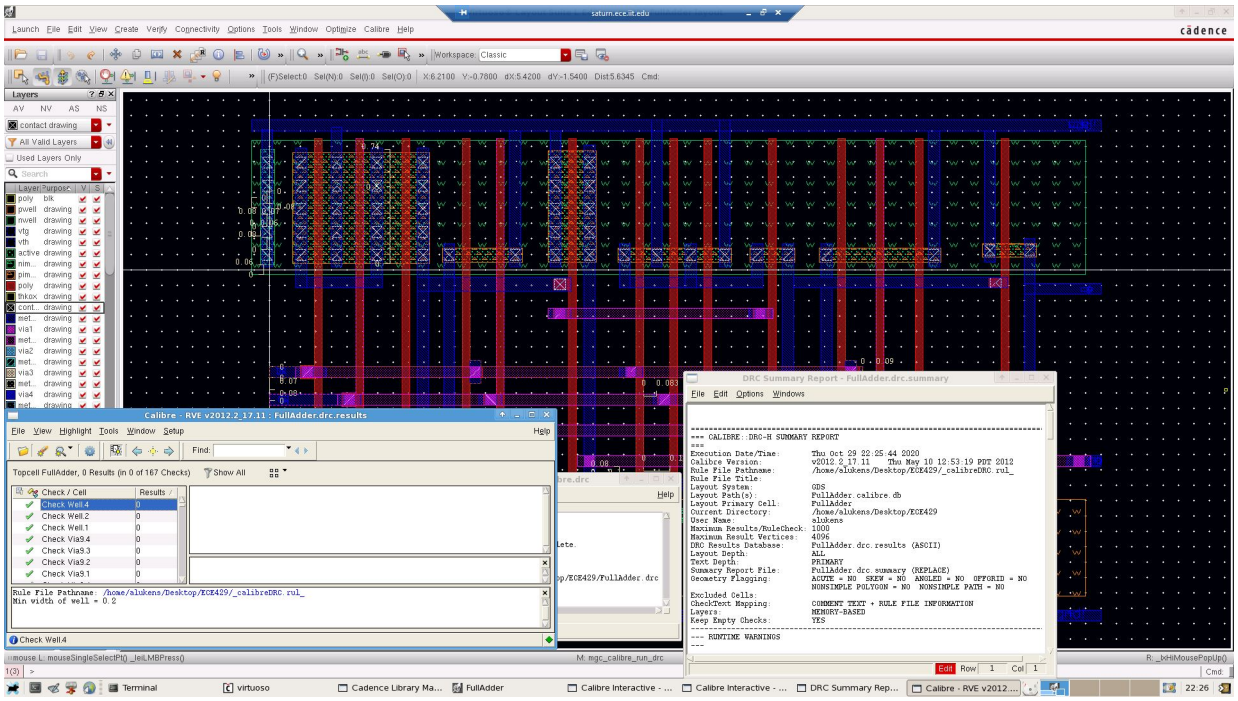

Figure 3: Full Adder DRC Results

After the layout was finalized and the design rules were passed, the next step was to verify the functionality of the full adder layout cellview versus the schematic cellview. This requires naming the different inputs and outputs correctly such that they match with the names of the signals in the schematic cellview.

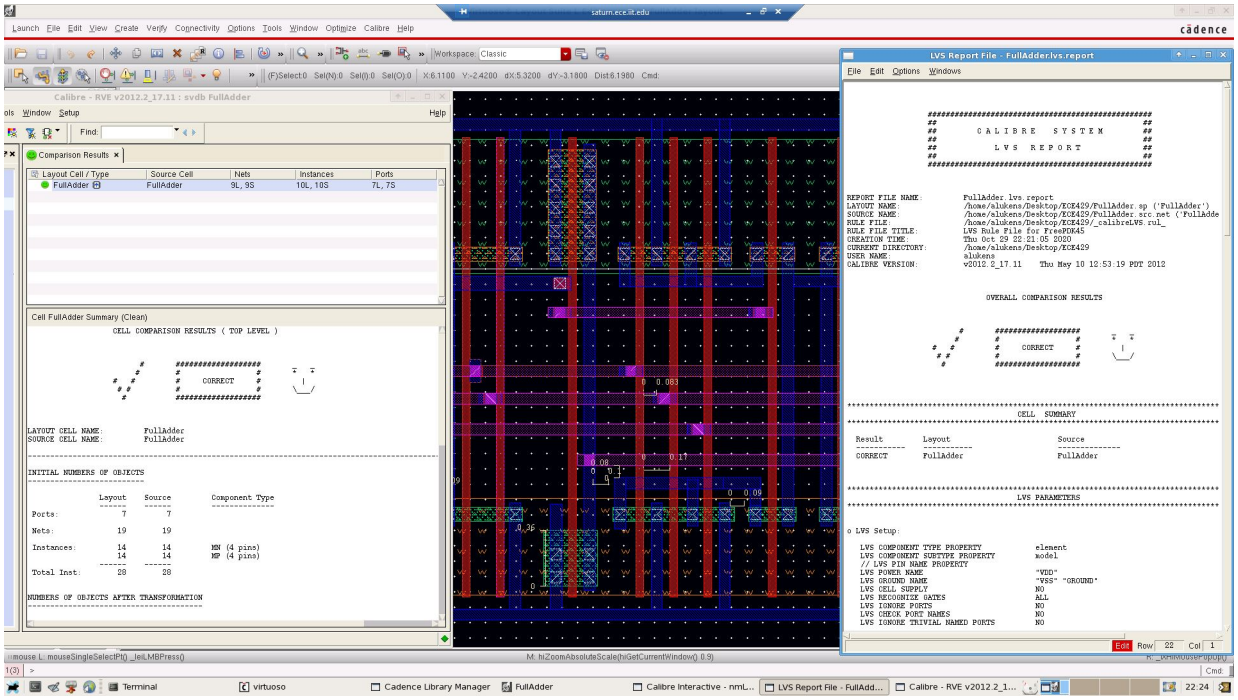

Figure 4: Full Adder LVS Results

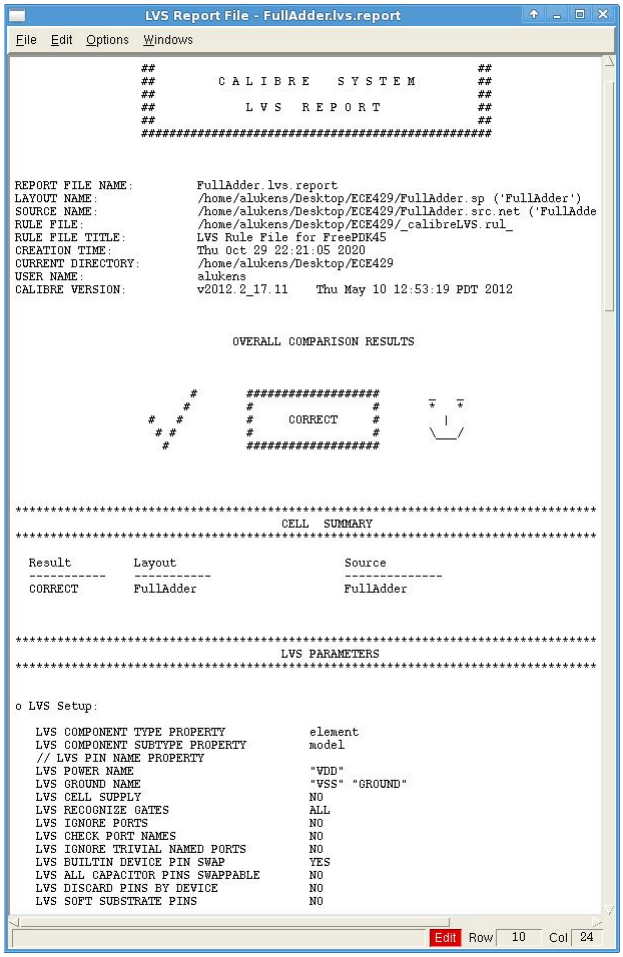

Figure 5: Full Adder LVS Report close-up

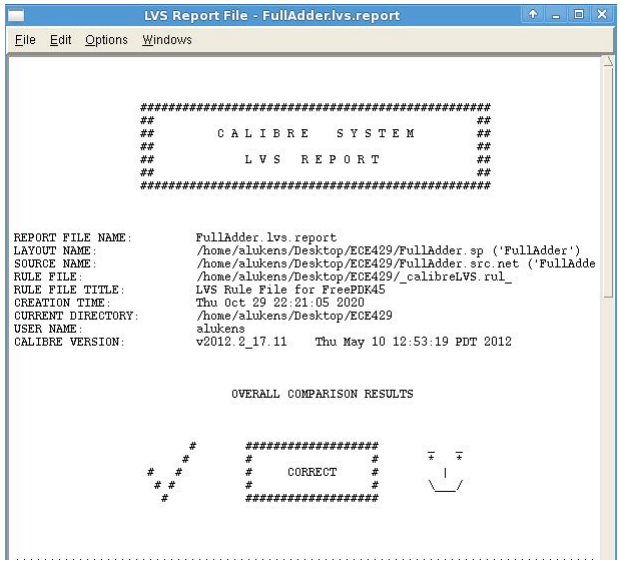

Figure 6: Full Adder LVS Smile close-up

4 Deliverables

In order to effectively tackle the design, a methodology for implementing the layout was required. In this case, I worked from left to right in the design, first defining how tall the cell must be in order to fit all required components (vertical height of cellview). Once this was defined, it was a matter of creating the individual transistors as shown in the stick diagram, and ensuring that they were sized correctly as according to the schematic cellview. This required manual adjustment of the height of each individual transistor region.

As a final verification check, I deselected the visibility of all layers and went through the layers one by one to ensure that they were placed in the correct regions. This helped me quickly diagnose an issue with missing contact areas between a metal1 layer and polysilicon region. This error was causing an additional net to appear in my design, which would have been hard to diagnose if on its own, as the contact areas are very small on the design, and are easy to miss, especially when covered by multiple metal and via layers.

5 Conclusions

This laboratory should be considered a success. Students were successfully able to plan and implement the layout cellview for a ripple-adder design. Students planned the location of ports in the full adder to ensure that they can be rapidly combined to produce a multi-bit adder. Students also utilized design rule checking to ensure that their design was complaint with the FreePDK process library, and then used Calibre LVS to ensure that the functionality was identical to the schematic cellview.

6 Resources

- Choi, Ken. "ECE 429 Laboratory 7 Manual." Illinois Institute of Technology, November 9, 2020.
- Kim, Victoria. "ECE 429 Guideline for Writing Report & Grading Criteria." Illinois Institute of Technology, November 9, 2020.