LM3940 1-A Low-Dropout Regulator for 5-V to 3.3-V Conversion

1 Features

- Input Voltage Range: 4.5 V to 5.5 V
- Output Voltage Specified over Temperature
- Excellent Load Regulation
- Specified 1-A Output Current
- Requires only One External Component
- Built-in Protection against Excess Temperature
- Short-Circuit Protected

2 Applications

- Laptop and Desktop Computers
- Logic Systems

3 Description

The LM3940 is a 1-A low-dropout regulator designed to provide 3.3 V from a 5-V supply.

The LM3940 is ideally suited for systems which contain both 5-V and 3.3-V logic, with prime power provided from a 5-V bus.

Because the LM3940 is a true low dropout regulator, it can hold its 3.3-V output in regulation with input voltages as low as 4.5 V.

The TO-220 package of the LM3940 means that in most applications the full 1 A of load current can be delivered without using an additional heatsink.

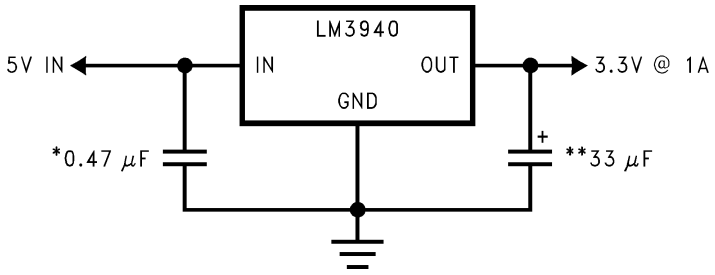
The surface mount DDPAK/TO-263 package uses minimum board space, and gives excellent power dissipation capability when soldered to a copper plane on the PC board.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3940	SOT-223 (4)	6.50 mm x 3.50 mm
	DDPAK/TO-263 (3)	10.18 mm x 8.41 mm
	TO-220 (3)	14.986 mm x 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



*Required if regulator is located more than 1 inch from the power supply filter capacitor or if battery power is used.
**See *Application and Implementation*.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2014) to Revision G — **Page**

- Changed pin names to TI nomenclature ... 1
- Deleted soldering information from Ab Max; this info is in POA ... 4
- Changed *Handling Ratings* table to *ESD Ratings* table; move storage temp to *Ab Max* ... 4
- Changed values in Input supply voltage row, ROC table ... 4
- Changed I_L to I_{OUT} ... 5

Changes from Revision E (March 2013) to Revision F — **Page**

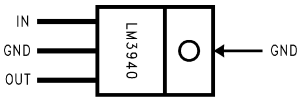
- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section; update thermal values ... 1

Changes from Revision D (March 2013) to Revision E — **Page**

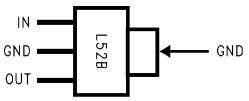
- Changed layout of National Data Sheet to TI format ... 14

5 Pin Configuration and Functions

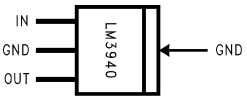
3-Pin
TO-220 Package
Front View



4-Pin
SOT-223
Front View



3-Pin
DDPAK/TO-263 Package
Front View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TO-220	TO-263	SOT-223		
IN	1	1	1	I	Input voltage supply. A 0.47-µF capacitor should be connected at this input.
GND	2	2	2, 4	—	Common ground
OUT	3	3	3	O	Output voltage. A 33-µF low ESR capacitor should be connected to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power dissipation(2)		Internally Limited	
Input supply voltage	–0.3	7.5	V
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of $R_{\theta JA}$ (for devices in still air with no heatsink) is 23.3°C/W for the TO-220 package, 40.9°C/W for the DDPAK/TO-263 package, and 59.3°C/W for the SOT-223 package. The effective value of $R_{\theta JA}$ can be reduced by using a heatsink (see *Heatsinking* for specific information on heatsinking).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Junction temperature, T_J	–40	125	°C
Input supply voltage, V_{IN}	4.5	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		LM3940			UNIT
		SOT-223 (DCY)	TO-263 (KTT)	TO-220 (NDE)	
		4 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High-K	59.3	40.9	23.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.9	43.5	16.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	23.5	4.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	10.3	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.0	22.5	4.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	0.8	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range, V_{IN} = 5 V, I_{OUT} = 1 A, C_{OUT} = 33 µF (unless otherwise noted). Limits apply for T_J = 25°C, unless otherwise specified in the Test Conditions column.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	5 mA ≤ I_{OUT} ≤ 1 A, T_J = 25°C	3.20	3.3	3.40	V
		5 mA ≤ I_{OUT} ≤ 1 A, –40°C ≤ T_J ≤ 125°C	3.13		3.47	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line regulation	I_{OUT} = 5 mA, 4.5 V ≤ V_{IN} ≤ 5.5 V		20	40	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load regulation	50 mA ≤ I_{OUT} ≤ 1 A, T_J = 25°C		35	50	
		50 mA ≤ I_{OUT} ≤ 1 A, –40°C ≤ T_J ≤ 125°C		35	80	
Z_{OUT}	Output impedance	I_{OUT} (DC) = 100 mA, I_{OUT} (AC) = 20 mA (rms), f = 120 Hz		35		mΩ
I_Q	Quiescent current	4.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA, T_J = 25°C		10	15	mA
		4.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA, –40°C ≤ T_J ≤ 125°C		10	20	
		V_{IN} = 5 V, I_{OUT} = 1 A, T_J = 25°C		110	200	
		V_{IN} = 5 V, I_{OUT} = 1 A, –40°C ≤ T_J ≤ 125°C		110	250	
e_n	Output noise voltage	f_{BW} = 10 Hz – 100 kHz, I_{OUT} = 5 mA		150		$\mu V_{(rms)}$
V_{DO}	Dropout voltage(2)	I_{OUT} = 1 A, T_J = 25°C		0.5	0.8	V
		I_{OUT} = 1 A, –40°C ≤ T_J ≤ 125°C		0.5	1	
		I_{OUT} = 100 mA, T_J = 25°C		110	150	mV
		I_{OUT} = 100 mA, –40°C ≤ T_J ≤ 125°C		110	200	
$I_{OUT(SC)}$	Short-circuit current	R_L = 0	1.2	1.7		A

(1) All limits specified for T_J = 25°C are 100% tested and are used to calculate Outgoing Quality Levels. All limits at temperature extremes are verified via correlation using standard Statistical Quality Control (SQC) methods.
(2) Dropout voltage is defined as the input-output differential voltage where the regulator output drops to a value that is 100 mV below the value that is measured at V_{IN} = 5 V.

6.6 Typical Characteristics

At T_J=25°C, unless otherwise noted.

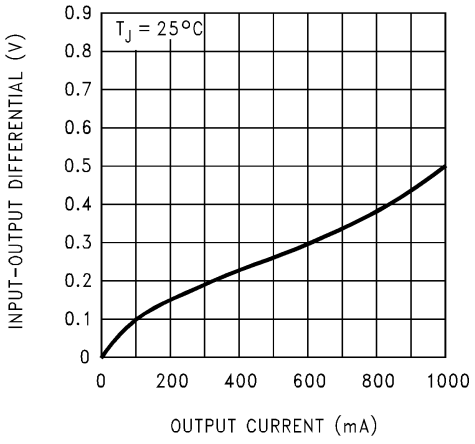


Figure 1. Dropout Voltage

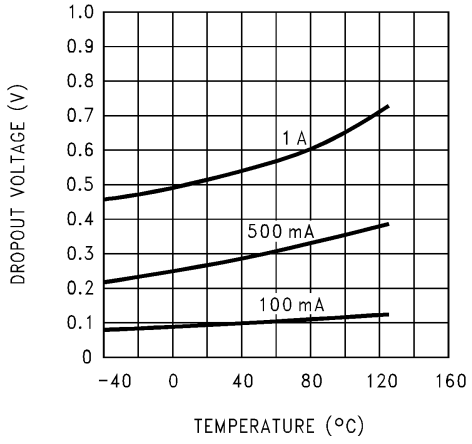


Figure 2. Dropout Voltage vs. Temperature

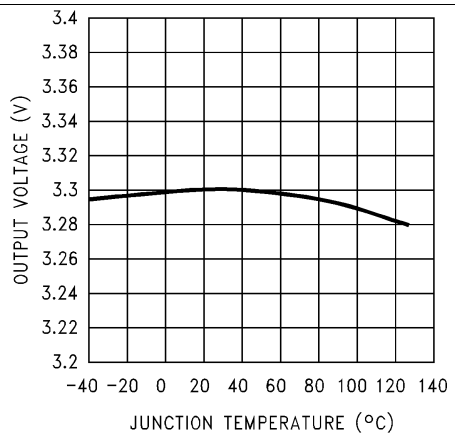


Figure 3. Output Voltage vs. Temperature

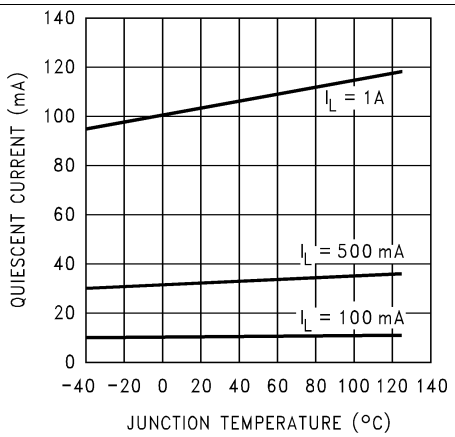


Figure 4. Quiescent Current vs. Temperature

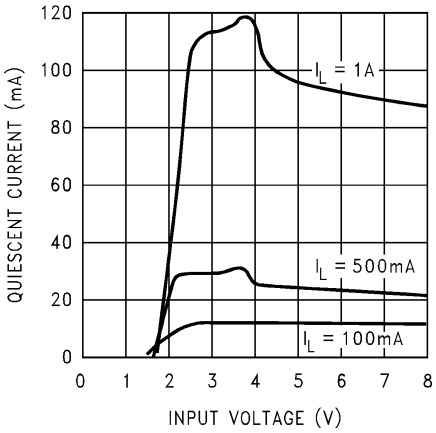


Figure 5. Quiescent Current vs. V_{IN}

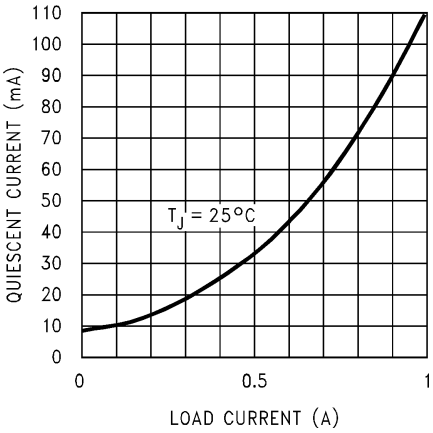


Figure 6. Quiescent Current vs. Load

Typical Characteristics (continued)

At T_J=25°C, unless otherwise noted.

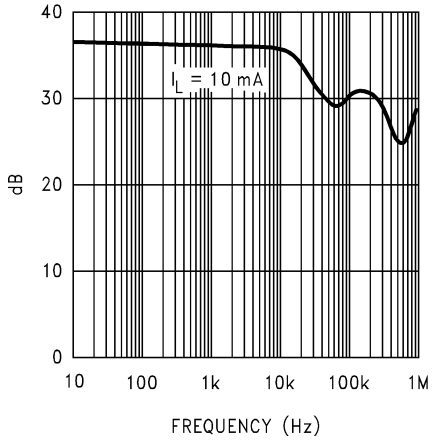


Figure 7. Ripple Rejection

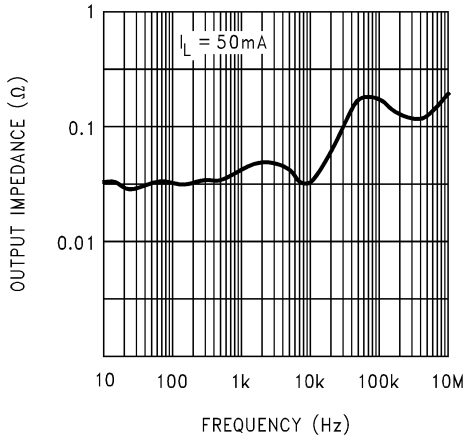


Figure 8. Output Impedance

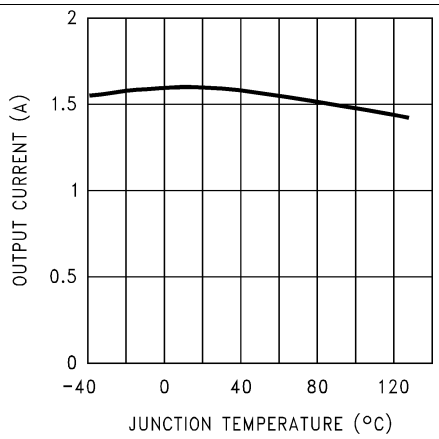


Figure 9. Peak Output Current

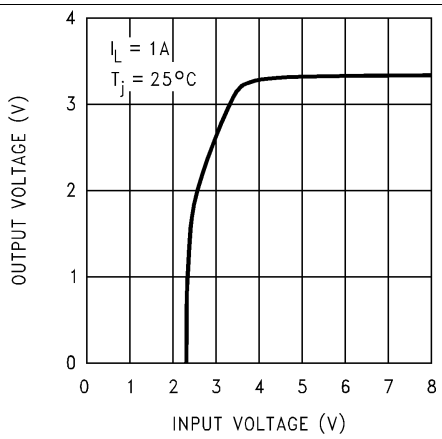


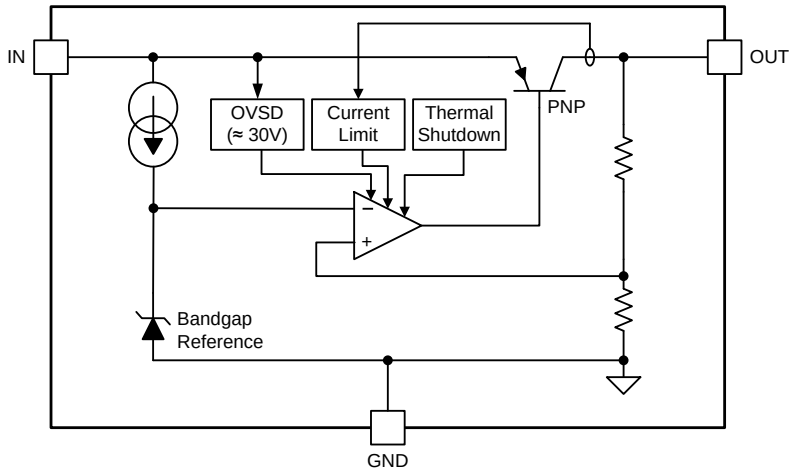
Figure 10. Low Voltage Behavior

7 Detailed Description

7.1 Overview

The LM3940 is a low dropout regulator capable of sourcing a 1-A load. The LM3940 provides 3.3 V from 5-V supply. LM3940 is ideally suited for system which contain both 5-V and 3.3-V logic, with prime power provided from a 5-V bus.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage. This accuracy error includes the errors introduced by line and load regulation across the full range of rated load and line operating conditions, unless otherwise specified by the Electrical Characteristics.

7.3.2 Short-Circuit Protection

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

7.3.3 Thermal Protection

The LM3940 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced.

The internal protection circuit of LM3940 is designed to protect against thermal overload conditions. The circuit is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.4 Device Functional Modes

7.4.1 Operation with V_{IN} = 5 V

The device operates at input voltage is 5 V and output voltage is 3.3 V. The LM3940 is a true low dropout regulator, it can hold its 3.3-V output in regulation with input voltages as low as 4.5 V.

8 Application and Implementation

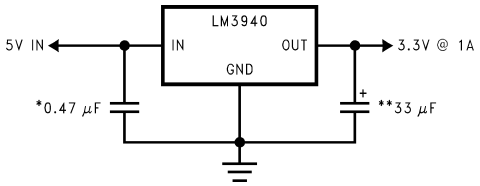
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3940 is a linear voltage regulator operating from 5 V on the input and regulates voltage to 3.3V with 1-A maximum output current. This device is suited for system which contain both 5-V and 3.3-V logic, with prime power provided from a 5-V bus.

8.2 Typical Application



*Required if regulator is located more than 1″ from the power supply filter capacitor or if battery power is used.
**See *Detailed Design Procedure*.

Figure 11. Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5 V, ± 10%
Output voltage	3.3 V, ±3%
Output current	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both equivalent series resistance (ESR) and minimum amount of capacitance.

8.2.2.1.1 Minimum Capacitance

The minimum output capacitance required to maintain stability is 33 µF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

8.2.2.1.2 ESR Limits

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in Figure 12. *It is essential that the output capacitor meet these requirements, or oscillations can result.*

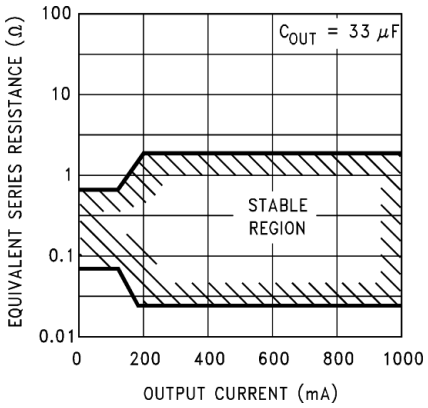


Figure 12. ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to −40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid tantalum, with the total capacitance split about 75/25% with the aluminum being the larger value.

If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The “flatter” ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

8.2.3 Application Curves

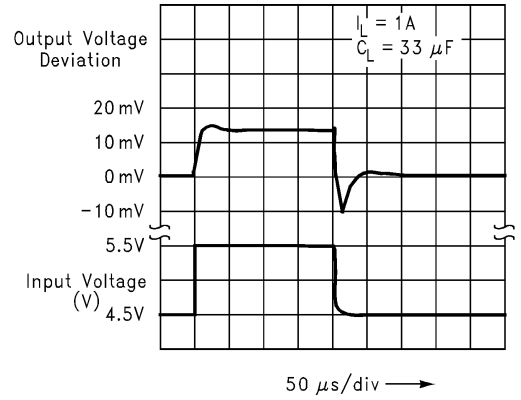


Figure 13. Line Transient Response

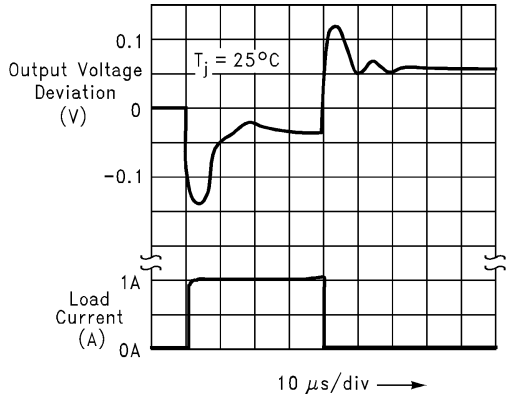


Figure 14. Load Transient Response

9 Power Supply Recommendations

The LM3940 is designed to operate from an 5-V input voltage supply. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

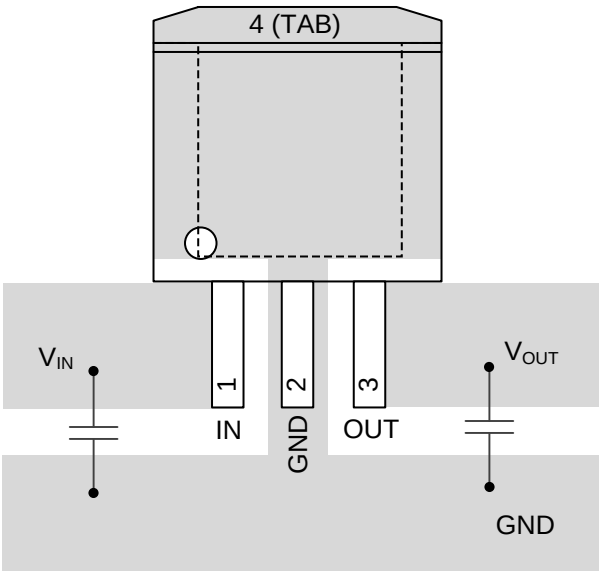


Figure 15. LM3940 Layout Example

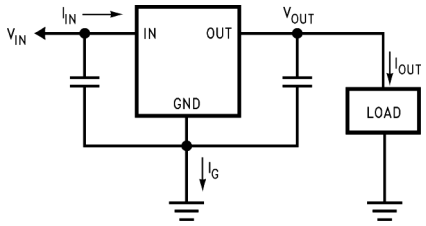
10.3 Heatsinking

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under *Absolute Maximum Ratings*.

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

Figure 16 shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:

Heatsinking (continued)



$I_{IN} = I_{OUT} + I_G$
$P_D = (V_{IN} - V_{OUT})\ I_{OUT} + (V_{IN})\ I_G$

Figure 16. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R(max). This is calculated by using the formula:

$T_R\ (max) = T_J\ (max) - T_A\ (max)$

Where: T_J (max) is the maximum allowable junction temperature, which is 125°C for commercial grade parts.

T_A (max) is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for T_R(max) and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $R_{\theta(JA)}$, can now be found:

$R_{\theta(JA)} = T_R\ (max)/P_D$

IMPORTANT: If the maximum allowable value for $\theta_{(JA)}$ is found to be ≥ 23.3°C/W for the TO-220 package, ≥ 40.9°C/W for the DDPAK/TO-263 package, or ≥59.3°C/W for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for $\theta_{(JA)}$falls below these limits, a heatsink is required.

10.3.1 Heatsinking TO-220 Package Parts

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board. If a copper plane is to be used, the values of $R_{\theta(JA)}$ will be the same as shown in the *Heatsinking DDPAK/TO-263 and SOT-223 Package Parts* section for the DDPAK/TO-263.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, $R_{\theta(H-A)}$, must first be calculated:

$R_{\theta(H-A)} = R_{\theta(JA)} - R_{\theta(C-H)} - R_{\theta(J-C)}$

Where: $R_{\theta(J-C)}$ is defined as the thermal resistance from the junction to the surface of the case. A value of 4°C/W can be assumed for $\theta_{(J-C)}$ for this calculation.

$R_{\theta(C-H)}$ is defined as the thermal resistance between the case and the surface of the heatsink. The value of $\theta_{(C-H)}$ will vary from about 1.5°C/W to about 2.5°C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2°C/W should be assumed for $\theta_{(C-H)}$.

When a value for $R_{\theta(H-A)}$ is found using the equation shown above, *a heatsink must be selected that has a value that is less than or equal to this number.*

$R_{\theta(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs. power dissipation for the heatsink.

10.3.2 Heatsinking DDPAK/TO-263 and SOT-223 Package Parts

Both the DDPAK/TO-263 (KTT) and SOT-223 (DCY) packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 17 shows for the DDPAK/TO-263 the measured values of $R_{\theta(JA)}$ for different copper area sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking.*

Heatsinking (continued)

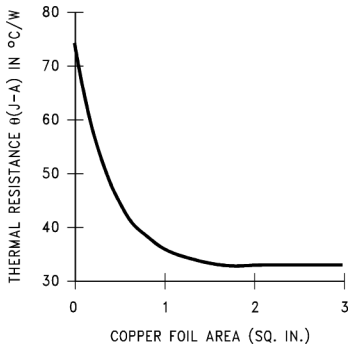


Figure 17. $R_{\theta(JA)}$ vs. Copper (1 ounce) Area for the DDPAK/TO-263 Package

As shown in Figure 17, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $R_{\theta(JA)}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

As a design aid, Figure 18 shows the maximum allowable power dissipation compared to ambient temperature for the DDPAK/TO-263 device (assuming $R_{\theta(JA)}$ is 35°C/W and the maximum junction temperature is 125°C).

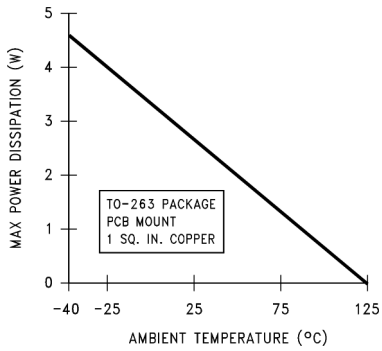


Figure 18. Maximum Power Dissipation vs. T_{AMB} for the DDPAK/TO-263 Package

Figure 19 and Figure 20 show the information for the SOT-223 package. Figure 20 assumes a $R_{\theta(JA)}$ of 74°C/W for 1 ounce copper and 51°C/W for 2 ounce copper and a maximum junction temperature of 125°C.

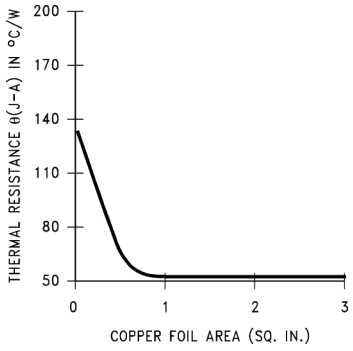


Figure 19. $R_{\theta(JA)}$ vs. Copper (2 ounce) Area for the SOT-223 Package

Heatsinking (continued)

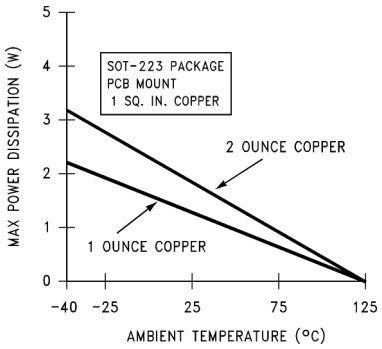


Figure 20. Maximum Power Dissipation vs. T_{AMB} for the SOT-223 Package

Please see *AN-1028 Maximum Power Enhancement Techniques for Power Packages*, SNVA036 for power enhancement techniques to be used with the SOT-223 package.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

AN-1028 Maximum Power Enhancement Techniques for Power Packages, SNVA036

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3940IMP-3.3	NRND	SOT-223	DCY	4	1000	TBD	Call TI	Call TI	-40 to 125	L52B	
LM3940IMP-3.3/NOPB	ACTIVE	SOT-223	DCY	4	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L52B	Samples
LM3940IMPX-3.3	NRND	SOT-223	DCY	4	2000	TBD	Call TI	Call TI	-40 to 125	L52B	
LM3940IMPX-3.3/NOPB	ACTIVE	SOT-223	DCY	4	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L52B	Samples
LM3940IS-3.3	NRND	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM3940IS -3.3 P+	
LM3940IS-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM3940IS -3.3 P+	Samples
LM3940ISX-3.3	NRND	DDPAK/ TO-263	KTT	3	500	TBD	Call TI	Call TI	-40 to 125	LM3940IS -3.3 P+	
LM3940ISX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM3940IS -3.3 P+	Samples
LM3940IT-3.3	NRND	TO-220	NDE	3	45	TBD	Call TI	Call TI	-40 to 125	LM3940IT -3.3 P+	
LM3940IT-3.3/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM3940IT -3.3 P+	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

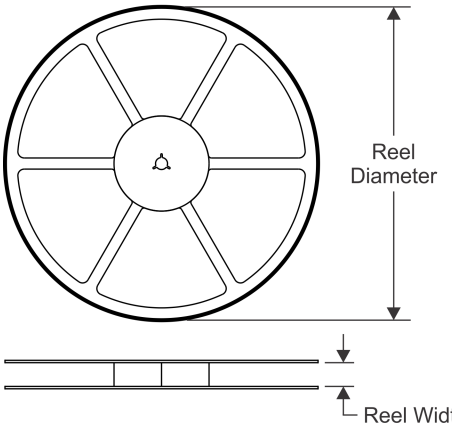
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

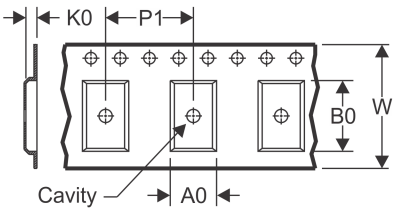
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

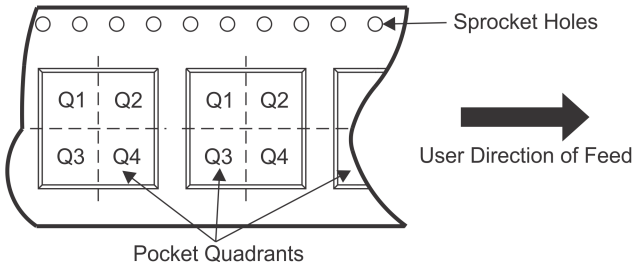


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

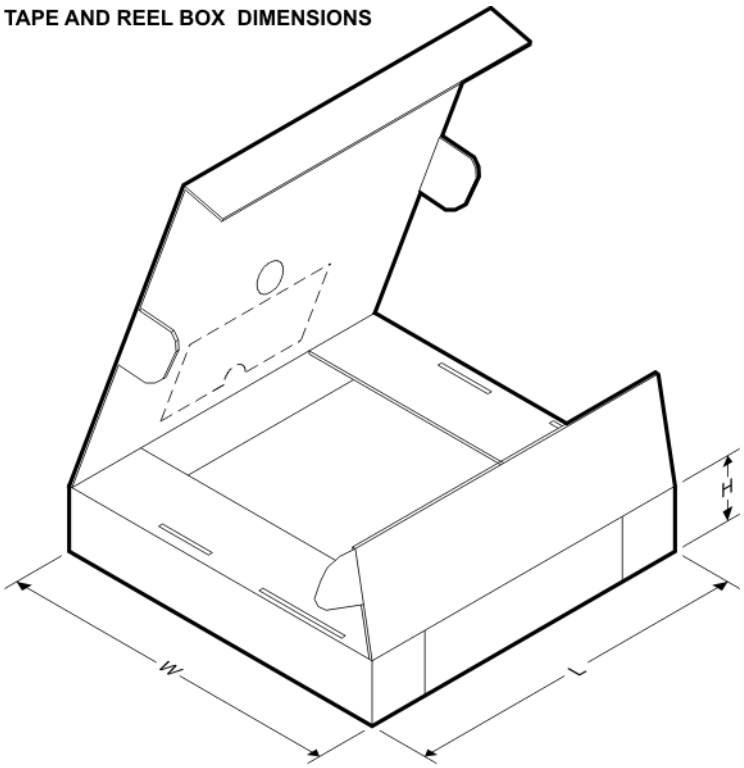
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3940IMP-3.3	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM3940IMP-3.3/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM3940IMPX-3.3	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM3940IMPX-3.3/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM3940ISX-3.3	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM3940ISX-3.3/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

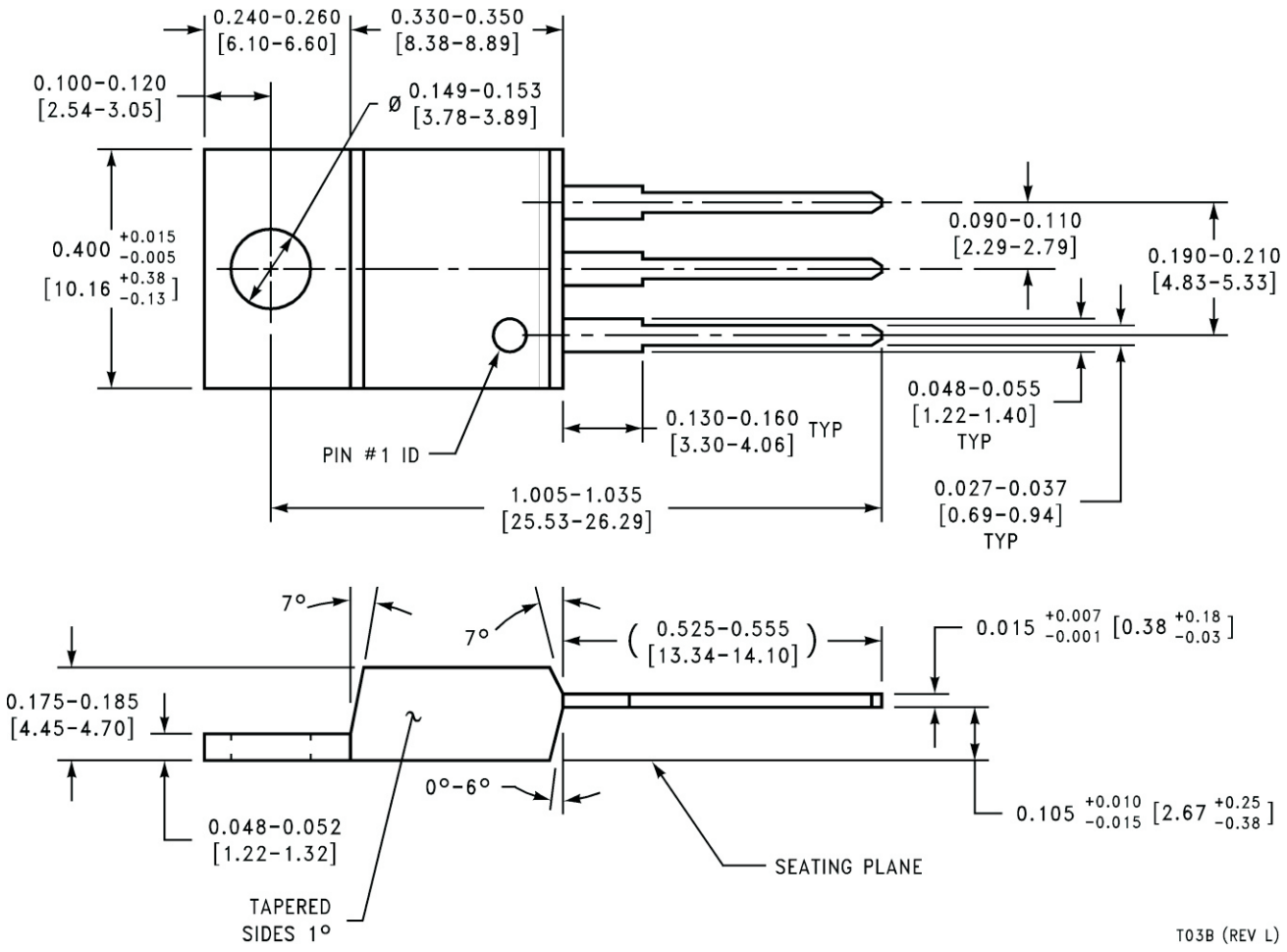
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

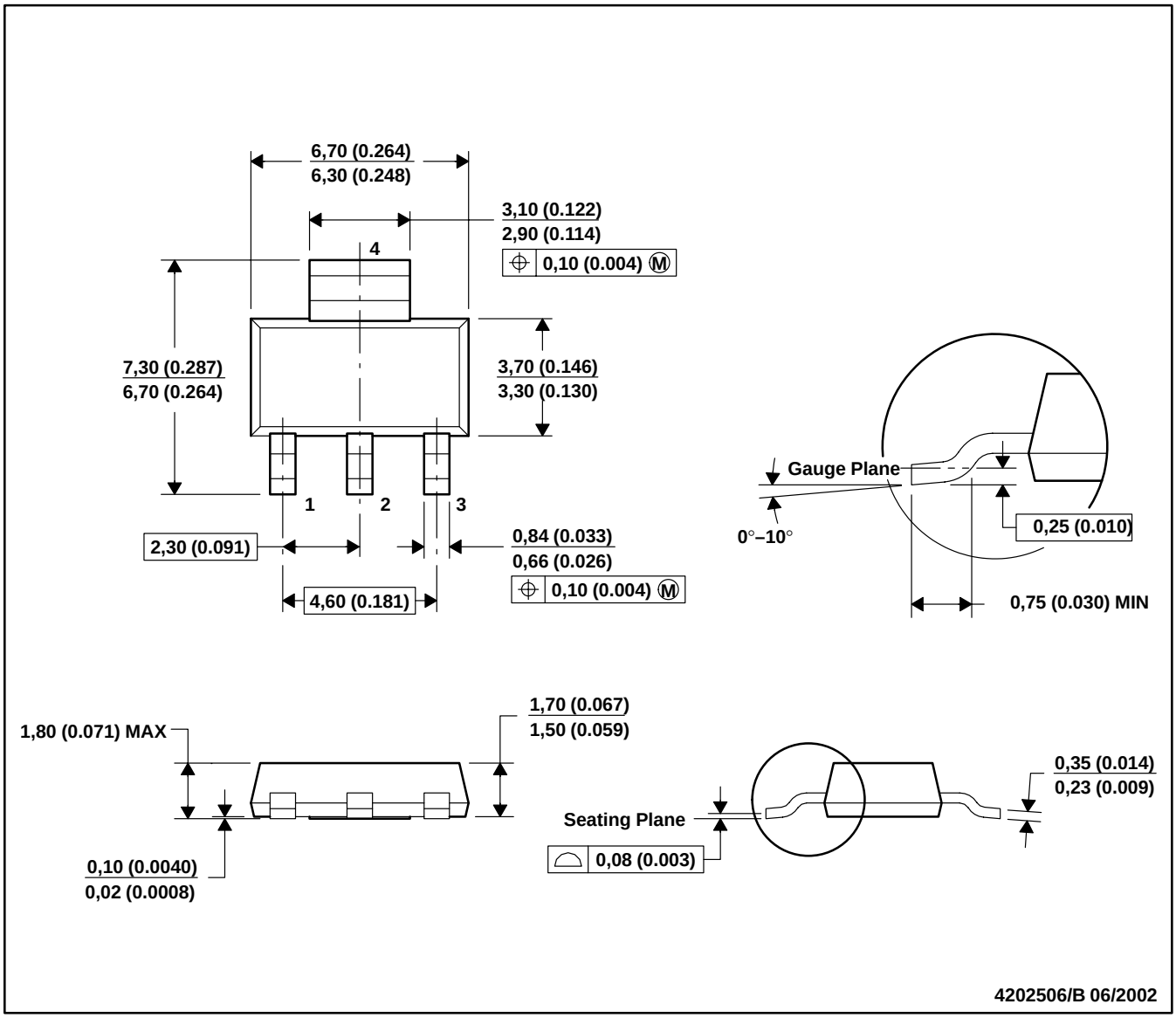
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3940IMP-3.3	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM3940IMP-3.3/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM3940IMPX-3.3	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM3940IMPX-3.3/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM3940ISX-3.3	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM3940ISX-3.3/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0

NDE0003B


0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
0.090-0.110
[2.29-2.79]
0.190-0.210
[4.83-5.33]
PIN #1 ID
0.130-0.160 TYP
[3.30-4.06]
0.048-0.055
[1.22-1.40]
TYP
1.005-1.035
[25.53-26.29]
0.027-0.037
[0.69-0.94]
TYP
7°
7°
(0.525-0.555
[13.34-14.10])
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185
[4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052
[1.22-1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

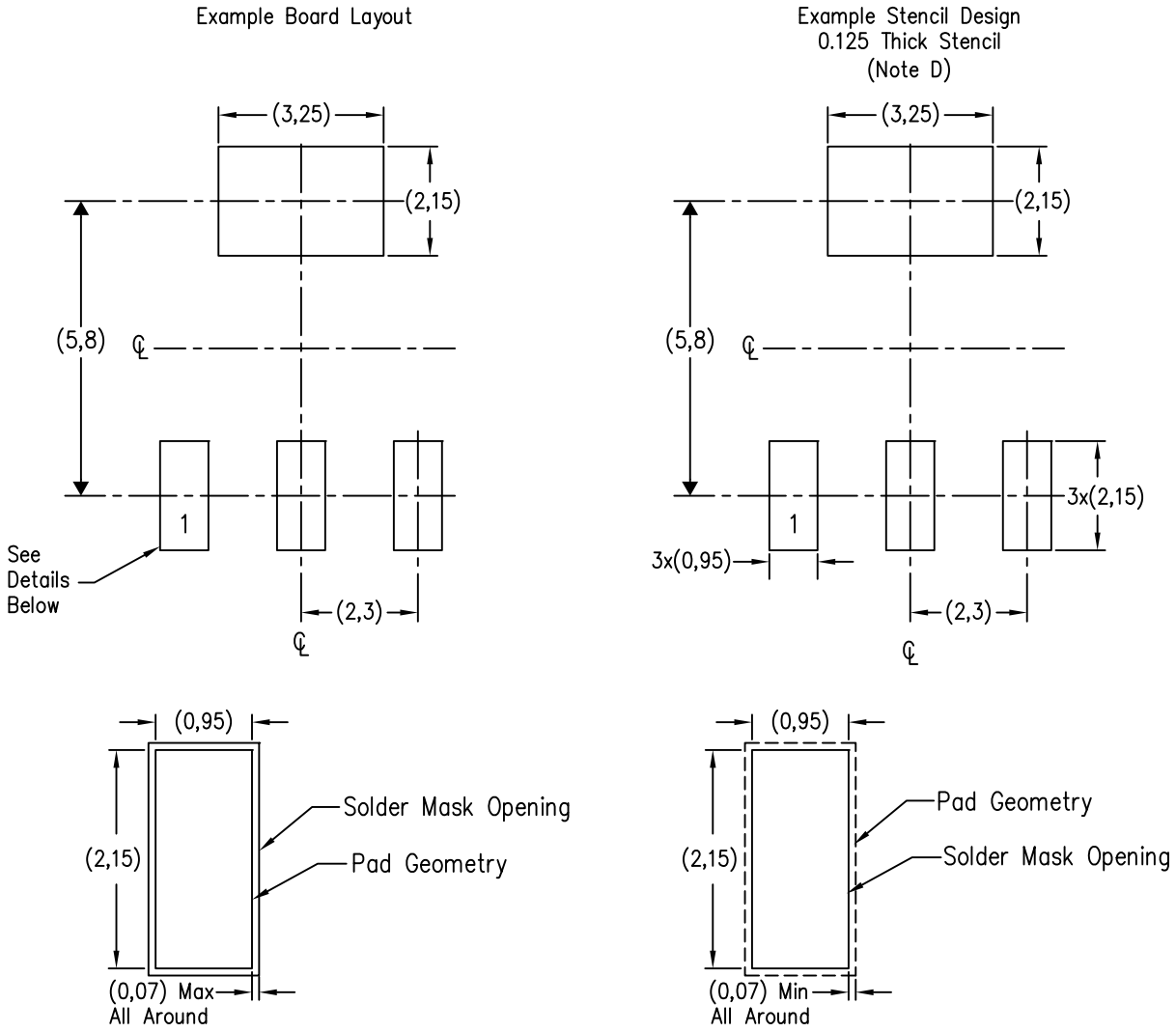
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

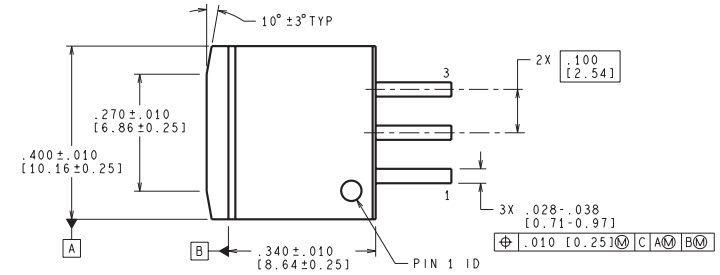
DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE

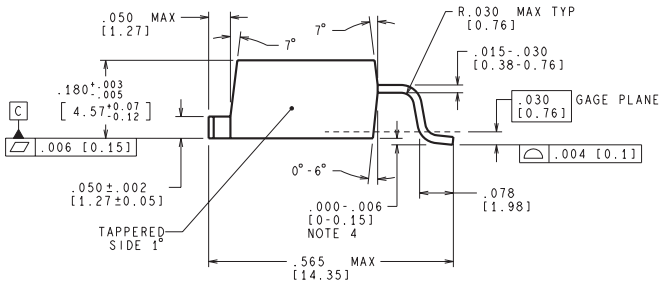


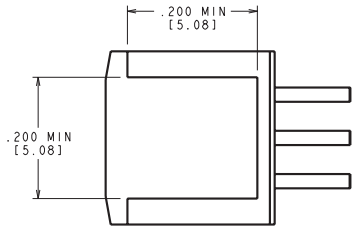
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

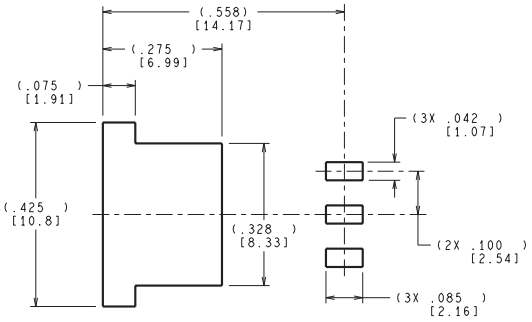
KTT0003B







BOTTOM SIDE OF PACKAGE



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TS3B (Rev F)

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