Problem 4.3

4.3.1
Clock cycle time is determined by the critical path, which for the given latencies is to get the data value for the load instructions. Without the improvement the clock cycle time is: 400ps + 200ps + 30ps + 120ps + 350ps + 30ps = 1130 ps. With the improvement the clock cycle time is: 400ps + 200ps + 30ps + 120ps + 350ps + 30ps + 300ps = 1430 ps.

4.3.2
The speedup comes from changes to the number of clock cycles and changes in clock cycle. (1/0.95)*(1130/1430) = 0.83. So there is actually a slowdown.

4.3.3
The cost is the total cost of all the components. The cost without the improvement is: 100 + 200 + 500 + 100 + 200 + 2*30 + 3*10 = 3890. The cost with the improvement is: 3890 + 600 = 4490. The relative cost is 4490/3890 = 1.15. The ratio of cost to performance is 1.15/0.83 = 1.39. The cost is higher for worse performance so the ratio of cost to performance is worse than the processor without the improvement.

Problem 4.4

4.4.1
The I-Mem takes more time than the Add unit, thus the clock cycle time is the latency of the I-Mem: 200 ps

4.4.2
The critical path goes through the Instruction Memory, Shift-left-2, Sign-Extend, the Add unit, and the Mux: 200ps + 15ps + 10ps + 70ps + 20ps = 315ps

4.4.3
200ps + 90ps + 20ps + 90ps + 20ps = 420ps

4.4.4
PC – relative branches

4.4.5
None

4.4.6
BNE has a longer critical path so it determines the clock cycle time. The unit is not on the critical path so its latency must be increased until the path to compute the address becomes longer than the path for PCSrc. The latency of Shift-left-2 must be increased by 105ps or more to affect the clock cycle time.

Problem 4.7

4.7.1
Output for Sign-Extend: 00000000000000000000000000010100
Output for Jump shift-left-2: 00011000100000000000001010000

4.7.2
ALUOp[1-0]: 00
Instructions[5-0]: 010100

4.7.3
New PC address: PC + 4
Path: PC to Add (PC + 4) to branch Mux to jump Mux to PC

4.7.4
WrReg Mux: 2 or 0
ALU Mux: 20
Mem/ALU Mux: X
Branch Mux: PC + 4
Jump Mux: PC + 4

4.7.5
ALU: -3 and 20
Add (PC+4): PC and 4
Add (Branch): PC+4 and 20*4

4.7.6
Read Register 1
Read Register 2
Write Register
Write Data
RegWrite

Problem 4.8

4.8.1
Pipelined Clock cycle time: 350ps
Non-pipelined Clock cycle time: 1250ps

4.8.2
Pipelined latency: 1750ps
Non-pipelined latency: 1250ps

4.8.3
Stage to split: ID
New Clock Cycle Time: 300ps

4.8.4
35%

4.8.5
65%