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Engineering Portfolio

McGill University

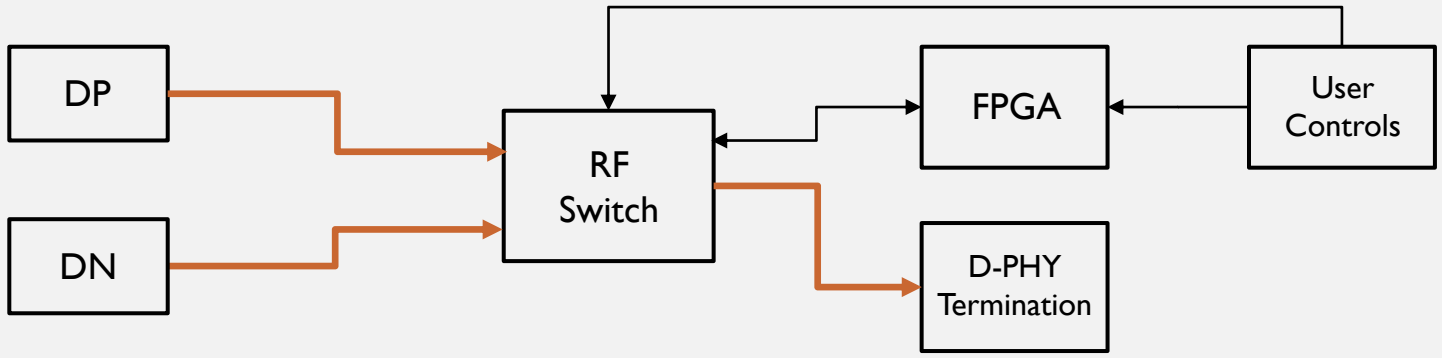
BEng Electrical Engineering

Junior

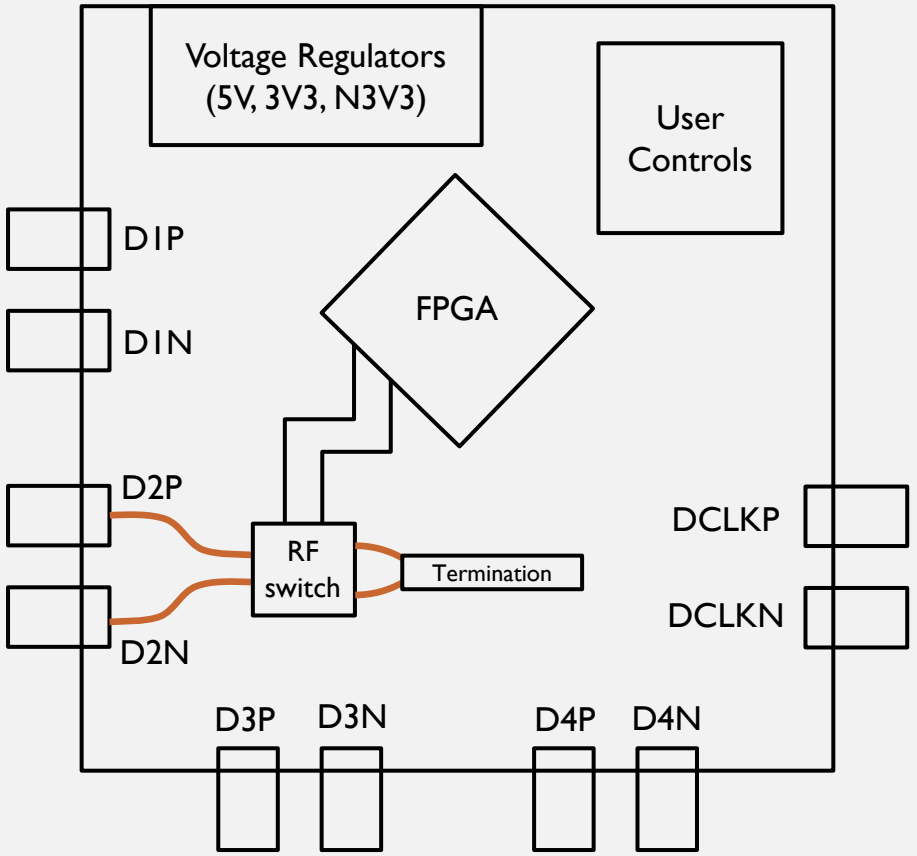
MIPI D-PHY Termination Board

introspect technology

- Project taken on for Introspect Technology as an intern
- MIPI D-PHY is a physical layer for CSI/DSI (Camera and Display Serial Interfaces)
- Designed a 4-layer PCB, with ~350 components, using Cadence OrCAD design tools
- The board is designed to allow active probing of high-speed D-PHY transmitter signals by providing proper D-PHY receiver termination
  - The FPGA detects when the transmitter data goes from low power to high-speed and controls the RF switch
  - RF switch connects the D-PHY termination impedance to the input for high-speed mode and disconnects it for low power mode (unterminated)
  - User can choose whether they want automatic termination or manual, in which case they can control the low power threshold voltage
- Based on the already existing design of Introspect's C-PHY Termination Board
  - C-PHY is trio-based (3 lanes), while D-PHY is differential data and differential clock (4 lanes), requiring significant changes to implement
  - Completely revisited the design by changing the high-speed routing type, termination, RF switches, FPGA pinout, voltage regulators, and general layout of the board



Board Layout



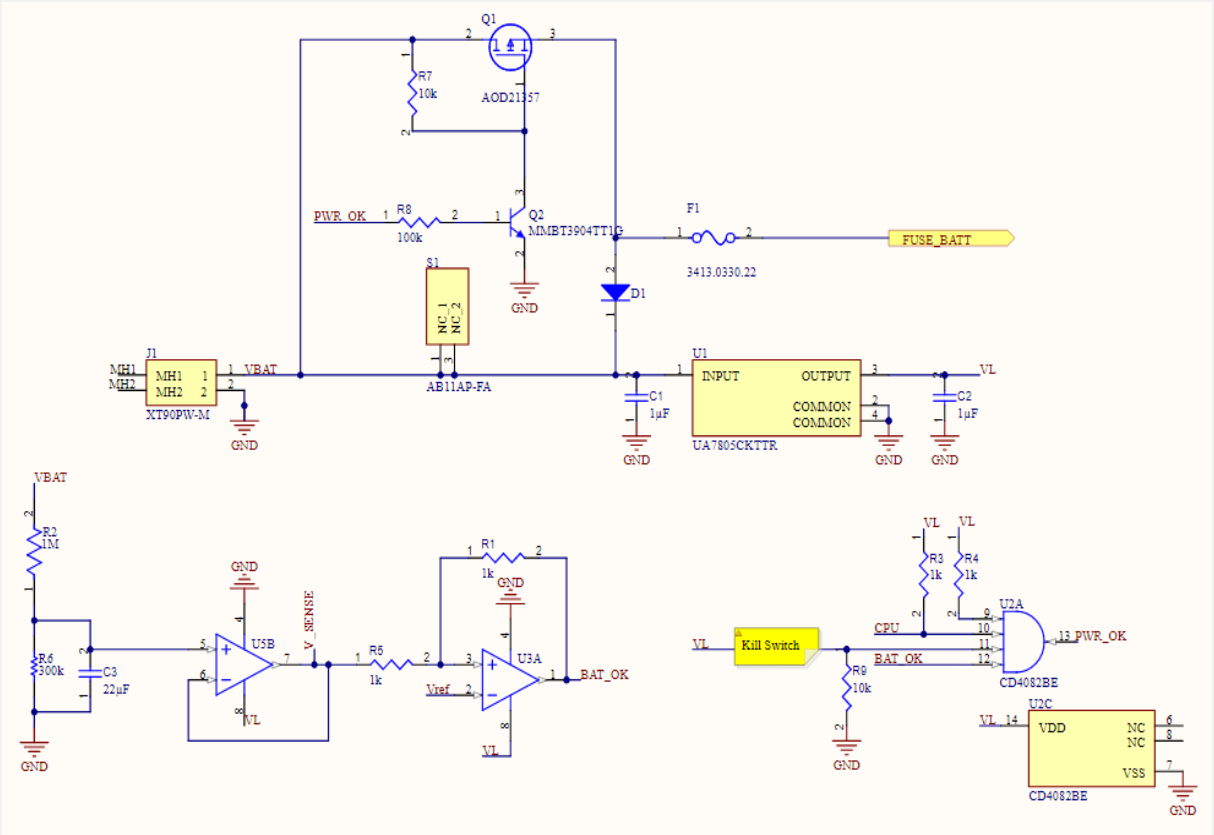
Input → RF switch → Termination configuration is identical for the five channels, only represented once above

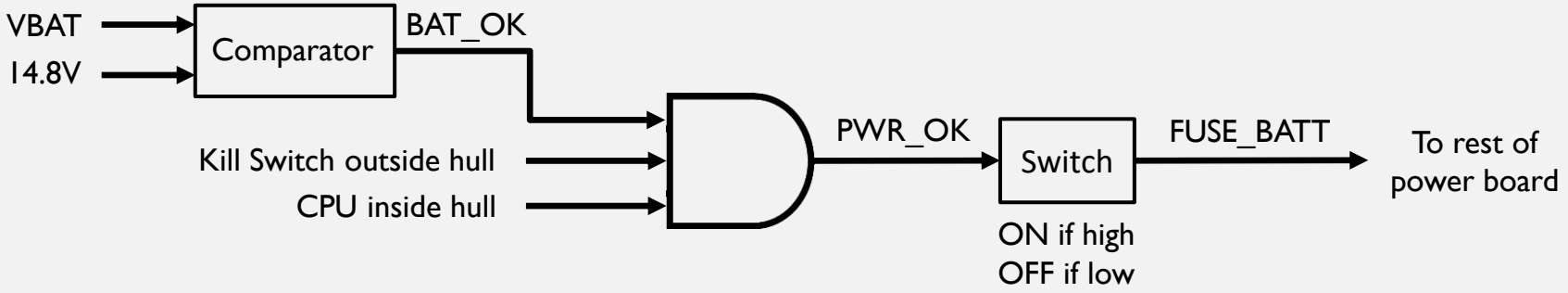
→ high-speed microstrip trace

Kill Switch and Low-Voltage Detection

- Circuit developed as a team of three in the context of McGill Robotics
- This circuit sheet is part of the power board design for the Autonomous Underwater Vehicle (AUV)
- Power board PCB will be developed when all power circuits are designed
- The purpose of the circuit is to cut-off the battery from the power board if a kill switch is pressed or if low battery voltage is detected
  - Battery connects to circuit through J1 and can be damaged if voltage goes below 14.8V
  - U3 comparator outputs BAT_OK signal as a digital low if VBAT < 14.8V
  - U2 AND gate outputs PWR_OK as a digital high to connect battery to power board
  - U2 AND gate outputs a digital low if either: CPU sends digital low signal, battery voltage under 14.8V, or kill switch is pressed
    - If PWR_OK is a digital low output, the transistors disconnect the battery from the rest of the power board

Schematic





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