Digital Design LU

Protocol

Lab Exercise IV

Group 7

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Forwarding Simulation

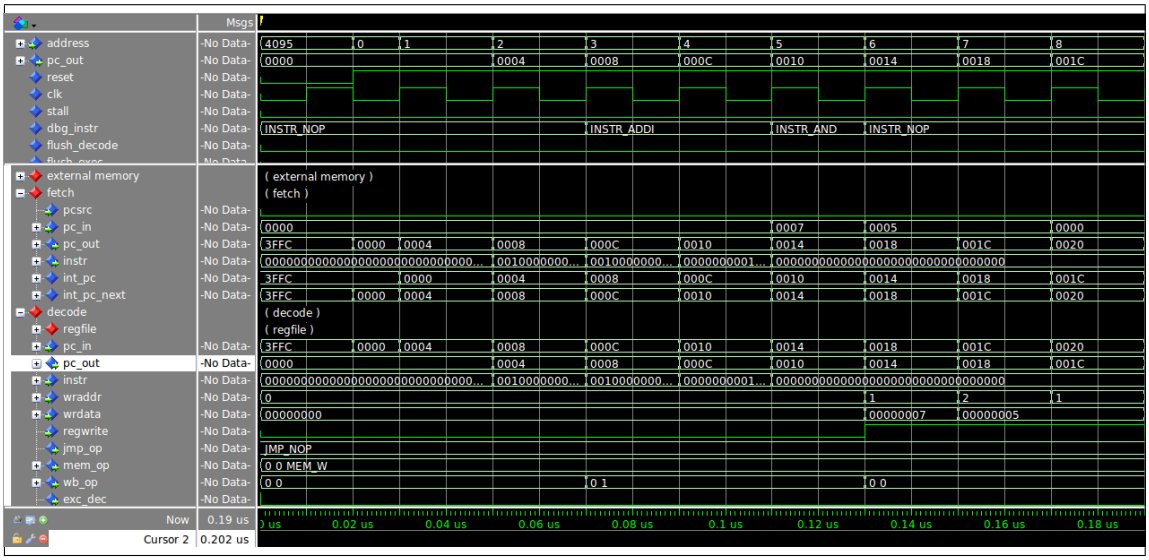

Figure 1: Simulation screenshot for Listing 1.

Make sure that at least the following signals are visible in Figure 1: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 1: Assembler example with forwarding

```
addi $1, $0, 7
addi $2, $0, 5
and $1, $2, $1
nop
nop
```

Branch Hazards Simulation

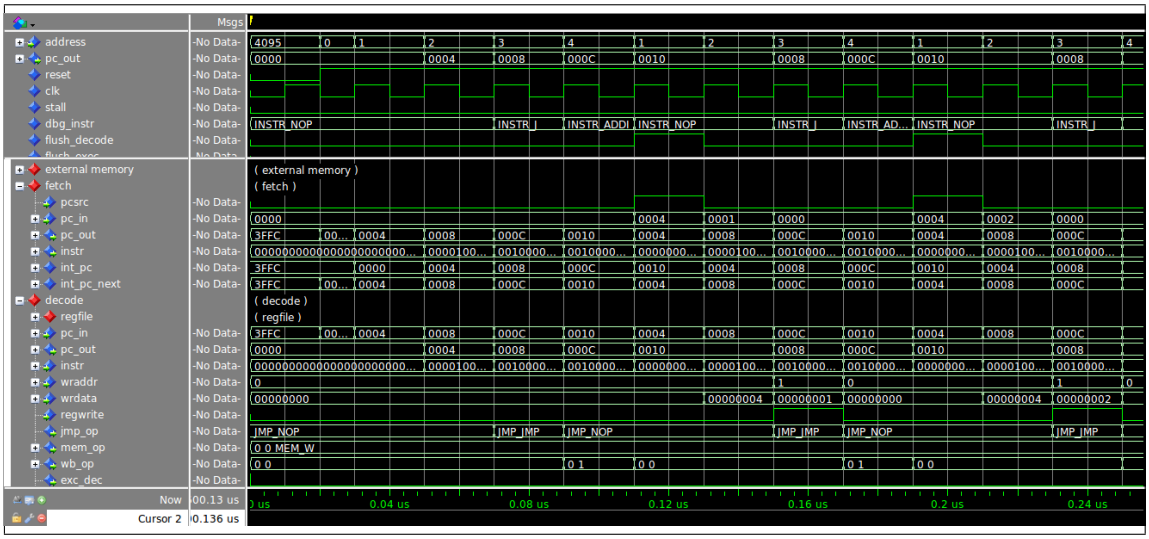

Figure 2: Simulation screenshot for Listing 2.

Make sure that at least the following signals are visible in Figure 2: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 2: Assembler example with branch delay slot

```
loop:   j loop
        addi $1, $1, 1
        addi $2, $2, 1
        nop
```

Synthesis Results

Table 1: Resource usage by entity, including resources used by sub-entities.

	LC Combinationals	LC Registers	Memory Bits
Fetch Stage	87	14	131072
Decode Stage	403 (252)	208 (46)	2048
– Register File	151	162	2048
Execute Stage	1047 (477)	171	0
– ALU	570	0	0
Memory Stage	188 (28)	115	0
– Jump Unit	4	0	0
– Memory Unit	156	0	0
Write-Back Stage	41	71	0
Forwarding Unit	22	0	0
Control Unit	267	218	0
Sum	2055	797	135168

Question: What is the maximum frequency of your design?

Answer: 86.7 MHz

Question: Where is the critical path of your design?

Answer: core:core—pipeline:pipeline—wb:wb_inst—int_op.memtoreg core:core—pipeline:pipeline—mem:mem_inst—int_aluresult_in[21] pll—altpll_component—pll—clk[0] pll—altpll_component—pll—clk[0]

– critical path is from writeback stage the forwarding signal to the alu result out

Feedback & Comments

By answering the optional questions below you can give us feedback and help us to further improve this lab course. Your answers will not influence your grading!

Question: How many hours did you need to solve this lab exercise? Please give us a rough estimate.

Answer:

Question: Were there any annoying problems you encountered (e.g. bugs in tools, flaws in the task description or documentation, etc.)?

Answer:

Question: Other remarks?

Answer: