Results for the final version of the firmware experiment with 768KB total, processed in 4KB chunks

For this experiment, the optimization level used for the speed analysis was -O3 (which generates the fastest code), and for the size it was -Oz (which generates the smallest code).

Below, we can see only the values needed to execute only the sha256 algorithm. (the vector declaration and initialization was subtracted from the final results – see the section *Raw Output*)

Note: All the commands used are listed in the section *Commands used*.

Cycle count

Difference: **960 cycles**

Without the function MatchSET1CLR1: **531,855,072**

With the function MatchSET1CLR1: **531,854,112**

Size

Difference:

text	data	bss	dec	hex
8	0	0	8	8

Without the function MatchSET1CLR1:

text	data	bss	dec	hex

2,012	288	128	2,428	97C

With the function MatchSET1CLR1:

text	data	bss	dec	hex
2,004	288	128	2,420	974

Raw output

Speed

- without the function MatchSET1CLR1:

Full Code: 550796921

Only Vector Generation: 18941849

Difference: **531,855,072**

- with the function MatchSET1CLR1:

Full Code: 550795961

Only Vector Generation: 18941849

Difference: **531,854,112**

Size

- without the function MatchSET1CLR1:

Full Code:

text   data   bss   dec   hex

2758   294   8446   11498   2cea

Only Vector Generation:

text	data	bss	dec	hex
746	6	8318	9070	236e

Difference:

text	**data**	**bss**	**dec**	**hex**
2,012	**288**	**128**	**2,428**	**97C**

- with the function MatchSET1CLR1:

Full Code:

text	data	bss	dec	hex
2750	294	8446	11490	2ce2

Only Vector Generation:

text	data	bss	dec	hex
746	6	8318	9070	236e

Difference:

text	**data**	**bss**	**dec**	**hex**
2,004	**288**	**128**	**2,420**	**974**

Commands used

Full Code

-- Speed --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -fsim -O3 4KB-chunks-full-code.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-full-code-without-function-speed-O3.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>rl78-elf-sim -v 4KB-chunks-full-code-without-function-speed-O3.out Exit code: 0 total clocks: 550796921

-- Size --
D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -Oz 4KB-chunks-full-code.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-full-code-without-function-size-Oz.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>llvm-size 4KB-chunks-full-code-without-function-size-Oz.out

text data bss dec hex filename

2758 294 8446 11498 2cea 4KB-chunks-full-code-without-function-size-Oz.out

Only vector generation

-- Speed --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -fsim -O3 4KB-chunks-only-vector-generation.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-only-vector-generation-without-function-speed-O3.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>rl78-elf-sim -v 4KB-chunks-only-vector-generation-without-function-speed-O3.out Exit code: 0 total clocks: 18941849

-- Size --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -Oz 4KB-chunks-only-vector-generation.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-only-vector-generation-without-function-size-Oz.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>llvm-size 4KB-chunks-only-vector-generation-without-function-size-Oz.out text data bss dec hex filename 746 6 8318 9070 236e 4KB-chunks-only-vector-generation-without-function-size-Oz.out

--- Subsection with the function MatchSET1CLR1 ---

Full Code

-- Speed --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -fsim -O3 4KB-chunks-full-code.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-full-code-with-function-speed-O3.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>rl78-elf-sim -v 4KB-chunks-full-code-with-function-speed-O3.out Exit code: 0 total clocks: 550795961

-- Size --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -Oz 4KB-chunks-full-code.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-full-code-with-function-size-Oz.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>llvm-size 4KB-chunks-full-code-with-function-size-Oz.out

text data bss dec hex filename

2750 294 8446 11490 2ce2 4KB-chunks-full-code-with-function-size-Oz.out

Only vector generation

-- Speed --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -fsim -O3 4KB-chunks-only-vector-generation.c -fdata-sections -ffunction-sections -Wl,--gc-sections -Tlinker_script.ld -o 4KB-chunks-only-vector-generation-with-function-speed-O3.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>rl78-elf-sim -v 4KB-chunks-only-vector-generation-with-function-speed-O3.out Exit code: 0 total clocks: 18941849

-- Size --

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>clang -Oz 4KB-chunks-only-vector-generation.c -fdata-sections -ffunction-sections -Wl,--gc-

sections -Tlinker_script.ld -o 4KB-chunks-only-vector-generation-with-function-size-Oz.out

D:\Repos\llvm-rl78\tests\lit\tests\tickets\ticket_3126\many-vectors\768KB\4KB>llvm-size 4KB-chunks-only-vector-generation-with-function-size-Oz.out

text data bss dec hex filename

746 6 8318 9070 236e 4KB-chunks-only-vector-generation-with-function-size-Oz.out