

Lab 5: Design and Simulation of 4-bit
Adder

ECEN 454-503

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Purpose:

This lab builds on the previous two labs and uses the 1-bit adder to create a 4-bit adder. This is important because it forms one stage of the logic required to build the complete 8-bit adder that will be created in the following labs.

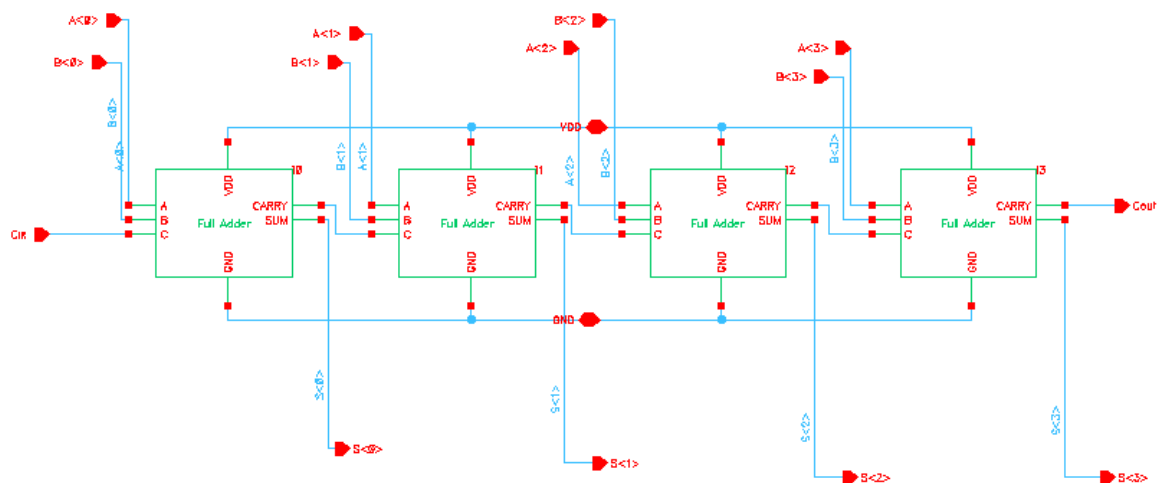
Procedure:

- 1) Create a schematic for the 4-bit adder using the 1-bit adder created in the previous lab. Check and save the schematic.
- 2) Create a symbol for the 4-bit adder from the schematic.
- 3) Create a layout for the 4-bit adder from the 1-bit adder layouts. Run the DRC and fix any errors that occur. Move forward when there are 0 errors reported.
- 4) Generate the extracted layout and perform the LVS. If the net lists do not match, fix the issue. Move forward when the netlists match.
- 5) Create a new schematic for the 4-bit adder post-layout simulation. Perform the simulation, and first make sure all outputs are correct given the inputs.
- 6) Test a subset of the input combinations as specified by the lab manual, and measure the power consumption for each case.

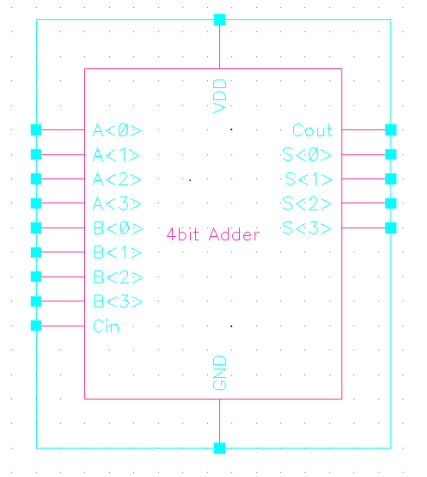
Results:

- 1) Below is the schematic, symbol, layout, and extracted layout for the 4-bit adder. When creating these aspects, there were no errors with the schematic or symbol, but there was an error when the LVS was reached. This turned out to be because a m2_m3 connection pin was forgotten in the layout, and thus the pin did not connect to the proper inputs. This issue was fixed and the LVS ran without any problem.

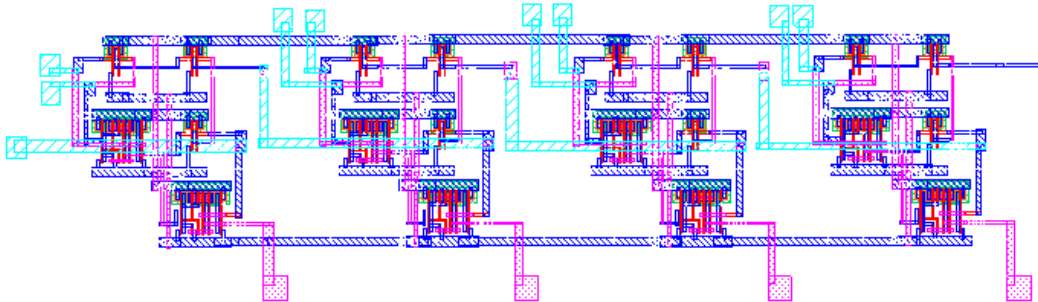
Schematic:



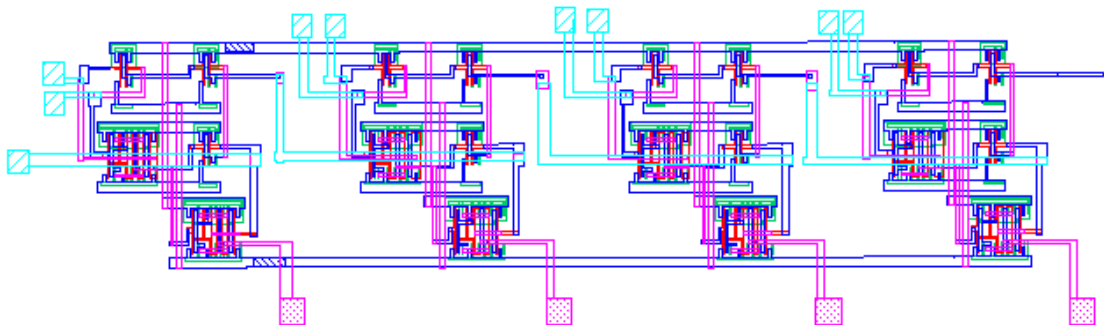
Symbol:



Layout:



Extracted Layout:



DRC:

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "4bitadder_Lab5 layout" *****
Total errors found: 0
```

LVS:

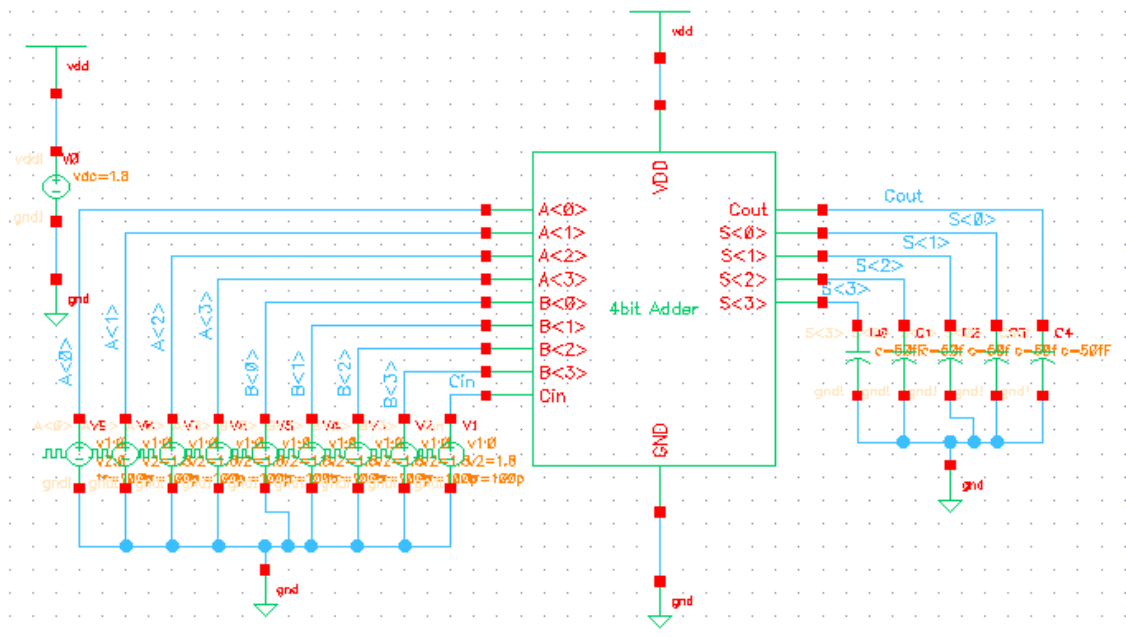
Terminal correspondence points		
N82	N11	A<0>
N80	N12	A<1>
N77	N13	A<2>
N75	N14	A<3>
N90	N5	B<0>
N88	N8	B<1>
N86	N9	B<2>
N84	N10	B<3>
N85	N0	Cin
N87	N6	Cout
N78	N15	GND
N83	N7	S<0>
N81	N2	S<1>
N79	N3	S<2>
N76	N4	S<3>
N89	N1	VDD

Devices in the netlist but not in the rules:
pcapacitor

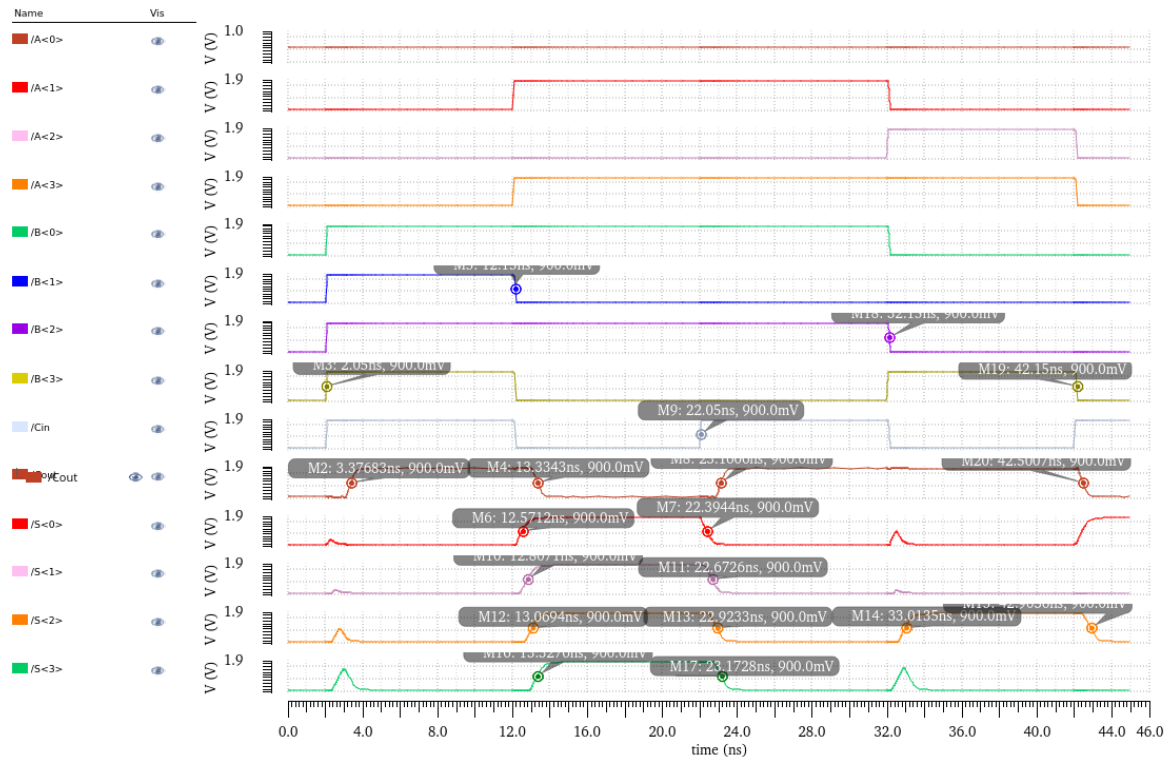
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

- The next step was to create the schematic for the simulation of the 4-bit adder. This was made in a similar method to the previous lab, although 9 pulse voltage sources had to be used to generate the desired signals. These signals were created based on the cases that the lab manual specified should be tested. The schematic can be seen below.



As can be seen by the waveform below, the two outputs produce the correct results for the given the inputs. Within the waveform a few spikes can also be seen on the output pins where they are not intended to be. This is caused by the input signal switching, which can result in a high signal on the output pin for a fraction of a second, but this does not affect the overall results.



The table below has been created from the waveform to show rising and falling delays for every output pin for each case.

Input	Output	Rising Delay	Falling Delay
A = 0000 B = 1111 C = 1	Cout	1.32 ns	1.18 ns
A = 1010 B = 0101 C = 1	Cout	1.05 ns	1.18 ns
	S<0>	0.42 ns	0.34 ns
	S<1>	0.65 ns	0.52 ns
	S<2>	0.92 ns	0.78 ns
	S<3>	1.17 ns	1.02 ns
A = 1010 B = 0101 C = 1	Cout	1.05 ns	N/A
	S<0>	N/A	0.34 ns
	S<1>	N/A	0.52 ns
	S<2>	0.86 ns	0.78 ns

A = 1100 B = 1000 C = 0	S<3>	N/A	1.02 ns
	Cout	N/A	0.35 ns
	S<0>	N/A	N/A
	S<1>	N/A	N/A
	S<2>	0.86 ns	0.75 ns
	S<3>	N/A	N/A

During the post-layout simulation, the power consumption was also measured. The results are displayed in the table below. The 0 W for the pulse voltage to A<0> is due to the fact that A<0> is never enabled.

Source	Power Consumed
V0 (DC voltage source)	8.98E-5 W
V9 (A<0> pulse source)	0 W
V8 (A<1> pulse source)	4.38E-8 W
V7 (A<2> pulse source)	2.07E-8 W
V6 (A<3> pulse source)	5.54E-8 W
V5 (B<0> pulse source)	3.48E-8 W
V4 (B<1> pulse source)	6.55E-9 W
V3 (B<2> pulse source)	2.01E-8 W
V2 (B<3> pulse source)	3.62E-8 W
V1 (C pulse source)	5.29E-7 W

Conclusion: This lab helped me understand how each of the individual components, such as the NAND and NOR, can affect the larger, 4-bit adder. For example, delays on each of the smaller gates add up and contribute the delays on the larger gate. This applies to power consumption as well. This lab also gave me the chance to practice setting up larger layouts with multiple layers, and creating and analyzing the post-layout simulations.