Lab 4: Design & Simulation of a 1-bit Adder

ECEN 454-503

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Purpose: This lab builds on the labs before it, and uses the previously made NAND and XOR gates to create a 1-bit adder. The student also learns how to run post-layout simulations on all the gates and the 1-bit adder. This is important for the next lab, in which the 1-bit adder will be used to create a 4-bit adder.

Procedure:

1) Create a directory called 'models' in the cadence directory, and download tsmc20N.m and tsmc20P.m from ecampus. Add these files into the models directory with nothing else.

2) Within cadence, create a new schematic called 'inverter_simulate' and place the inverter symbol made in lab 2. Add a vdd, gnd, vdc, vpulse, and a capacitor. Wire up the design, with vdc connected to vdd and gnd, vpulse connected to the inverter input, and the capacitor connected to the inverter output and gnd. Set the vdc to 1.8V and the vpulse with the specification in the lab manual. Set the capacitor value to 50fF. Add wire names to the input and output wires for measurement purposes.

3) Launch ADE L. Click Setup > Model Library, and add the models from the first step into this field, and delete any others. Click Setup > Environment, and type 'extracted' right before schematic to include the layout. Then, click Analyses > Choose and set the stop time to 30ns. Finally, select Outputs > To be Plotted > Select on Schematic, and click on the input and output wires that were named in the previous step.

4) Start the simulation by clicking Run > Simulation. Measure the rising and falling delay by adding markers and setting the Y value to 900mV. For the power measurement, open the results, and use the calculator to take the average of the current source and the voltage source – multiply those together for the power delivered and save the result.

5) Repeat steps 2-4 for the NAND and XOR gates designed in Lab 2.

6) Now, create a new schematic and symbol for the 1-bit adder using the symbols created in Lab 2, and then create a layout using the NAND and XOR layouts from Lab 2. Run the DRC, extract the layout, and run the LVS. Ensure no errors occur for each test, and fix them if they do.

7) Now, perform steps 2-4 on the 1-bit adder just created. In addition, calculate the maximum frequency that the 1-bit adder can achieve.

Results:

1) The simulation schematic for the inverter was very straight forward. There were no errors in creating it, and the schematic is displayed below.
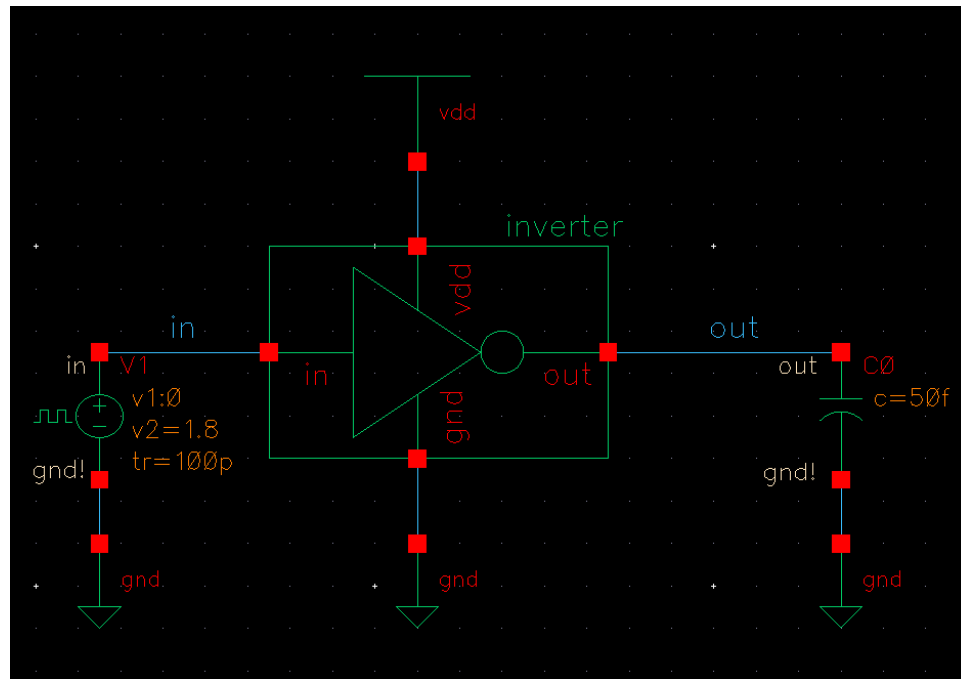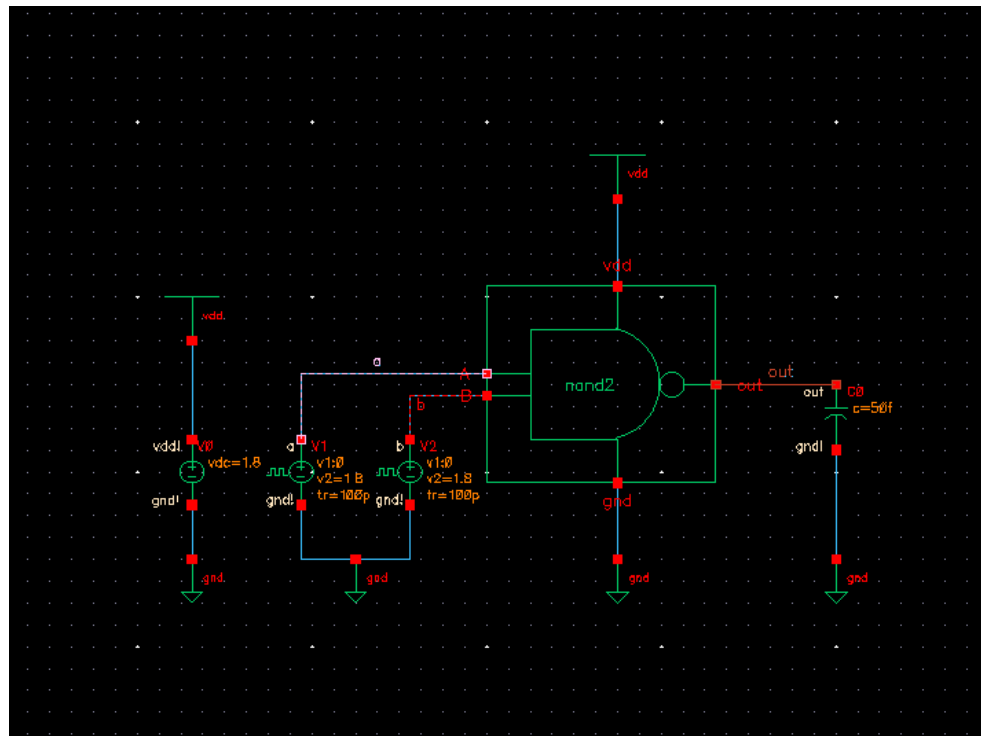

The rising delay of the inverter was found to be 0.25ns, and the falling delay was found to be 0.22ns. These delays have an error of about 10% with respect to each other.
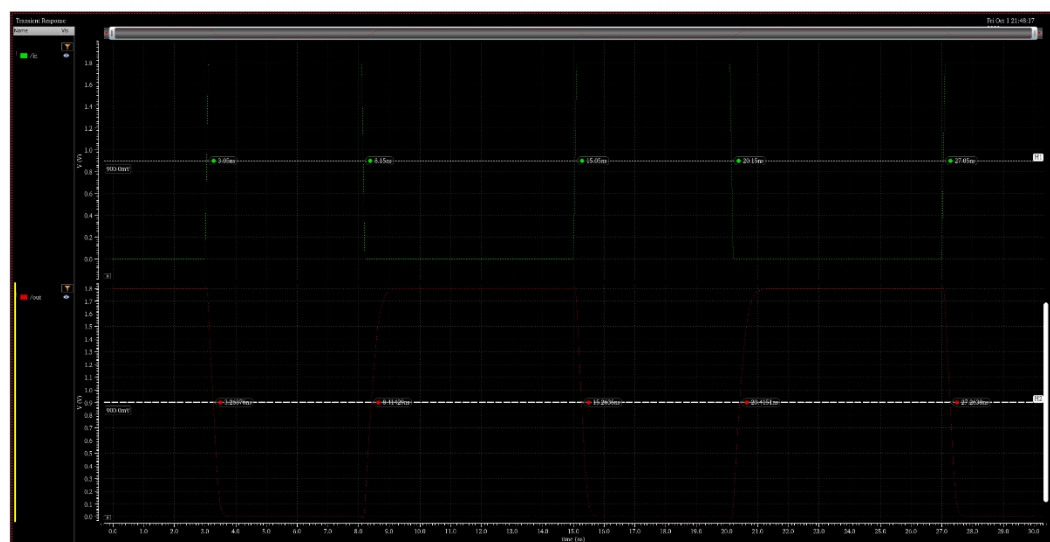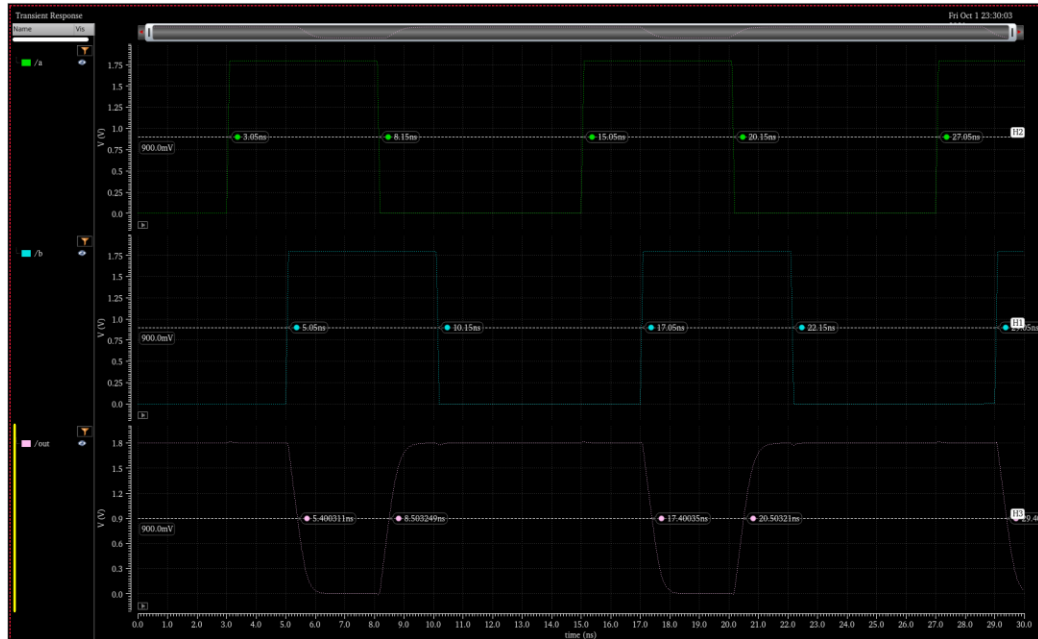
Finally, the power dissipation of the inverter for V0/PLUS was found to be 1.17E-05 W, and the power dissipation for the pulse voltage was found to be 5.11E-06 W.

2) The NAND simulation schematic was setup in a similar way to the inverter, but there were two vpulse inputs used for the two inputs of the gate. One vpulse was offset by a couple more nanoseconds than the other to achieve every possible combination of inputs. The schematic is displayed below.
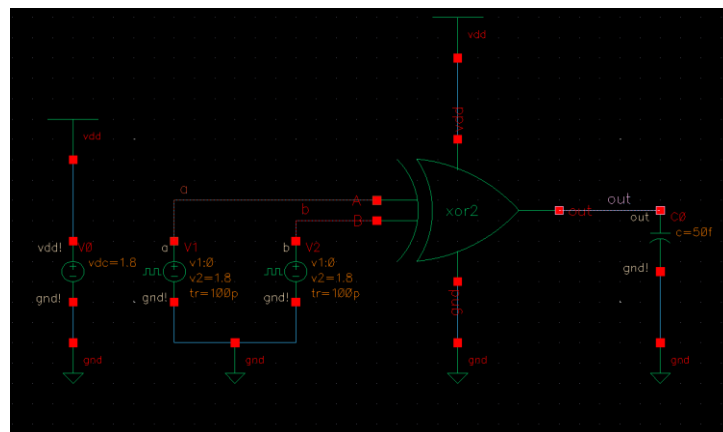
The rising delay for this simulation was found to be 0.27ns and the falling delay was found to be 0.25ns, which have an error of 8% with respect to each other.
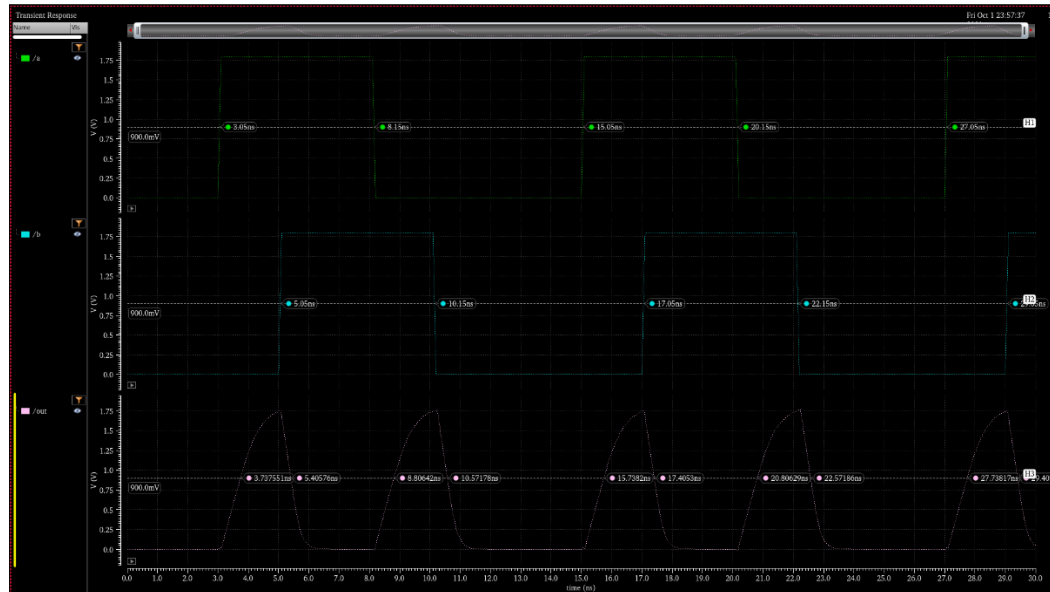

Finally, the power dissipation of the inverter for V0/PLUS was found to be 1.21E-05 W, the power dissipation for the pulse voltage to input A was found to be 1.96E-07 W, and the power dissipation for the pulse voltage to input B was found to be 1.49E-07 W.

3) The XOR simulation schematic was created in the same way the NAND was, with the same offset for the second vpulse input. This also serves to create all possible input combinations. The schematic is displayed below.

The rising delay for this simulation was found to be 0.40ns and the falling delay was found to be 0.35ns, which have an error of 12% with respect to each other.


Finally, the power dissipation of the inverter for V0/PLUS was found to be 3.56E-05W, the power dissipation for the pulse voltage to input A was found to be 4.60E-07W, and the power dissipation for the pulse voltage to input B was found to be 4.33E-07W.

4) Finally, the 1-bit adder was assembled using the NAND and XOR gates created in Lab 2. 3 NAND gates and 2 XOR gates were used to build the schematic, which is displayed below.
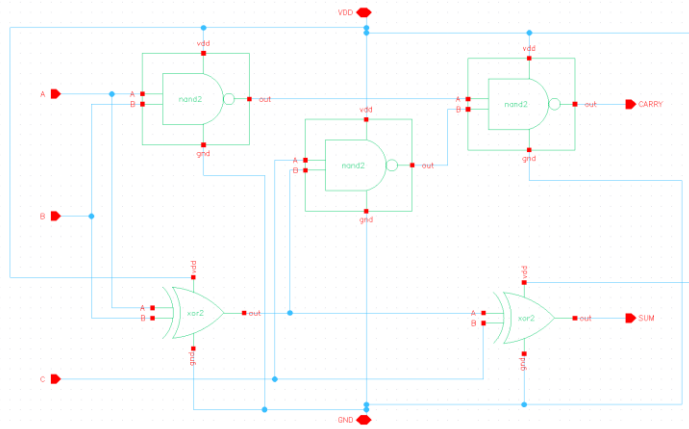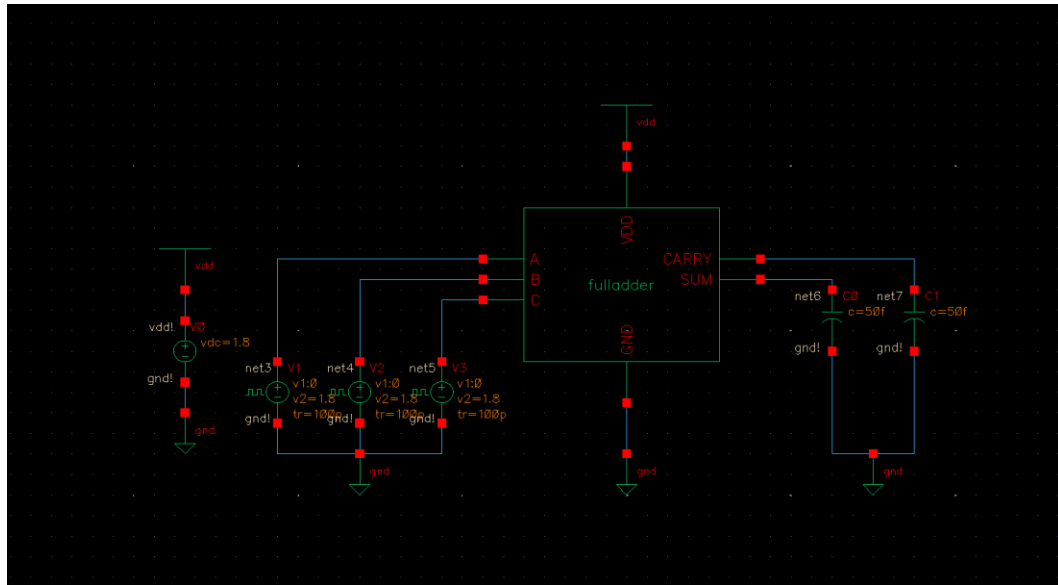
Based on the schematic created, the layout for the 1-bit adder was created using the layouts of the NAND and XOR gates. There are 3 'rows' to this design, with 2 NAND gates on the first, a XOR and a NAND on the second, and just a XOR on the third. For this layout, only metal 1 and metal 2 layers were used for interconnects.
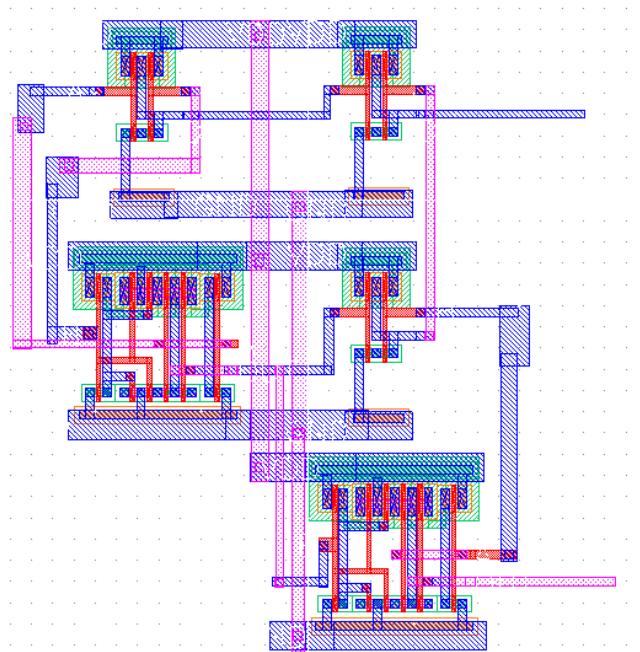
The initial DRC had a few errors, but they were all proximity errors, and were corrected. When run again, the DRC executed with no errors.

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "fulladder layout"   *********
  Total errors found: 0
```

For the LVS, the first LVS run resulted in error – it was found that an instance of m1_m2 was forgotten in the layout where input B needed to connect, and this error was fixed. When run again, the LVS executed with no errors.

```
Terminal correspondence points
N22        N4         A
N21        N9         B
N19        N3         C
N24        N6         CARRY
N18        N0         GND
N20        N1         SUM
N23        N8         VDD

Devices in the netlist but not in the rules:
       pcapacitor
Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4

The net-lists match.
```

Displayed below is the schematic used to simulate the 1-bit adder. It was created in the same way the NAND and XOR were, with an extra vpulse for the C input.
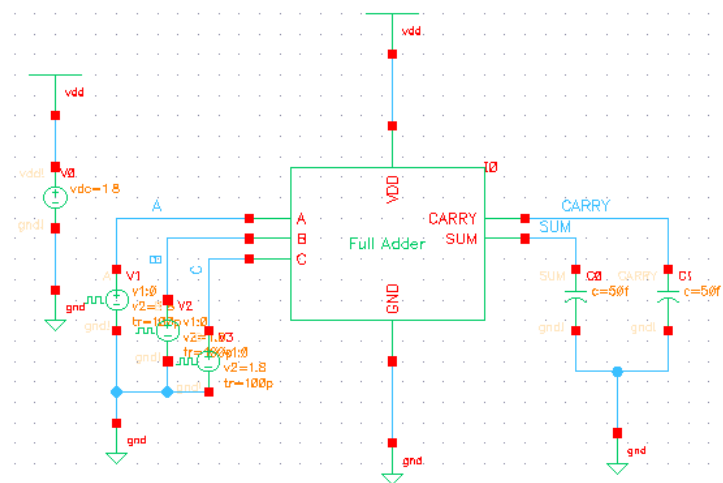

For CARRY, the rising delay for this simulation was found to be 0.43ns and the falling delay was found to be 0.58ns, which have an error of 20% with respect to each other. For SUM, the rising delay for this

simulation was found to be 0.61ns and the falling delay was found to be 0.55ns, which have an error of 15% with respect to each other.
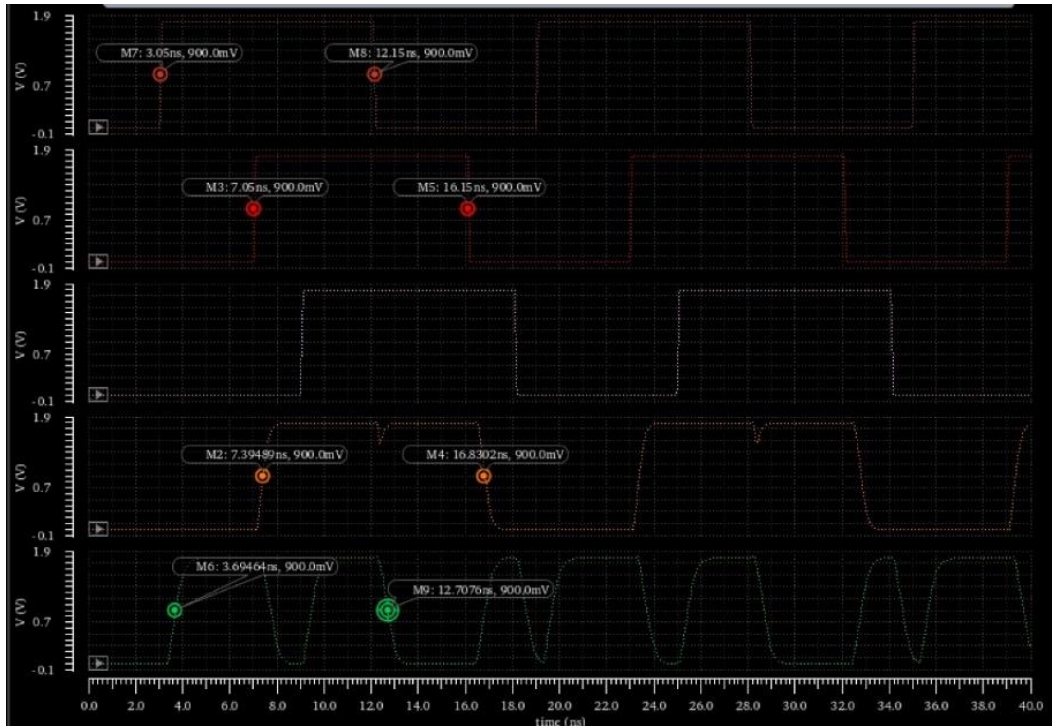
In the waveform below, the period for input C was set to 2.8ns. At SUM, it can be seen that the signals do not completely reach VDD or GND before they get pulled again, whereas they did at a period of 3ns. Thus, the maximum frequency this circuit can achieve is 333 MHz.
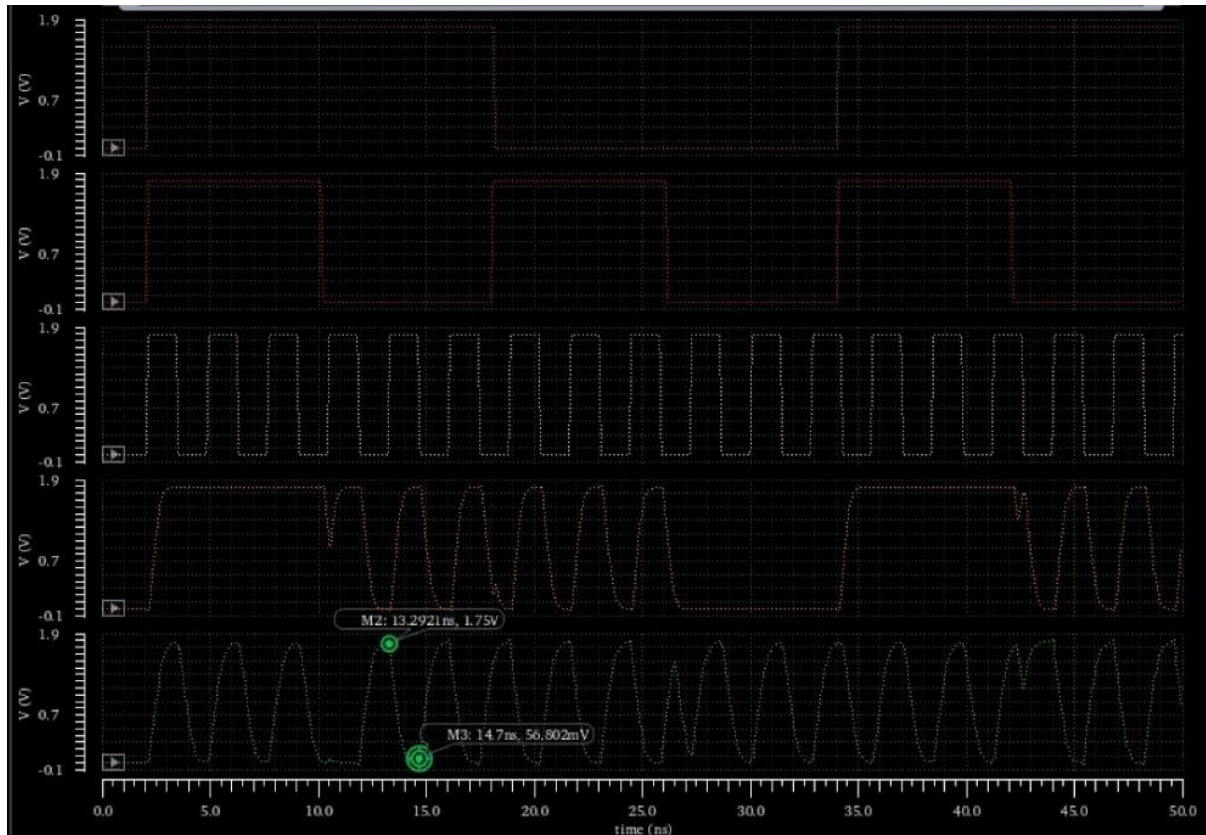
Conclusion: Although a not all of the delays met expectations, they were pretty close to the desired error. Creating the layout for the 1-bit adder helped the student to understand how larger scale layouts can come together with components of other, smaller layouts. Hopefully, the layout of the 1-bit adder in this lab makes it easier to put together a 4-bit adder layout in the next lab.