Lab 6: Design & Characterization of a Flop-Flop

ECEN 454-503

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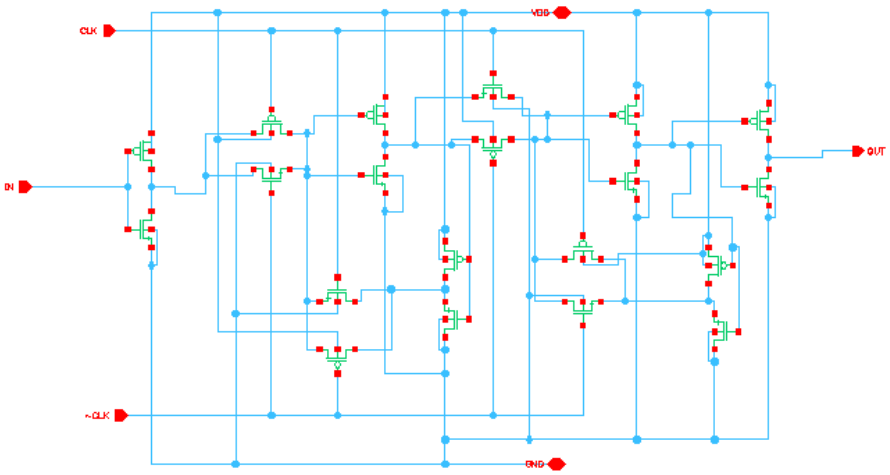
Purpose: This lab serves to further students' knowledge of creating schematics, layouts, and post-layout simulations. It also introduces a new concept, setup time, and teaches students how to measure it.

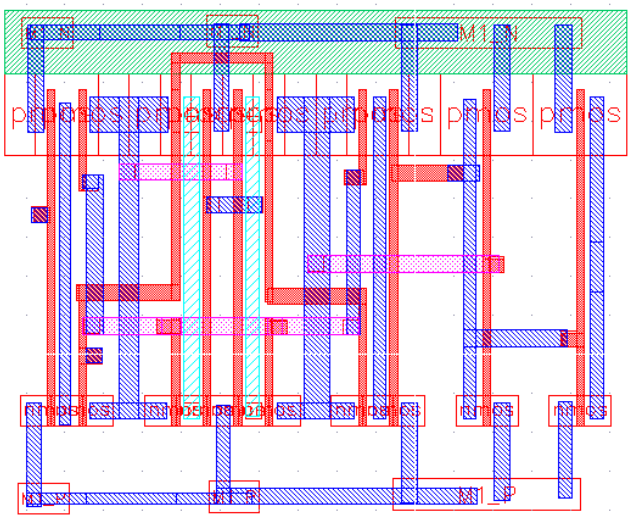
Procedure:

1) Create a Flip-Flip schematic based on that given in the lab manual. Check and save.
2) Create a layout for this Flip-Flip that matches the schematic, and run DRC. If DRC passes, run LVS. If LVS passes, create the post-layout schematic.
3) Vary the load at the output to find the rising and falling delays of the Flip-Flop. Ensure that the rising and falling delays have a different less than 10% when the load is 100fF.
4) Use a sinusoidal voltage source and run an ac analysis of the circuit to measure input capacitance.
5) Vary the delay time of the input to the Flip-Flop, and record the delay of the last signal that went through the Flip-Flop without reaching a meta-stable state. Repeat this process to find the falling setup time as well.

Results:

1) The schematic and layout are displayed below. The schematic is based off of that given in the lab manual, and there were no problems creating this circuit. However, creating the layout took much longer, as many proximity issues came up in the DRC originally. Those issues were fixed, and the LVS passed.



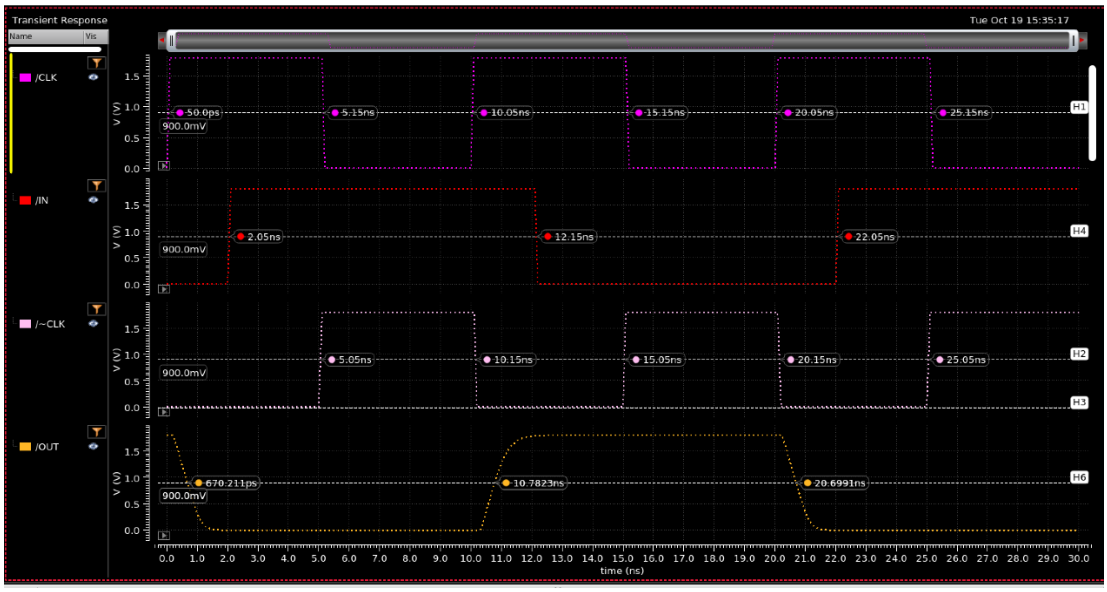


Below are the DRC and LVS results from the schematic and layout.

```
DRC started.......Wed Oct 20 20:40:18 2021
    completed ....Wed Oct 20 20:40:18 2021
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "FlipFlop layout"   *********
   Total errors found: 0
```

```
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/a/alexia_perezv/cadence/LVS/layout/netlist
       count
          13              nets
          6               terminals
          10              pmos
          10              nmos

    Net-list summary for /home/ugrads/a/alexia_perezv/cadence/LVS/schematic/netlist
       count
          13              nets
          6               terminals
          10              pmos
          10              nmos


    Terminal correspondence points
    N9          N3          CLK
    N7          N1          GND
    N11         N12         IN
    N8          N0          OUT
    N12         N10         VDD
    N10         N5          ~CLK

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```

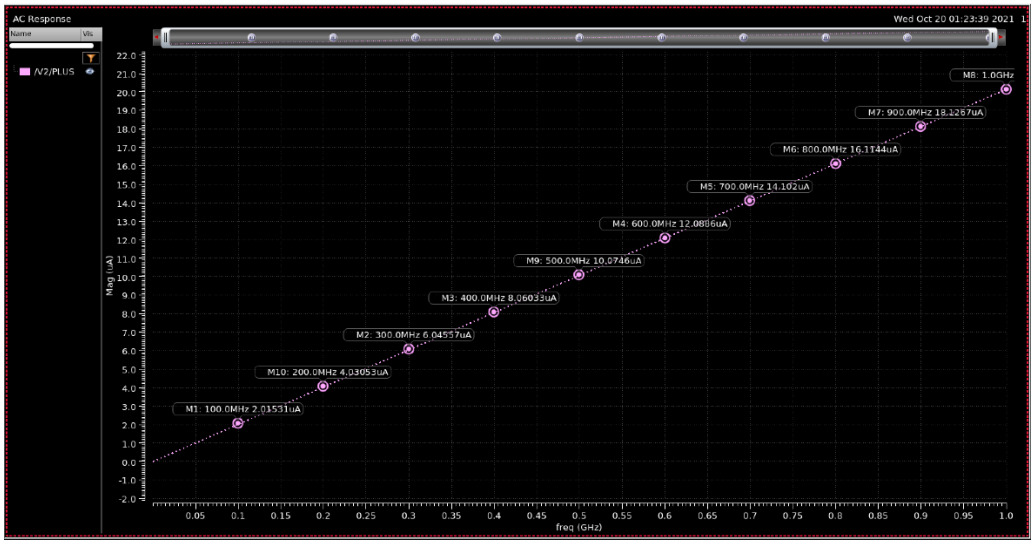
2) Below is the first plot saved to verify correctness of the design. It can be seen that the input propagates to the output only on the rising edge of the clock. This simulation was done with a 100fF load.



3) Below is a table displaying the recorded rising & falling clock-to-Q delays. As it can be seen, at 100fF the error difference between rising and falling delay is ~10%, but as the load capacitance decreases, this error increases.

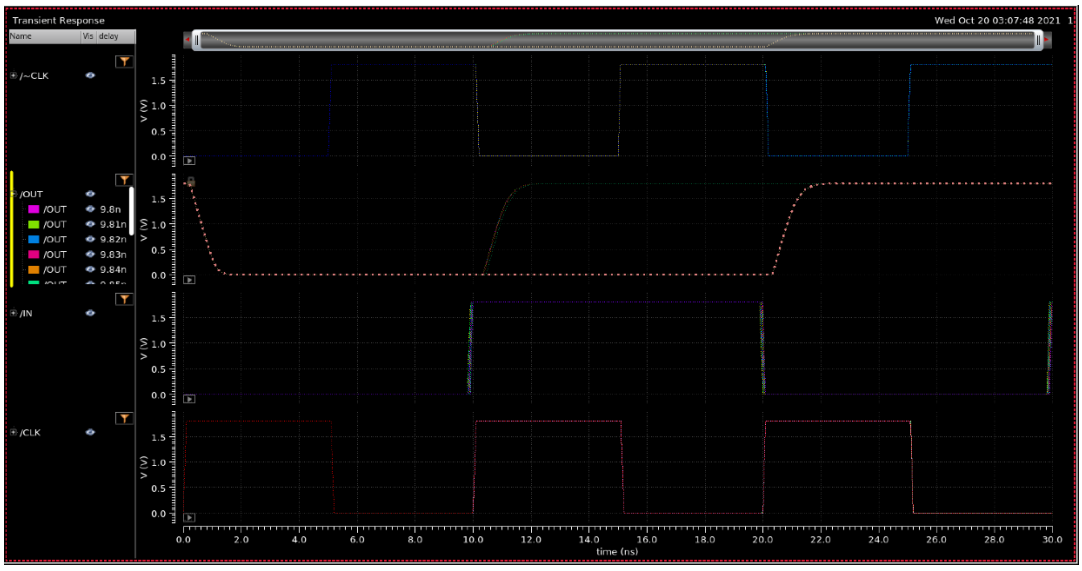
Capacitance	**Rising Delay**	**Falling Delay**	**Error**
100fF	0.73 ns	0.65 ns	10.96%
90fF	0.68 ns	0.6 ns	11.76%
70fF	0.6 ns	0.51 ns	15%
50fF	0.51 ns	0.43 ns	15.69%
40fF	0.46 ns	0.38 ns	17.39%
30fF	0.42 ns	0.34 ns	19.05%
20fF	0.37 ns	0.29 ns	21.62%
10fF	0.33 ns	0.25 ns	24.24%
5fF	0.3 ns	0.22 ns	26.67%
1fF	0.28 ns	0.2 ns	28.57%

4) For the sink capacitance measurement, the waveform obtained is displayed below.

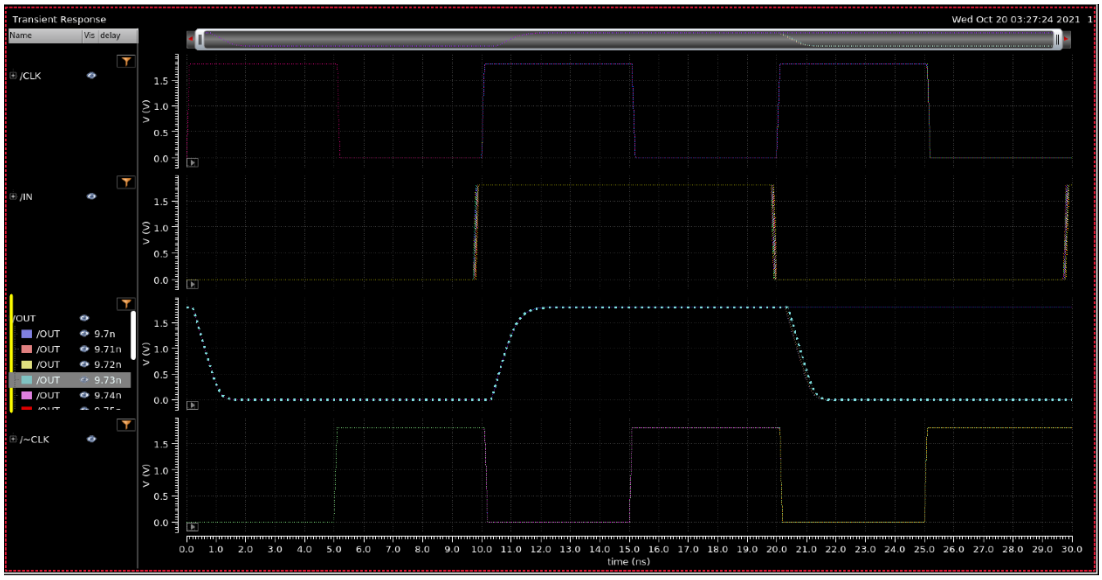


To calculate the sink capacitance for each point, the formula C = I/2*pi*f was used, and then the 10 results were averaged for an **overall sink capacitance of 3.207fF**.

5) The graphs for the rising and falling setup times are displayed below. For this lab, the parametric simulation method was used to find these values, so as you can see below, there are multiple output signals for the varying input delays.



The rising setup time was found to be 10ns – 9.85ns = 0.15ns



The falling setup time was found to be 20ns – (10ns + 9.73ns) = 0.27ns. Thus, the overall setup time is 0.27 ns.

Conclusion: This lab helped the student to further develop their skills in creating schematics, layouts, and post-layout simulations. It also became apparent how the delays of the circuit affect the rising and falling setup time.