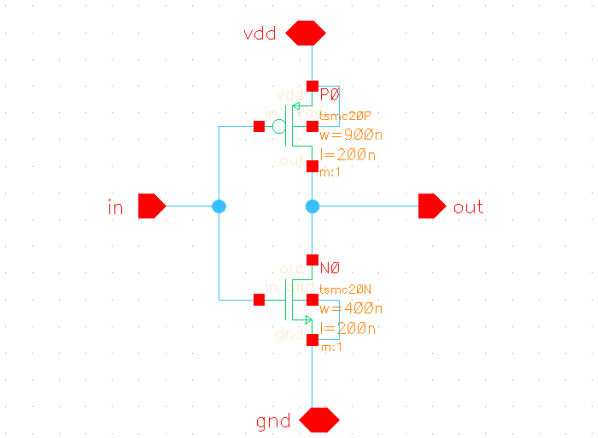
Purpose: This lab is designed to introduce students to design rules, extraction, and verification of corresponding layout and schematic designs. After schematics for each gate is designed, a stick layout can be drawn on paper to guide the student in connect the materials on the layout. This also helps students get practice with creating layers, such as metal 1 and metal 2 layers, so connections don't have to weave around the design.

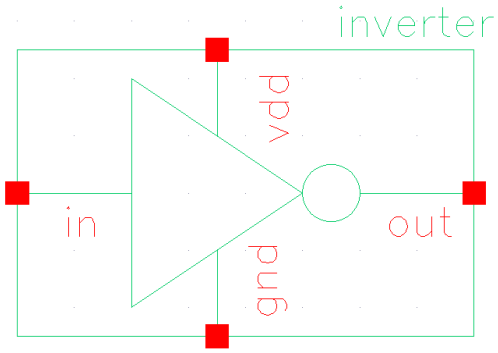
Procedure:

1) Launch cadence and create an inverter schematic from nmos and pmos transistors based on the image given in the lab manual. Check and save the design. Create a symbol from this schematic, and design it to look like a typical inverter gate.
2) Navigate back to the library manager, and create a layout for the inverter. One pmos and one nmos must be placed. Ensure the pmos is twice the width of the nmos. Then, to create a point of contact for two materials, use create > instance. For VDD to the nwell, use M1_N, and for GND to the nmos sources, use m1_poly. Use create > rectangle and the material of choice to connect the terminals based on the schematic. Once this is arranged, use create > pin to place VDD, GND, In, and Out.
3) Verify this layout with the Design Rule Check. Fix any errors that arise. Then, choose verify > extract to create the extracted layout. Once the extracted view pops up, choose verify > LVS. Ensure the schematic and layout chosen are both for the same gate. Run the LVS. If it fails, recheck the schematic and layout to ensure everything is correct. If it succeeds, click 'output', and ensure the text file displays "The net-lists match." This means the design has succeeded. Save this file, or it will be overwritten the next time LVS is run.
4) Repeat the above steps for a 2-bit input NAND (4 transistors) gate, and a 2-bit input XOR (12 transistors) gate. Do not use the inverter within these schematics; create one with a pmos and nmos within the schematic if it is needed.

Results:

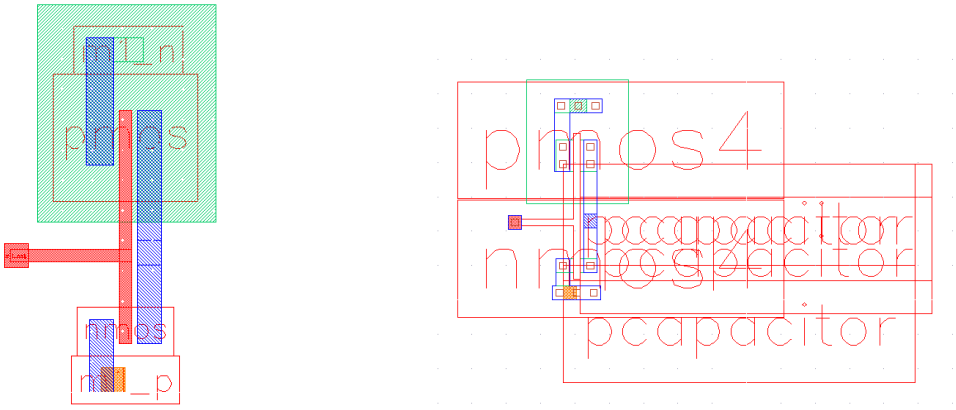
1) For the inverter, one nmos and one pmos were used for the schematic. Both gates were connected to a single input, A, and the pmos source and nmos drain were both connected to the output, out. The drain of the pmos was connected to VDD, and the source of the nmos was connected to GND. From this, a symbol was created, and made to look like a typical inverter. Both are displayed below.





Next, the layout was created. A pmos was placed, along with a nmos half the width. An extension of the nwell of the pmos was made and a VDD pin was placed over this. A metal 1 layer was then drawn from the pmos drain to the m1_n connection point. Below the nmos, m1_poly connection points were created, and a GND pin was placed over this. A metal 1 layer connected the m1_poly to the source of the nmos. Finally, both gates were connected together by poly, and then an A pin was created over a m1_poly connection point to connect the input signal. For the output signal, the pmos source was

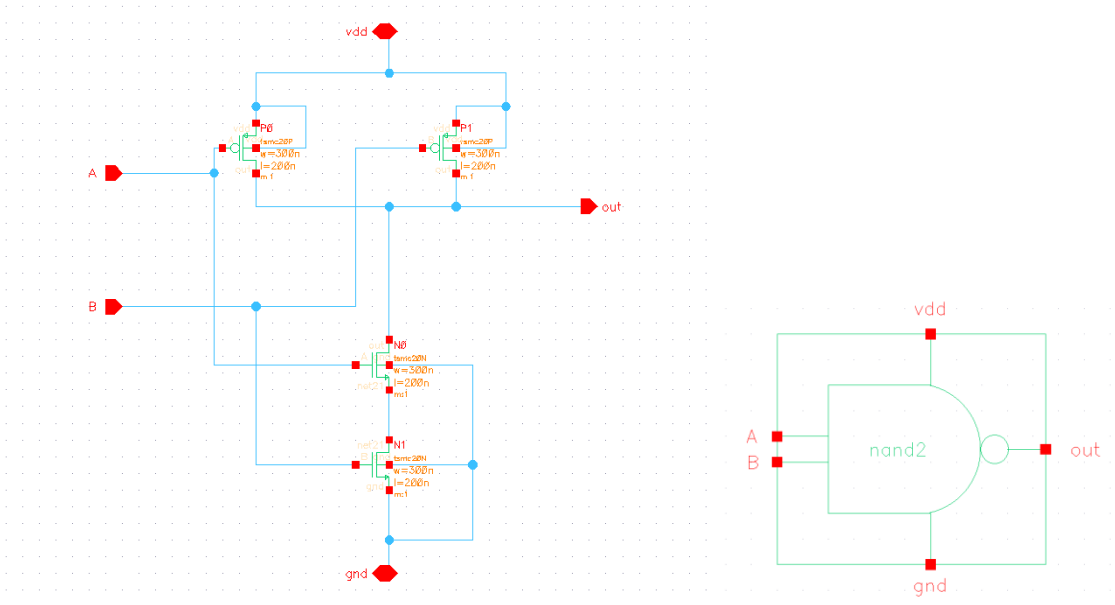
connected to the nmos drain vi metal 1 layer, and a pin for out was created over this. The layout and extracted layout can be seen below.



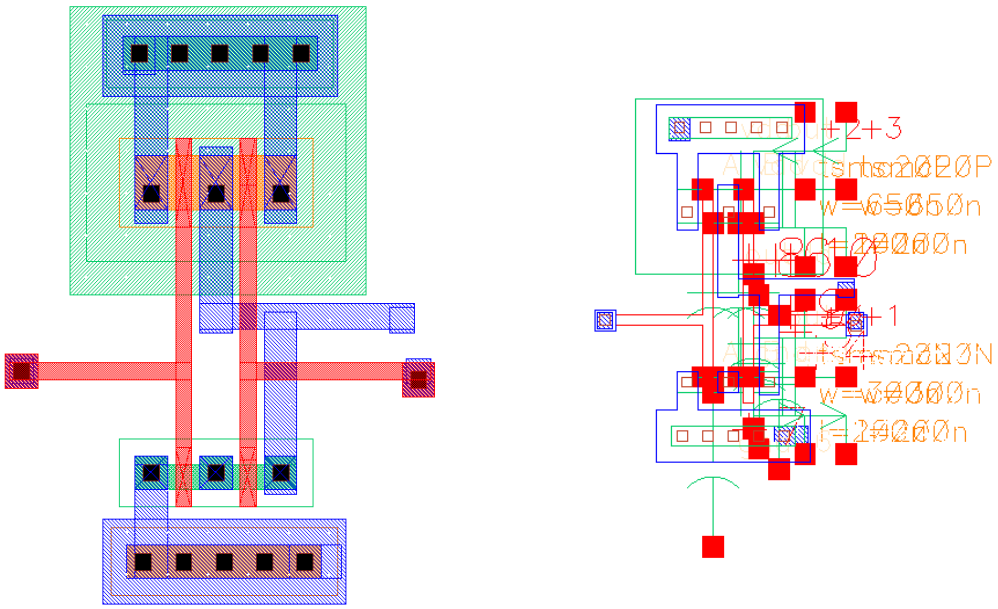
After creating the layout, DRV was run, and any errors were corrected. Finally, in the extracted layout, the LVS was run. This succeeded with no errors, and it can be seen below that the netlists match.

```
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/a/alexia_perezv/cadence/LVS -l -s -t /home/ugrads/a/alexia_perezv/cadence/LVS/layout /home/ugrads/a/alexia_perezv/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/a/alexia_perezv/cadence/LVS/layout/netlist
        count
            4               nets
            4               terminals
            1               pmos
            1               nmos

    Net-list summary for /home/ugrads/a/alexia_perezv/cadence/LVS/schematic/netlist
        count
            4               nets
            4               terminals
            1               pmos
            1               nmos


    Terminal correspondence points
    N1          N3          gnd
    N3          N2          in
    N2          N1          out
    N0          N0          vdd

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    2       2
        total                     2       2

                                  nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    4       4
        total                     4       4

                              terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     4       4
```

2) For the NAND gate, 4 transistors had to be used: two pmos transistors, one with input A and the other with input B, in parallel along with two nmos transistors, one with input A and the other with input B, in series. For the output, the sources of the pmos transistors were connected to the drain of one of the nmos transistors. From this, a symbol was created to look like a typical NAND gate. The schematic and symbol can be seen below.



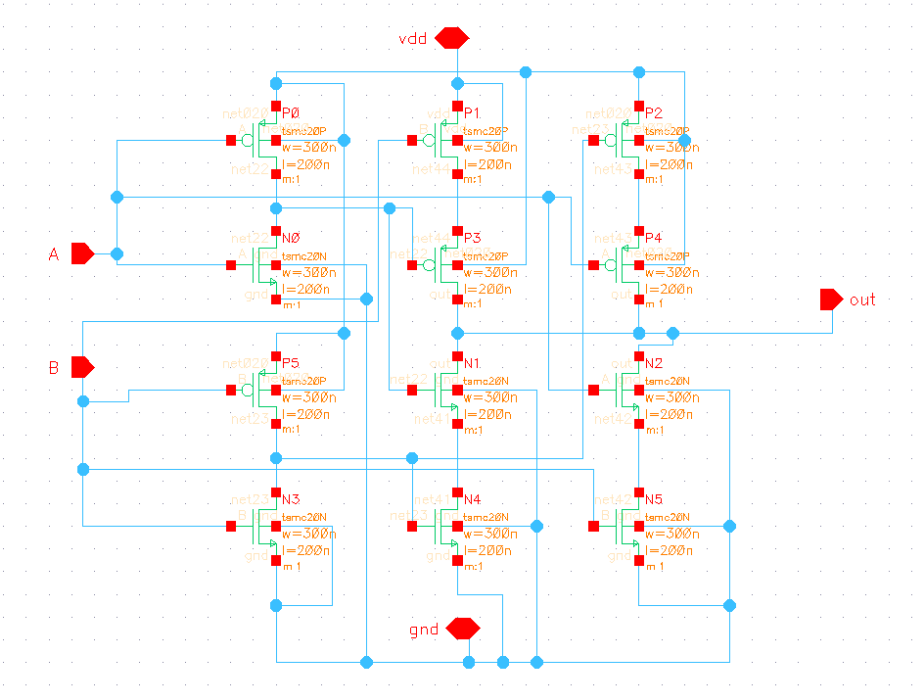
After the schematic, the layout was created. In this schematic, the two pmos sources were placed to overlap one another, and the one nmos was placed so that it's source overlapped with the other nmos' drain. Then, VDD and GND were connected appropriately, and the gate for each pair of nmos and pmos were connected via poly, with one being connected to the input A, and the other to input B. The pmos sources were then connected to one of the nmos' drain (in this case, the one with input A).

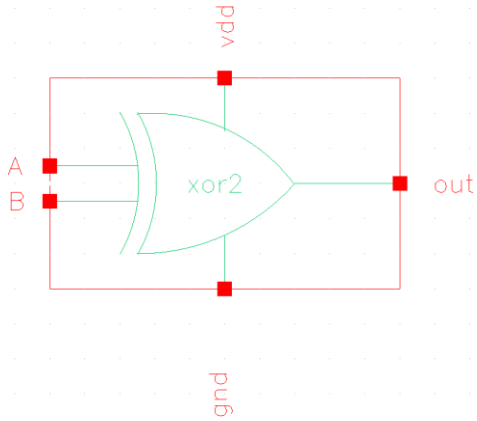


After creating the layout, DRV was run, and any errors were corrected. Finally, in the extracted layout, the LVS was run. This succeeded with no errors, and it can be seen below that the netlists match.

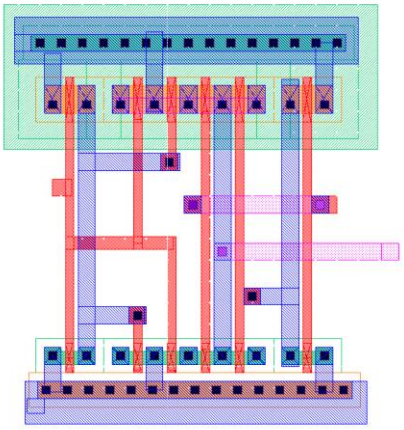
```
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/a/alexia_perezv/cadence/LVS -l -s -t /home/ugra
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/a/alexia_perezv/cadence/LVS/layout/netlist
       count
         6              nets
         5              terminals
         2              pmos
         2              nmos

    Net-list summary for /home/ugrads/a/alexia_perezv/cadence/LVS/schematic/netlist
       count
         6              nets
         5              terminals
         2              pmos
         2              nmos


    Terminal correspondence points
    N4          N4          A
    N3          N5          B
    N2          N1          gnd
    N5          N3          out
    N1          N0          vdd

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.
```

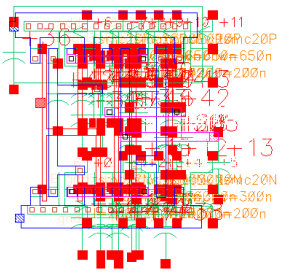
3) Finally, the XOR was created with 12 transistors; 6 pmos and 6 nmos. 2 of each were used just to create inverted input signals. For the pmos, a B and a ~A in series were connected in parallel with a ~B and A in series, and for the nmos a ~A and ~B in series were connected in parallel with an A and B in series. The schematic and symbol are displayed below.





The layout for the XOR was connected in a similar way to the inverter and NAND, and modeled after the XOR schematic. The only difference in this layout is that two metal layers were used, metal 1 and metal 2, so that metal to metal connections would not overlap one another and connect unintentionally, and so that the nets wouldn't become convoluted. The final layout and extracted layout are displayed below.





After creating the layout, DRV was run, and any errors were corrected. Finally, in the extracted layout, the LVS was run. The first time it was run, it failed for this design. After carefully reviewing both the schematic and layout, I was unable to determine why the netlist was failing. I plan on meeting with my TA on Monday to resolve this issue before Lab 3, and I have not included the LVS output screenshot due to the error. I will create a comment in this submission once I resolve this issue and include a screenshot of the LVS passing all netlist tests.

Conclusion:

At the beginning of the lab, connecting and understanding layouts was difficult because I did not have previous experience with it, but as the lab progressed, it became more apparent how the schematic related to the layout.