Texas A&M University

Lab 3: Cell Characterization

ECEN 454

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Purpose: This lab is intended to introduce students to cell characterization. Although there are many factors that can go into cell characterization, for this lab, the student will focus on delays and input capacitance. By modeling the NAND and XOR gates off of the circuits created in the previous lab, students will be able to see how these parameters effect circuits they've created.

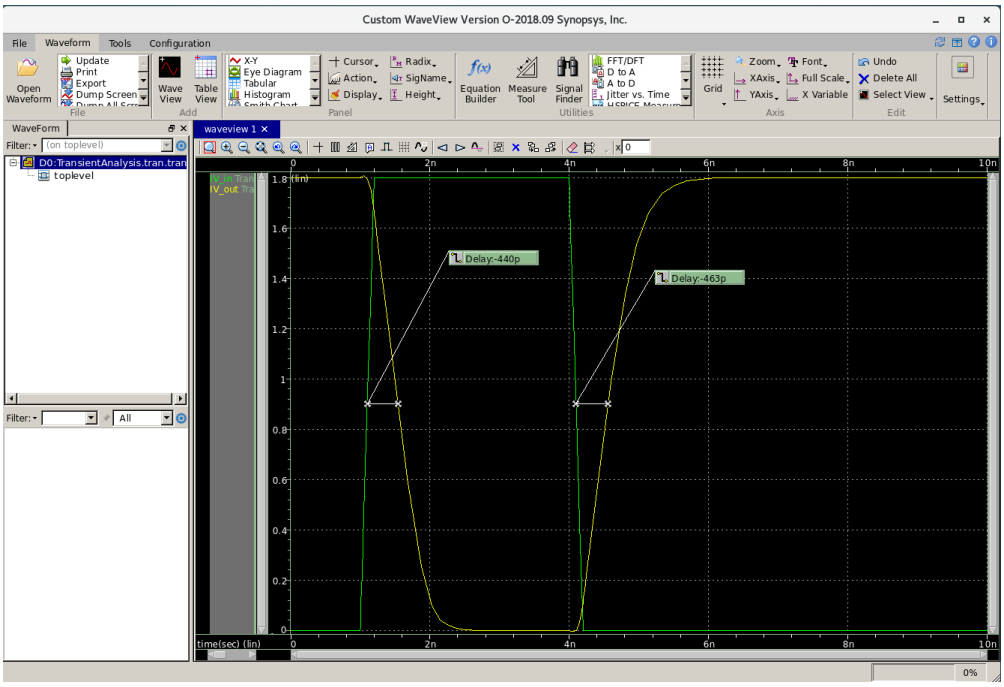
Procedure:

1) Download all the necessary files from eCampus, and look over cell18.spi to understand what it is doing. Make a copy of demo.spi and rename it inverter.spi to use as the first simulation.
2) Run the simulation for inverter.spi. Open waveforms and import the waveform created from this simulation, located in the directory inverter.raw/, and click TransientAnalysis.
3) Click on tools > measurement and set a time domain to measure the delay from 50% to 50%. Drag the measurement box along the waveform to obtain rising delay and falling delay.
4) Modify inverter.spi with the values used in the previous lab for width of the nmos and pmos. Record the rising and falling delay, and compute the error between the two delays. If it is larger than 10%, change the widths of the nmos or pmos to get the error under 10%.
5) Copy the demo.spi file again and rename it inverter_delaytable.spi. Remove the resistor, and change the output connection of the capacitor. Choose 15 values for the capacitor between 1fF and 100fF, and record the rising and falling delay for each value.
6) Use the file simcap.spi to run the AC simulation. Open the file and understand what it is doing. Run the simulation, and set up the measuring tool for a general Data(x,y) measurement. Add 10 of these measurements and use these to acquire sink capacitance.
7) Add NAND2 and XOR2 subckts to the cell18.spi file, and redo steps 1-6 for both of these gates.

Results:

1) The first inverter simulation was done without making any changes to the files, which resulted in a large difference between the rising and falling delay. After this, the inverter.spi file was modified to have a pmos width of 0.98um and a nmos width of 0.35um. The delays became closer in value, within a 10% error of one another, as shown below.

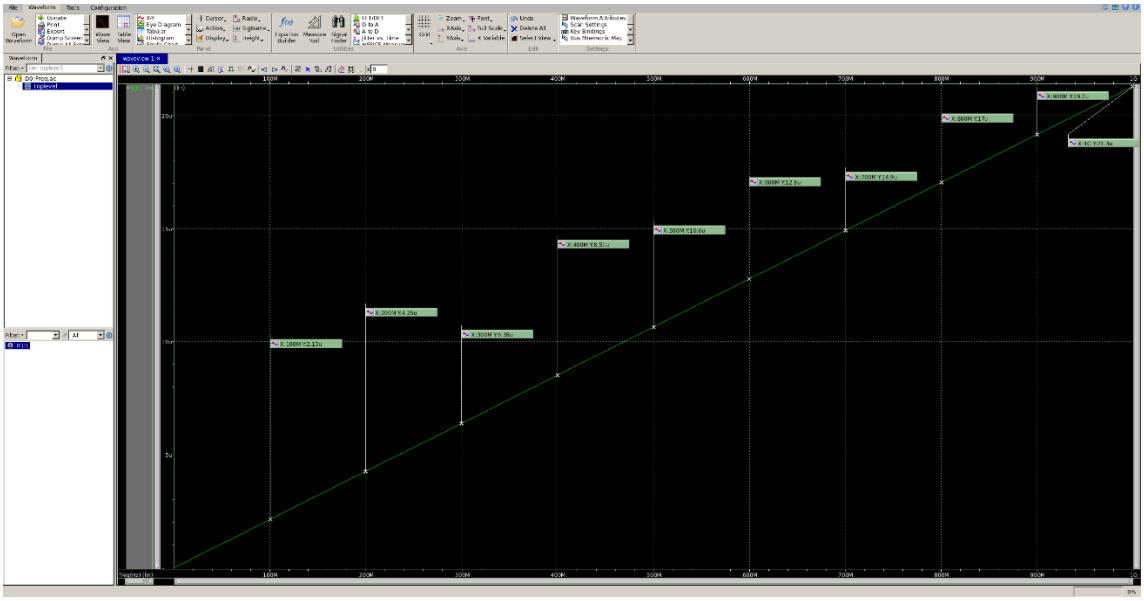
```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.98u lp=0.2u wn=0.35u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```



2) The table below shows the rising and falling delay for different values of capacitance. As can be seen, the delays increase as the capacitance increases, but the error decreases as the capacitance increases.

Capacitance	Rising Delay (pF)	Falling Delay (pF)	Error
1fF	-26.5	-44.7	68.67925
8fF	-71.1	-88.2	24.05063
15fF	-103	-118	14.56311
22fF	-131	-145	10.68702
29fF	-159	-174	9.433962
36fF	-186	-203	9.139785
43fF	-215	-231	7.44186
50fF	-242	-261	7.85124
57fF	-270	-290	7.407407
64fF	-297	-317	6.734007
71fF	-325	-348	7.076923
78fF	-354	-376	6.214689
85fF	-381	-403	5.774278
92fF	-408	-430	5.392157
100fF	-441	-464	5.21542

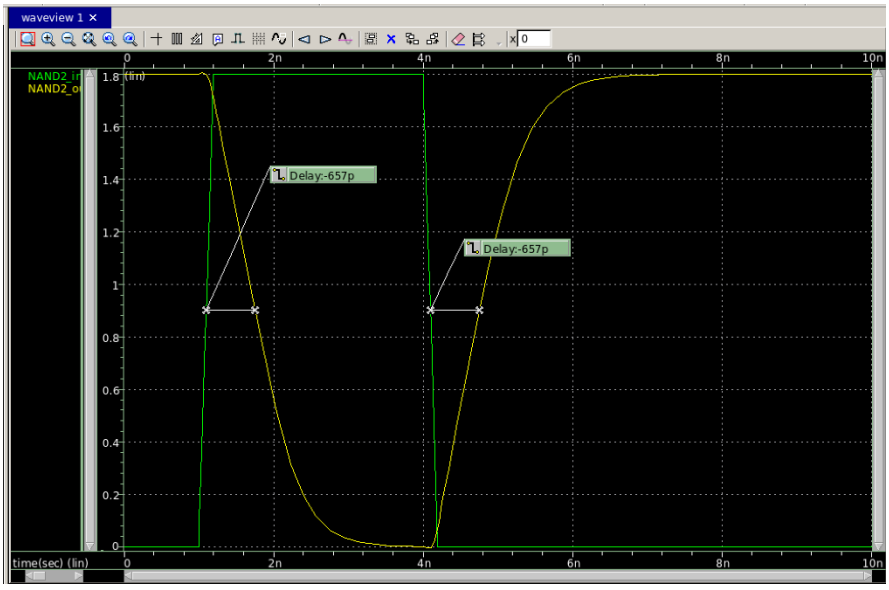
3) For the AC simulation, the simulation file and waveform are displayed below with 10 sample points.



To calculate the sink capacitance for each point, the formula C = I/2*pi*f was used, and then the 10 results were averaged for an overall sink capacitance of 2.75fF.

4) After the inverter was completed, the NAND2 gate was connected on the cell18.spi, and simulation files for the NAND were made. The delay was observed for the default pmos and noms widths, and then was adjusted to have a pmos width of 0.65um and a nmos width of 0.3um to obtain rising and falling delay with a 0% error. The waveform and simulation file are displayed below.

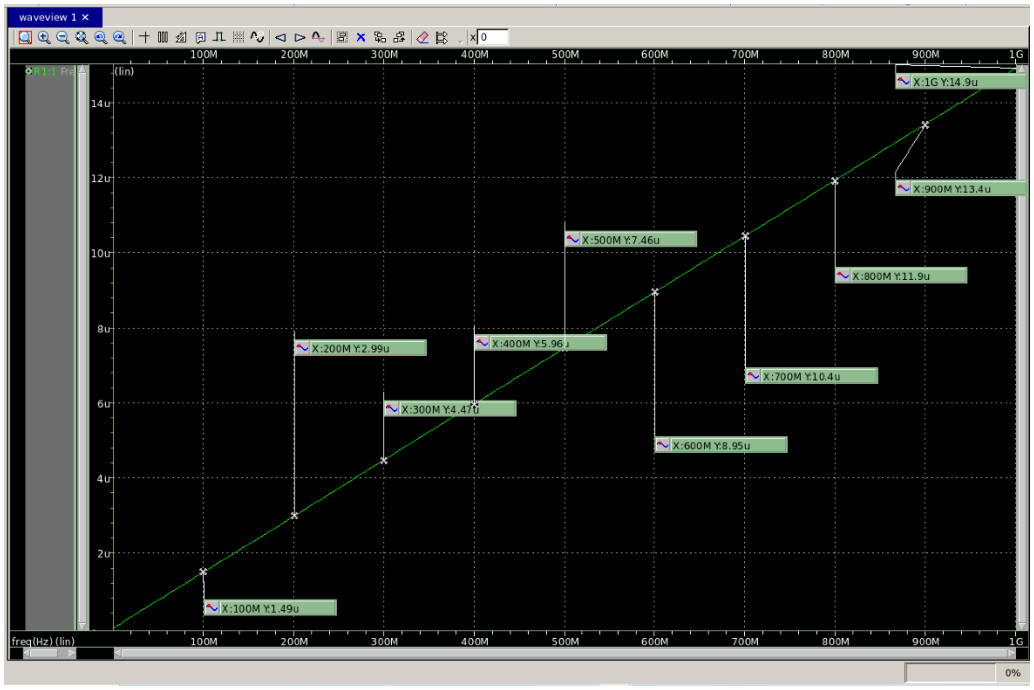
```
;Spice netlist for a nand2 gate and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND2_in vdd NAND2_out vdd gnd) NAND2 wp=0.65u lp=0.2u wn=0.3u ln=0.2u

R1 (NAND2_out 1) resistor r=1
C1 (NAND2_out 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND2_in NAND2_out
```



5) The table below shows the rising and falling delay for different values of capacitance. As can be seen, the delays increase as the capacitance increases.

Capacitance	Rising Delay (pF)	Falling Delay (pF)	Error
1fF	-37.2	-56.2	51.07527
8fF	-95	-109	14.73684
15fF	-138	-150	8.695652
22fF	-181	-192	6.077348
29fF	-224	-234	4.464286
36fF	-268	-277	3.358209
43fF	-310	-320	3.225806
50fF	-352	-360	2.272727
57fF	-397	-401	1.007557
64fF	-439	-441	0.455581
71fF	-481	-484	0.623701
78fF	-523	-525	0.382409
85fF	-566	-567	0.176678
92fF	-604	-609	0.827815
100fF	-657	-657	0

6) For the AC simulation, the waveform is displayed below with 10 sample points.

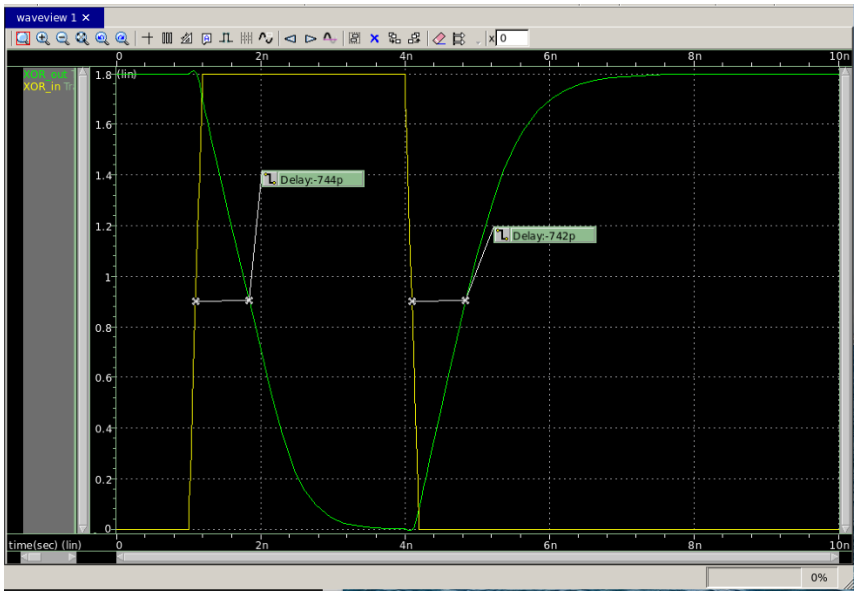


To calculate the sink capacitance for each point, the formula C = I/2*pi*f was used, and then the 10 results were averaged for an overall sink capacitance of 2.37fF.

7) After the inverter was completed, the XOR2 gate was connected on the cell18.spi, and simulation files for the XOR were made. The delay was observed for the default pmos and noms widths, and then was adjusted to have a pmos width of 1.2um and an nmos width of 0.2um to obtain rising

and falling delay with a -0.2688% error. The simulation file and waveform are displayed below.

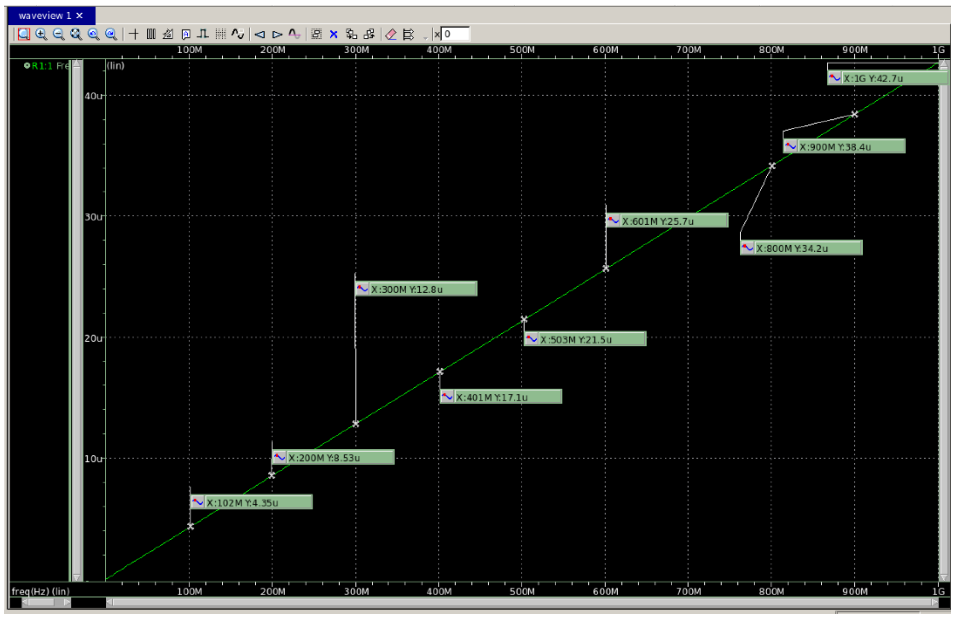
```
;Spice netlist for an xor and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR_in XOR_out vdd gnd) XOR wp=1.1u lp=0.2u wn=0.2u ln=0.2u

R1 (XOR_out 1) resistor r=1
C1 (XOR_out 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR_in XOR_out
```



8) The table below shows the rising and falling delay for different values of capacitance. As can be seen, the delays increase as the capacitance increases, but the error decreases as the capacitance increases.

Capacitance	Rising Delay (pF)	Falling Delay (pF)	Error
1fF	-42	-50.7	20.71429
8fF	-96.7	-109	12.71975
15fF	-147	-157	6.802721
22fF	-197	-206	4.568528
29fF	-246	-254	3.252033
36fF	-296	-303	2.364865
43fF	-345	-351	1.73913
50fF	-394	-399	1.269036
57fF	-444	-448	0.900901
64fF	-493	-495	0.40568
71fF	-542	-543	0.184502
78fF	-591	-593	0.338409
85fF	-640	-640	0
92fF	-689	-687	-0.29028
100fF	-744	-742	-0.26882

9) For the AC simulation, the waveform is displayed below with 10 sample points.



To calculate the sink capacitance for each point, the formula C = I/2*pi*f was used, and then the 10 results were averaged for an overall sink capacitance of 5.02fF.

10) Finally, the cell18.spi file is included below with each subckt defined and connected. This file was made with reference to each circuit created in the previous lab.

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV

//Spice netlist for nand2 gate
subckt NAND2 (input1 input2 output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        //order is drain, gate, source, body
        M1 output input1 VDD VDD tsmc18P w=wp l=lp
        M2 output input2 VDD VDD tsmc18P w=wp l=lp
        M3 output input1 net VSS tsmc18N w=wn l=ln
        M4 net input2 VSS VSS tsmc18N w=wn l=ln
ends NAND2

//Spice netlist for xor2 gate
subckt XOR (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u

        // First we need four inverters
        M1 inv1 input VDD VDD tsmc18P w=wp l=lp
        M2 inv1 input VSS VSS tsmc18N w=wn l=ln
        M3 inv2 VDD VDD VDD tsmc18P w=wp l=lp
        M4 inv2 VSS VSS VSS tsmc18N w=wp l=lp

        // Next, we need 4 PMOS transistors
        M5 net56 VDD VDD VDD tsmc18P w=wp l=lp
        M6 output inv1 net56 VDD tsmc18P w=wp l=lp
        M7 net78 inv2 VDD VDD tsmc18P w=wp l=lp
        M8 output input net78 VDD tsmc18P w=wp l=lp

        // Lastly, we need 4 NMOS transistors
        M9 output inv1 net910 VSS tsmc18N w=wn l=ln
        M10 net910 inv2 VSS VSS tsmc18N w=wn l=ln
        M11 output input net1112 VSS tsmc18N w=wn l=ln
        M12 net1112 VDD VSS VSS tsmc18N w=wn l=ln
ends XOR
```

Conclusion: For the first task, it was learned that by decreasing/increasing the pmos width would increase/decrease the rising delay, while the same was true of the nmos width for the falling delay. For the second task, it was learned that generally, increasing output capacitance would increase the rising and falling delay, but decrease the error of the delays with respect to each other. Finally, for the last task, it was learned that the XOR gate had about twice as much sink capacitance as the NAND gate, suggesting a circuit with more transistors would result in a larger sink capacitance.