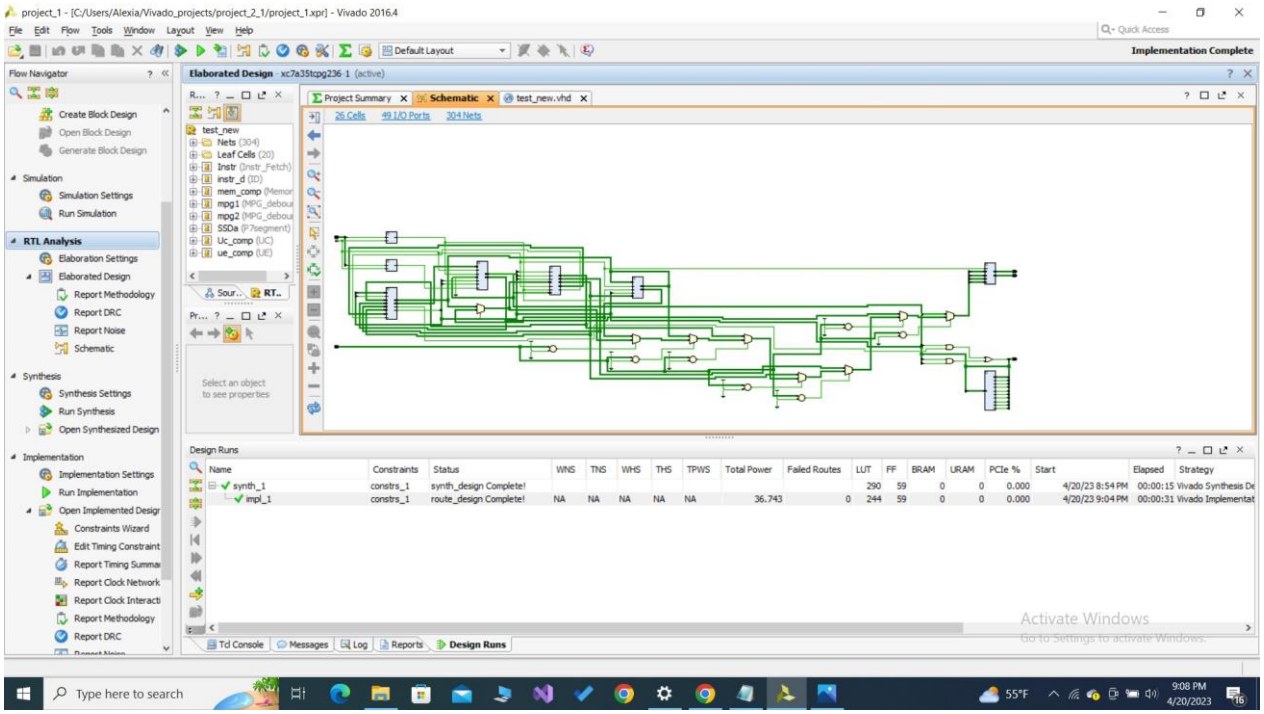
project_1 - [C:/Users/Alexia/Vivado_projects/project_2_1/project_1.xpr] - Vivado 2016.4
File Edit Flow Tools Window Layout View Help
Default Layout
Implementation Complete
Flow Navigator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Elaborated Design - xc7a35tcpg236-1 (active)
Project Summary
Schematic
test_new.vhd
26 Cells
49 I/O Ports
304 Nets
test_new
Nets (304)
Leaf Cells (20)
Instr (Instr_Fetch)
instr_d (ID)
mem_comp (Memor
mpg1 (MPG_debou
mpg2 (MPG_debou
SSDa (P7segment)
Uc_comp (UC)
ue_comp (UE)
Select an object to see properties
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAM
URAM
PCIe %
Start
Elapsed
Strategy
synth_1
constrs_1
synth_design Complete!
0.000
4/20/23 8:54 PM
00:00:15
Vivado Synthesis De
impl_1
constrs_1
route_design Complete!
NA
NA
NA
NA
NA
36.743
0
244
59
0
0
0.000
4/20/23 9:04 PM
00:00:31
Vivado Implementat
Tcl Console
Messages
Log
Reports
Design Runs
Activate Windows
Go to Settings to activate Windows.
Type here to search
55°F
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4/20/2023