Design and Implementation of a FPGA-based Direct Digital Synthesizer

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Abstract: **A method for the design as well as implementation of FPGA-based Direct digital synthesizer (DDS) is firstly presented in this paper. And then corresponding system simulation and experimental results are given. The DDS for generating a sinusoidal signal owns the features of simple circuit, easy to be controlled, stable performance, high frequency conversion speed and fine accuracy etc. And its output frequency falls in the range of 0Hz ~ 160KHz with 5 Hz of steps.**

Keywords-Direct digital synthesizer (DDS); FPGA; pipeline technology; look-up table

I. INTRODUCTION

Frequency synthesis technology is widely used in telecommunications, aerospace, instrumentation and other fields. At present, the commonly used frequency synthesis includes three branches such as direct, phase-locked, and direct digital ones. Thereinto, Direct digital frequency synthesis (DDFS, generally referred to as DDS) is a new frequency synthesis technique through which waveforms are synthesized directly from phase of signals [1]. In recent years, DDS has been widely used in digital communication systems due to its fine frequency resolution, high frequency conversion speed, and continuously variable phase characteristics etc. With the development of microelectronics technology, field programmable gate array (FPGA) devices show a rapid development [2]. And the device shows daily increasing attractions to hardware design engineers and therefore has already been widely used in digital processing for its merits of high run speed, large scale integration and outstanding field-programmable advantages, etc. This paper describes the principle and design of FPGA-based DDS, especially implementations of the DDS technology on a FPGA device platform. For that, the QuartusII software is used for programming and simulation, and finally simulation results from FPGA-based DDS are given.

II. PRINCIPLE OF A DIRECT DIGITAL SYNTHESIZER

Figure 1 shows a basic block diagram of the DDS circuit.

The DDS is generally composed of a reference clock, a phase accumulator, a phase to amplitude conversion unit, a D/A converter and a low pass filter (LPF), etc. On receiving each clock pulse f_{clk}, an addition of frequency control word X to cumulative sum of the phase data, which is output from accumulate register, is implemented on a N-bit adder, and the sum of the results Y is immediately fed into the accumulation register. The newest phase data generated in last clock cycle are on the one hand feedback to the adder by the accumulator register, so that an addition of frequency control data X with the adder's input is implemented in the next clock cycle; the other hand, as a sample address this value is sent into the phase to amplitude conversion circuit, through which corresponding waveform data are output according to the address value. Finally, the waveform data are converted into analog waveforms by the D/A converter and low-pass filter. Linear phase accumulation will continue on the phase accumulator in the role of the reference clock, and an overflow will occur when the cumulative result of the phase accumulator is equal to or greater than 2^N, then it turn back to the initial state, and waveform of a cycle is completed and output. This cycle is a frequency one for synthesizing DDS signal [3].

Changes in output frequency is achieved by changing the frequency control word X, when the control word X changes, the address through which the phase accumulator access RAM will be accordingly changed. If the value of X is small, the accumulator will access each RAM unit, thus sampling points in the lookup table are continuously accessed, and the output frequency is low; when the value of X is larger, the phase accumulator will skip some of the RAM unit, the number of sampling points reduces while the output frequency increases.

The frequency of DDS output signal is as following：

$$f_{out} = \frac{f_{clk}}{2^N} \times X \tag{1}$$

where , f_{out} means output signal , f_{clk} system synchronization clock, N bit length of adder, X frequency control word. As can be seen from the above equation, one can get waveform with any frequency by changing bit length N of phase accumulator, frequency control word X, and synchronization clock f_{clk} .

Frequency resolution of DDS is as following:

$$\Delta f = f_{clk} / 2^N \tag{2}$$

When the reference clock holds constant, frequency resolution is determined just by bit length of the phase accumulator. In fact, waveform output from the D/A converter can be considered as a sampling of a continuous smooth waveform, so

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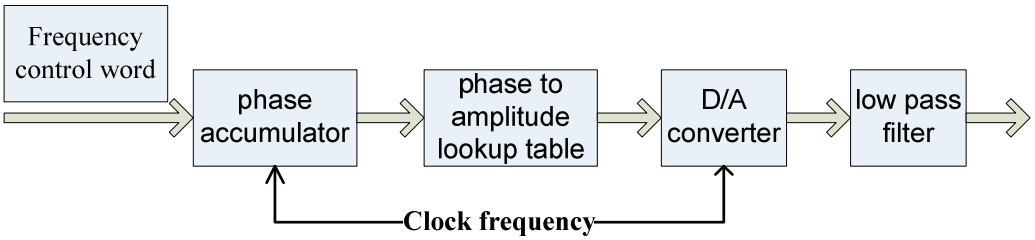

Figure 1. A basic block diagram of the DDS circuit

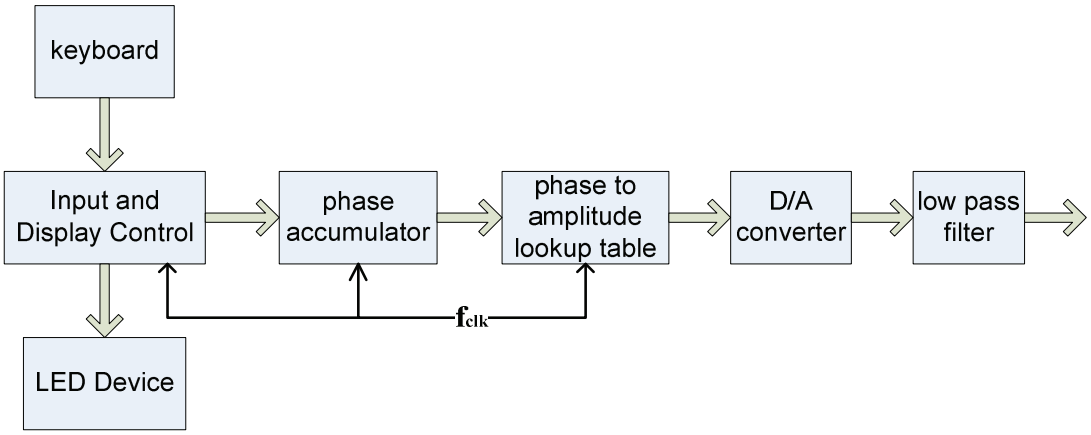

Figure 2. Block diagram of FPGA-based DDS

according to Nyquist law, the sampling rate should be more than twice the signal frequency. That's to say, if you want to fully recover signal from D/A converter's output, then the frequency of output waveform must be less than $f_{clk}/2$, while the actual maximum output frequency of DDS is no more than $0.4 f_{clk}$.

III. DESIGN OF DIRECT DIGITAL SYNTHESIZER SYSTEM

Block diagram of FPGA-based DDS is shown in Figure 2. Quantified waveform data are stored in a ROM region, and an accumulated phase, whose value is recursive accumulation of phase with step X, as address to access the ROM unit. The obtained ROM data are then fed into the D/A converter and low pass filter, the required waveform, whose frequency is determined by clock CLK frequency f_{clk} and step X, is finally generated. The main function of the input and display control module is to convert the frequency of the keyboard input value to corresponding frequency control word, and the frequency value is sent to LED display circuit [4].

The output frequency of DDS falls in the range of 0Hz~160KHz, with steps of 5Hz. Computational results show that, 48MHz of CLK frequency meets the design requirements:

$$f_{out} = 48MHz \cdot 40\% = 19.2MHz \geq 160KHz$$

$$\Delta f = \frac{f_{clk}}{2^N} = \frac{48MHz}{2^{32}} \leq 5Hz$$

Considering that frequency resolution should be equal to or less than the frequency step, and also word length of accumulator is generally in multiples of 8, the word length is finally chosen as N=32, while output width is 8-bit.

IV. DESIGN OF SUB-MODULES IN DDS SYSTEM

A. The design of phase accumulator

Operating speed of the phase accumulator directly affects the highest frequencies of output signal, so the most critical question of the module is how to improve the run speed of phase accumulator. The number of bits of frequency control word is 32, and accordingly that of the phase accumulator is also 32. If an wider bit adder is used directly to form the phase accumulator, the delay generated by the adder will leads to reduced accumulator speed. To improve the working speed of the accumulator, a pipeline design method has been adopted here [5]. Figure 3 is the diagram of a 32-bit phase accumulator with four level pipelined structures. In this module, 32-bit cumulative data are split into four bytes, and each of which is fed into a pipeline level respectively. The accumulator is composed of an 8-bit data latch, an 8-bit full adder, a 1-bit data latch. And it bears the phase accumulation function of adding the data output from a 32-bit accumulator register to a 32-bit input control word. Let the control word *a* be 7, then the simulation results of a 32-bit phase accumulator is shown in Figure 4.

B. Design of Phase to Amplitude lookup table

Phase to Amplitude lookup table is actually a ROM region where stored encoded point array obtained by sampling a sinusoidal signal. This table is in fact a map of a phase sequence to a sampled sinusoidal signal, thereinto, the output

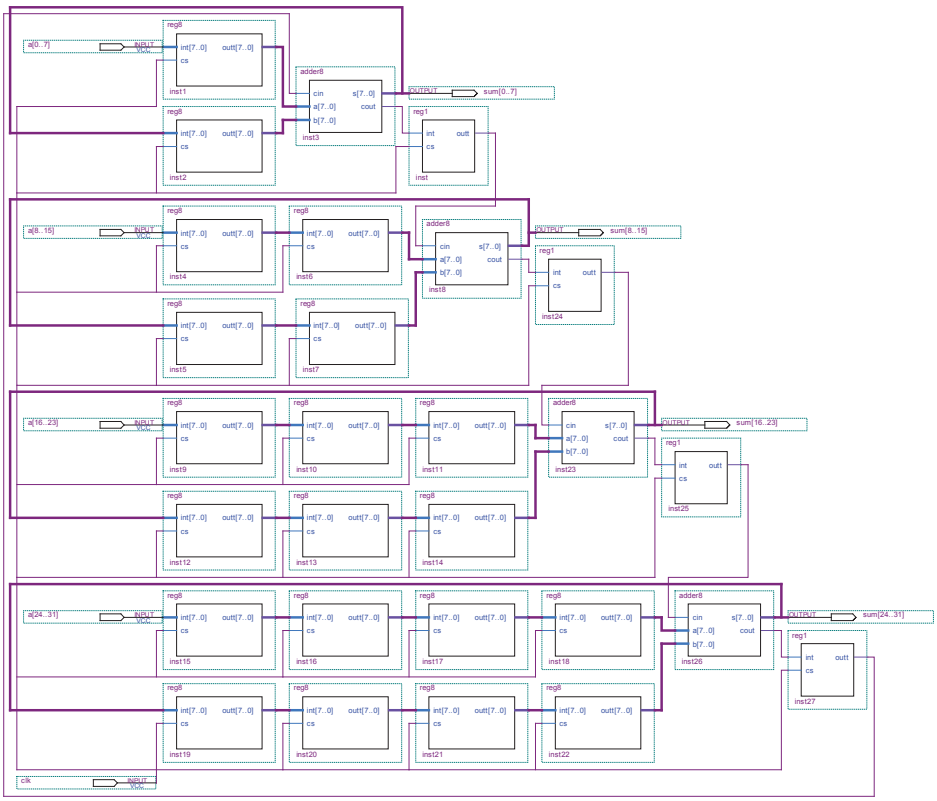

Figure 3. Diagram of a 32-bit phase accumulator with four level pipelined structure

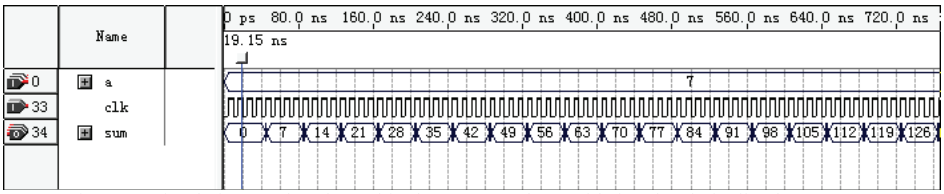

Figure 4. Simulation results of a 32-bit phase accumulator with four level pipelined structure

of phase accumulator as the address for accessing corresponding ROM unit. In this case, the accuracy of output signal frequency resolution is determined by the number of bits N of phase accumulator, and the accuracy of the phase resolution is determined by ROM address width.

In most Waveform Generator products, waveform data are stored in external ROM, which makes a clear system structure, convenient testing and maintenance service. But due to its low access speed the ROM itself possesses, both the overall system performance and operating frequency decreases. To solve this problem, a FPGA-based ROM for waveform data is designed. The Mega Wizard Plug-In Manager, whose settings interface is shown as Figure 5, in Quartus II is used to design a ROM.

The highest 8 bits of output waveform of the phase accumulator are as address lines for accessing waveform memory, and corresponding binary sine amplitude is output, its amplitude falls in the range of 00000000-11111111. Finally, the binary sinusoidal data are used to achieve implementation of a sine ROM based on VHDL programming.

C. Design of Input and Display Control Module

The sub-module is composed of a keyboard input module, a frequency to frequency control word converter, and a display module. Thereinto, the first module includes a frequency divider, a keyboard scanning circuit, and a keyboard jitter eliminating unit; and according to the frequency to frequency control word look-up table in the second module, the keyboard input is converted into an appropriate frequency control word and sent to DDS phase accumulator; finally, the value of output frequency is translated into a seven-segment code and decoded by a LED device.

V. SIMULATION WAVEFORMS AND EXPERIMENTAL RESULTS

The above mentioned modules and the whole system are all designed by using VHDL. Figure 6 demonstrates the simulation waveforms of DDS main module when frequency of output signal is 10KHZ. The system discribed by using VHDL is compiled in Quartus Ⅱ,which is a set of

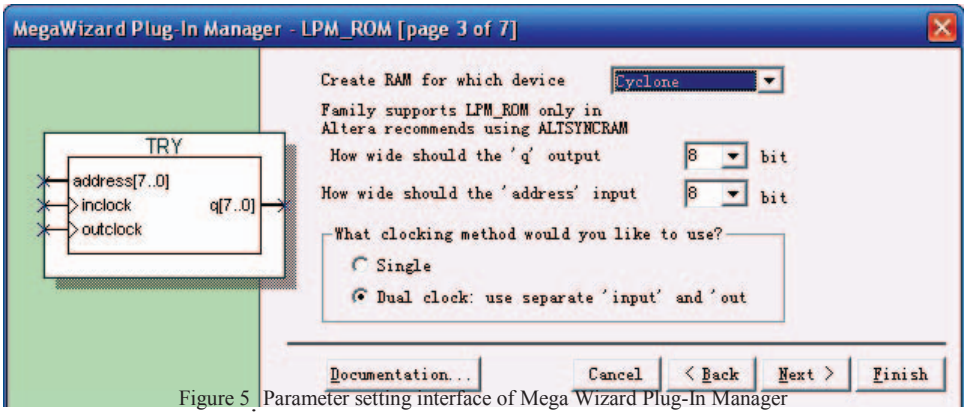

Figure 5. Parameter setting interface of Mega Wizard Plug-In Manager

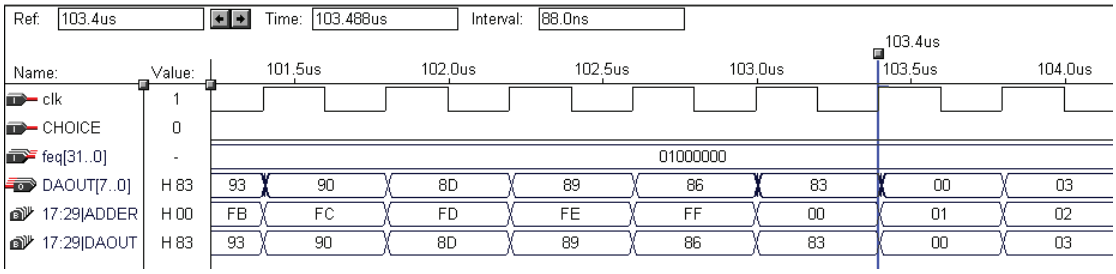

Figure 6. Simulation waveforms of DDS main module when frequency of output signal is 10KHZ

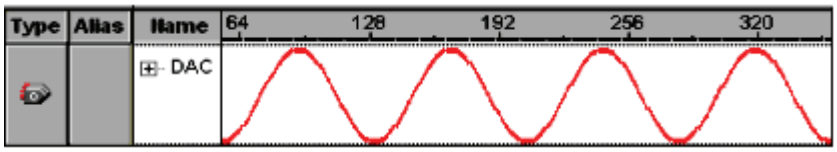

Figure 7. Output signal waveform observed on embedded logic analyzer

development tools for FPGA-based system, and then downloaded into a FPGA development board for constructing a target running environment. Figure 7 shows the output signal waveform observed on embedded logic analyzer Signal Tap Ⅱ in Quartus Ⅱ.

VI. CONCLUSIONS

In this paper, a DDS design and implementation method based on EDA technology is proposed. The system runs on a FPGA chip with the support of necessary peripheral circuit units and user interface devices. Output frequency falls in the range of 0Hz ~ 160KHz with steps of 5 Hz. The system for generating a sinusoidal signal owns the features of simple circuit, easy to be controlled, stable performance, high frequency conversion speed and fine accuracy etc.

REFERENCES

[1] Jue-sheng Zhang, Lina Cao, "PLL frequency synthesis" [M], Chengdu: University of Electronic Science and Technology Press, 1995.

[2] Song Pan, Ji-ye Huang, "EDA technology and VHDL" [M], Tsinghua University Press, 2007.

[3] Yan-an Deng, "FPGA-based digital synthesized signal generator" [D], Hefei University of Technology, 2007.

[4] Ping Jiang, Jian-xin Wang, Xun-sheng Ji, "A Direct Digital Frequency Synthesizer Implemented with FPGA" [J], Electronics Engineer, 28 (5), 2002.

[5] Xu Li, "Research on applications of FPGA-based pipeline technology"[J], Electronic Measurement Technology,30 (2), 2007.