A Hardware-Accelerated Qubit Control System for Quantum Information Processing

Nizar Messaoudi*, Clayton Crocker *, Marc Almendros *
Keysight Technologies
Email: nizar.messaoudi@keysight.com

***Abstract*—In this paper we present a flexible, high-performance, integrated qubit control system using modular PXIe equipment. To manipulate qubits, a classical control system is required to generate and acquire a mix of baseband, radio frequency, and/or optical signals, with the specific mix different for each qubit technology. Typically, a quantum system requires many of these signals with a high degree of synchronization and phase coherence, and increasingly needs real-time data processing and on-the-fly sequencing capabilities for feedback experiments. The proposed system is scalable to hundreds of channels, all of them being phase coherent and fully time-synchronized.**

The system includes a programmable real-time sequencer for precise execution timing and decision making; and open FPGA capabilities for custom Digital Signal Processing (DSP) by hardware. Using the latter, we present FPGA IP to generate one-/two-qubit gates efficiently with the AWG, and to analyze high-frequency signals to measure the qubit states in real time on the digitizers. This IP features very low latencies for Quantum Error Correction (QEC) and Frequency Division Multiplexing (FDM) capabilities, among others.

I. Introduction

Quantum computers require classical electronics to manipulate and read out their quantum state [1]. The challenge with these operations is that qubits are sensitive to external perturbations. This requires the classical control system have low-noise, high accuracy signal generation, and receiving capabilities [2]. While standard lab-grade equipment can produce the necessary signal quality to obtain high gate fidelities, it has several limitations that restrict this being a viable approach for the Noisy Intermediate-Scale Quantum (NISQ) computing [3] that are emerging today.

The traditional approach of using test and measurement equipment is bulky and expensive. Furthermore, while these instruments can be coordinated using an external trigger generator, external triggering can cause increased system jitter and does not allow for a dynamic sequencing without the use of switches or hardware duplication to handle sequence branching [4], [5]. Finally, test and measurement equipment typically does not support custom real-time DSP required to quickly process qubit states. This is critical for scaling the size of Quantum Information Processors (QIP), as Quantum Error Correction (QEC) [6] requires the system to complete a measurement and take a decision in a time-span several orders of magnitude below the qubit's coherence time. Currently, several superconducting qubits have demonstrated coherence times on the order of hundreds of micro-seconds. Thus, for a control system to successfully implement QEC, it must be able to implement feedback/feedforward operations in under 1 μs.

Field Programmable Gate Arrays (FPGA) offer an excellent platform for implementing the DSP required for qubit control and measurement as they interface easily with Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC), excel in parallel data processing and provide a fixed latency, unlike Central Processing Units (CPU) or Graphical Processing Units (GPU). While the use of FPGAs to control and readout qubits is not novel, the efforts in this area have been restricted to either custom solutions for small experiments [4], [5], or specialized systems that can only address one qubit platform [7].

This paper presents one approach to solve these challenges through an off-the-shelf, control system available commercially. The solution is comprised of several PXIe modules:

- A 14 bit 1 Gsample/s Arbitrary Waveform Generator (AWG)
- A 14 bit 500 Msample/s digitizer
- A 20 GHz DDS based dual Local Oscillator (LO)

The AWG and digitizer modules are equipped with an FPGA, featuring a re-configurable sandbox, allowing the user to insert custom DSP into the module, all while protecting the core functionality of the instrument. Moreover, each module has a programmable sequencer that leverages the time determinism of FPGAs to ensure that instructions are executed precisely with nano-second precision.

The control system leverages the modular platform of PXIe, allowing it to expand with the number of qubits by simply adding more AWG and digitizer modules. PXIe provides a high-speed PCIe back-plane for transferring data between the modules and the control computer, allowing for fast upload of waveform data and transfer of experimental results. The PXIe chassis also provides clock and trigger distribution, eliminating the need for these signals to be routed externally and hard-wired between different instruments. A single chassis can accommodate the modules required to control more than 20 qubits, and up to six chassis can be linked together allowing for control of 120 qubits, which is larger than any gate-based quantum computer available today. While previous approaches have relied on a central processing unit to process measure-

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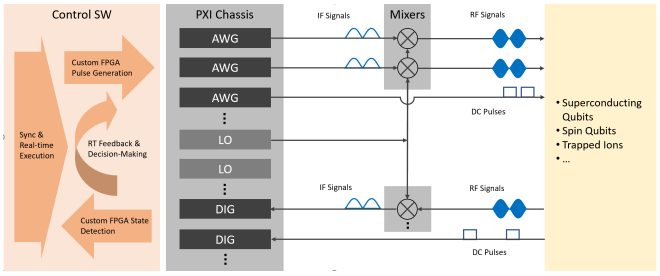

Fig. 1. A high level block diagram of the proposed qubit control solution showing the the component modules and capabilities

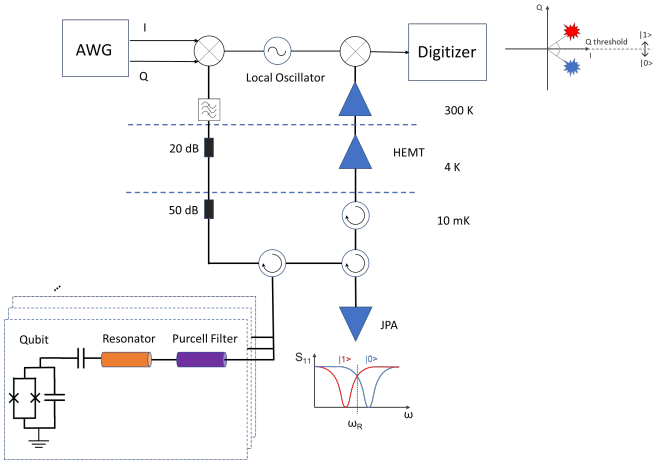

Fig. 2. A simplified schematic of a multi-qubit readout used in superconducting qubits. The readout signal is generated by the AWG and upconverted to the resonator frequency before being sent down the cryostat. The reflected signal, S11, is amplified by a Josephson Parametric Amplifier (JPA) and cryogenic High Electron Mobility Transistor (HEMT) amplifier. The signal is then downconverted to an IF, typically with the same LO, and sampled with a digitizer.

ment results and distribute actions, the proposed architecture uses a distributed processing model, where each module runs its own individual sequence. This will be explored in further detail in section IV. A high level block diagram of the control system is shown in Fig. 1. While this paper focuses on superconducting and spin qubits, for optical based platforms, the RF up-converters could be replaced by Acousto Optic Modulators (AOM) to up-convert AWG outputs to optical frequencies. Similarly, Photo-Multiplier Tubes (PMTs) can be used to convert photons to base-band "clicks" that can be acquired by the digitizer.

II. Real-Time Qubit State Detection

Superconducting [8] and more recently spin qubits [9], [10] use circuit quantum electrodynamics (QED) for qubit read out, where the qubit is dispersively coupled to a microwave resonator. A microwave pulse can be used to probe the readout resonator, producing an amplitude and phase shift that depend on the qubit state. Due to the limited cooling power available in the cryogenic environments necessary to operate both of these qubit platforms, multiplexed readout using FDM has become a popular method to limit the number of microwave lines necessary to operate a quantum processor [11].The architecture of the readout circuitry in Fig. 2 closely resembles that of superheterodyne transceivers used for modern communications, allowing for the Intermediate Frequency (IF) stages to be handled digitally.

The digitizer modules presented here operate with a 100 MHz FPGA clock rate, with data enters the sandbox in 5 parallel samples. While the modules have an open FPGA architecture, allowing users the option to design their own custom DSP, to minimize programming complexity, the proposed solution also provides a quantum specific IP library, including a set of heterodyne qubit state detection IP blocks. These blocks consist of a Numerically Controlled Oscillator (NCO), multiplier, downsampling filter, and qubit state detector as shown in Fig 3. These blocks have been optimized to minimize computational resources, requiring less than two percent of the total resources available in the sandbox of the FPGA. Furthermore, the use of these specialized blocks only adds three clock cycles (30 ns) of additional latency to decode the qubit state.

The NCO generates a sine and cosine at a specified frequency; this same NCO is also used to digitally up convert the read out signal in the AWG (see section III), ensuring phase coherence between the transmitted and received IF signals and eliminating the need for symbol clock recovery. The incoming data is then multiplied with the NCO outputs to digitally downconvert it to baseband. As with FDM in wireless communications, special attention must be payed to the filtering to maximize the Signal to Noise Ratio (SNR). Matched filter theory [12] tells us that the optimal filter to maximize the SNR at the receiver is the one used by the transmitter. In the case of cQED, this is a convolution of the read out pulse, the read-out resonator and Purcell filter response. Since the optimal filter response is heavily dependant on the quantum processor, the downsampler can be loaded with arbitrary coefficients allowing for a fully customized integration window from 20 ns to 20 μs long with 10 ns granularity. Since the solution provides a simple graphical user interface to re-configure the FPGA sandbox, these blocks can be easily replicated to account for FDM. The NCO frequency, filter coefficients and thresholds for the qubit state decoder can be uploaded to the downsampler using a python API.

III. Custom Pulse Generation for Qubit Control

For superconducting [13] and spin qubit platforms [14], qubits can be controlled primarily using RF pulses in the 4-10 GHz range. A common method for producing the resonant and near-resonant signals needed to control solid state qubits is to generate baseband or intermediate IF pulses from an AWG, then to up-convert these signals by mixing them with the output of a microwave LO as shown in Fig. 4. Using an IF IQ generation allows for the image to be rejected naturally through the mixer allowing for the use of lower bandwidth AWGs and removing the need for specialized analog filters.

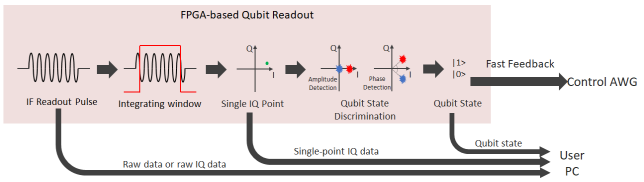

Fig. 3. An overview of the DSP used to analyze the qubit state. The read out pulse will be down converted with a digital oscillator and filtered using an integration window. At the end of the integration process, a single point on the IQ plane is obtained. This result can then be compared to thresholds in the IQ plane to discriminate the state of the qubit. This result is all that needs to be communicated to the qubit control AWG to achieve the desired result.

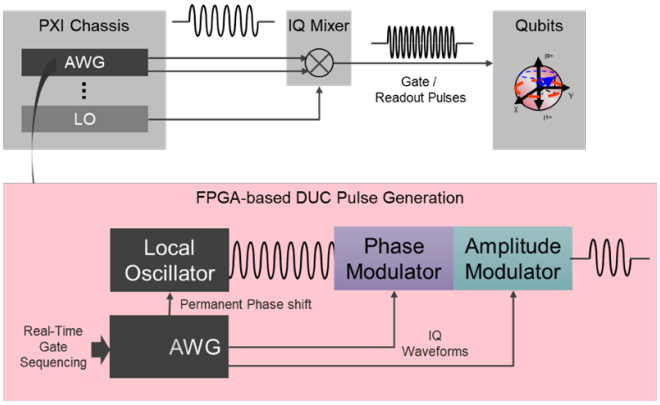

Fig. 4. An example of a Digital UpConversion (DUC) engine used in modern instrumentation for solid-state qubit control. This implementation takes advantage of a real-time sequencer to dynamically sequence and trigger waveforms.

Since qubit control is typically done in a rotating frame, generating the qubit drive at IF comes at a cost, requiring the phase of individual pulses to be managed. The issue of pulse phase management requires one of following:

- Resetting the phase of the LO to ensure pulses are phase coherent
- Restricting pulse generation to multiples of the IF's period
- Pre-calculating all of the waveforms for the sequence and playing them out like a tape recorder
- Using an NCO on the AWG to track phase

Given that typical superconducting gates are around 20 ns long and the need for multiple locked LOs when manipulating multiple qubits, the first of these options is not feasible. Furthermore, the precise waveform envelopes needed to ensure high gate fidelity makes the second option highly undesirable. Moreover, as the amount of dynamic branching for algorithms will increase over time, the third approach will be faced with severe scaling penalties. So now we discuss the remaining option: using NCOs.

The use of NCOs provides many advantages in generating pulses for quantum control [15]. First, the NCO does not consume any DDR memory in the AWG, greatly reducing the number of waveforms that need to be calculated and stored. If clock distribution is well managed across the control system (as it is in a PXIe chassis), these NCOs will be fully phase coherent across the entire control system. Thus, the use of digital oscillators is the best approach to ensure phase coherence.

Furthermore, the phase of the NCO can be shifted to perform Z-rotations, shifting the phase of all subsequent pulses. Traditionally, this phase shift has been achieved by applying a baseband pulse to a flux-bias line in superconducting qubits [16], by modulating the local magnetic field of a quantum dot [17], or by inducing a stark shift using an off-resonant driving field [18]. The method used in the proposed system is to implement a virtual Z (VZ) rotation by shifting the phase of the classical oscillator used to control the qubits [19]. Because it is virtually error-free, this approach represents a compelling approach for implementing Z gates and presents a compelling argument for the use of NCOs.

While some modern AWGs do have some digital up-conversion capability, these typically do not offer real-time phase control of the NCO. Additionally, most are restricted to some finite number of NCO's and may not offer the ability to change these dynamically throughout the sequence. Furthermore, for FDM applications, traditional AWGs require data for all of the carriers to be encoded in a single waveform, since they only have one AWG engine per channel, fetching waveforms associated with the NCOs.

In the proposed solution, the NCO for each channel exists in the FPGA sandbox and can be replicated many times. Additionally, we have also implemented a Block RAM based AWG engine as part of our quantum IP library, which can be instantiated multiple times per physical channel. This novel AWG is designed to support fast dynamic queuing of the very short waveforms required for conditional branching. This is explored in greater detail in the following section. The light AWG can accommodate up to 128 individual waveforms of up to 400 μs of waveform length. As discussed previously, the gates used to control superconducting qubits and spin qubits are usually tens of ns long, so this is more than sufficient to address the needs of these qubits. Furthermore, for qubit platforms that require longer waveforms, the light AWG also has a pre-scaler, capable of stretching out each waveform point by multiples of 5, allowing for individual waveforms to extend to hundreds of μs.

IV. Sequencing and Dynamic Flow Control

Modern AWGs are equipped with powerful sequencing capabilities that can handle pre-determined waveforms, allowing for simplified waveform creation and more efficient memory utilization. This divides the AWG memory into waveform segments that can be queued to form a sequence. This sequencer is usually a basic state machine that is running on the instrument's FPGA under the hood, allowing the user some real-time control of the instrument. Often, the sequencing capabilities will include simple flow control such as:

- Looping of segments and sequences

- Waiting, either for a fixed amount of time or for an external event, such as a trigger

This functionality is usually enough to address the signal generation requirements for basic experiments that are used to characterize a qubit's performance (e.g. Rabi, Ramsey, energy relaxation, etc.)
Some AWG's are even able to handle dynamic triggering from a digital input, allowing the waveform to be selected dynamically [15] [20]. While this approach is viable for small QIP, it suffers severe scaling penalties as the number of qubits increases.
Our solution proposes the use of a distributed architecture that enables users to program one or multiple instruments to execute time-deterministic sequences of operations and execute them with precise synchronization. This real-time sequencer achieves this by deploying an executable code into each module's FPGA to be executed by the sequence engine integrated into the instrument. The code executes on these engines in parallel, across multiple instruments. The user-defined hardware operation of the group of instruments is called a Hard Virtual Instrument (HVI). The sequences of operations or instructions executed by the HVI engines are called HVI sequences.
HVI technology supports, transforms, and enhances individual instruments by enabling them to execute real-time sequences and precisely synchronize with other instruments. An HVI instance (or implementation) executes one or more HVI sequences associated with one or more instruments. The instruments are synchronized to a common digital clock reference .

HVI engines control each instrument with:

- Clock signals
- Triggers
- Actions
- Events
- Product-specific instructions

As shown in Fig. 5, this means that the HVI engine has access to the PXIe backplane triggers and clocks within the chassis. Upon startup, HVI calibrates and de-skews the backplane signal automatically, meaning users do not have to preform complex trigger calibration required with complex trigger fan-outs. HVI can also communicate with the FPGA sandbox of the instrument allowing the sequencer to access final measurement results. This allows for conditional branching directly within the instrument, without having to communicate with the PC. Each HVI engine is also equipped with sixteen 32 bit registers, that can be used to parameterize sequences and for loop counting. Registers can also be shared between modules to broadcast measurement results between modules across the system.

HVI sequences are composed of an ordered list of HVI statements with associated timing information. A sequence is executed in a time-deterministic manner by the HVI hardware engine located within an instrument. An HVI application is

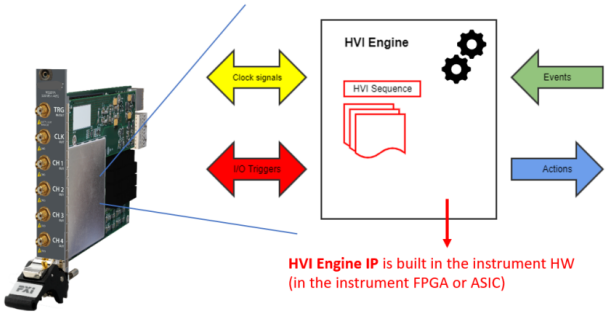

Fig. 5. An example of an HVI engine running in a PXIe module.

composed of one or more sequences that run in parallel and synchronously. HVI sequences can be global (i.e. running in parallel across all instruments), or local (i.e. running on a single instrument's engine).
Global sequences can consist of synchronous while loops, synchronous if-else branching, and synchronous register sharing. This allows for dynamic sequencing such that a readout result on a digitizer can be used to determine pulse selection on an AWG, enabling applications such as fast qubit reset, and QEC under $1s$. For simple feedback loops, as shown in Fig. 6 where the decision logic in the digitizer is minimized, the feedback time of the system is 360 ns. This is comprised of:

- The time from the digitizer input to the digitizer FPGA sandbox (200 ns)
- Decision time in the digitizer FPGA (30 ns)
- Sending a selection word to the AWG (20 ns)
- Triggering the agile AWG (20 ns)
- The time from the AWG FPGA to the AWG SMA (90)

This time is dominated by the interface time between the data-converters and the FPGA on the individual modules.

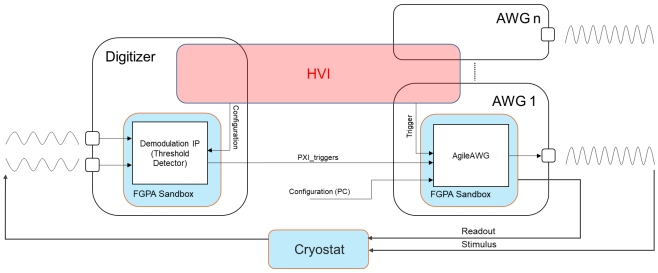

Fig. 6. A feedback loop example

V. Discussion and Future Work

While the system can scale to hundreds of physical channels in multiple chassis, the main limitation for scaling the system is the number of PCIe peripherals that can be enumerated by a single host computer. As the PCIe standard continues to evolve, the possibility of implementing a Flattening Portal Bridge (FPB) to exceed the current limitation of six chassis may be possible. Alternately, we may also enable multi-host capabilities in HVI to allow for multiple control PCs to be

used to co-ordinate large experiments. Another limiting factor is the FPGA clock speed on the modules. Currently, the AWG and digitizer's modules run at 200 and 100 MHz, respectively. However, the latest generation of FPGAs can easily support clock speeds of 300MHz, allowing for the DSP logic to run up to three times faster. Finally, data converters have advanced significantly in the last few years, supported by the need for massive MIMO systems for FR-1 deployments of 5G. Thes new products would allow for direct digital signal generation and acquisition up to 6 GHz, eliminating the need for additional IQ upconversion.

VI. Conclusion

In this paper, we presented a room-temperature Quantum Computing control system that is composed of standard, PXIe AWGs and digitizers. The control system is qubit agnostic, allowing experimenters to explore a variety of qubit technologies, including hybrid quantum systems. We explored some examples of how the open FPGA technology integrated in each module allows researchers to integrate the custom DSP required in quantum engineering research. We also discussed how the platform allows for inter-modular synchronization, without the need for external triggers, clock distribution, allowing for dynamic trigger distribution. This dynamic triggering capability allows the system to be used for active qubit reset and QEC.

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