Jeonghyun Park

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SUMMARY

FPGA/Hardware design developer with 3 years experience building full-stack RFSoC-based quantum computer control system. Delivered 1 GSPS DDR4 SDRAM based AWG, 3.2 GB/s multi-threaded flow controlled DMA IP, and these were validated in trapped-ion experiments. Skilled in SystemVerilog, DDR4, mixed-signal PCB and SI analysis.

EDUCATION

Seoul National University Mar 2018 - Aug 2024

- Bachelor, Electrical and Computer Engineering (Major) Summa Cum Laude, Total GPA 3.77/4.0
- Bachelor, Physics (Double Major)

Gwangju Science High School for the Gifted Mar 2015 - Feb 2018

WORK EXPERIENCE

Research Assistant

Quantum Information and Quantum Computing Lab, Seoul National University Mar 2023 - Apr 2025

- Designed and implemented a Xilinx RFSoC-based full-stack quantum computing control system, including a custom PCB, RTL design and firmware. Moreover, automated various tasks with scripting language.
- Developed peripheral electronic devices or programs, and participated in trapped-ion two-qubit gate experiments to verify the custom RFSoC-based control system.

Service Social Service Agent (Alternative Military Service)

Elderly Care Center, Dongtan Feb 2022 - Mar 2023

- Assisted elderly residents in daily activities.

Senior Airman, Computer Technician (Mandatory Military Service)

Republic of Korea Air Force, Suwon Feb 2021 - Oct 2021

- Responsible for server administration and security.

Research Assistant

Quantum Information and Quantum Computing Lab, Seoul National University Feb 2020 - Jan 2021

- Researched state-of-the-art QC control digital architecture, and designed custom RTL design for electronic device test.

PUBLICATIONS

- “INQC: Integrated Trapped-Ion Quantum Computer Controller”, *In Prep.*, 2025, First Author
- “A silicon-based ion trap chip protected from semiconductor charging”, *Quantum Sci. Technol.,* 2025, Co-author
- "Radio-Frequency Pseudo-Null Induced by Light in an Ion Trap", *arXiv preprint* arXiv:2504.13699, Apr. 2025, Co-author
- “Efficient quantum frequency conversion of ultra-violet single photons from a trapped ytterbium ion”, *Appl. Phys. Lett.,* vol. 126, no. 8, Art. no. 084001, 2025, Co-author

PROJECTS

Full-stack RFSoC-based Integrated TIQC Control Electronic System (Details) Mar 2023 - Apr 2025

Overall RTL Design

- Developed integrated real-time SoC controller (Xilinx RFSoC, ZCU111) which have conducted actual experiments successfully.
- Automated generating fully-connected block diagram and assigning AXI address configured by JSON metadata, which significantly reduced reconfiguration time and made the system much flexible. (Details)

Firmware Development (FPGA) & Control Server Development (PC)

- Removed stall from queue saturation between the PL and PS an interrupt-driven flow control algorithm achieving 160MBps.
- Developed a TCP server that manages C/C++ codes, transfers the compiled binary to an FPGA which executes or halt binary via an custom loader and GICv2.
- Developed a remote procedure call between the main server and the FPGA to control external peripheral devices.

DDR4 SDRAM based Ceaseless Multi-channel True-arb 1GSPS AWG IP

- Performed analytical analysis of DRAM refresh overhead, read latency, and optimal buffer size of AWG which fits with measured value within 5 %.
- Developed an AWG IP achieving WCET latencies of 900 ns, and 2.16 us with one and eight channels respectively. Double buffering, and row-aligned memory allocation are utilized.

Multi-threaded Flow Control Capable DMA IP

- Developed a DMA IP, which prevents stalling due to a queue saturation of IP. 3.2 GBps throughput is verified in real hardware. Optimal queue depth of the IP is found through Monte Carlo simulation written in CUDA.

2GSPS DDS IP

- Developed a Vedic-based MAC for 48-bit multiplication, and a 5 stage pipelined harmonic signal generation.

PCB Design/Electronic Circuit Design Mar 2023 - Apr 2025

RF Frontend Board (Details)

- Developed a mixed-signal 8-layer PCB with Cadence OrCAD achieving -27 dB RF reflection, 100dB analog-digital isolation.
- A stripline-SMA transition was simulated to optimize connector hole size through ANSYS HFSS improving the reflection by 10 dB.

High Speed FMC Router (Details)

- Developed a FMC VITA57.1/57.4 to router with Cadence OrCAD. Signal integrity is verified in 1 GHz. It is utilized in Camera Link frame grabber and digital I/O for photon count or RF switch control.

Bidirectional LVDS to TTL (Details)

- Developed a bidirectional LVDS-TTL converter board with Cadence OrCAD.

Low Noise DAC System (Details) Nov 2024 - Apr 2025

- Led development of a custom, fully-shielded, low-noise DAC system that avoids ground loops considering EMC, while mentoring a junior teammate.
- Developed a DAC PCB (TI DAC81416). Signal integrity between FPGA and DAC board of 50 MHz digital communication on 3 m shielded cable is verified with exported S-parameter from cable via, IBIS and ANSYS EDT.

RF Generator Control System Feb 2020 – Jan 2021

- Developed a QSPI IP to control a direct digital synthesis board (AD9910) in real time through a Digilent Arty S7.

Image Display/Frame Grabber on MPSoC (ZCU104) (Details) Feb 2024 - Jun 2024

- Developed a custom double buffer based 60FPS DVI IP leveraging a GTH transceiver.

- Developed a custom real time 60FPS Camera Link frame grabber IP using 7:1 SERDES and DDR4 SDRAM.

SKILLS

Programming Languages: Verilog/SystemVerilog | ARMv8 Assembly | TCL | C/C++ | Python | Java | MATLAB

Tools: Xilinx Vivado/Vitis | LTSpice | Autodesk Inventor | ANSYS SIwave/HFSS/EDT | Cadence OrCAD

Measurement Equipment: Rigol MSO7054 Mixed Signal Oscilloscope | Keysight FieldFox N9917A Spectrum Analyzer

Communication Protocols: HDMI | DVI | Camera Link | UART | RS232 | SPI | AMBA AXI4

SCHOLARSHIP

Presidential Science Scholarship, Korea Student Aid Foundation(KOSAF) Mar 2018 - Aug 2024

- Selected as one of 147 STEM undergraduates nationwide (top 0.1 %). Covered full tuition with a living allowance, for a cumulative award of CAD $44,000.

AWARDS

Awarded Gold Medal at the 37th University Mathematics Competition (Second Category) Nov 2018

South Korean National Team Candidate, for 48th International Physics Olympiad (Top12) Jan 2017

LANGUAGE

IELTS Academic 6.5 May 2025