Jeonghyun Park

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Portfolio : https://alexist2623.github.io/index.html

SUMMARY

FPGA/RFSoC research assistant with 3 years of hands-on experience building nanosecond-level quantum-control hardware. Delivered a 1 GSPS DDR4 SDRAM-based true-arbitrary AWG IP that expanded pulse-sequence depth by 1,000-fold; 3.2 GB/s multi-threaded, flow controlled AXI DMA IP; a bare-metal embedded system; and mixed-signal, high-speed PCB designs validated through ANSYS RF/SI simulations.

EDUCATION

Seoul National University Mar 2018 - Aug 2024

- B.S. in Electrical and Computer Engineering (Major) Summa Cum Laude, GPA 3.77/4.0
- B.S. in Physics (Double Major)

PROFESSIONAL EXPERIENCE

Research Assistant

Quantum Information and Quantum Computing Lab, Seoul National University Mar 2023 - Apr 2025

- Led development of Xilinx RFSoC based real-time quantum computer controller from scratch that increased pulse-sequence depth by 1,000 times and integrated eight external RF chips to a single chip. (Details)
- Designed a double-buffered DDR4 SDRAM-based true-arb 1 GSPS AWG microarchitecture with row-aligned DRAM allocation, achieving deterministic worst-case latencies of 900 ns (1ch) and 2.16 us (8ch).
- Modeled DDR4 latency as a function of AWG buffer size, which achieved accuracy within 5 % of measured values.
- Removed AXI4 stall between the PL and PS by inventing an interrupt-driven flow-control scheme, which achieved 160 MB/s.
- Removed AXI4 stall between the DRAM and PL by developing a multi-threaded microarchitecture of AXI4 DMA IP (rate-based flow-control) that achieved 3.2 GB/s.
- Developed multi-processor (three ARM Cortex A53) bare-metal firmware (LWIP server, binary loader, and monitor) which ran continuously for months.
- PCB Designs (Cadence OrCAD)
  - Achieved -27 dB RF reflection, 100 dB A/D isolation of a mixed-signal 8-layer PCB. Improved the reflection by 10 dB via optimizing a stripline-SMA transition through ANSYS HFSS. (Details)
  - Verified 1 GHz signal integrity of FMC VITA57.1/57.4 router via ANSYS SIWave. It is deployed in Camera Link frame grabber, photon count and RF switch control. (Details)
  - Verified 50 MHz signal integrity of 3m shielded cable between FPGA and DAC through IBIS and ANSYS EDT. Designed EMC-cosidered, low-noise DAC sub-system (TI DAC81416). (Details)
- Mentored a junior engineer on EMC-aware layout and grounding.
- Automated Vivado IP integration (block diagram generation and AXI address assignment) cutting setup time from hours to 5 minutes.

Mandatory Military Service

Republic of Korea Air Force & Elderly Care Center, Korea Feb 2021 - Feb 2023

- Responsible for server administration and security elderly residents assist in daily activities.

Research Assistant

Quantum Information and Quantum Computing Lab, Seoul National University Feb 2020 - Jan 2021

- Tested an AD9910 EVB custom with Arty S7 through custom QSPI RTL design.

PROJECTS

Image Display/Frame Grabber on MPSoC (Capstone) (Details) Feb 2024 - Jun 2024

- Developed a custom double buffer-based 60FPS DVI IP leveraging a GTH transceiver.
- Developed a custom real time 60FPS Camera Link frame grabber IP using 7:1 SERDES and DDR4 SDRAM.

PUBLICATIONS

- "INQC: Integrated Trapped-Ion Quantum Computer Controller", *In preparation*, 2025, First Author
- "A silicon-based ion trap chip protected from semiconductor charging", *Quantum Sci. Technol.,* 2025, Co-author
- "Radio-Frequency Pseudo-Null Induced by Light in an Ion Trap", *arXiv preprint* arXiv:2504.13699, Apr. 2025, Co-author
- "Efficient quantum frequency conversion of ultra-violet single photons from a trapped ytterbium ion", *Appl. Phys. Lett.,* vol. 126, no. 8, Art. no. 084001, 2025, Co-author

SKILLS

Programming Languages: Verilog/SystemVerilog | C/C++ | ARMv8 Assembly | Python | TCL | MATLAB
Tools: Xilinx Vivado/Vitis | ANSYS SIwave/HFSS/EDT | Cadence OrCAD | LTSpice | Autodesk Inventor
Measurement Equipment: Rigol MSO7054 Mixed Signal Oscilloscope | Keysight FieldFox N9917A Spectrum Analyzer
Communication Protocols: AMBA AXI4 | Camera Link | HDMI | DVI | UART | RS232 | SPI
Techniques: CDC | SI Validation

SCHOLARSHIP

Presidential Science Scholarship, Korea Student Aid Foundation(KOSAF) Mar 2018 - Aug 2024

- Selected as one of 147 STEM undergraduates nationwide (top 0.1%) with a cumulative award of CAD $44,000.

AWARDS

Awarded Gold Medal at the 37th University Mathematics Competition (Second Category) Nov 2018
South Korean National Team Candidate, for 48th International Physics Olympiad (Top12) Jan 2017

LANGUAGE

IELTS Academic Overall Band 6.5 May 2025