CPU FSM Diagram
CS141 Lab 4 - CPU
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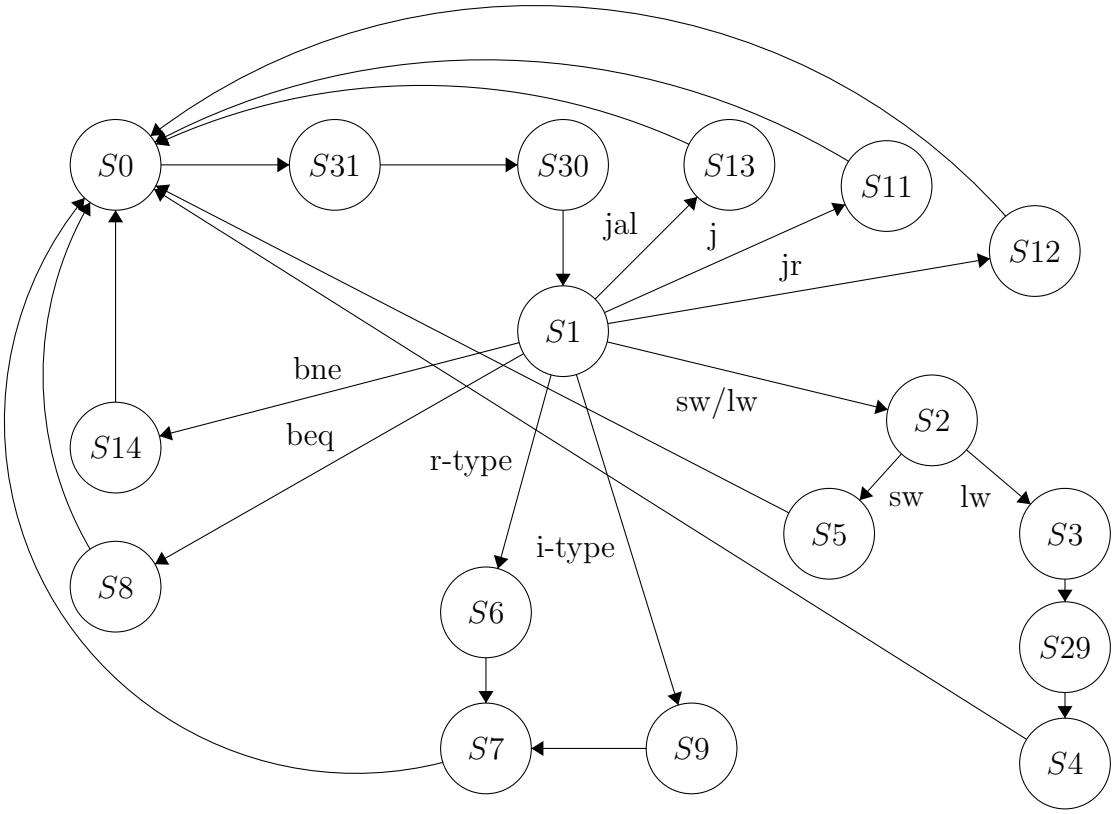


Control

S0: FETCH
pc_write
ir_write
aluSrcA = 0
aluSrcB = 01
aluOp = 000
pcSrc = 00

S1: DECODE
aluSrcA = 0
aluSrcB = 11
aluOp = 000

S2: MEMADDR
aluSrcA = 1
aluSrcB = 10
aluOp = 000

S3: MEMREAD
IorD = 1

S4: MEM_WRITEBACK
regDst = 00
memToReg = 01
reg_write

S5: MEMWRITE
IorD = 1
mem_wr_ena

S6: EXECUTE
aluSrcA = 1
aluSrcB = 00
aluOp = 10

S7: ALU_WRITEBACK
reg_write
aluSrcB = 10

S8: BEQ
aluSrcA = 1
aluSrcB = 00
aluOp = 01
pcSrc = 01
branch

S9: EXECUTE_IMM
aluSrcA = 1
aluOp = 11

S11: JUMP
pcSrc = 10
pc_write

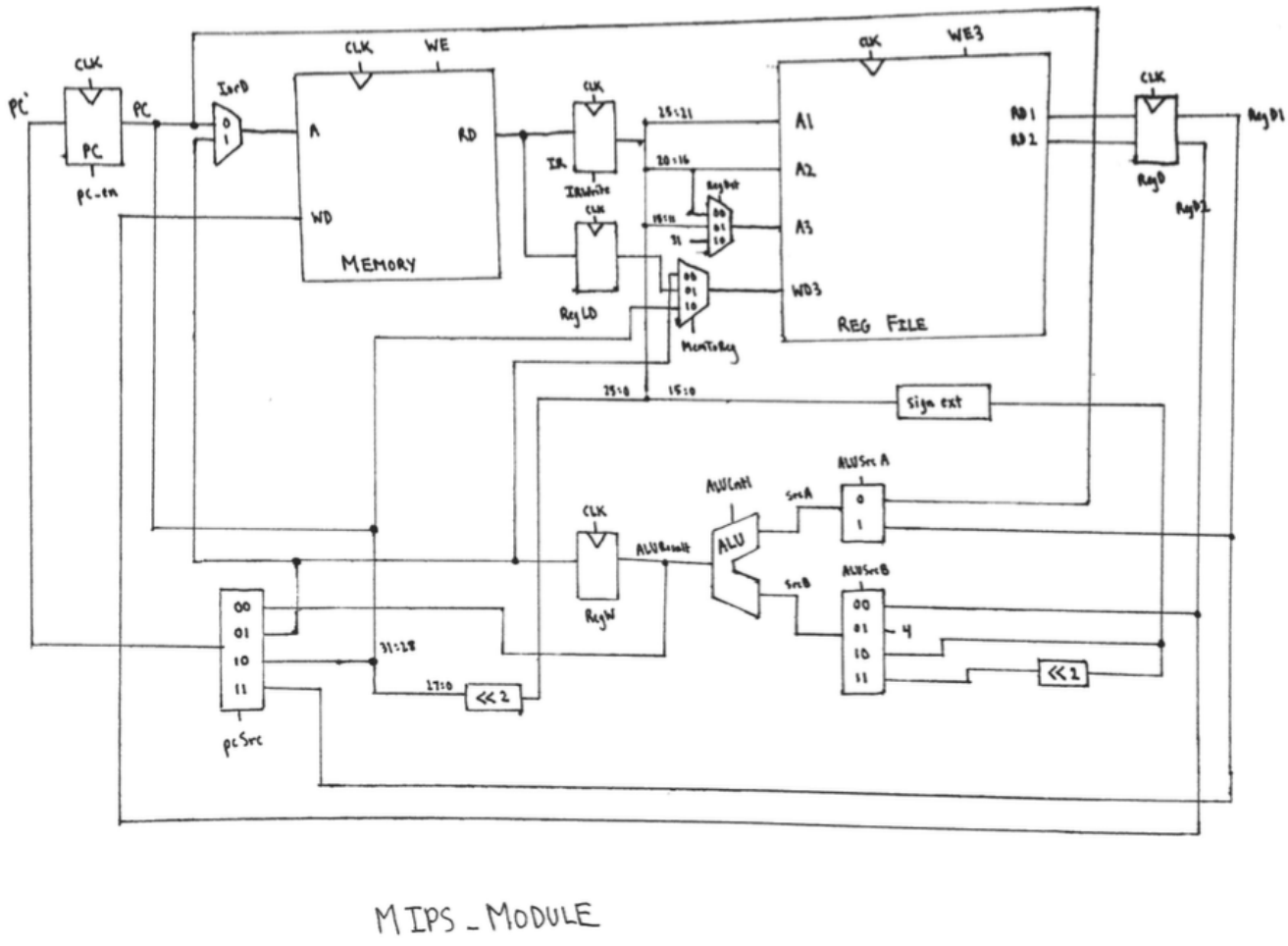
S12: JR
pcSrc = 11
pc_write

S13: JAL
pcSrc = 10
pc_write
reg_write
regDst = 10
memToReg

S14: BNE
aluSrcA = 1
aluSrcB = 01
aluOp = 01
pcSrc = 01
brancheNE

S29: MEMREAD_WAIT
S30: READ_FROM_MEMORY
S31: FETCH_FROM_MEMORY

Datapath



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