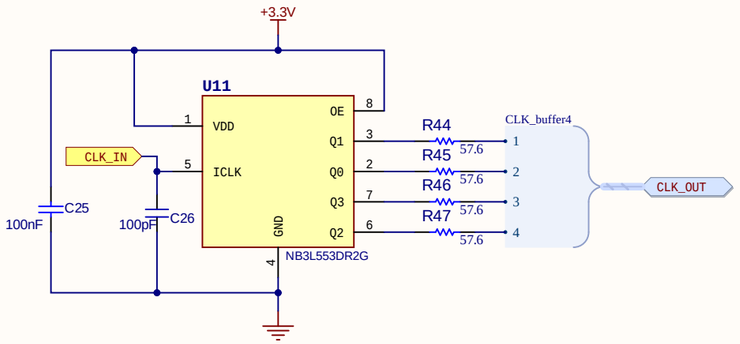
DWG. NO. | REV. | 4 SHT.

REVISION	DESCRIPTION	DATE	APPROVED

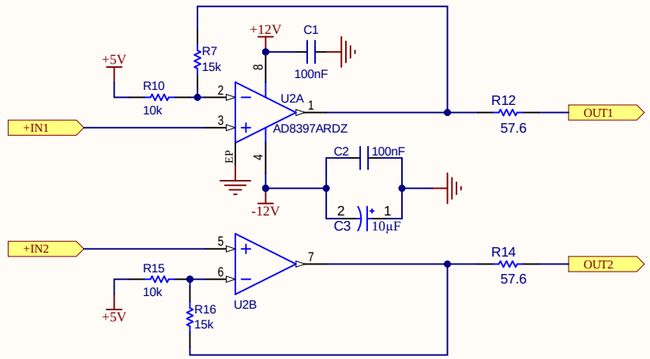


TITLE	*		
SIZE B	CAGE CODE	DWG NO.	REV
SCALE:	FILE NAME CLK_buffer.SchDoc	SHEET 4	OF 7

DWG. NO. | REV. | SHT.
* | *

REVISION	DESCRIPTION	DATE	APPROVED

Range = [-7.5, -1.25] V
Each channel can source/sink 310 mA of current
Transfer functions:
GBIAS = 2.5*VOUT - 7.5
GBIAS = (DAC input code / 655) - 7.5

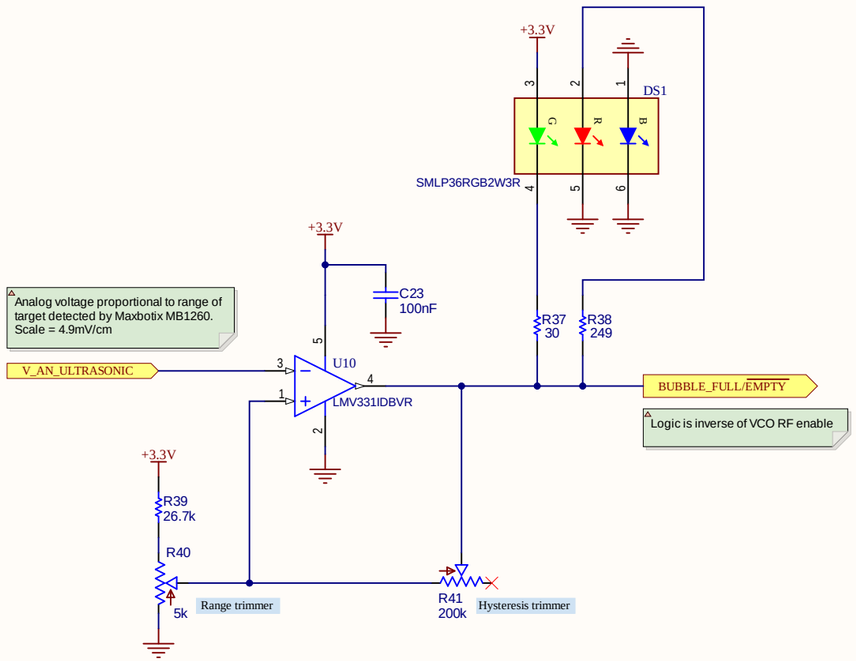


TITLE			
*			
SIZE: B	CAGE CODE	DWG NO.	REV
SCALE:	FILE NAME: dual_opamp.SchDoc	SHEET * OF *	

DWG NO.
REV
SHT
*

DWG. NO. | REV. | SHT. *

REVISION	DESCRIPTION	DATE	APPROVED



TITLE *

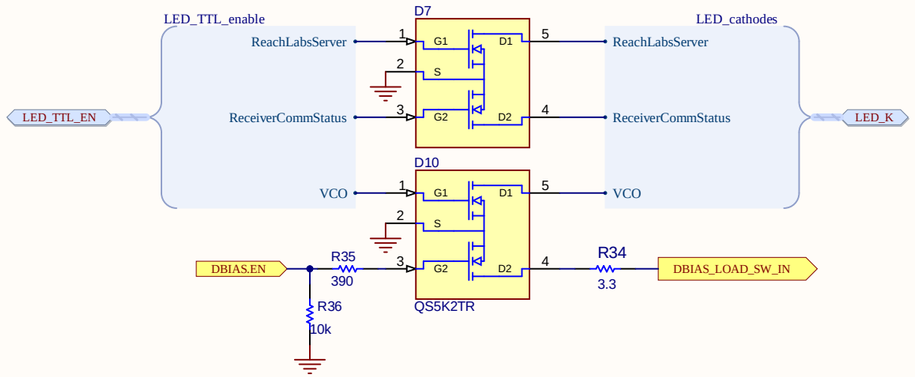
SIZE	CAGE CODE	DWG NO.	REV
B			

SCALE: | FILE NAME keepout_bubble.SchDoc | SHEET * OF *

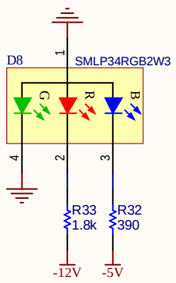
REVISION	DESCRIPTION	DATE	APPROVED

DWG. NO. | REV. | SHT. *

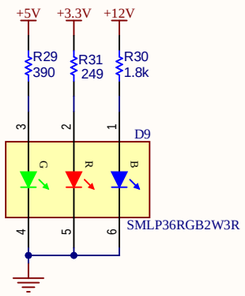
N-CH MOSFETs for the panel-mounted status LEDs. The "K"s go to the cathodes via a harness, and the anode of each LED will be connected to +12V.



Violet if all is well



White if all is well



TITLE			
*			
SIZE B	CAGE CODE	DWG NO.	REV
SCALE:	FILE NAME LEDs.SchDoc	SHEET *	OF *

REVISION	DESCRIPTION	DATE	APPROVED

TO DO:
-Add transfer function for VDET voltage --> RF power at the antenna inputs (dBm).
-Add table for SPI command bytes

+3.3V
C27 1µF
C28 100nF
U13
VA
GND
VIN
CS
SDATA
SCLK
CE0.ADC
ADC.DOUT
SE5004L.VDET
R52 15k
1kHz lowpass
C29 10nF
ADC121S021CIMFX/NOPB

To implement pulsed operation: alternatively write 0x000 and 0xB00. Duty cycle = (duration set to 0xB00) / (duration set to 0x000). Since the RPi SPI interface is 250 MHz maximum, the switching frequency is capped to (DAC slew rate / 4), which is 500 kHz.

Action	Data Word
Initial Configuration: -External reference -Buffered -Gain 1x	0x800C
Enter continuous update mode: Drives LDAC low persistent	0XA000
Power down unused outputs {G,H}	0xC0C0
Reset all outputs to 0V (quick-disable all gate biases)	0xE000
Write 0xNNN to VOUTA	0x0NNN
Write 0xNNN to VOUTB	0x1NNN
Write 0xNNN to VOUTC	0x2NNN
Write 0xNNN to VOUTD	0x3NNN
Write 0xNNN to VOUTE	0x4NNN
Write 0xNNN to VOUTF	0x5NNN

SCLK
DAC.DIN
CE0.DAC
U4
SCLK
DIN
SYNC
LDAC
VOUTA
VOUTB
VOUTC
VOUTD
VOUTE
VOUTF
VOUTG
VOUTH
VREFABCD
VREFEFGH
VDD
GND
AD5328BRUZ-REEL7
Range = [0, 2.5] V
+3.3V
C10 10uF
C11 100nF
U5
OUT
IN
GND
REF3025AIDBZR
2.5V reference
C9 100nF

Due to the DAC's low-driving power-on-reset behavior, all outputs are set to 0V until data is written to the DAC. So upon system start, all the gate biases will be off, which is convenient.

Range = [-7.5, -1.25] V
Each channel can source/sink 310 mA of current
Transfer functions:
GBIAS = 2.5*VOUT - 7.5
GBIAS = (DAC input code / 655) - 7.5

dual_opamp.SchDoc
+IN1
+IN2
OUT1
OUT2

TVS Diodes
Reverse breakdown voltage = 10V
D1
D2
D3
D4
D5
D6
VCO
H
1
2
3
4
GBIAS

+3.3V
U1
G1
G2A
G2B
SPI0.CE0
select
LSB
B1
MSB
SELECT
A
B
C
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
EP
VCC
GND
SN74LVC138ARGYR
Selected output index = 4*MSB + 2*B1 + LSB
C4 1µF
C5 100nF
R1 1.8k
R2 1.8k
R3 1.8k
R4 1.8k
R5 1.8k
R6 100
R8 100
R9 100
R11 100
R13 100
demux_out
DAC
phase_shifter_bank1
phase_shifter_bank2
phase_shifter_bank3
phase_shifter_bank4
ADC
6
7
CE0
TTL_OUT

TITLE			
*			
SIZE B	CAGE CODE	DWG NO.	REV
SCALE:	FILE NAME RF_control.SchDoc	SHEET * OF *	

REVISION	DESCRIPTION	DATE	APPROVED

J14
Placeholder for RPi STEP
Raspberry Pi Model 4B

Mating cable assembly:
Molex 0151340603
J4
GBIAS.VCO
SE5004L.VDET
SDA
SCL
EN
0532610671
R42
10k

Connects to rocker SW
GRB244B802BR1.
Mating cable assembly:
Molex 151340306
J3
+12V
2A
1B
2B
53261-0371
voltage_regulators.SchDoc
PYB_EN

Extender:
Samtec ESQ-120-23-T-D
J7
+5V
C24
4.7µF
RPI_3.3V
SDA
SCL
EN
VCO
MSB
B1
LSB
DEMUX SELECT
SPI0
MOSI
MISO
SCLK
30
SDA0
SCL0
SPI0.CE0
SPI0.CE1
nRF.RESET
SPI_NOTIFY
BUBBLE_FULL/EMPTY
DBIAS.EN
PPTC202LFBN-RC
NRF chip select

Debug header
J8
UART.TX
UART.RX
PWM0
BUBBLE_FULL/EMPTY
SDA0
SCL0
57202-G52-07LF

RF_control.SchDoc
SE5004L.VDET
SELECT
GBIAS
SCLK
DAC.DIN
ADC.DOUT
CE0
TTL_OUT
SPI0.CE0

CLK_buffer.SchDoc
CLK_IN
CLK_OUT
SPI0.SCLK
SPI0.MOSI
SCLK
MOSI
MISO

keepout_bubble.SchDoc
BUBBLE_FULL/EMPTY
V_AN_ULTRASONIC
+5V
J12
05326-10471
Mating cable assembly:
Molex 151340406

parallel headers with 18.3 mm
separation (center-center)
for CommsModule PCB
J10
UART.TX
UART.RX
+5V
NPTC061KFXC-RC
J11
MISO
MOSI
SCLK
SPI0.CE1
SPI_NOTIFY
nRF.RESET

J1
J2
J5
J6
SPI0.SCLK.1
SPI0.MOSI.1
CE0.phase_shifter_bank1
SPI0.SCLK.2
SPI0.MOSI.2
CE0.phase_shifter_bank2
SPI0.SCLK.3
SPI0.MOSI.3
CE0.phase_shifter_bank3
SPI0.SCLK.4
SPI0.MOSI.4
CE0.phase_shifter_bank4
+3.3V
-5V
GBIAS.1
GBIAS.2
GBIAS.3
GBIAS.4
GBIAS.H
3020-10-0100-00
D11
D12
SMDA03-6/TR7
TVS diodes
Reverse breakdown
voltage = 4V

LED_TTL_enable
ReachLabsServer
ReceiverCommStatus
VCO
LEDs.SchDoc
LED_TTL_EN
LED_K
DBIAS.EN
DBIAS_LOAD_SW_IN
LED_cathodes
J9
S6B-PH-SM4-TB(LF)(SN)
C33
10µF
+12V
Cable assembly:
A06KR06KR26E305B
LED Colors:
Blue
Green
Amber

J13
S3B-PH-SM4-TB(LF)(SN)
V+_COSEL_UNFUSED
V+_COSEL_FUSED
F1
MF-MSMF150/24X-2
D13
CUS10S30,H3F
Polyfuse
1.5A hold
3.0A trip
Reverse-voltage protection
Shottky diode, 230mV
forward drop @ 1A
Mating cable assembly:
JST A03KR03KR26E305A
DBIAS_LOAD_SW_IN

APPROVALS	DATE
ENG: *	--/--/--
DSN: *	--/--/--
CHK: *	--/--/--
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

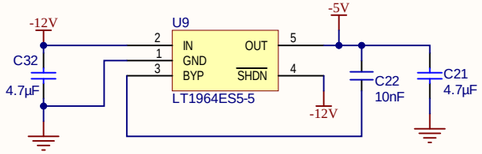
PROJECT: *
PROJECT REVISION: 2f9a7381704bdecef5a8b
TITLE: *
SIZE: B
CAGE CODE:
DWG NO.:
REV:
SCALE:
FILE NAME: top_media_conglomerate_adult_v01.2.SchDoc
SHEET: OF *

DWG. NO. | REV. | SHT. *

REVISION	DESCRIPTION	DATE	APPROVED

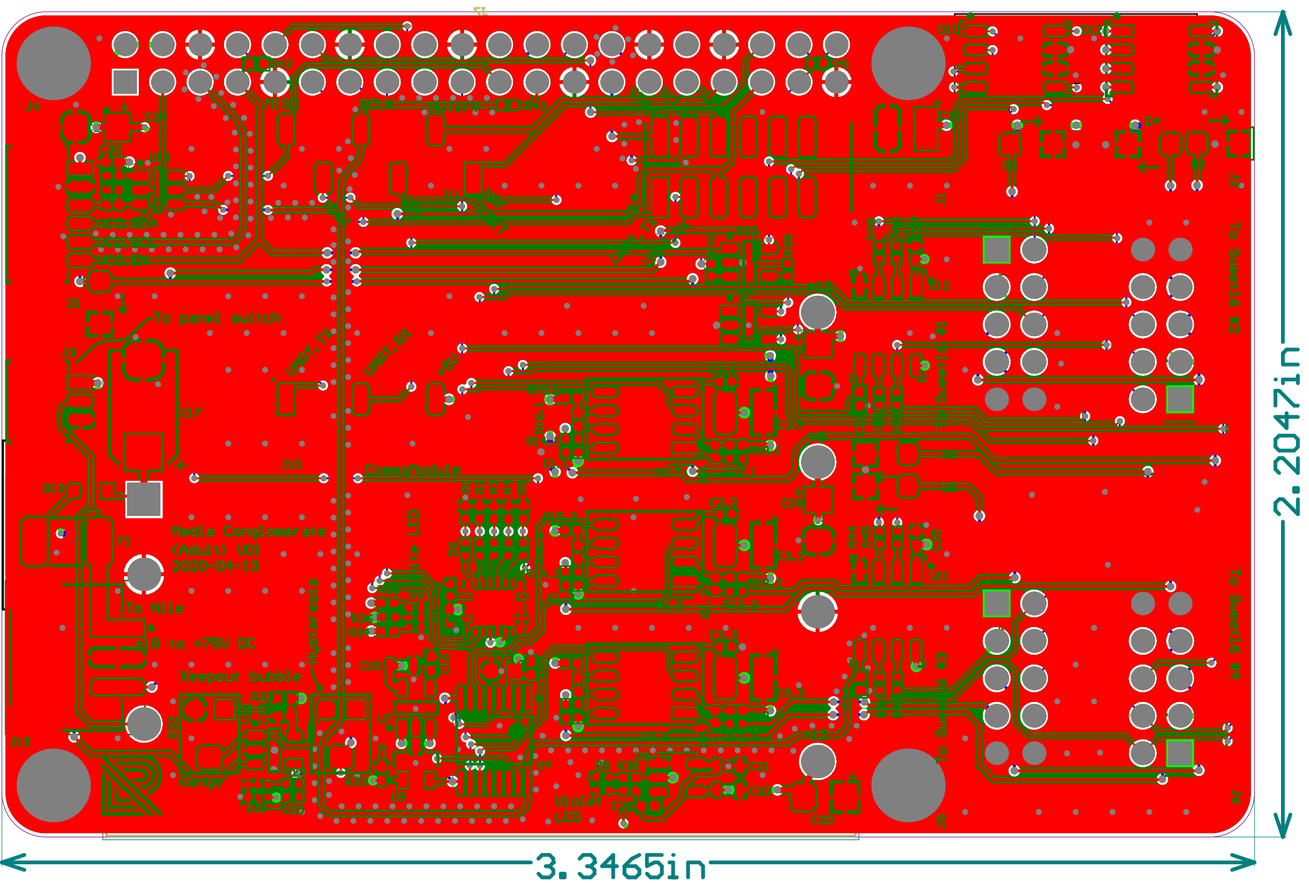
3.3V rail for digital ICs

-5V rail for phase shifters



TITLE *			
SIZE B	CAGE CODE	DWG NO.	REV
SCALE:	FILE NAME voltage_regulators.SchDoc	SHEET *	OF *

Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0.50mil	3.5
1	Top Layer	Copper	1.40mil	
	Dielectric 1	370HR	3.50mil	4.5
2	L2 GND	Copper	1.40mil	
	Dielectric 2	370HR	48.40mil	4.5
3	L3 Power	Copper	1.40mil	
	Dielectric 3	370HR	3.50mil	4.5
4	Bottom Layer	Copper	1.40mil	
	Bottom Solder	Solder Resist	0.50mil	3.5
	Bottom Overlay			
Total board thickness:			62.00mil	



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL

MIN. CLEARANCE: 5 MIL

MIN. VIA PAD SIZE: 40 MIL

MINIMUM ANNULAR RING 3MIL EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [ ] FR-4 High Tg [X] OTHER _____

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/- _____

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/- _____

DRILLING:

REFERENCE: [X] AS SHOWN [ ] NC_DRILL FILES

PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER _____

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____

[ ] MATTE [X] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] UL 94V-0 [ ] RoHS [ ] OTHER PER ORDER

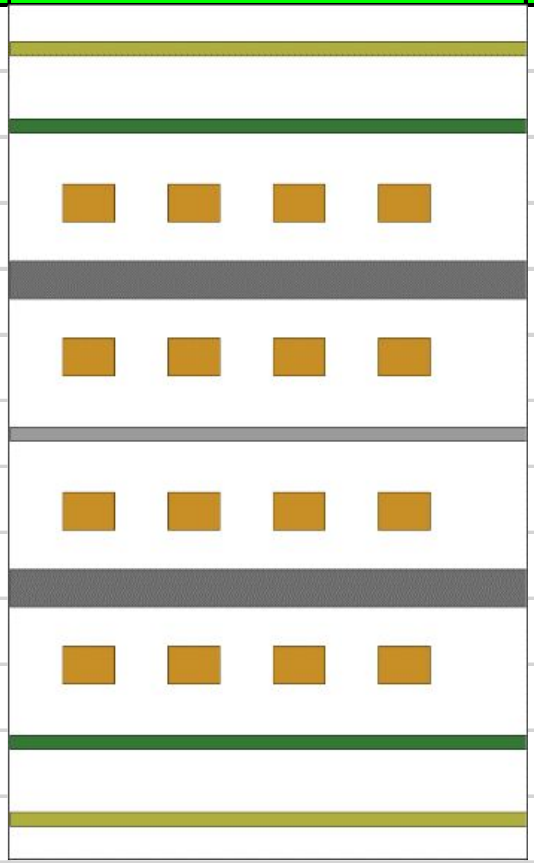
ADDITIONAL REQUIREMENTS:

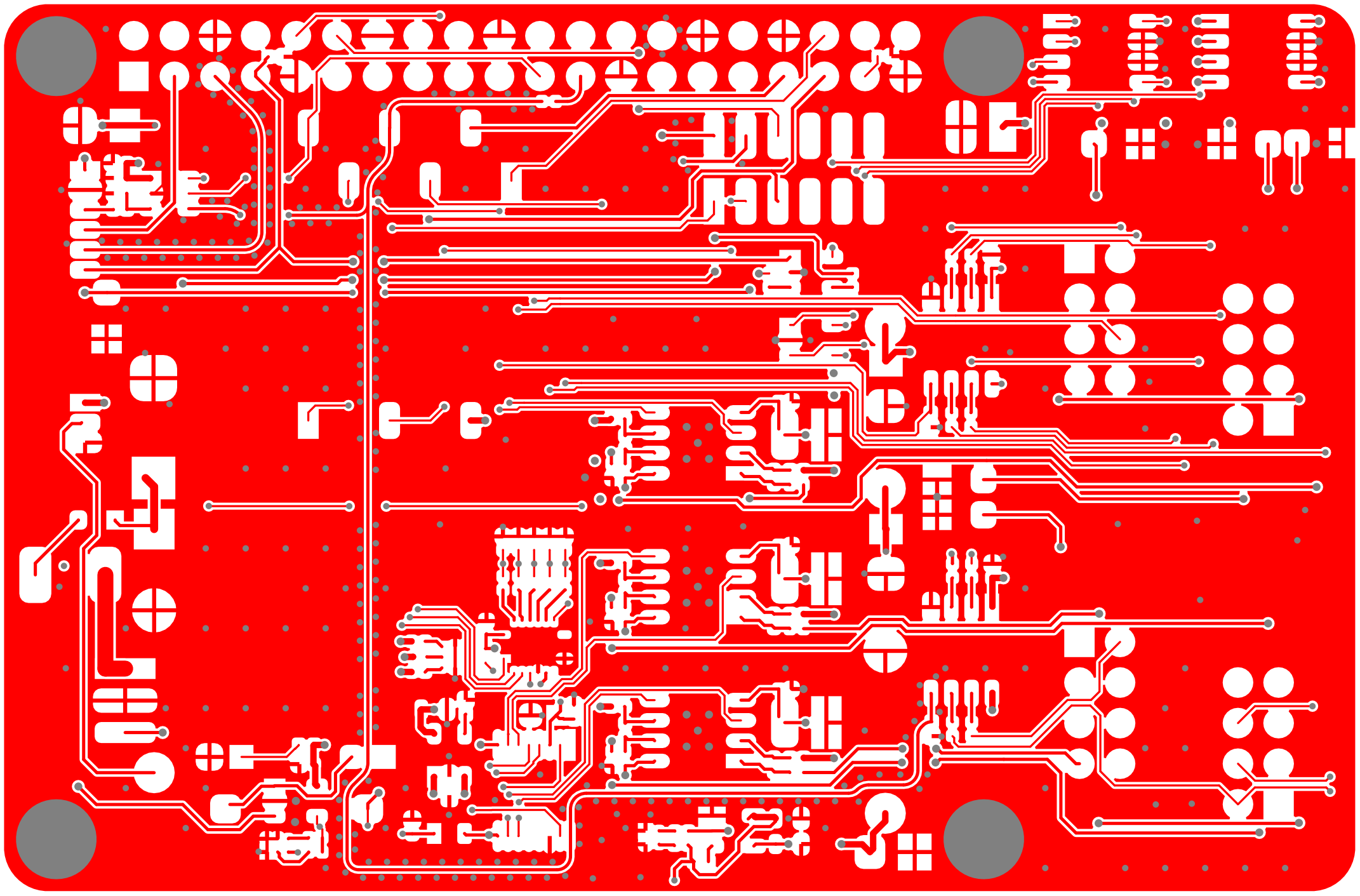
MICROSECTION: [ ] YES

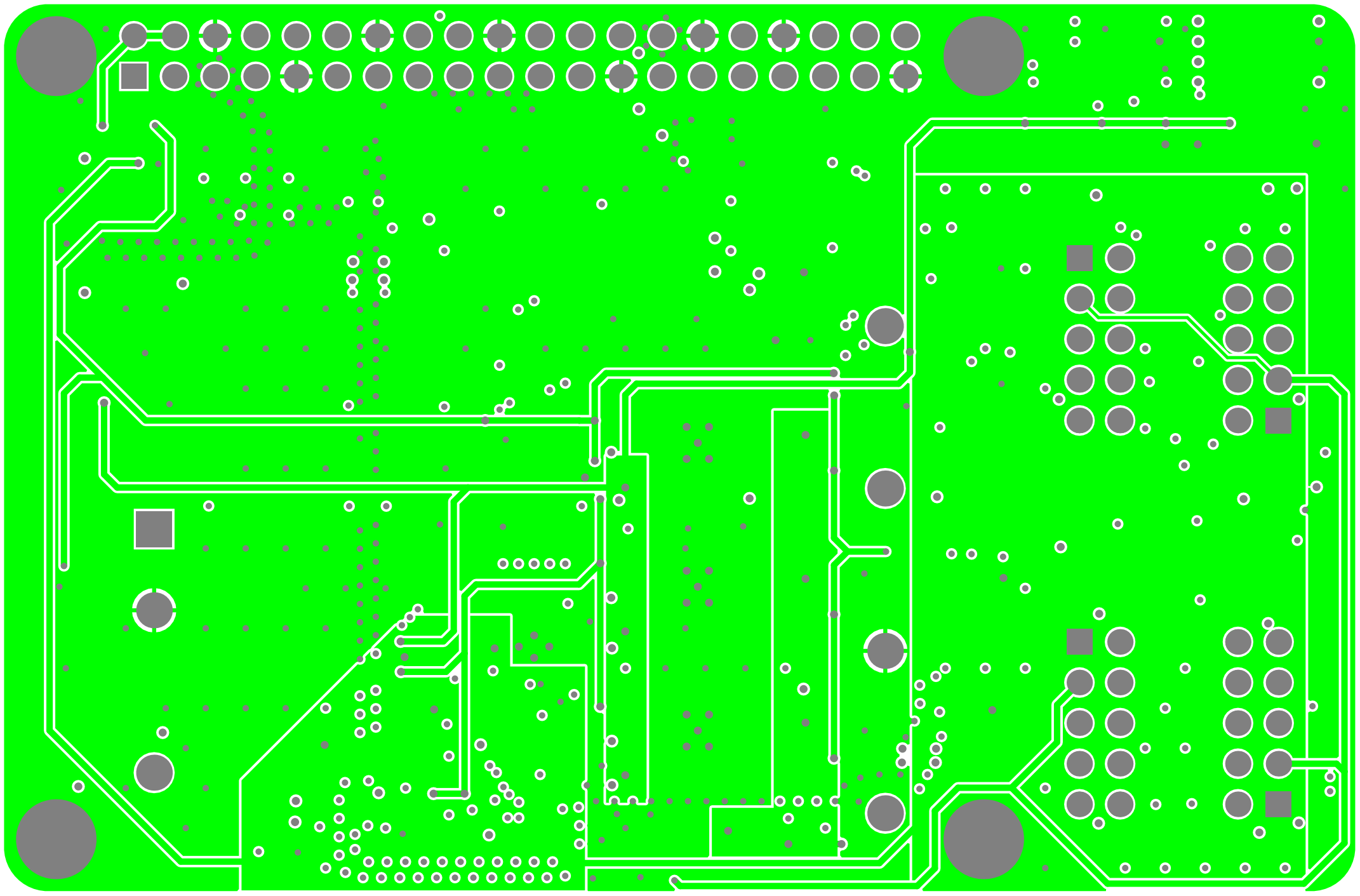
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

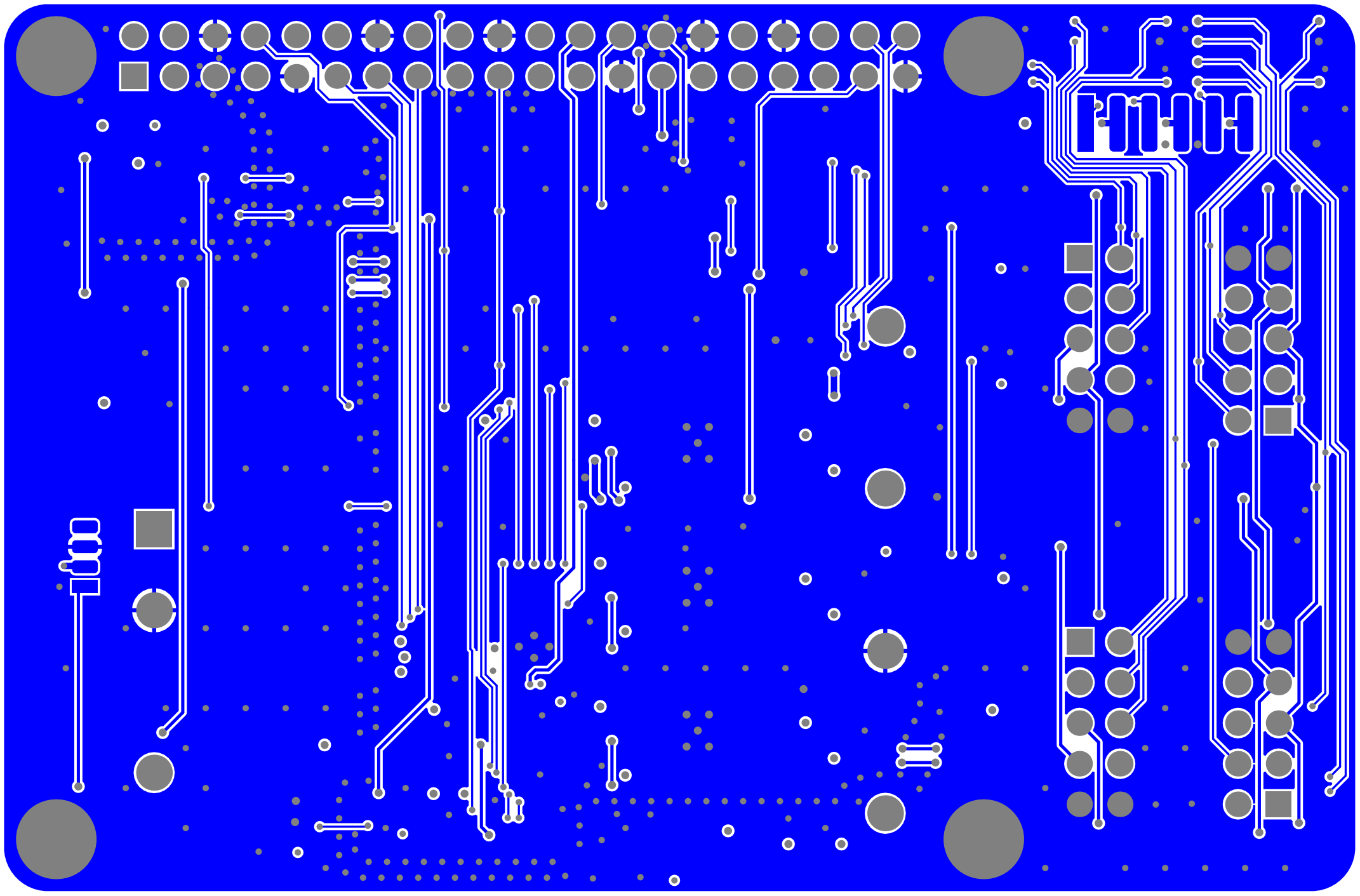
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

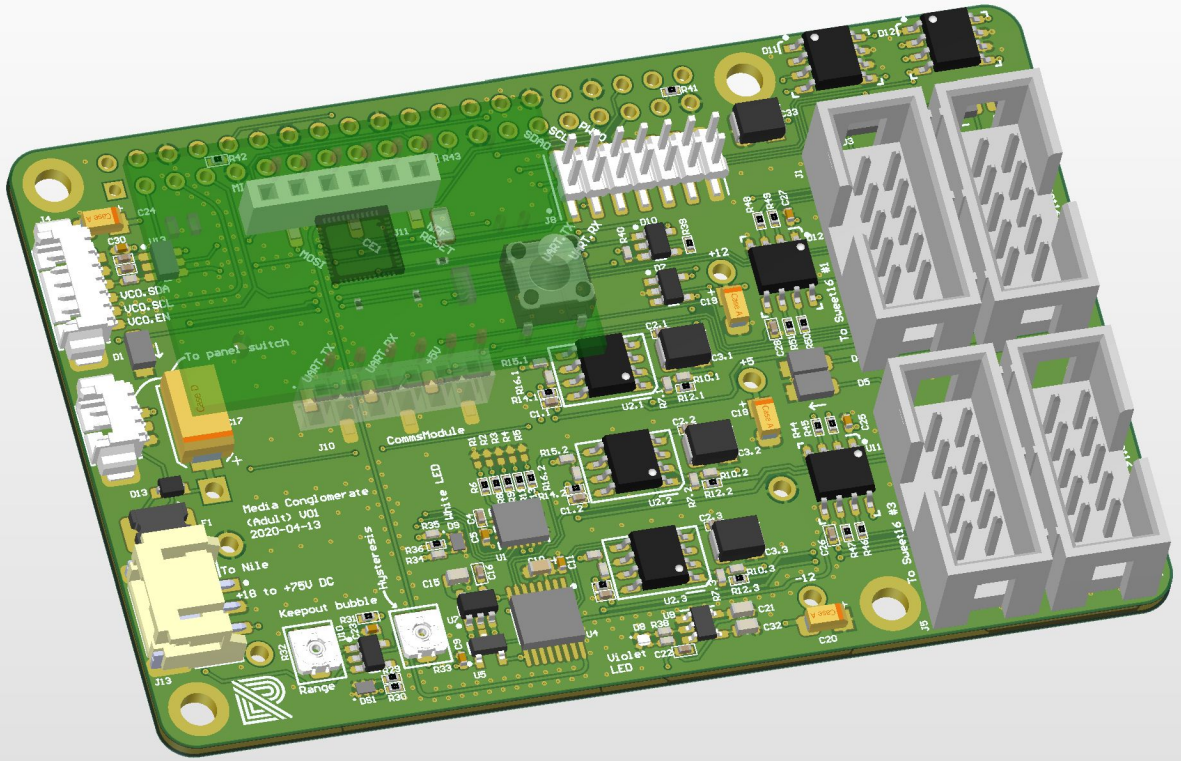
Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0.50mil	3.5
4		Top Layer	Copper	1.40mil	
5		Dielectric 1	370HR	3.50mil	4.5
6		L2 GND	Copper	1.40mil	
7		Dielectric 2	370HR	48.40mil	4.5
8		L3 Power	Copper	1.40mil	
9		Dielectric 3	370HR	3.50mil	4.5
10		Bottom Layer	Copper	1.40mil	
11		Bottom Solder	Solder Resist	0.50mil	3.5
12		Bottom Overlay			
13		Bottom Paste			
	Height : 62.00mil				








Media Conglomerate
(Adult) V01
2020-04-13
To panel switch
To Nile
+18 to +75V DC
Keepout bubble
Range
Hysteresis
White LED
Violet LED
CommsModule
To Swarm 16
To Swarm #3
VCO.SDA
VCO.SCL
VCO.EN
UART.TX
UART.RX
+5V
+12
-12
+5
SCL
SDA
MOSI