Addressing the Performance Bottlenecks of Device Driver Synthesis

Alexander Legg

Supervised by
Leonid Ryzhyk, Nina Narodytska, and Gernot Heiser

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Abstract

Device drivers are notorious for their contribution to the failure of software systems. A driver forms the interface between two complicated systems: an operating system and a hardware device. As a result, driver development is complicated and highly prone to human error. Driver reliability has been the focus of much research over the past two decades. One result of this research is device driver synthesis.

Device driver synthesis aims to remove human error from the development process by removing humans. A synthesis tool can take a formal specification of requirements and produce a system. Thus, a driver can be synthesised by providing the tool with a specification of the OS and the hardware that it must interface with. The resulting driver is guaranteed to be correct with respect to the specifications.

The drawback of this approach is that synthesis is a computationally intensive task belonging to 2-EXPTIME. In practice synthesis tools are capable of producing drivers though there remain cases where synthesis is impossible. In this thesis I will present an algorithm that provides results on many of these previously unattainable cases.

Acknowledgements

Acknowledge some people

1 Introduction

This is the introduction.

1.1 Device Drivers

Device drivers are the software that allows the operating system to interface with hardware. The role of the driver is to manipulate the inputs of the device so that it remains in a error-free state and correctly handles the requests of the operating system. By way of example consider an ethernet driver. The driver accepts requests to send and receive data packets from the OS and acts on those requests by reading from and writing to buffers on the device. It must ensure that those buffers are maintained in a usable state by correctly updating a register containing the location of the head of the buffer queue.

According to a study performed in 2011 [3], drivers account for approximately 57% of the lines of code in the Linux kernel and subsequently is the largest source of bugs. The study also analysed the staging directory of the kernel, which contains all in-progress drivers, and found it to contain the highest fault rate (faults per line of code) out of any directory in the kernel. The results of the study give evidence to the widely held belief that correct drivers are hard to produce.

Consequences of buggy drivers

This thesis focuses on automatic construction of correct drivers as a solution to the driver problem. Alternate approaches, of which there are many, will be discussed in Chapter 2.

1.2 Synthesis

Explain what synthesis is

- Briefly describe the current state of the art
- Explain state space explosion

1.3 Synthesis with SAT

Explain SAT solvers

- Explain how they might help with state space explosion
- (Explain that there is room for both approaches in the world)
- Explain QBF and/or why this is nontrivial

2 Related Work

3 Formalisation of Software

Synthesis is a process that demands mathematical formalisation in order to provide a strong guarantee of the correctness of the resultant software. As such we require a mathematical language to describe the system we wish to produce, the environment in which it operates, and the properties we want the system to adhere to. This chapter will outline that language and the ways we can reason about what we describe in it.

3.1 Reactive Systems

Devices drivers are an example of a reactive system. A reactive system is a system that is in a continuous process of responding to input from its environment. A driver accepts requests from the operating system and state information from the device, and it responds by sending commands to the device and reporting to the operating system.

Büchi automata [1] are a formalisation of reactive systems. Büchi automata are ω-automata, which means they describe finite systems that accept an infinite stream of input. This is a useful formalism for synthesis because we want to create finite systems that responds to input indefinitely.

Like all ω-automata, the language of a Büchi automaton is ω-regular. A regular language over the alphabet Σ is

- The empty language , *or*
- A singleton language $\{a\}$ for $a \in \Sigma$, *or*
- For two regular languages A and B:
  - $A \cup B$ the union of those languages, *or*

- $A \,.\, B$ the concatenation of those languages, *or*
- $A*$ the Kleene operation on that language.

An ω-regular language is a regular language with infinitely long words.

3.2 Temporal Logic

Temporal logic takes propositional logic and provides additional semantics for the concept of time. In order to reason about program executions, which are a series of discrete steps, the logic must have the expressiveness to talk about the future.

Linear temporal logic (LTL) allows for statements that refer to a single execution trace of a system. Pnueli introduced LTL in 1977 [4] to succinctly describe the outcomes of program execution by referring to global invariants and eventualities. The syntax is:

- ϕ is a propositional formula referring to the current state,
- $X\phi$ - ϕ is true in the next state of the execution,
- $F\phi$ - Eventually (finally) ϕ will be true, and
- $G\phi$ - ϕ is always (globally) true.

The semantics of this logic is formally defined with respect to

In 1981 Clarke introduced computation tree logic (CTL) [2], which has the expressiveness to reason about multiple execution paths of a program. The syntax of CTL is as follows:

- $A\phi$ - ϕ is true on all paths
- $E\phi$ - there exists a path on which p is true

3.3 Reactive Synthesis

Synthesis as a Game

GR(1) Games

3.4 Binary Decision Diagrams

3.5 Abstraction

3.6 SAT

3.7 Interpolation

4 Synthesis with SAT

5 Evaluation

6 Conclusion

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