



## 1. Description

### 1.1. Project

Project Name	Injection_STM32F407
Board Name	custom
Generated with:	STM32CubeMX 6.12.0
Date	12/08/2024

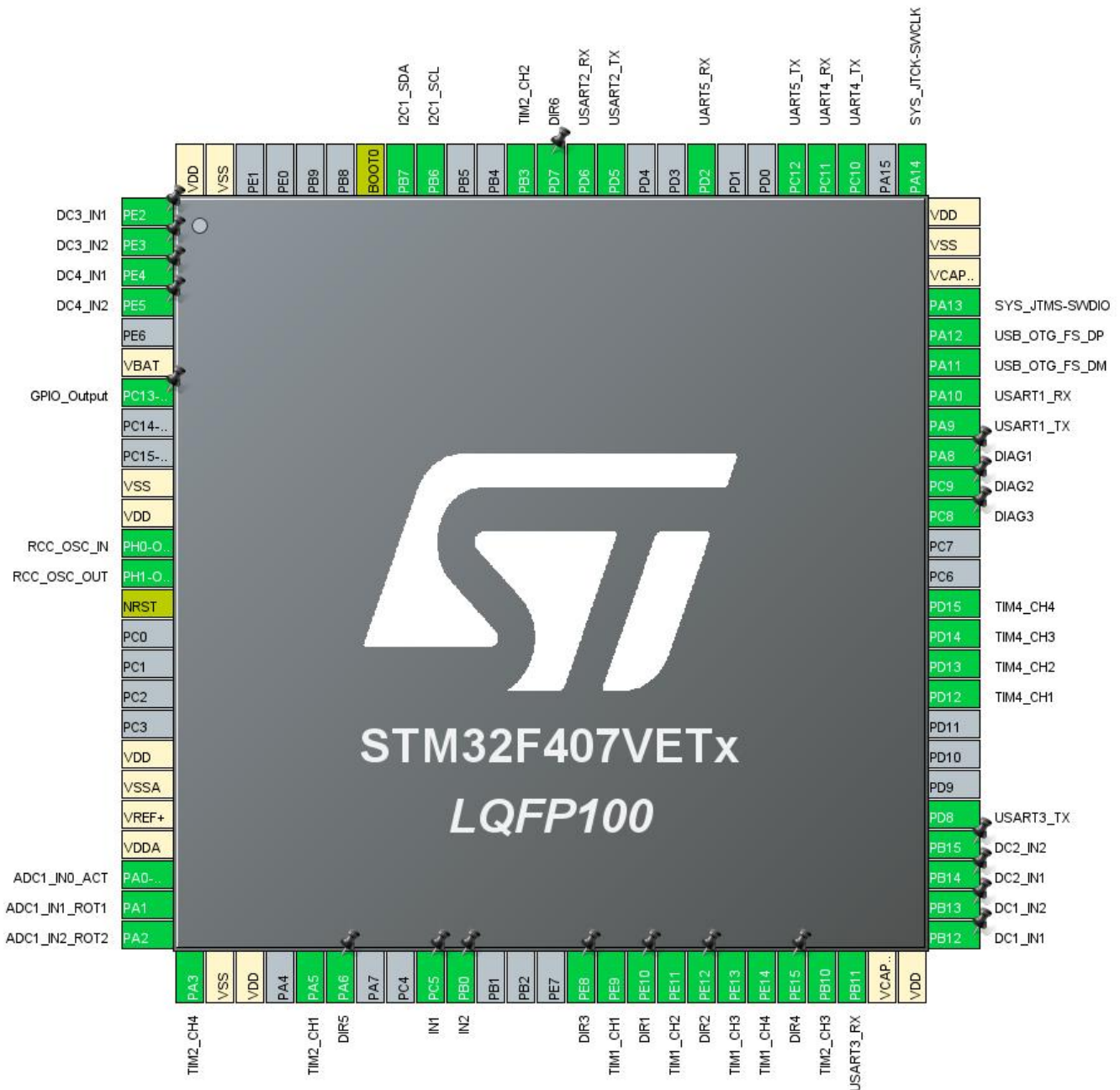
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



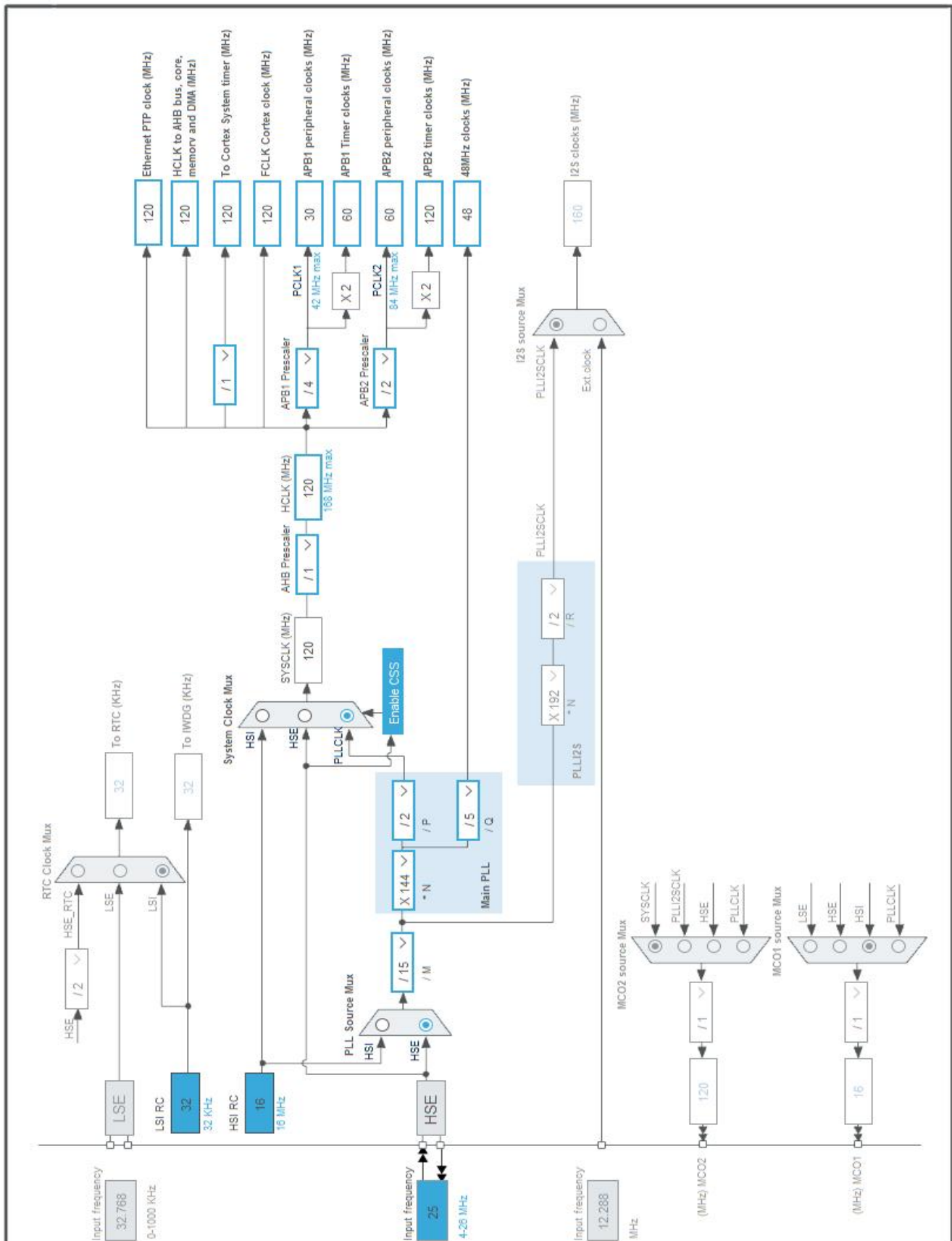
### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	DC3_IN1
2	PE3 *	I/O	GPIO_Output	DC3_IN2
3	PE4 *	I/O	GPIO_Output	DC4_IN1
4	PE5 *	I/O	GPIO_Output	DC4_IN2
6	VBAT	Power		
7	PC13-ANTI_TAMP *	I/O	GPIO_Output	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	ADC1_IN0_ACT
24	PA1	I/O	ADC1_IN1	ADC1_IN1_ROT1
25	PA2	I/O	ADC1_IN2	ADC1_IN2_ROT2
26	PA3	I/O	TIM2_CH4	
27	VSS	Power		
28	VDD	Power		
30	PA5	I/O	TIM2_CH1	
31	PA6 *	I/O	GPIO_Output	DIR5
34	PC5 *	I/O	GPIO_Output	IN1
35	PB0 *	I/O	GPIO_Output	IN2
39	PE8 *	I/O	GPIO_Output	DIR3
40	PE9	I/O	TIM1_CH1	
41	PE10 *	I/O	GPIO_Output	DIR1
42	PE11	I/O	TIM1_CH2	
43	PE12 *	I/O	GPIO_Output	DIR2
44	PE13	I/O	TIM1_CH3	
45	PE14	I/O	TIM1_CH4	
46	PE15 *	I/O	GPIO_Output	DIR4
47	PB10	I/O	TIM2_CH3	
48	PB11	I/O	USART3_RX	
49	VCAP_1	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	DC1_IN1
52	PB13 *	I/O	GPIO_Output	DC1_IN2
53	PB14 *	I/O	GPIO_Output	DC2_IN1
54	PB15 *	I/O	GPIO_Output	DC2_IN2
55	PD8	I/O	USART3_TX	
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
61	PD14	I/O	TIM4_CH3	
62	PD15	I/O	TIM4_CH4	
65	PC8 *	I/O	GPIO_Input	DIAG3
66	PC9 *	I/O	GPIO_Input	DIAG2
67	PA8 *	I/O	GPIO_Input	DIAG1
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	UART4_TX	
79	PC11	I/O	UART4_RX	
80	PC12	I/O	UART5_TX	
83	PD2	I/O	UART5_RX	
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
88	PD7 *	I/O	GPIO_Output	DIR6
89	PB3	I/O	TIM2_CH2	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	DS8626_Rev8

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

#### 1.4. Sequence

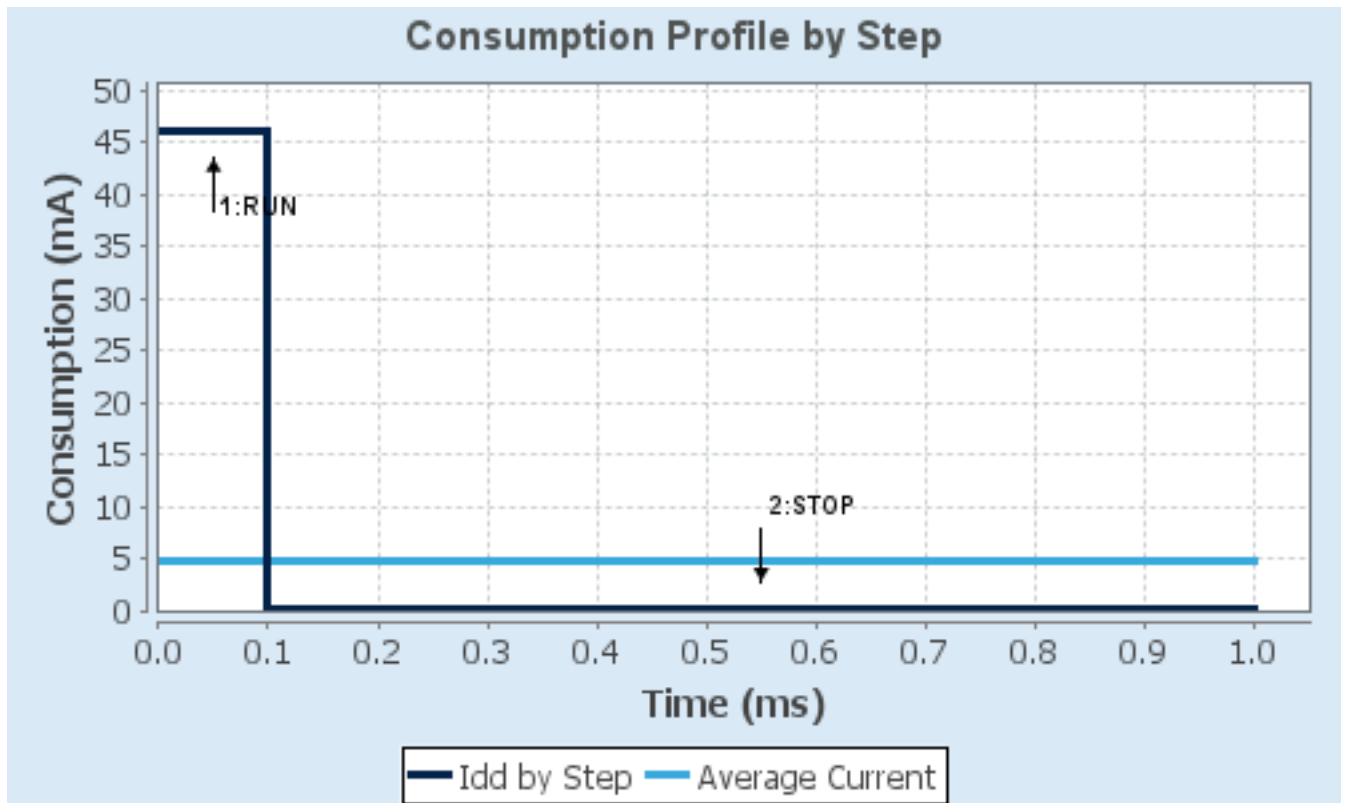
<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	168 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	46 mA	280 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	210.0	0.0
<b>Ta Max</b>	98.47	104.96
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

#### 1.6. Chart





## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	Injection_STM32F407
Project Folder	Z:\Desktop\igen\Injection\Injection_STM32F407
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_I2C1_Init	I2C1
5	MX_TIM1_Init	TIM1
6	MX_TIM2_Init	TIM2
7	MX_UART4_Init	UART4
8	MX_UART5_Init	UART5
9	MX_USART1_UART_Init	USART1
10	MX_USART2_UART_Init	USART2
11	MX_USART3_UART_Init	USART3

Rank	Function Name	Peripheral Instance Name
12	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
13	MX_TIM4_Init	TIM4

## 3. Peripherals and Middlewares Configuration

### 3.1. ADC1

mode: IN0

mode: IN1

mode: IN2

#### 3.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode	Independent mode
<b>ADC_Settings:</b>	
Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

##### **ADC\_Regular\_ConversionMode:**

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

##### **ADC\_Injected\_ConversionMode:**

Number Of Conversions	0
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##### **WatchDog:**

Enable Analog WatchDog Mode	false
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### 3.2. I2C1

I2C: I2C

#### 3.2.1. Parameter Settings:

##### **Master Features:**

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

**Slave Features:**

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

**3.3. RCC****High Speed Clock (HSE): Crystal/Ceramic Resonator****3.3.1. Parameter Settings:****System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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**3.4. SYS****Debug: Serial Wire****Timebase Source: SysTick****3.5. TIM1**

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

**3.5.1. Parameter Settings:**

#### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

#### Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

### 3.6. TIM2

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

#### 3.6.1. Parameter Settings:

##### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

##### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

##### **PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

##### **PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (32 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

#### **PWM Generation Channel 4:**

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### **3.7. TIM4**

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

#### **3.7.1. Parameter Settings:**

##### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

##### **PWM Generation Channel 1:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

##### **PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High



#### **PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

#### **PWM Generation Channel 4:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### **3.8. UART4**

#### **Mode: Asynchronous**

##### 3.8.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

### **3.9. UART5**

#### **Mode: Asynchronous**

##### 3.9.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
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Over Sampling

16 Samples

### 3.10. USART1

**Mode: Asynchronous**

#### 3.10.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

### 3.11. USART2

**Mode: Asynchronous**

#### 3.11.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

### 3.12. USART3

**Mode: Asynchronous**

#### 3.12.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1
<b>Advanced Parameters:</b>	
Data Direction	Receive and Transmit
Over Sampling	16 Samples

### 3.13. USB\_OTG\_FS

#### Mode: Device\_Only

##### 3.13.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	ADC1_IN0_ACT
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC1_IN1_ROT1
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	ADC1_IN2_ROT2
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
USART3	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC3_IN1
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC3_IN2
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC4_IN1
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC4_IN2
	PC13-ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR5
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN1
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IN2
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR3
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR1
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR2
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR4
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC1_IN1
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC1_IN2
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC2_IN1
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC2_IN2
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIAG3
	PC9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIAG2
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIAG1
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR6

#### **4.2. DMA configuration**

nothing configured in DMA service

### 4.3. NVIC configuration

#### 4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
UART4 global interrupt	unused		
UART5 global interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

#### 4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

\* User modified value



## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

#### Middleware

#### System Core

#### Analog

#### Timers

#### Connectivity

#### Multimedia

#### Security

#### Computing

DMA

ADC1 ✓

TIM1 ✓

I2C1 ✓

GPIO ✓

TIM2 ✓

UART4 ✓

NVIC ✓

TIM4 ✓

UART5 ✓

RCC ✓

USART1 ✓

SYS ✓

USART2 ✓

USART3 ✓

USB\_FS ✓

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f4-svd.zip">https://www.st.com/resource/en/svd/stm32f4-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
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